Improving the performance of digitally-controlled high power grid-connected inverters

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ABSTRACT

The availability of high speed and high power switching devices, such as the IGBT, has opened the opportunity for an increasing number of grid-connected inverter applications that have historically been unachievable. Recently, the number of inverter applications has surged, with now the focus being on increasing the relative performance and power capability. Such applications include UPSs, dynamic voltage restorers, STATCOMs, frequency converters and distributed grid sources such as solar panels.

The inverter switching frequency limits its associated bandwidth and hence performance. Every application can benefit by reduction of the extent of this limitation. While state of the art devices like IGBTs enable such applications, the onus is now on developing high bandwidth digital controllers; the ability to connect multiple devices together to achieve power scaling; and having the confidence that the applications will work with other systems on a grid.

Constraints and limitations imposed by the hardware and traditional continuous-time derived controllers are identified. A discrete-time direct design controller is then developed specifically for digital controllers, that for the same inverter configuration, achieves twice the bandwidth of a well-tuned traditional controller. An important feature of a controller is having the configurability of being able to choose inverter bandwidth over stability margin.

To provide power scaling above that of a single switching module, investigations are performed on the suitability of actively paralleling inverter modules. Both the use of the developed discrete direct design controller and the identification of potential inter-module instabilities for a particular configuration enables the application of paralleled inverters. The operation is confirmed

through the application of a sixteen paralleled module inverter system.

Finally, a graphical analysis technique is introduced for analysing complex grids that may include inverter systems. The graphical technique demonstrates stability constraints with a range of sources and loads, including both inverters and rotating machines, which historical analysis techniques have been unable to do.

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PUBLICATIONS ASSOCIATED WITH THIS THESIS

The following papers have either been published, accepted or submitted during the course of the research described in this thesis:

JOURNAL PAPERS

1. Turner, R.W., Walton, S., and Duke, R., 'Robust High Performance Inverter Control Using Discrete Direct Design Pole Placement', *IEEE Trans. Ind. Elec.*, 58(1):348-357, Jan 2010.

2. Turner, R.W., Walton, S., and Duke, R., 'Stability and Bandwidth Implications of Digitally Controlled Grid-Connected Parallel Inverters', *IEEE Trans. Ind. Elec.*, 57(11):3685-3694, Nov 2010.

3. Turner, R.W., Walton, S., and Duke, R., 'A Graphical Technique for Analysing the Stability of Modern Interconnected Loads and Sources on Grids', accepted for publication in *IEEE Trans. Ind. Elec.*, April 2011.

CONFERENCE PAPERS

1. Turner, R.W., Walton, S., and Duke, R., 'Technique to improve IGBT converter efficiency and transient response', paper presented at *Power Electronics and Motion Control Conference, EPE-PEMC*, Poznań, Poland, 1-3 September, 2008.

2. Turner, R.W., Walton, S., and Duke, R., 'Dynamic frequency scaling to improve converter efficiency', paper presented at *Australasian Universities Power Engineering Conference,*

AUPEC, Perth, Australia, 9-12 December, 2007.

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GLOSSARY OF TERMS

Abbreviation	Definition
ADC	Analog to Digital Converter
BW	Bandwidth
CAN	Controller Area Network
CSI	Current Sourcing Inverter
dB	Decibels. $20log_{10}(x)$ for voltages/currents. $10log_{10}(x)$ for power.
DSP	Digital Signal Processor
EMF	Electromotive Force
FPGA	Field Programmable Gate Array
Hz	Hertz - unit of frequency
IAE	Integral Absolute Error
IGBT	Insulated Gate Bipolar Junction Transistor
ISE	Integral Squared Error
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
P	Real Power
P.U. or pu	Per Unit
PWM	Pulse Width Modulation
VA	Volt-Ampere
VSI	Voltage Source Inverter
Q	Reactive Power
RMS	Root Mean Squared
SCR	Silicon Controller Rectifier
THD	Total Harmonic Distortion
T_s	Sample time
VAr	Reactive power
ZOH	Zero Order Hold

The following conventions are used for linear algebra variables:

Complex variables are denoted with an underline. For example, a dq frame voltage is $\underline{V} = V_d - jV_q$.

Corresponding real space vectors are denoted with italic letters. For example $v = [V_d, V_q]^T \leftrightarrow \underline{V}$.

Matrices are in bold type $\mathbf{G}$.

Chapter 1

INTRODUCTION

Since the advent of both the digital processor and fast switching high power transistors, inverters for converting between AC and DC have been increasingly moving into applications that demand higher performance, higher power, the ability to change operational modes, and greater reliability. The availability of transistors that can both control hundreds of kilowatts and do so faster than the waveform being generated, is opening up the possibility of creating high power grid-connected inverters that offer unprecedented response rates.

The flexibility of inverter systems has increasingly seen them being used in a vast range of different applications. The increasing number of applications stems from different grid types, ranging from small grids that power only a single load, up to large interconnected international grids. As power usage increases, so too does the number of different load types that are connected to grid systems. At the same time as the number of different loads are increasing, so too is the number of different types of power source, recently including wind turbines, photovoltaic installations, and battery-energy storage systems. Due to their control flexibility and high efficiency, inverters are increasingly being used to either improve or enable different sources and loads.

As sources, the flexibility and control offered by inverters has seen them integrated into applications where they had not previously been required. The two most common applications for inverters have been Variable Speed Drives (VSD) and a component of DC power supplies. With the increasing focus on sustainable energy sources, inverters are often a key component for

interfacing the power source (AC or DC) to grid systems, operating as either a load or a source, or both.

As the number of different inverter load and source applications has increased, so too has the requirement for increased power capability and control performance. Emerging state of the art grid connected applications require both the performance typically achieved with low power systems, and the high power capability of traditional SCR converters. Modern switching devices like the IGBT provide a crossover by offering both relatively high switching frequencies with high voltage and current capabilities.

Although modern switching devices like the IGBT offer high switching frequencies and moderately high power capabilities, the possibility of further increasing the performance and/or power can only be achieved by using multiple interconnected devices. Through the use of reprogrammable digital processors generic inverters can be mass-produced, with specific software loaded for a given application. Digital processors with high speed networks also permit arrays of inverters and overriding controllers to be connected together to produce a large distributed system. Large distributed systems allow smaller but higher performance blocks to be interconnected to produce a larger high power system, meeting both the requirement of high power and high performance. An example would be a number of parallel-connected small inverters that all receive the same control reference, effectively operating as one high power inverter. Figure 1.1 shows an example break-down of a grid connected inverter system made up of multiple parallel inverter modules.

1.1 INVERTER REQUIREMENTS

The use of multiple connected inverters has several key requirements that must be addressed either by hardware or software.

- High performance. The inverter controller must achieve a relatively high performance

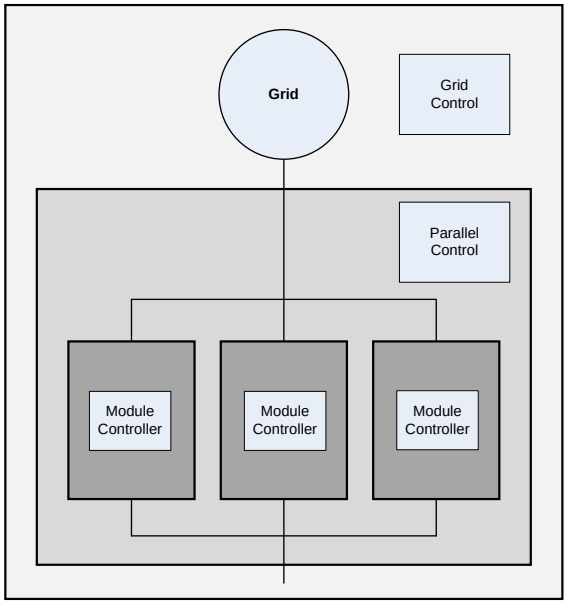


Figure 1.1: Parallel grid-connected inverter system.

within the switching frequency constraint imposed by the transistors. For grid connected applications the inverter typically uses an inductor-capacitor filter to reduce the voltage and current ripple. In the absence of passive damping, the controller has to manage the filter to prevent resonance.

- Ability to power share with other inverters. To achieve power scaling by connecting together multiple inverters, the controllers need to be not only capable of power sharing, but also to ensure that there are no high frequency effects such as resonances between inverters.

- Operate with other grid connected sources and loads. The controllers in emerging grid connected applications need to be designed with the intention of not disturbing other sources and loads, and there should be a method for evaluating if they will.

1.2 AIM OF RESEARCH

The focus of this research is to develop control methods for parallel grid connected inverter systems that satisfy the requirements listed in the previous section: high performance, power

scaling and grid-connectibility. The control methods and analysis should not only be effective at meeting the requirements, but also address the implications of applicability, reliability and reasonable cost. The controllers should be applicable using existing readily available state of the art hardware for the inverter platform; should be as reliable as a single smaller inverter; and have comparable cost to large inverter systems of similar ratings.

1.3 STRUCTURE OF THESIS

The thesis is broken into six sections. Chapters 2 through 4 review the application inverter requirements, the constraints imposed by the hardware, and the current methods for inverter control. Chapter 5 introduces a high performance discrete-time inverter controller for use with high power inverters, and includes proof of design. Chapter 6 provides in depth stability analysis of parallel connected inverters, uncovering stability constraints as a result of the control algorithms used and how to prevent them. Chapter 7 then continues by looking at the implications of grid connected inverter systems, such as how they are controlled, and more importantly, how to analyse high complexity systems with multiple sources and loads.

Chapter 2

INVERTER REQUIREMENTS

2.1 INTRODUCTION

Inverters are increasingly being applied to a wide range of different applications, and the performance and power requirements are continually increasing. This chapter first investigates the various applications inverters are being applied to. Having defined the performance and power requirements, the capabilities of the state of the art devices are reviewed and suitable devices are chosen to meet the application requirements.

2.2 INVERTER CONTROL MODES

Whether or not an inverter system consists of a single inverter module or an array of connected modules, at the Point of Common Coupling (PCC) to a grid an inverter system operates in one of two main modes, a current source inverter (CSI) or voltage source inverter (VSI). While most inverter systems operate in either one of these modes, typically the hardware for both is similar and it is possible to operate in a mixed mode. Both CSIs and VSIs exhibit some form of impedance, as shown in Figure 2.1. Low impedance systems are considered voltage sources, while high impedance systems act as current sources.

A voltage sourcing inverter is usefully described by the equivalent circuit shown in Figure 2.1b. Ideal voltage sourcing inverters are immune to loading, and would therefore have zero output impedance. In defining the voltage, voltage sources also define the frequency. Voltage sourcing

(a) Current Source (b) Voltage Source

Figure 2.1: Current and voltage sources.

systems are capable of acting as standalone grid sources as they can be used to define the grid voltage and fundamental frequency. As a result, most of the large power *sources* in grid systems are voltage sources and align their voltage and phase for power-sharing compliance.

A current sourcing inverter is usefully described by the equivalent circuit shown in Figure 2.1a. Ideal current sourcing inverters are immune to the external voltage, and would therefore have an infinite output impedance. Without any additional grid impedance current sourcing systems are unable to directly control the grid voltage and frequency, and are therefore most often used in applications where they are coupled to a load or source with a back emf. Typical applications include VSDs, static synchronous compensators, regenerative rectifiers and harmonic compensators.

2.3 APPLICATIONS

The two fundamental inverter modes are used to implement application specific systems. In each case a higher level control function is wrapped around the underlying CSI or VSI mode. Different applications have different requirements of the inverters response to an input reference and its output impedance. Often different applications are available that trade off certain features. For instance in some applications perfect response may be traded off against its operating efficiency.

2.3.1 Power Quality

Inverter systems are used in many power quality applications. Common applications are dual conversion systems, series-connected voltage sourcing system and shunt-connected current sourc-

ing systems.

Uninterruptible power supplies (UPS) are full conversion systems which use batteries to supply the load when the input supply sags or disappears. A CSI is used as the grid-connected rectifier that under normal operation charges the batteries, and a VSI is used to create a local grid for the load. The VSI is expected to have a low output impedance but does not need a fast reference (setpoint) response as it runs at a constant output voltage and frequency.

Series connected voltage sourcing systems, also known as Dynamic Voltage Restorers (DVR), are typically used in sag (and swell) mitigation and voltage regulation applications. A VSI is connected in series with the grid (transformer coupled) to provide active voltage adjustments. For voltage regulation applications the inverter is rated to the amount of regulation required. For instance a voltage regulator with a $\pm 10\%$ adjustment only needs to be rated at 10% of the load. The same applies to sag mitigation applications. For sag mitigation applications the reference response must be fast enough to respond to sudden voltage sags, typically in the millisecond range. The DC bus supply for series connected systems may be either via external storage or an additional supply. Although sag mitigation systems do not provide the same level of power security as UPSs, they have a lower operating cost footprint. Statistical analysis is often performed on the voltage quality history for a given application to determine if sub-perfect sag correction provided by series connected systems is acceptable due to the lower operating cost.

Shunt connected applications typically include Static Compensators (STATCOM), harmonic correction and power sourcing. STATCOMs typically source and sink VArs to provide voltage or power factor regulation at a common point of coupling in large grid systems. The STATCOM or power sourcing reference response is typically in the range of several milliseconds. Harmonic correction applications require a reference frequency response at least as high as the harmonics that are to be corrected. Where similar response rates are required VAr compensation, power

sourcing and low-order harmonic correction functionality may be incorporated into the same unit.

2.3.2 Frequency Converters

Frequency converter applications can contain a mix of fast and slow responding CSIs and VSIs. In applications where voltage and frequency support is not required CSIs are predominantly used as they can also provide other current sourcing functionality listed in the previous section. If voltage and/or frequency regulation is required voltage sourcing systems are required. These include applications where one of the inverters may be the only voltage source, or where multiple voltage sources are present and voltage/frequency droop is used (refer to Chapter 7).

In back-to-back applications where little or no DC storage is present, at least one of the inverters is required to regulate the DC bus. Typically at least one CSI is used as it provides a rapid response. The DC bus regulator provides power flow by either sourcing or sinking current from the DC bus to maintain its level.

Frequency converter applications have mixed range of response and impedance requirements, which are dependent on the different modes used. Current sourcing modes need a relatively fast response to ensure the DC bus is controlled in the presence of any load changes. Voltage sourcing systems have either a fixed output reference (standalone operation) or must provide voltage/frequency droop, which is an intrinsically slow response (similar to generator mechanical time constants). Standalone systems require a low output impedance to ensure low voltage distortion, whereas voltage/frequency droop applications require a relatively high inductive output impedance (refer to Chapter 7).

2.3.3 Distributed power

Examples of distributed power sources are large photovoltaic installations, fuel-cell systems, and battery energy storage systems. The inverter is typically used to couple DC sources or loads to a grid. The control response speed requirement for distributed power applications is similar to frequency converters. Distributed sources are often sparsely connected with little or no intercommunication aside from through the grid itself. They can either utilise CSIs where simple current sourcing is required, or VSIs can provide islanded grid operation.

In distributed power applications, depending on the geographical locations and the compatibility of different equipment, multiple inverters may be either coupled using high speed communication links or may only have the grid itself for power balancing. High speed communication links allow multiple separate systems to accurately balance their load, effectively operating as a large single system. Systems that provide power balancing using the traditional voltage/frequency droop method are subject to any associated stability implications.

2.4 DEVICE CONSTRAINTS

The applications discussed illustrate the requirement for high power inverters, and sometimes with high bandwidth as well. The various switching devices available for construction of inverters impose physical constraints that force a trade-off between power and bandwidth.

To produce high power inverters power electronic switching devices are used as they are the most efficient way of electronically controlling a voltage or current. In low power and high fidelity systems, such as audio amplifiers, linearly controlled devices are often used, but have a low efficiency due to dissipation in the devices. The bandwidth constraint that switching devices impose is the rate at how fast and often they can transition between the on and off states. The rate at which a device can transition is typically related to the inverse of how much power it can switch.

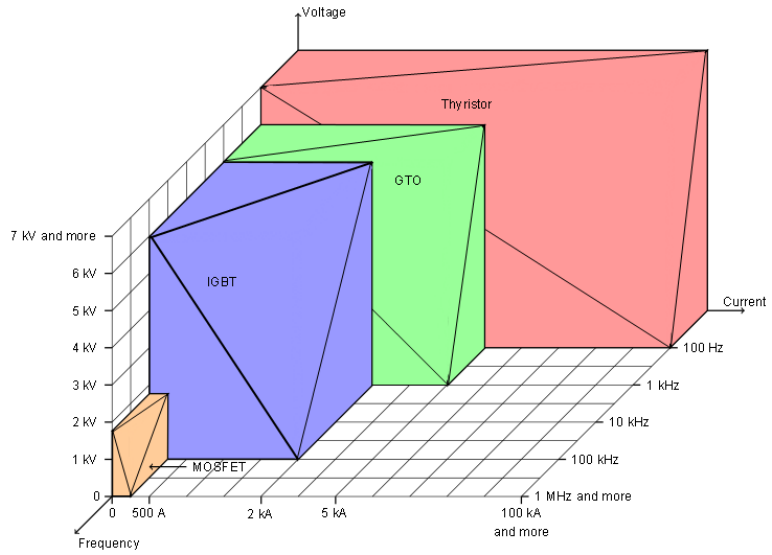


Figure 2.2: Modern power semiconductor device operating voltages and currents vs switching frequency. Information compiled from ABB [1] and Semikron [2] product catalogs.

For a given device there is an associated energy dissipation each time the device transitions between the on and off states. The greater the rate of transitions, the greater the switching energy dissipation, and how much energy a device can dissipate is determined by the physical structure of the device. The on-state losses, switching losses and the device package's ability to dissipate the losses are used to back-calculate a tolerable switching frequency.

Over the last 50 years a wide and mature range of power electronic switching devices have become available. They range from the high power but slow thyristor, invented in 1957; to high speed devices such as the MOSFET, invented in late 1970's. While the design and construction of the different devices varies, each provides a trade-off in terms of specification such as forward current capability, blocking voltage and switching frequency. Figure 2.2 shows the common voltage and current ranges against switching frequency for modern switching devices (at time of writing). Figure 2.3 shows more generally the switching power rating of modern devices versus switching frequency and where particular devices typically operate. While the development of new devices and the improvement of existing devices has in no way ceased or declined, new devices tend to offer finer granularity in Figure 2.3, while improved devices make incremental improvements by increasing the safe operating area boundary upwards.

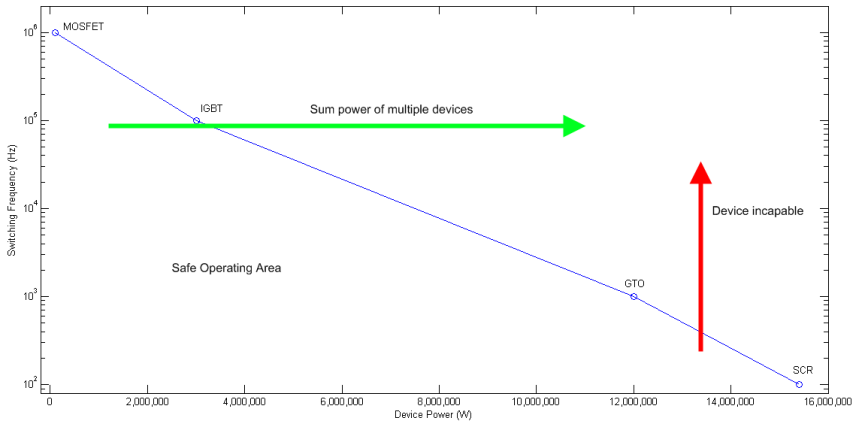


Figure 2.3: Modern power semiconductor device power vs switching frequency.

For the applications considered in the previous chapter, control bandwidths up to and above the the tenth harmonic are required. Of course to achieve a particular bandwidth, the switching device must switch at least twice as fast (Nyquist limit). In practice, the switching 'noise' created by switching devices must be filtered which at the same time hinders the available bandwidth. To achieve the bandwidths required in the previous chapter, from Figure 2.2 the only suitable devices for medium power applications are MOSFETs and IGBTs. While MOSFETs easily achieve the bandwidth requirements, it is simply impractical to scale them in parallel or series configurations to achieve megawatt power levels. IGBTs meet the bandwidth requirements and can also achieve high power levels, and as a result are often the switching device of choice for high power and high bandwidth applications. The control methods developed here in this thesis have been targeted at IGBT inverters that have switching frequencies around the ten kilohertz range.

The frequency calculation formula given in Appendix A can theoretically determine the maximum switching frequency and output power for a particular device. The results for a range of IGBT devices from various manufacturers are shown in Figure 2.4. The light blue line in Figure 2.3 that stands out in front of the rest of the data is from the original device power vs frequency plots presented in literature [4]. The distance between the literature quoted maximums for devices clearly highlights that although there are devices that can hit one of the limits

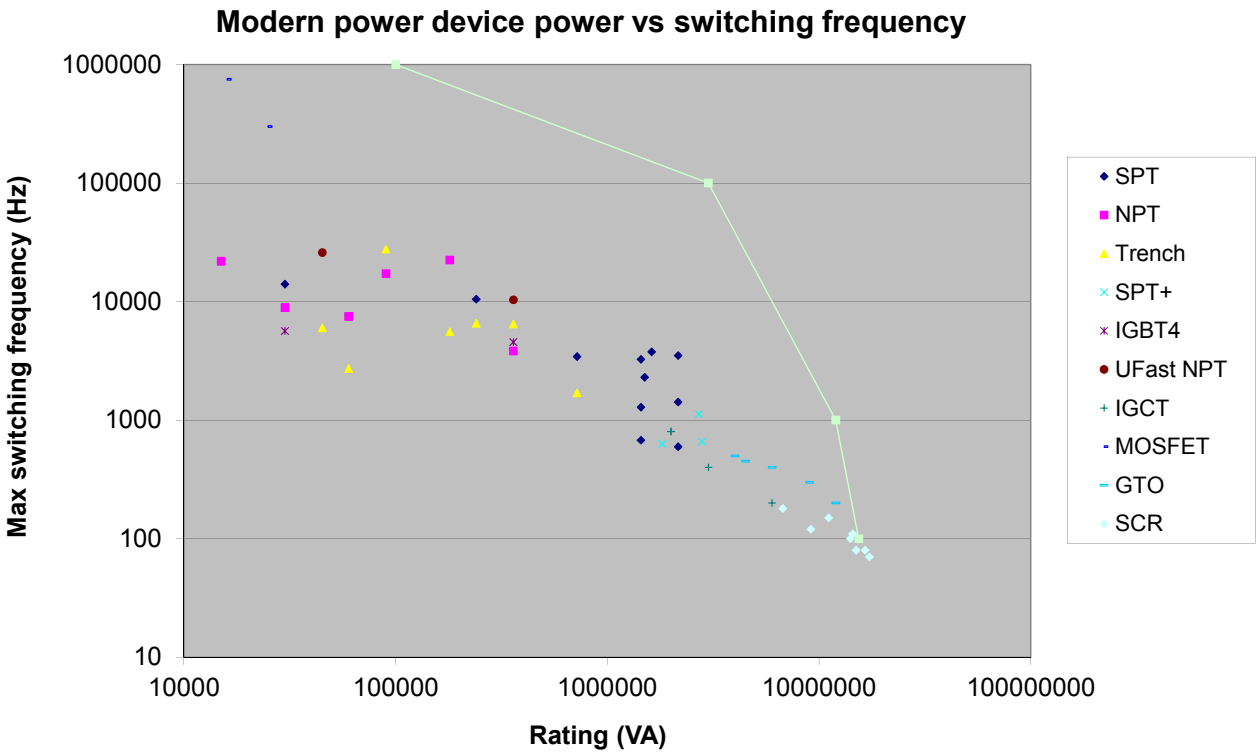


Figure 2.4: Actual modern device power vs switching frequency. (Note log scales)

such as current, voltage or frequency, there are no single devices that can simultaneously achieve all of these as suggested.

Given the channel bandwidth constraint for devices in Figure 2.3, to achieve greater power levels for a given device bandwidth multiple devices must be used. Naturally, device manufacturers package larger device dies into larger packages to achieve greater power ratings. Unfortunately however, devices can only be scaled up to a certain size before they geographically become too large to operate effectively. This is already employed by manufacturers of different device types. Majority carrier devices such as MOSFET intrinsically lend themselves to being paralleled, however, they lower on-state performance at higher voltages (¿200V). Minority carrier devices however, such as IGBTs, are are not easy to parallel and must be geographically close and have very similar characteristics (eg from the same manufacturing batch) to ensure current sharing [4].

2.5 CONTROL REQUIREMENTS

As the switching devices in an inverter are the only controllable power device, the device's bandwidth defines the inverter's maximum achievable control bandwidth. So for a given application that requires a minimum controllable bandwidth, either a device with a sufficient switching frequency is required, or multiple interleaved slower devices are required. While PWM-modulated devices provide an accurate voltage (on or off with a definable duty cycle), the output filters, which are low-loss inductors and capacitors, must be included in the control algorithm in order to prevent undesired resonance. As a result, high performance controllers must be used that offer the best inverter bandwidth for a given device switching frequency. For low power inverters (less than $\sim$ 1kW) high speed devices are often used that switch often well in excess of the required control bandwidth. However, for higher powered inverters the switching frequency of the devices can become a constraint.

In addition to achieving the greatest bandwidth for a given switching frequency, modern controllers are often required to be realisable in discrete-time so they can be used with digital processors. Digital processing devices such as Digital Signal Processors (DSP) and Field Programmable Gate Arrays (FPGA) are invaluable due to their ability to be reconfigurable. Being reconfigurable permits high complexity controllers that can be modified during run-time, however, due to the sampling nature of digital processors the controllers must be designed accordingly.

The design and implementation of existing inverter controllers is discussed in detail in Chapter 3. Later in Chapter 5 a high performance discrete-time controller is derived.

Herein an inverter's bandwidth is defined as its forward response: its output as a function of its input reference. An ideal forward response is a 0dB attenuation with no phase lag for all frequencies, but this is rarely achievable. Most forward responses roll off with a -3dB bandwidth defining frequency.

A controller's bandwidth is typically a linear transfer function in either continuous or discrete-

time. However, all inverters have actuator limits imposed by their bus voltage. These concepts and implications are further explored in Chapter 3.

Given the switching frequency constraints imposed by high power devices, the inverter power is traded off against its achievable bandwidth (a function of its switching frequency). To increase the power beyond that of a single device while still maintaining a certain switching frequency, devices have to be connected in parallel (or series).

This thesis is primarily concerned with actively paralleled inverter configurations to achieve an increase in inverter power while maintaining a control high bandwidth. In Chapter 6 the outcomes regarding actively paralleled inverters in [5] are further investigated.

Actively paralleling inverters not only enables higher powered inverter systems for a given control bandwidth. By using distinct modules of a fixed size, inverter systems of a wide range of powers can be constructed by simply adding more modules, whilst maintaining a high control bandwidth. This has significant manufacturing advantages as it means that a wide range of products can be made using the same module. The maximum power limitation is only constrained by how many modules can be connected in parallel. The limitation on the number of modules that can be connected in parallel is related to how they are connected together and their control strategy. In Chapter 6 investigations uncover stability constraints that are a based on the interconnecting impedance between a given type of actively paralleled inverter. If the stability constraints are appropriately managed then the maximum number of parallel modules is only constrained by size and by the mechanism for propagating reference signals to the modules.

A key consideration when developing a modular system is the individual module size. Again this decision comes back to the availability of devices, their power rating and switching frequency. The available device packages dictate how much power a device can dissipate and therefore what power and switching frequency can be used for a given enclosure's ability to dissipate heat.

Conceptually, implementing parallel or series configurations is quite simple. If ideal sources are

used, in the case of parallel configurations current sources ($Z_o = \infty$) must be used, whereas for series configurations voltage sources ($Z_o = 0$) must be used. In practice however, it will be later shown that ideal sources are not achievable. In certain applications it may be advantageous to implement parallel configurations using voltage sources, in particular this is useful if the inverter array will be used as a voltage source. In a parallel configuration where the input voltage references are the same (or similar) it is possible to use voltage sources with low output impedances without large current imbalances. If two voltage sources similar to that shown in Figure 2.1b are connected in parallel and assuming $Z_{o,1} = Z_{o,2}$, the unbalanced current ΔI from one module to the other module is simply:

$$\Delta I = \frac{V_1 - V_2}{Z_o} \tag{2.1}$$

Later in Chapter 4 the derivation of a continuous-time VSI is discussed and in particular how the controller implementation lends itself to being used in parallel configurations. The advantages and disadvantages of different parallel VSI implementations are further discussed in Chapter 6.

2.6 RELIABILITY

When producing industrial equipment one of the key considerations is reliability. For the often high-uptime applications and the 20+ year life cycles expected of industrial equipment, inverter manufacturers must be able to ensure a high reliability product. The reliability of an inverter configuration is the probability of the system—which may include many inverters in a single system—being operational.

Many different characteristics contribute to a product's reliability. Each individual component used in a product, the way in which they are assembled, and the manner in which they are enclosed and the environment they are in, all contribute to the system's reliability. A common misconception is that individual, one-off, hand-made products are of the best quality, and that

therefore they have a high reliability. On the contrary, products manufactured in high volume where continued refinements can be made typically offer a much higher reliability. This is evident in the consumer electronics and automotive industries. For many high power electrical systems however, each scenario is often quite different and it may be hard to standardise on one product. Inverter systems that can be connected in parallel or series to offer power scalability have the advantage of being able to be used in many different applications, especially if the common inverter modes (CSI and VSI) are easily configurable.

While large arrays of inverters (parallel or series) lend themselves to manufacturing in high volumes, unfortunately they also present a high degree of complexity. Increased complexity can, if not appropriately managed, lead to reduced product reliability. If the complexity of a component can be abstracted, such that a well-defined simplified model can be used, then the increased complexity may be potentially mitigated. A good example is of parallel inverter modules. While each inverter may include many components including the power electronic devices, the controller, transducers, communications links, etc, the complexity can be abstracted by setting up the module to do a single defined task, such as a VSI or CSI. In this manner the complexity of all the different components is abstracted to the module's output impedance and its forward response. The abstraction also allows the components, controllers and algorithms to be different between different inverters as long as they all behave in the same manner.

The ability to abstract complexity is further discussed in Chapter 6 and [5] regarding actively and passively balanced parallel inverters. The actively controlled configuration, where each module has its own controller and transducers, despite being intrinsically more complex is able to sufficiently abstract the component complexities, allowing the modules to be paralleled without any power derating. The passively balanced parallel system, however, not only has to be derated, but the implemented systems exhibit a higher rate of failures. At time of writing, the test hardware in Appendix G which uses actively paralleled inverter modules has demonstrated zero

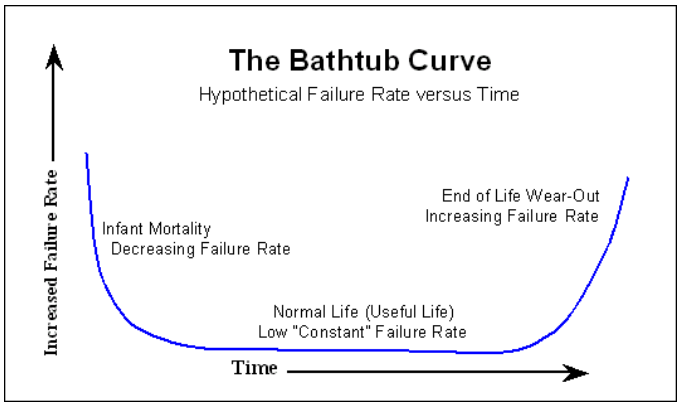


Figure 2.5: Unit reliability "Bathtub" curve.

module failures in the field, with a range of systems from single to up to 32 parallel modules. The previous generation of passively paralleled systems, with a similar number of products in the field, have demonstrated a greater level of failures where multiple parallel devices are used, while still using similar manufacturing techniques. Due to the tight coupling between devices in the passively paralleled system, when they did fail, the initial failure of one device would inevitably destroy the remaining paralleled devices, whereas during testing failures in the actively paralleled system were confined to a single failed module.

The reliability for equipment is often defined by its Mean Time Between Failures (MTBF). MTBF figures represent the average lifetime of a unit, where a 'unit' is a single piece of hardware such as an inverter module). For most equipment where the failure distribution is exponential, the MTBF is simply the reciprocal of the failure rate λ. Most units typically have a failure rate that follows the "bathtub" curve, as shown in Figure 2.5. The area of the bathtub curve that MTBFs typically refer to is the flat area in the middle where the failure rate is constant. MTBF calculations in Appendix B show that inverter arrays with redundant modules can deliver MTBFs that are proportion to the square of monolithic inverter MTBFs.

Industrial equipment can have life cycles that are decades long. In this time however, components required for constructing new or maintaining existing equipment may become obsolete and may no longer be available. This commonly happens with emerging technology devices which are

constantly being improved. Unfortunately for high reliability industrial systems not only do replacement components need to be rigorously tested, there simply may no longer be suitable replacements. For industrial systems with life cycles of thirty-plus years, obsolete components is not only a risk, they are inevitable.

As introduced in Section 2.5 in large inverter systems it is common to parallel multiple devices to achieve a greater current capacity. In passively controlled systems (detailed in Section 3.5) the similarity of devices is exploited to ensure current sharing. The paralleled devices are matched, often from the same production run, to ensure current balance. However, when these systems fail catastrophically, even if they do not destroy every paralleled device (which they commonly do), every device has to be replaced to ensure current sharing. If one of the devices becomes obsolete the entire system may have to be replaced.

2.7 SUMMARY AND DISCUSSIONS

Different inverter applications have different performance and power requirements. Common applications such as STATCOMs, distributed generation and frequency converters have sub-cyclic response requirements requiring both high performance semiconductor devices and high power capability. Grid connection and frequency converter applications can have continuously varying power requirements stipulated by the grid conditions. Power quality applications have to respond in sudden transients in often under a millisecond.

An inverter with a fast response rate requires a switching devices with a fast switching frequency. The study of various power electronic devices indicates an inverse relationship between device switching frequencies and power switching capability. While power requirements can be met with low power devices by parallel or series connection, increasing the switching frequency is limited by the device. As a result, devices which can achieve the minimum switching frequency are chosen, and for the applications addressed herein the IGBT is the optimum device.

If device power sharing is controlled in parallel or series connected systems, another advantage of having multiple identical hardware units emerges which is manufacturability and reliability. Continued manufacturing of identical items leads to increased reliability, manufacturability and, as a roll-on effect, cost.

Following the investigation of achieving a high performance inverter from parallel or series connected systems, the next chapter investigates how current state of the art inverter controllers are designed and explores their associated constraints.

Chapter 3

INVERTER DESIGN

3.1 INTRODUCTION

Having defined the key requirements for different inverter applications, the components for implementation of an inverter are now defined and developed. As expected, over time improved components have allowed not only more powerful and more compact designs (for a relative power rating), but have also permitted different topologies and control techniques which may have been previously restricted to theoretical analysis. New components and techniques also present different constraints to control design.

State of the art inverter implementation requires detailed design which considers the power electronic components, the digital controller, and the interfaces between them. This chapter details the various processes and components involved, and the associated constraints imposed by each of these. Firstly the fundamental principles for inverter design are discussed, and then how the designs are extended, for example to three-phase or parallel systems. Individual key components which must be addressed when designing digital controllers are reviewed and their associated constraints are presented. Performance indices for benchmarking controllers are then discussed.

3.2 DESIGN AND IMPLEMENTATION

The inverter design follows an iterative process which typically involves the following steps:

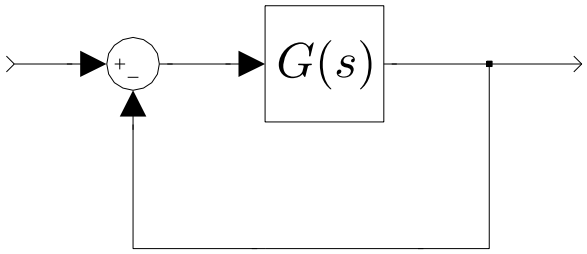


Figure 3.1: Closed-loop system in negative feedback.

- Theoretical design and analysis.
- Numerical testing.
- Physical implementation.
- Roundtrip verification to test and confirm the operation against numerical investigations.

While inverter hardware topologies can be configured to be either a voltage source or current source, by closing the loop (controlling) the output filter can produce either a voltage or current sourcing output. For instance, current sourcing operation from a voltage sourcing topology can be achieved by implementing it with a current control loop. Multiple voltage and current control loops can be cascaded in applications consisting of multiple filter elements, such as an LC filter. Herein this thesis the hardware topology is assumed to be a standard three-phase voltage configuration, although the concepts are equally applicable to current sourcing topologies.

3.3 CONTROL FUNDAMENTALS

In this section the key concepts of linear control systems are reviewed [6]. Primarily all linear control systems stem from the closed-loop negative feedback system as shown in Figure 3.1, which is trivially simple. Beyond a simple linear closed-loop system, practical realities introduce complexity and non-linearity. This section deals with differing techniques common in analysing control systems, specifically continuous-time and discrete-time systems, and also the delays inherent in both of these. Often an additional cause of delays are the parasitic elements typically

present in inverter systems, such as computational delays, sampling delays and those introduced by the modulation process. Finally the methods for dealing with multi-phase systems are detailed in Section 3.3.4.

In three-phase AC systems the voltage and current vectors are often represented in a rotating reference frame (Section 3.3.4) allowing the signals to be treated as DC signals. An exception is discussed in Section 4.2 where integrators and resonators are used for eliminating steady-state errors.

The controllers discussed and developed in this thesis are primarily concerned with Linear Time Invariant (LTI) systems which can be expressed and analysed using transfer functions. Non-linear control systems such as hysteretic systems are beyond the scope of this thesis. In addition to LTI systems, pure delays in continuous-time are also examined.

3.3.1 Continuous-time systems

Continuous-time systems are herein modelled in the frequency domain using the Laplace differential notation, where s is the Laplace operator. Continuous-time systems and control loops have historically been the most common representation of systems as they are the easiest to comprehend. They provide simple models for practical systems, including electrical and mechanical components. Frequency response is found by using the conventional Laplace evaluation of $F(s)$ at $s = j\omega$.

To briefly review, when analysing continuous-time systems the poles and zeros determine the response of the system, while the poles alone govern the stability of the system. For continuous-time systems a pole or zero has a natural frequency ω_0, and if it is a complex pole-pair it also has a damping ratio ζ. For real poles and zeros the natural frequency is its magnitude, whereas for a complex pole-pair the natural frequency and damping ratio are given by:

$$s^2 + 2\zeta\omega_0 s + \omega_0^2 = 0 \tag{3.1}$$

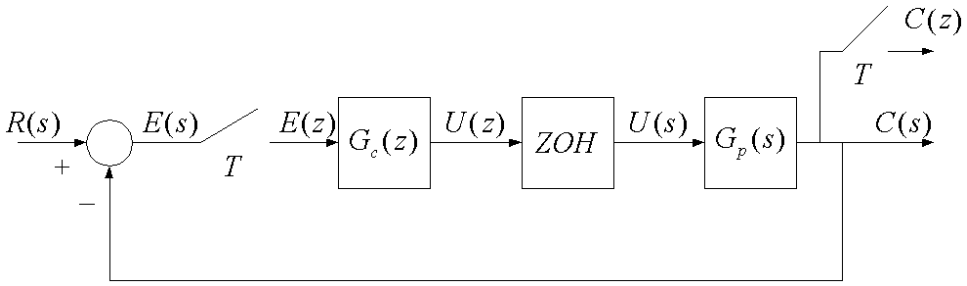


Figure 3.2: Example of a mixed discrete and continuous-time sampled system.

While Laplace operators are ideal for modelling linear continuous-time systems, non-linear components common in inverter controls, such as transport delays, cause these systems to become computationally complex. In the Laplace domain a transport delay τ is represented as $e^{-s\tau}$. Frequency responses for systems with delays may still be evaluated, allowing the use of Bode and Nyquist diagrams, but the non-linear nature makes analysis difficult.

Despite their non-linear nature, there are several methods for dealing with delays in systems. In the Laplace domain a common method is by means of a Padé approximation which approximates the delay with an n-order linear system. Second or third order approximations typically achieve results to within 1% at low frequencies, but with the disadvantage that the system order is significantly increased.

Despite its non-linear nature, the Lambert W function can be used to solve non-linear equations which involve exponentials. The Lambert W function is the multivalued inverse function of $y = W(x)e^{W(x)}$. Its exponential relationship allows analytical solutions to be found for simple systems with delays. Unfortunately application of the Lambert W function becomes non-trivial as the system order increases. Several examples provided in the literature [7, 8] document the use of the Lambert W function with higher order systems.

The application of the Lambert W Function to closed-loop control systems is given in Appendix C.

3.3.2 Discrete-time systems

Discrete-time sampled systems are herein modelled and analysed in the Z domain, using the Z discrete notation, where z is the Z operator and z^{-1} is a unit delay. When analysing mixed continuous and discrete-time systems, discrete-time analysis is used. Figure 3.2 illustrates the typical scenario of a discrete-time system, where $G_c(z)$ is a discrete-time transfer function and $G_p(s)$ is a continuous-time transfer function. To analyse mixed continuous and discrete-time systems, the continuous-time system is first discretised. The complete closed-loop system in Figure 3.2, including all appropriate delays, may then be analysed in discrete-time.

Due to the sampling process, discrete-time systems are often less intuitive than similar continuous-time systems, although thankfully most LTI systems in nature are fundamentally continuous-time based. This of course includes electric components. When analysing mixed continuous and discrete-time systems, the simplest approach is to design discrete-time systems which operate in a similar manner as continuous-time systems. For this reason transforms which provide mappings between continuous and discrete-time are employed.

For transitions between continuous and discrete-time systems, the Analog to Digial Converter (ADC) and Pulse Width Modulation (PWM) transitions in inverter systems insert Zero Order Hold (ZOH) sampling delays. ZOH discretisation is performed using the common process:

$$G_{p,ZOH}(z) = \mathcal{Z}\left[\mathcal{L}^{-1}\left\{\frac{1-e^{-sT_s}}{sT_s}G_p(s)\right\}\Big|_{t=kT_s}\right] \tag{3.2}$$

$$= \left(1-z^{-1}\right)\mathcal{Z}\left\{\frac{G_p(s)}{s}\right\} \tag{3.3}$$

Where $\mathcal{Z}\{\}$ and $\mathcal{L}^{-1}\{\}$ are the Z and inverse Laplace transforms respectively. T_s is the discrete sample period. Delays which are an integer multiple of the sample period are simply added as z^{-n}, whereas fractional delays can be converted using the Advanced Z transform.

3.3.3 Parasitics

In practical systems all components have some form of parasitic effect. Most parasitic effects are trivial and although they may be considered during the physical design, most have little or no effect on a system's overall closed-loop control. There are however, some parasitic effects which do have significant effects on control systems and must be considered. The most common parasitic effects which can affect inverter control systems are device deadtimes, parasitic inductances, inductance non-linearity (due to saturation), and transducer errors.

During the design phase each parasitic effect is evaluated and design choices are made in order to minimise the effect on the overall control response. In all practical systems however, it is not possible to eliminate all parasitic effects, and therefore robust controller designs which have a high immunity to parasitics are required. The most significant parasitic effects which affect control systems are transducer errors. Both voltage and current transducers are often exposed to large common-mode $\frac{dV}{dt}$ and $\frac{dI}{dt}$ relative to the differential signals they are sensing. Current transducers with a sufficiently high common-mode rejection ratio, suitable to be used in inverter control systems have only become available in the last decade as a result of the development of high quality Hall Effect sensors. Even with improved transducers, inductor current signals intrinsically have a high ripple as a result of being directly connected to the switching devices. One method of improving control robustness to transducer errors is to simply reduce the number of transducers required and to ensure that the ones which are used have a high immunity to disturbances. An example of only using voltage feedback is the controller designed in Chapter 5. Inductor current feedback is used only to to provide current limiting.

3.3.4 Multiphase systems

With the exception of a few applications, such as locomotive traction applications, above a few kilowatts most electrical systems are typically three-phase. At a national grid level all loads

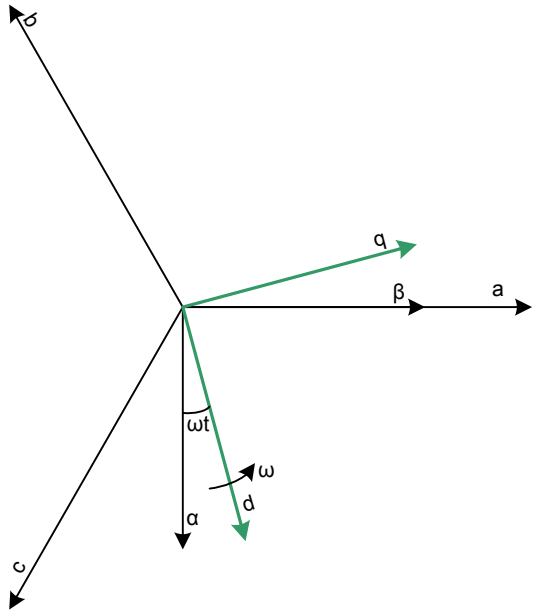


Figure 3.3: Three-phase stationary and rotating reference frame coordinate relationships.

and sources are strictly three-phase. Given that the inverter systems described in this thesis are designed for application to high power grid-connected systems, their implementation is based on three-phase hardware. When dealing with three phase systems where the three-phases each have a 120 degree separation rotating at a fundamental frequency (usually 50 or 60Hz), vector notation is used to describe the trajectory of each phase.

Herein, for the stationary reference frame the three individual phases (*abc* frame) are projected onto two axes denoted $\alpha\beta$ (alpha-beta) with a separate zero sequence axis. This thesis is only concerned with three wire systems where the zero sequence component is uncontrolled and therefore neglected. In many applications the $\alpha\beta$ stationary axis is projected onto the two rotating axes, denoted the *dq* axis (direct-quadrature). The convention used in this thesis is that the *q*-axis is aligned to the real component and the *d*-axis lags by 90 degrees (and is on the imaginary axis), the same as the convention used in machine modelling where the *d*-axis is aligned to the synchronous machine salient rotor. Figure 3.3 shows the relationship between these three reference frames. The reference frame transforms for three-phase variables are the

Clarke (eqns 3.4 and 3.5) and Park transforms (eqns 3.6 and 3.7), respectively, defined as:

$$\begin{bmatrix} v_\alpha \\ v_\beta \\ v_0 \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{\sqrt{3}} & \frac{1}{\sqrt{3}} \\ \frac{2}{3} & -\frac{1}{3} & -\frac{1}{3} \\ \frac{1}{3} & \frac{1}{3} & \frac{1}{3} \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \tag{3.4}$$

$$\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \begin{bmatrix} 0 & 1 & 1 \\ -\frac{\sqrt{3}}{2} & -\frac{1}{2} & -\frac{1}{2} \\ \frac{\sqrt{3}}{2} & -\frac{1}{2} & 1 \end{bmatrix} \begin{bmatrix} v_\alpha \\ v_\beta \\ v_0 \end{bmatrix} \tag{3.5}$$

$$\begin{bmatrix} v_d \\ v_q \end{bmatrix} = \begin{bmatrix} \cos\phi & \sin\phi \\ -\sin\phi & \cos\phi \end{bmatrix} \begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} \tag{3.6}$$

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \begin{bmatrix} \cos\phi & -\sin\phi \\ \sin\phi & \cos\phi \end{bmatrix} \begin{bmatrix} v_d \\ v_q \end{bmatrix} \tag{3.7}$$

Often when using two-axis models for the stationary ($\alpha\beta$) and rotating (dq) reference frames, complex vector notation is used. This further simplifies the $\alpha\beta$ to dq projection which is inherently a frequency shift. The transformation equations 3.6 and 3.7 can then be written:

$$\mathbf{v}_{dq} = e^{-j\theta}\mathbf{v}_{\alpha\beta} \tag{3.8}$$

$$\mathbf{v}_{\alpha\beta} = e^{j\theta}\mathbf{v}_{dq} \tag{3.9}$$

$$\text{Where} \quad \theta = \omega t \tag{3.10}$$

When referring to three-phase systems in the stationary reference frame, unless specifically mentioned the $\alpha\beta$ frame is used rather than the abc frame. In digital systems the use of the Clarke transform is often assumed and may not be explicitly mentioned. As the Park transform performs a frequency shift and requires knowledge of the fundamental frequency, the use of a Phase Locked Loop (PLL) will either be implied or specifically mentioned.

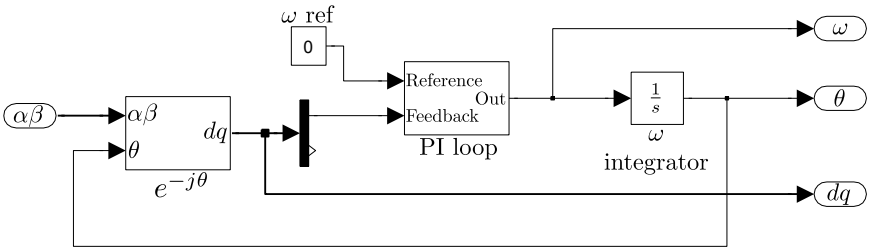


Figure 3.4: PLL model.

A PLL is typically used to lock to a reference voltage (often the grid voltage). The PLL implements a proportional-integral (PI) controller which seeks to zero the d-axis component, synchronising to a given frequency, usually the fundamental. In most power electronic applications the fundamental frequency is positive sequence 50 or 60Hz. The PLL form is shown in Figure 3.4 and the effects of PLLs in grid-connected inverter applications are explored in Chapter 7.

When designing multiphase controllers a decision has to be made as to which parts of the controller will be implemented in each reference frame, specifically the $\alpha\beta$ and dq reference frames. In some applications it is often advantageous to implement different parts of the controller in different reference frames. The use of a particular reference frame is specific to different applications. There are several applications where the choice of a particular reference frame is obvious, and other applications where there may be cases for using either.

Due to the mathematical relationship between reference frames, representations of electrical components, for example in simulation or a state observer, may be implemented in either reference frame. Usually a particular reference frame may have a simpler representation. Electrical components modelled in the $\alpha\beta$ frame are independent on each axis (no cross coupling), but have cross coupling terms in the dq frame. For example an inductor with admittance $\frac{1}{sL}$ has no cross coupling in the $\alpha\beta$ frame, but when frequency shifted to the dq frame the admittance is $\frac{1}{L(s-j\omega)}$, where the imaginary component becomes a cross coupling term.

Mechanical machines couple torque and flux to the individual electrical rotating axes d and q respectively, which results in an asymmetric model in the d and q-axis. In electrical sys-

tems real and reactive currents relate to the q and d axes respectively, favouring the dq frame representation.

Often there is a tendency to implement a controller in the dq frame as the frequency shifting effect allows the fundamental AC signals to be treated as DC signals, thereby permitting the use of easier to understand components such as integrators and differentiators. The use of a resonator in the $\alpha\beta$ frame is inherently more complex than an integrator. In systems where only positive sequence is of interest, such as machines, integrators in the dq frame are an appropriate choice. If both positive and negative sequence components are of interest the $\alpha\beta$ frame is well suited as simple uncoupled resonators operate on both the positive and negative frequency components.

When implementing three-phase systems, modulation schemes such as Space Vector PWM (SVPWM) or Third Harmonic Injection PWM (THIPWM) achieve a greater line to line modulation index by effectively injecting a zero sequence component. Both SVPWM and THIPWM inject a triplen-frequency component [6]. SVPWM injects a triangular component whereas THIPWM injects a sinusoidal component. Both methods have the effect of increasing the maximum modulation depth from 1.0 to 1.15 $\left(\frac{2}{\sqrt{3}}\right)$.

3.4 INVERTER ELEMENTS

This section details the core hardware elements which combine with the control concepts to complete an inverter. To control any system the control system provides actuator references to the core elements. In the case of an inverter the actuator is the PWM controlled switching stack, and the core elements are the filter components and the load. The three main parts of an inverter are the PWM switching converter stack, the output filter and load, and the controller interface.

3.4.1 PWM

Fundamentally PWM modulators provide an almost perfect voltage amplifier, where the output voltage is a defined ratio of the input voltage (typically a DC bus). For digital modulutors, the resolution and accuracy are defined by the carrier resolution, and any switching parasitics such as deadtimes. In systems with stiff DC bus voltages PWM provides an almost perfect voltage source. Unfortunately the almost perfect amplifier characteristic is polluted with both common-mode and differential-mode switching noise. While the common-mode noise can be referred to either the AC or DC side, the differential-mode ripple must be filtered to achieve the underlying reference waveform.

Aside from producing a signal with a modulated signal where the pulse width is relative to the reference signal, PWM modulators come in several different varieties. The key differences are the carrier wave shape (triangular or sawtooth) and the sampling method (natural or regular). Without loss of generality the analysis in this thesis only deals with triangular (symmetric) carrier wave shape for use in generating three-phase voltage references, and generated PWM signals are typically used to directly control the gate drive signals driving the switching stack.

The difference between natural and regular PWM is that for natural PWM the input reference is sampled in continuous-time, whereas the regular sampled PWM is only sampled either once or twice per switching period (each half of the triangular carrier wave). In practice due to the discrete-time nature of digital controllers, true natural digitally controlled PWM is not achievable. That said, it is possible to implement PWM modulators which calculate and update at rates greater than the carrier frequency. Herein the convention of a nomalised PWM carrier top and bottom is +1 and -1 respectively, therefore a reference signal of 0 produces a 50% duty cycle.

Theoretically, due to their continuous-time nature and lack of delays (apart from propagation delays), natural PWM modulators have an infinitely wide bandwidth for any single chosen carrier

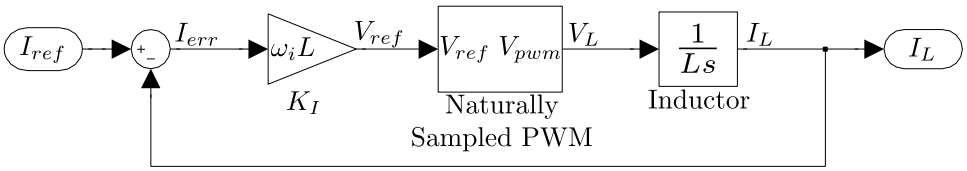


Figure 3.5: Current controller with naturally sampled PWM.

frequency. Unfortunately, to achieve this a natural PWM modulator has no limitation which restricts the switching frequency to the carrier frequency. If the reference signal intersects the carrier more than twice in one carrier period then the switching frequency will go beyond that of the carrier, therefore natural modulation only imposes a minimum switching frequency equal to the carrier frequency (or lower during over-modulation).

To constrain the switching frequency to the carrier frequency, the reference and carrier signals must only intersect twice per carrier period (once for the rising edge and once for the falling). This is achieved by constraining the slope of the reference signal to be less than that of the carrier. For a closed-loop control system the slope constraint can be used to constrain the control variable (typically its bandwidth). Figure 3.5 shows a simple continuous-time, naturally sampled current controller operating into a short circuit. Given that the carrier triangle wave has one rising and one falling slope per period between the top and bottom values, the carrier slope $\frac{\Delta V_{pwm,carrier}}{\Delta t}$ is:

$$\frac{\Delta V_{pwm,carrier}}{\Delta t} = \pm\frac{4}{T_s} = \pm 4 f_s \tag{3.11}$$

The slope of the PWM reference signal $\frac{\Delta V_{pwm,ref}}{\Delta t}$ is:

$$\frac{\Delta V_{pwm,ref}}{\Delta t} = K_I \left(\frac{\Delta I_{ref}}{\Delta t} - \frac{\Delta I_L}{\Delta t} \right) \tag{3.12}$$

The slope of the inductor current $\frac{\Delta I_L}{\Delta t}$ in this scenario is governed by the PWM modulator

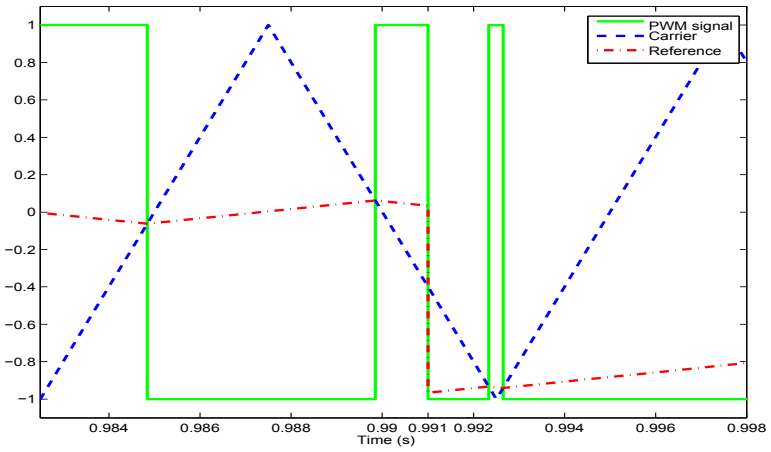


Figure 3.6: Natural PWM mid-period update.

output voltage V_L, which is either +1pu or -1pu, resulting in the slope:

$$\frac{\Delta I_L}{\Delta t} = \pm\frac{1}{L} \tag{3.13}$$

Constraining the PWM reference signal slope to be less than or equal to the carrier slope gives the following relationship for the rising edge:

$$\frac{\Delta V_{pwm,carrier}}{\Delta t} \geq \frac{\Delta V_{pwm,ref}}{\Delta t} \tag{3.14}$$

$$4f_s \geq \omega_i L\left(\frac{\Delta I_{ref}}{\Delta t} - \frac{1}{L}\right) \tag{3.15}$$

$$\therefore \omega_i \leq \frac{4f_s}{L\frac{\Delta I_{ref}}{\Delta t} - 1} \tag{3.16}$$

Where ω_i is the controller bandwidth.

From equation 3.16, for a DC system where the controller input reference signal remains unchanged $\left(\frac{\Delta I_{ref}}{\Delta t} = 0\right)$ the switching frequency will not exceed the carrier frequency as long as the controller bandwidth ω_i is less than four times the carrier frequency. It is worth noting that equation 3.16 is only the worst case scenario as small input reference changes may not necessarily cause a switch to occur. This simple naturally sampled PWM scenario, with no delays, gives an indication of the likely best-case scenario upper limit for a CSI bandwidth.

In practice only analog systems can realistically achieve almost zero-delay continuous-time feedback systems. Digital systems with close to this performance can be achieved by sampling at a greater rate than the carrier frequency, known as oversampling. In digital applications further complications arise as a result of how the PWM modulator is implemented. Most if not all PWM peripheral modules in microcontrollers and DSPs use equality comparators rather than magnitude comparators. In most applications a PWM reference signal is only updated once or twice per period and at the top or bottom carrier values (regular sampled PWM), so as the PWM carrier counter increments (or decrements on the falling slope) it is guaranteed to at some point be equal to the reference value and cause a PWM switch event. In naturally sampled systems the reference is updated more than twice per switching period and if the reference value is again updated during the same carrier period the updated value may be on the other side of the carrier waveform causing an immediate switching event. If an equality comparator is used this type of event would be missed or would have to be performed in software. Figure 3.6 is an example of a mid-period reference update at time 0.991 which causes an immediate switching event. If an equality comparator was used in the PWM module this switching event would have been missed. Figure 3.6 also illustrates a reference change which doubles the switching frequency for one period.

By only updating once or twice per period the reference signal is effectively zero order held, as proven in [9]. Frequency response expressions for a ZOH are given in Appendix D. As a regular sampled PWM has the same small-signal response as a ZOH module, it is sufficient to use the ZOH discretising method when analysing mixed sample time systems which use PWM. This assumption only applies to small-signal analysis and is further discussed in Section 3.4.2.

3.4.2 Filter

As mentioned in Section 3.4.1, PWM modulators provide an almost perfect voltage source, except their output voltage is polluted with common-mode switching noise. The use of a filter

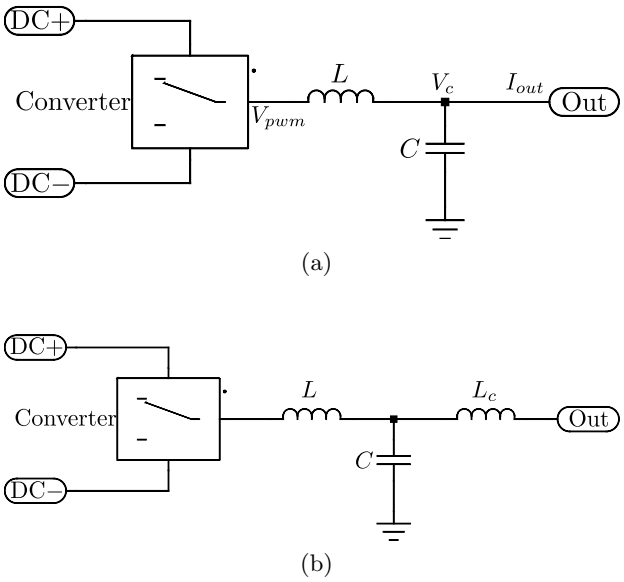


Figure 3.7: Common filter configurations.

on the output of the PWM voltage source allows the differential switching noise to be removed or minimised at the cost of additional output impedance. These filters comprise inductors in series to filter voltage ripple and capacitors in shunt to filter current ripple. The sizing of filter components directly relates to the voltage and current ripple and also directly relates to the large-signal bandwidth. While usually intended to filter only switching ripple, the filter will also inadvertently filter the modulation reference.

LC filters are also intrinsically resonant and must be actively or passively damped to prevent ringing. Passive damping is typically achieved with resistors. In high power systems, losses at levels of even a few percent may be unacceptable. Active damping methods are able to dampen resonances without dissipating energy, and instead return all filter energy to the system.

For continuous-time systems a filter's impedance is relatively easy to derive. The two most common filters in use today are the LC and LCL filters shown in Figure 3.7. The LC filter output voltage (voltage across the capacitor V_c) as a function of the PWM voltage V_{pwm} and output current I_{out} is given as

$$V_c(s) = \frac{V_{pwm}(s) - I_{out}(s)sL}{LCs^2 + 1} \tag{3.17}$$

The LCL output current as a function of the PWM voltage and output voltage V_{out} is given as

$$I_{out}(s) = \frac{V_{pwm}(s) - V_{out}(s)(1 + LCs^2)}{s(LCL_cs^2 + L + L_c)} \tag{3.18}$$

When analysing converters in discrete-time the filter must first be discretised using the ZOH method. Due to its prominent use in later chapters, the discretised LC filter voltage, using equation 3.3, is provided here as:

$$\begin{aligned}
\frac{V_c(z)}{V_{pwm}(z)} &= \mathcal{Z}_{ZOH}\left\{\frac{1}{LCs^2+1}\right\} && (3.19)\\
&= \mathcal{Z}\left\{\frac{1-e^{-sT_s}}{sT_s}\frac{1}{LCs^2+1}\right\} && (3.20)\\
&= (1-z^{-1})\mathcal{Z}\left\{\frac{1}{s(LCs^2+1)}\right\} && (3.21)\\
&= \frac{(z+1)(1-\cos(\omega_n T_s))}{z^2 - 2z\cos(\omega_n T_s) + 1} && (3.22)\\
\text{Where} \quad \omega_n &= \frac{1}{\sqrt{LC}} && (3.23)
\end{aligned}$$

Delays that are integer multiples of the sample period (T_s) are added as z^{-1}, and ratio delays can be incorporated when the filter is discretised, using the Advanced Z Transform.

3.5 INVERTER TOPOLOGIES

While different inverter topologies are regularly developed, they all fundamentally operate by transforming voltages and currents using devices which can be actively switched from an off state to an on state, and vice versa. This thesis concerns itself with the control of AC/DC converters, either as current sources or voltage sources. In each case a DC bus is chopped and then filtered using at least a second-order LC filter.

Without lack of generality the control analysis derivations are not particular to a fixed switch stack. In Section 3.4.1 the PWM analysis referred to two-level systems, but any stack which provides a ZOH response is applicable to the control analysis in the later chapters. Applicable

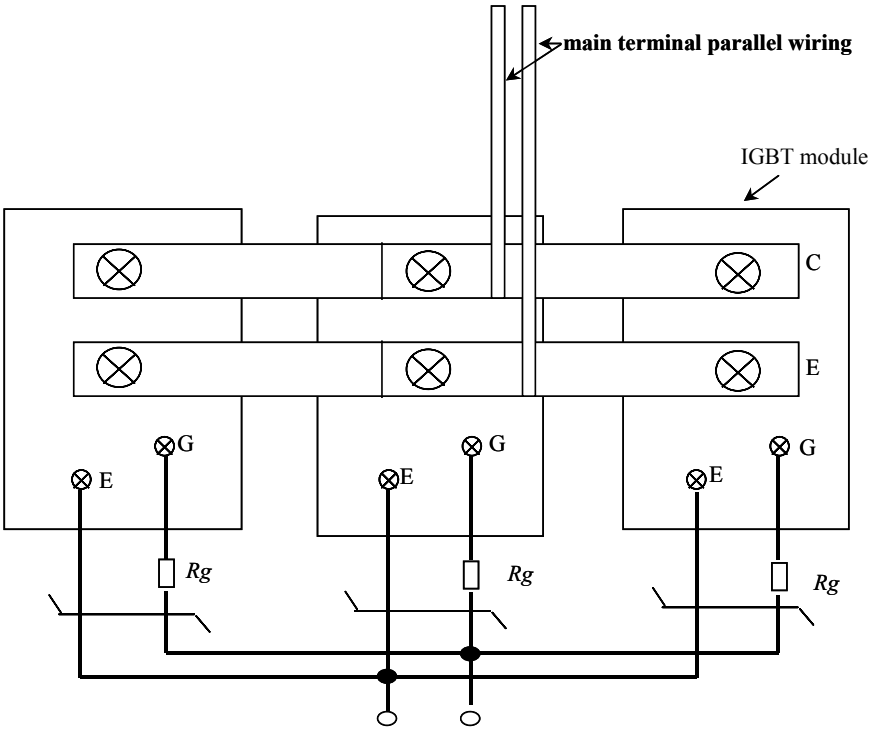


Figure 3.8: Parallel monolithic IGBT topology [3].

systems are multi-level stacks which can produce the reference voltage at the next sample point. For example, interleaved systems which have the same sample rate as the PWM period exhibit a moving average response based on the number of interleaved modulators. Due to the effects of the switching ripple, the modulator has to be taken into account when performing control analysis.

When scaling inverter systems to increase the power output there are two methods for connecting inverters. In Section 2.5 the fundamental methods of paralleling or series connecting current or voltage sourcing inverters was introduced. In practice inverters are not perfect voltage or current sources, but are a combination of switching devices and ripple filter components. The point at which multiple inverters are connected defines how they interact and what constraints the systems will have.

3.5.1 Monolithic

Monolithic inverter topologies achieve power scaling at the device level, and a large single filter is used. Parallel monolithic systems connect switching devices in separate packages in parallel as shown in Figure 3.8. Series monolithic systems connect the switching devices in series. In parallel configurations, monolithic systems require that each of the parallel devices (IGBT etc) is identical to ensure current sharing, as discussed in Section 2.6 and [5]. Both device manufacturing tolerances and thermal effects impose limits on the size of large monolithic-paralleled systems.

3.5.2 Independent Control

To ensure device balancing over a large number of subtly different devices, an active balancing method must be used.

In parallel configurations it is difficult to achieve balancing for hard-connected devices, such as shown in Figure 3.8, as each device can be modelled as a voltage source with a low impedance, so any small voltage change results in a large current imbalance. The practical alternative to paralleling at the device level is to parallel individual inverters, where each inverter has its own ripple filter. This is known as active paralleling and is employed in the test hardware detailed in Appendix G and is further analysed in Chapters 4 and 6.

3.6 CONTROLLER

The section details several of the key components which must be used when constructing closed-loop digital control systems. Each of the components mentioned are unavoidable and also have their own associated constraints.

The controller contains all devices relevant to implementing the control algorithm. For digital systems this would typically include a Digital Signal Processor (DSP) and/or a Field Programmable Gate Array (FPGA). In addition to the main processor, the controller also includes

all relevant interfaces, such as ADCs, signal conditioning, PWM generation and gate drivers. Deciding whether a DSP and/or FPGA is required for implementing the controller depends entirely on the application. Modern DSPs typically include ADCs, PWM modulators, and are often optimised for high speed calculations. Despite there being a wide range of DSPs available, for some applications one or more of the built-in peripherals may not be suitable. Common limitations are in the resolution, accuracy or sample rate of the ADC; the PWM modulator may not support natural sampling; or the processing speed may not be fast enough. If any of these requirements are unable to be met by a given DSP, external ADCs may be used; a PWM modulator could be implemented in a FPGA; or the control algorithm could be implemented in a FPGA.

Each of the development stages requires a different set of engineering skills and resources. At the theoretical and numerical testing stages simulation tools such as Matlab, Simulink^{TM}and PSIM^{TM}are commonly used to confirm the suitability of the approach and algorithms. The simulation models include both the designed inverter controller targeted for the embedded processor, an accurate model of the the inverter hardware and one or more usage scenarios.

In discrete-time LTI controllers the operations consist of basic arithmetic operations including summation, multiplication, division and sample period delays; each of which are implemented in the control processor. At the time of writing there are typically two families of devices which are used to implement discrete controllers: Digital Signal Processors (DSP) and Field Programmable Gate Arrays (FPGA). DSPs are microcontroller devices which are optimised for digital signal processing. As the performance of general purpose microprocessors increases, the distinction between a DSP and a microcontroller has become increasingly blurred. FPGAs provide a matrix of reconfigurable logic blocks to implement complex custom logic circuits. Many common FPGAs allow the synthesis of DSP cores and/or provide DSP cores alongside the reconfigurable logic.

DSPs are often the most popular choice for implementing controllers as they often include both peripherals used in control systems, such as ADCs and PWM modulators, but also because they can be used for additional functionality such as running communication stacks and more general processing functions. Where FPGAs dominate is in applications where low latency and/or specialist functionality is required. Due to the flexibility of microprocessors and the real-time aspect of FPGAs, many power electronics systems may incorporate both devices. The microprocessor is commonly used for communications and control tasks, whereas the FPGA may be used for high speed tasks such as device protection, critical control tasks and PWM generation.

For the test hardware described in Appendix G a 150MHz DSP processor with builtin ADC and PWM is used for the main controller, while a separate FPGA provides high speed protection functions.

3.6.1 Hardware Interfaces

The interfacing components between a controller and the hardware are a critical part of the system design, as they are the sole method which the controller has for both measuring external conditions and to control actuators (inverter switching stack). Despite being common to all control system designs, in each scenario they deserve particular attention due to their associated side effects. This thesis assumes that the resolutions of ADCs and PWM modulators available in digital microcontrollers are adequate for the given application.

Assuming a sufficient resolution, the key consideration for an ADC is the sample delay. Similar to regular PWM as described in Section 3.4.1, ADCs have a ZOH response. Figure 3.9 shows the effect of sampling inductor current twice per switching period with two different sample points. Despite the ripple in the second figure of Figure 3.9, if the sample period is the same as the switching period (half the sample period shown in the figure) the samples will be on either the

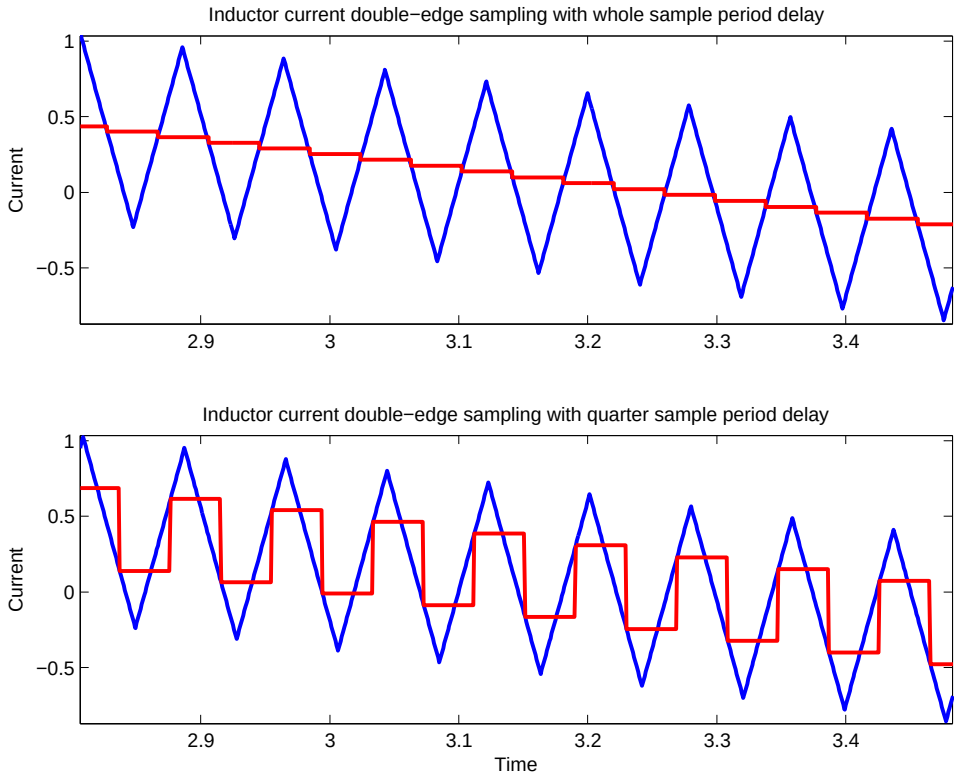


Figure 3.9: Example of inductor current sampling aliasing effect. The top picture shows how the switching ripple can be removed by sampling at integer-multiple delays of the sample period. The bottom figure illustrates the effect of not sampling at integer-multiple delays of the sample period.

rising or falling edge and will result in an offset error, causing distortion.

Common to any sampled system, frequencies above the Nyquist limit must be filtered to prevent aliasing in ADCs. Alias filtering also changes the response of a discretised system above the Nyquist frequency. By filtering any high frequency components above the Nyquist frequency, the impedance of an inverter above the cutoff frequency is determined by the output filter. This condition is later used to convert discrete-time systems to continuous-time.

3.6.2 Developing test inverter

A graphical simulation model is commonly used as the design document for controller implementations. At the implementation stage the simulation controller sections are translated into a form appropriate for the given controller hardware and software language. At this stage additional changes to the controller form may be made to suit the target platform. Such changes

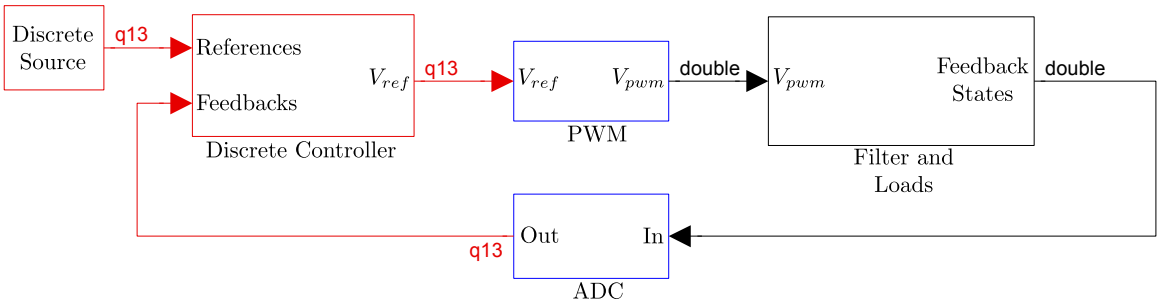


Figure 3.10: Example control diagram for code generation.

may include translating floating-point signal paths to fixed-point representations.

The process of reformatting the controller design and then writing the controller code is relatively labour intensive. As a consequence of being both a tedious mechanical process and of having to reformat the graphical design, the process is highly prone to human errors. The time required to perform the conversion, identify and fix human errors, and to confirm the suitability of performed translations (ie choice of fixed-point locations) can be significantly reduced if these processes are automated. Modern simulation tools such as Simulink now include toolboxes aimed at embedded controller development. Mathworks' Fixed Point toolboxes allow the designer to choose and simulate with appropriate data types for each signal. The Real-Time Workshop® toolbox generates C code directly from a simulation model, and the Simulink HDL Coder® generates VHDL for an FPGA.

Automating the controller implementation process offers a greater degree of confidence that the controller will perform as expected when tested in hardware. A strong correlation between simulation and the implementation was achieved when developing and testing the new control designs in this thesis. Both the Fixed Point and Real-Time Workshop toolboxes were used when developing control models to rapidly confirm their operation in hardware, as the time taken to generate the control code from a model, compile it, download it into the target hardware and to run it was in the order of several minutes. A typical simulation layout is shown in Figure 3.10. The model is colour coded to represent different sample times, in this case red is discrete-time, black is continuous-time and blue is a combination of sample times. Signal data types are shown

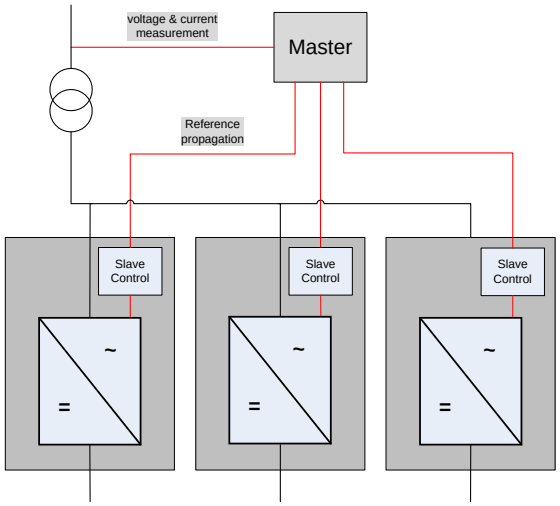


Figure 3.11: Example master-to-slave reference propagation.

at the output of each block, in this case '$q13$' refers to a fixed-point data type and 'double' is a double precision floating data type. When testing in hardware, the control code is generated from the 'Discrete Controller' block.

The laboratory test setup consisted of a scaled production inverter, detailed in Appendix G. The inverter current and voltage ratings were scaled down accordingly to allow the inverter to be safe in an office environment, but still representative of a full power system. By including key characteristics of the inverter hardware such as voltage and current sample points, digital delays and anti-aliasing filters, not surprisingly the inverter responses over a range of tests closely matched the simulation results. In Chapters 4 to 6 the use of the code generation tools provided rapid confirmation of the simulations. With discrete-time control models for code generation and continuous-time electrical models matching the electrical hardware, the hardware tests were predominantly quick confirmation tests. The simulations were able to quickly test many different usage cases so that when it came to hardware testing, an efficient setup and test procedure could be used.

3.6.3 Reference propagation

With the paralleled inverter configuration, a master controller was used to propagate voltage or current references to each of the parallel modules. Herein a 'master' device propagates a reference to one or more 'slave' inverters. The act of reference propagation requires particular attention, as the channel bandwidth and propagation delay between master and slave devices can severely affect the response and achievable bandwidth of closed-loop systems. An example closed-loop system is where the master controls the slave device(s) to control a sensed signal (such as output voltage), as shown in Figure 3.11. When used in closed-loop control, the master to slave propagation delay is included in the analysis. The minimum introduced delay in master/slave systems is the sum of the master reference calculation time, the reference propagation delay and the slave calculation time. The master-slave configuration which is used for the test hardware in Appendix G is shown in Figure 3.11.

In some applications there may be more than one propagation channel. For example, in the case of arrays of inverter arrays, a global controller may propagate references to local masters which then propagate further references to individual slave modules.

3.7 INVERTER PERFORMANCE EVALUATION

When evaluating inverter controllers, performance measures give an idea of the performance of a system for a given set of constraints. One such performance measure is an inverter's output impedance for a given switching frequency. All performance measures are only useful when the system is stable. Both continuous and discrete-time systems can be analysed using the following methods by mapping discrete-time poles via the relationship e^{sT_s}.

An inverter's forward bandwidth is by far the most commonly used and referenced performance measure. By definition the bandwidth of an inverter is the frequency range which it can reproduce, with the cutoff point being when the upper and lower bound is -3dB (half of the input

signal). Most inverters, by design, are capable of operating down to DC, thereby making the bandwidth the first (lowest) frequency where the forward attenuation is -3dB. When evaluating forward bandwidth and impedance responses, both the magnitude and phase response is important. For forward responses both a unity magnitude and low phase shift are preferred.

The forward transfer frequency response is by far and away the most common inverter performance indicator. Unfortunately in applications where the load is unknown and not incorporated into the control loop transfer function, the inverter's output impedance affects its ability to reproduce the reference signal. When comparing the performance of developed controllers, a perfect current source would have an infinite output impedance whereas a perfect voltage source has an impedance of zero. There has recently been a large surge in publications for deriving impedance (or admittance) expressions for high-order electronic inverters as sources or loads [10–14].

Performance indicators such as Integral Squared Error (ISE) and Integral Absolute Error (IAE) are often used in control design. They provide measures for determining a relative least amount of error for a reference step. In addition to traditional performance measures such as overshoot and settling time, different controller responses can be traded off to determine the best for a given application. By squaring the error term, ISE puts emphasis on large error deviations such as overshoots and slow rise times. The IAE is similar to the ISE but without the squaring component it reduces the emphasis on large error components. Calculations for ISE and IAE as applied to transfer functions are given in Appendix E.

A controller's robustness is defined as its ability to be tolerant to electrical effects which are a side-effect of practical implementation. These include component parasitic effects as discussed in Section 3.3.3, component value variations, and external loads. In grid-connected applications often the load and its associated response may be either well defined (such as a motor) or may be completely undefined (aside from voltage and current rating). Large industrial plants typically consist of a wide range of linear and non-linear loads.

Designing controllers that are robust is discussed in Section 4.4, and a robust discrete-time controller is derived in Chapter 5.

3.8 SUMMARY AND DISCUSSIONS

This chapter has covered the primary constraints and modelling paradigms encountered when implementing high performance inverter controllers. The constraints and modelling paradigms consist of a mix of control theory, hardware implications imposed by the power switching devices, the output filter required to resolve the underlying control signal, the ability to scale inverters to achieve a greater power capability, and how the performance for an inverter can be gauged.

The primary constraint in the control analysis is dealing with delays, as they are intrinsically non-linear elements in the continuous-time domain. While analysis techniques such as the Padé approximation or the Lambert W function can be of assistance, they are still not without their complications.

One of the primary sources of system delays is often the use of regular-sampled PWM. While naturally-sampled PWM inherently has no ZOH delay, in practice in modern Digital Signal Processors it is often not implementable.

The inverter topology and associated PWM filter impose practical constraints that must be addressed when designing controllers. The undamped resonant response of the PWM LC filter, and ensuring power sharing parallel inverter configurations must both be considered.

Finally, performance indices such as inverter bandwidth, output impedance, Integral Squared Error, and Integral Absolute Error are industry standard ways of evaluating inverter performance.

All of the associated control and hardware constraints, and the analysis and performance paradigms set the benchmark for designing inverter controllers. All of these are considered in the following chapters when state of the art controllers are examined and new ones are developed.

Chapter 4

INVERTER CONTROLLER FORMS

4.1 INTRODUCTION

In this chapter the fundamental concepts used for designing and implementing digital controllers are introduced. The chapter begins by first introducing the traditional methods of implementing current and voltage controllers in continuous-time. The continuous-time designs are then discretised and evaluated to determine their suitability in discrete controllers. As fundamental concepts, they provide the basis for all advanced controller designs.

For the remainder of the thesis per unit terms are used for all values, including voltage, current and time. In doing so, numerical units are often omitted unless specified.

4.2 TRADITIONAL FORMS

Fundamentally controllers implement current and voltage source converters in the following two ways:

- Voltage is applied across an inductor to cause a change in current.
- Current is injected into a capacitor to cause a change in voltage.

A particular type (current or voltage sourcing) is implemented by cascading each of the different forms, for instance a voltage source converter has an LC filter and operates as a cascaded current and then voltage source.

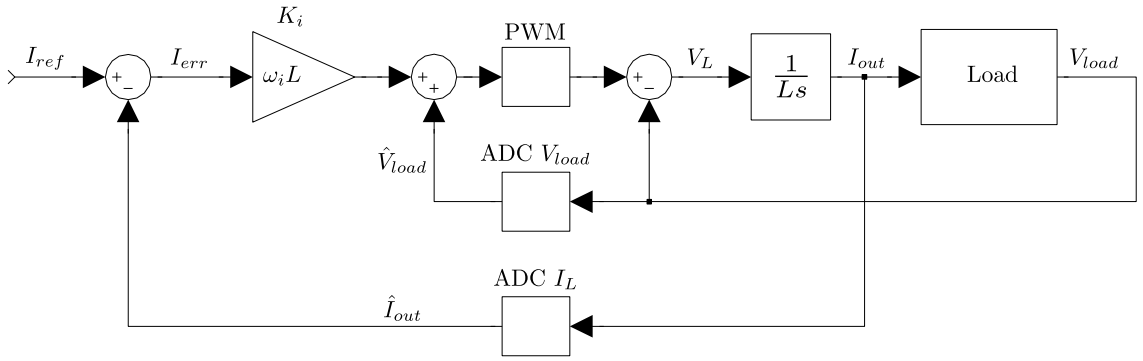


Figure 4.1: First-order current controller.

Figure 4.1 shows a first-order current controller. In continuous-time and with no delays from the PWM or ADC blocks, the forward transfer function can be shown to be

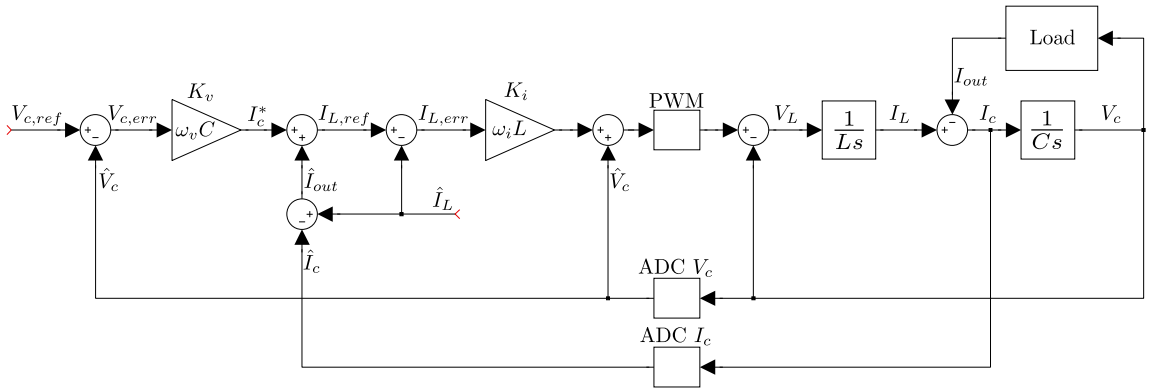
$$H_{CSI}(s) = \frac{I_{out}(s)}{I_{ref}(s)} = \frac{\omega_i}{s + \omega_i} \tag{4.1}$$

Where ω_i is the converter forward bandwidth. Note that the current bandwidth is independent of the load. The output admittance is

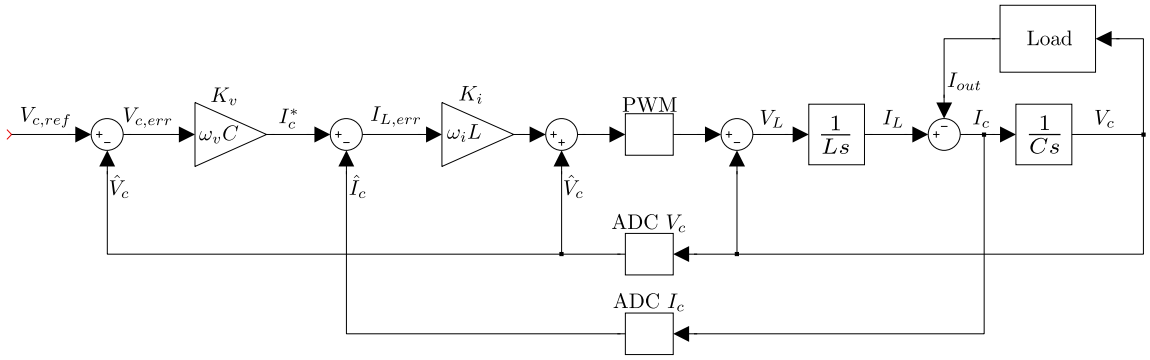
$$Y_{CSI,out}(s) = \frac{I_{out}(s)}{V_{out}(s)} = 0 \tag{4.2}$$

Being first-order the system is critically damped. In this ideal scenario where there are no loop delays the current bandwidth ω_i is not limited by any stability constraints (assuming the bandwidth is positive) and can therefore be infinite. As the dominant pole dictates the frequency at which a transfer functions response begins to roll off, for controllers the *dominant pole is effectively the control bandwidth.*

A current and voltage controller are often cascaded, as shown in Figure 4.2a. Figure 4.2b shows a simplified model of the controller by eliminating the inductor current feedback term I_L. The capacitor current feedback can also be eliminated by calculating I_C from V_C. In continuous-time



(a) Cascaded current-voltage controller



(b) Cascaded current-voltage controller after simplification

Figure 4.2: Second-order voltage controller.

the forward transfer function can be shown to be

$$H_{VSI}(s) = \frac{V_c(s)}{V_{c,ref}(s)} = \frac{\omega_i \omega_v}{s^2 + s\omega_i + \omega_i \omega_v} \tag{4.3}$$

And the output impedance is

$$Z_{VSI,out}(s) = \frac{V_c(s)}{I_{out}(s)} = \frac{s}{C(s^2 + s\omega_i + \omega_i \omega_v)} \tag{4.4}$$

Figure 4.3 shows a typical VSI output impedance frequency response. From the figure the VSI has an inductive response up to the natural frequency and then above that is capacitive. The inductive portion of the curve can be shown to be $\frac{s}{\omega_i \omega_v C}$ and the capacitive portion is $\frac{1}{sC}$. The inductive response indicates that to achieve a low output impedance, high gains are required.

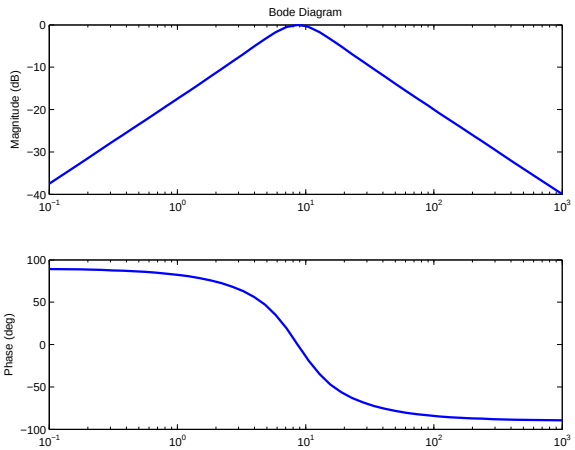


Figure 4.3: Example of continuous-time VSI output impedance frequency response. $\omega_i = 10$, $\omega_v = \frac{3}{4}\omega_i$.

Inverters are commonly assumed "perfect" and VSIs are therefore expected to have a zero output impedance. As this is not the case, an impedance at or below a typical grid impedance (below 10% inductive) is typically desired. For high power systems an impedance below 5% at the fundamental is typical. To achieve a 5% impedance for a continuous-time VSI, with a 10% capacitor would require an $\omega_i\omega_v$ product of 200, which corresponds to a natural frequency ($\sqrt{\omega_i\omega_v}$) of 14.

The second-order voltage controller has a corner (natural) frequency of $\sqrt{\omega_i\omega_v}$ and a damping ratio ζ of

$$\zeta = \frac{1}{2}\sqrt{\frac{\omega_i}{\omega_v}} \tag{4.5}$$

Although there is no strict requirement that the voltage gain ω_v is less than the current gain ω_i, it would produce a lightly damped system. The voltage controller is critically damped when $\omega_i = 4\omega_v$. In practice damping ratios between 0.5 and 1 are typically chosen.

The ISE of equation 4.3 can be shown to be

$$ISE = \frac{\omega_i + \omega_v}{2\omega_i\omega_v} = \frac{1}{2}\left(\frac{1}{\omega_i} + \frac{1}{\omega_v}\right) \tag{4.6}$$

This indicates that increasing either of the controller gains will lower the ISE.

The formulation of the second-order VSI by using an inductor current controller to control the voltage across the capacitor can lend itself to implementing a parallel VSI. The ideal method of creating parallel inverter arrays is to use high impedance current sources. Using the cascaded current/voltage controller a parallel configuration can be created by implementing multiple current controllers (one per module) and then controlling the total current into the parallel capacitors (the combined bulk capacitance). Unfortunately this method assumes the parallel capacitors act as one large capacitor, and if the capacitors are geographically quite far apart there is no means of controlling any inter-module current flows. The consequences of this are further explored in Chapter 6.

So far both the current and voltage controllers have only had to be proportional controllers to achieve zero steady-state error. In practical systems however, every component has parasitic resistive losses which result in a steady-state error. The non-zero VSI output impedance intrinsically shows that for a non-DC signal, when loaded the output voltage will not exactly equal the reference. To compensate for steady state errors, integrators (in DC or rotating reference frames) or resonators (AC systems in stationary reference frame) can be used. The resonator transfer function is

$$H_{resonator}(s) = \frac{s\omega_r}{s^2 + \omega_n^2} \tag{4.7}$$

Where ω_r is the resonator gain and ω_n is the fundamental frequency.

4.2.1 Discretised traditional forms

So far continuous-time current and voltage controllers have been demonstrated that have both well defined first and second-order responses (both forward response and impedance), and theoretically have no upper bandwidth limitation. In practice, however, perfect continuous-time systems are not achievable. Systems using naturally-sampled PWM, as described in Section 3.4.1, impose a signal slew rate limitation that limits the maximum bandwidth. Discrete-time imple-

mentations impose sampling and calculation time delays. This section demonstrates the effect of discretising continuous-time controllers. Particular attention is applied to the effect of the converter's response as the controller bandwidth approaches the discrete-time sample rate.

When discretised the PWM and ADC blocks in Figure 4.1 define ZOH boundaries for the continuous-time filter. The ZOH discretised inductor is

$$P_L(z) = \frac{T_s}{L(z-1)} \tag{4.8}$$

As there are no dynamic elements in the CSI controller, the discrete form remains unchanged. In all practical discrete systems there is a delay between sampling continuous-time inputs and the PWM output. Often ADC sampling points are synchronised with the PWM sample point (as mentioned in Section 3.6.1), resulting in a whole sample period delay. The CSI discrete forward transfer function with a single sample period delay is

$$H_{CSI}(z) = \frac{zT_s\omega_i}{z^2 - z + T_s\omega_i} \tag{4.9}$$

The continuous-time system had a single pole with a natural frequency equal to the bandwidth. The discrete-time system has the following two poles:

$$z = \frac{1 \pm \sqrt{1 - 4T_s\omega_i}}{2} \tag{4.10}$$

The two poles are critically damped when $\omega_i < \frac{1}{4T_s}$ and are unstable when $\omega_i > \frac{1}{T_s}$. To put the critical damping and stability conditions into perspective, for a 50Hz system with an 8kHz sample rate $T_s = \frac{2\pi}{160} = 0.0393$, the system would be unstable with a bandwidth of $\omega_i = 25.5$, and just critically damped when $\omega_i = 6.4$.

For the continuous-time system the gain ω_i is the cutoff frequency, but with the discrete system ω_i only corresponds to the cutoff frequency as the frequency tends to zero (low bandwidths).

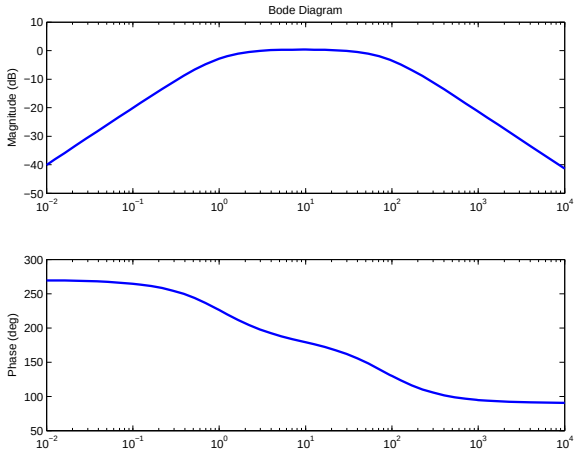


Figure 4.4: Example of discretised CSI output admittance frequency response. $\omega_i = 10$pu, $T_s = \frac{2\pi}{160}$, $L = 4\%$.

The natural frequency of the dominant pole (pole with the lowest natural frequency) is greater than ω_i. When critically damped the natural frequency of the dominant pole is a non-linear function of T_s and ω_i, given by:

$$\omega_n = \frac{\ln(2) - \ln(1 + \sqrt{1 - 4T_s\omega_i})}{T_s} \tag{4.11}$$

For example, an ω_i of 6.4 has a natural frequency of 17.7, which is more than double the cutoff frequency for the same ω_i gain in a continuous-time system. For a 50Hz system with an 8kHz sampling frequency, a cutoff frequency of 17.7 corresponds to 885Hz, which is a sample frequency to bandwidth ratio of 9.

The admittance of the discretised current controller is also no longer zero. With a single sample period delay the admittance can be shown to be:

$$Y_{CSI,out}(z) = \frac{T_s(z-1)}{L(z^2 - z + T_s\omega_i)} \tag{4.12}$$

Figure 4.4 shows an example discretised CSI output admittance. Similar to the forward response, the discretised admittance approaches the continuous-time admittance of zero (equation 4.2) for low frequencies. Above the Nyquist limit the admittance drops away like the continuous-time

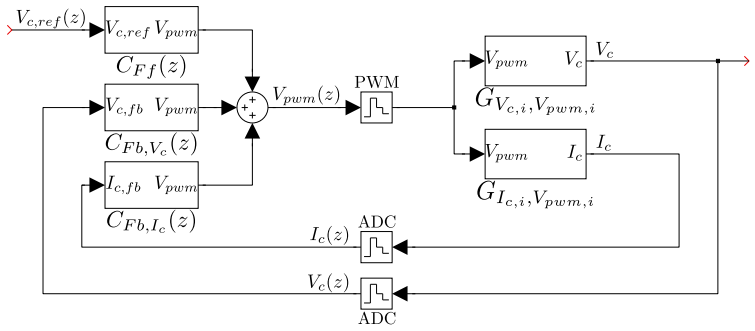


Figure 4.5: VSI controller and filter blocks.

system, however, with an admittance greater than zero the discretised CSI in not immune to deviations in the supply voltage.

Equation 3.22 is the ZOH discretised LC filter in Figure 4.2. The proportional VSI controller in Figure 4.2b is easily discretised with a single sample period delay:

$$V_{pwm} = \left(\left(V_{c,ref} - V_c z^{-1}\right)\omega_v C - I_c z^{-1}\right)\omega_i L + V_c z^{-1} \tag{4.13}$$

For analysis purposes the controller is separated into a feed-forward path $C_{Ff}(z)$, and the capacitor voltage and current feedback paths, $C_{Fb,V_c}(z)$ and $C_{Fb,I_c}(z)$ respectively:

$$V_{pwm} = V_{c,ref}C_{Ff} + V_c C_{Fb,V_c} + I_c C_{Fb,I_c} \tag{4.14}$$

Figure 4.5 shows the closed loop connection of the controller and filter components. In practice the capacitor current may be approximated by differentiating the sampled voltage, removing the need for a capacitor current sensor. The closed loop forward transfer function is:

$$\frac{V_c(z)}{V_{c,ref}(z)} = \frac{C_{Ff}C_{Fb,V_c}G_{V_c,V_{pwm}}}{1 - \left(C_{Fb,V_c}G_{V_c,V_{pwm}} + C_{Fb,I_c}G_{I_c,V_{pwm}}\right)} \tag{4.15}$$

Substituting the discretised filter and controller expressions produces a third-order system. The full third-order equations are given in Appendix F. Solving for the discrete poles of the sys-

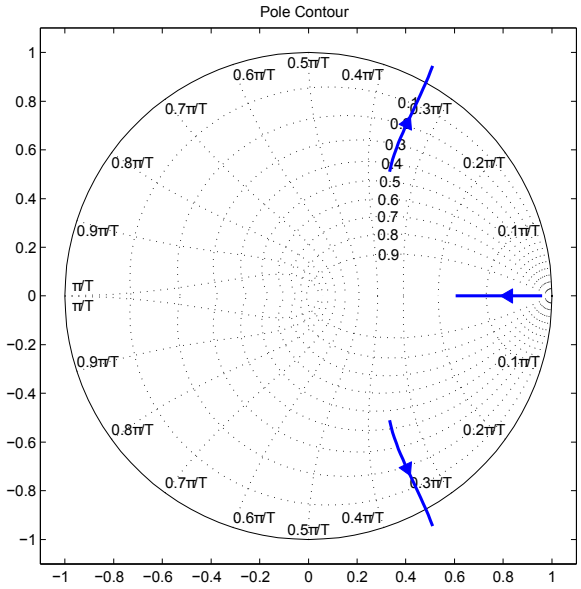
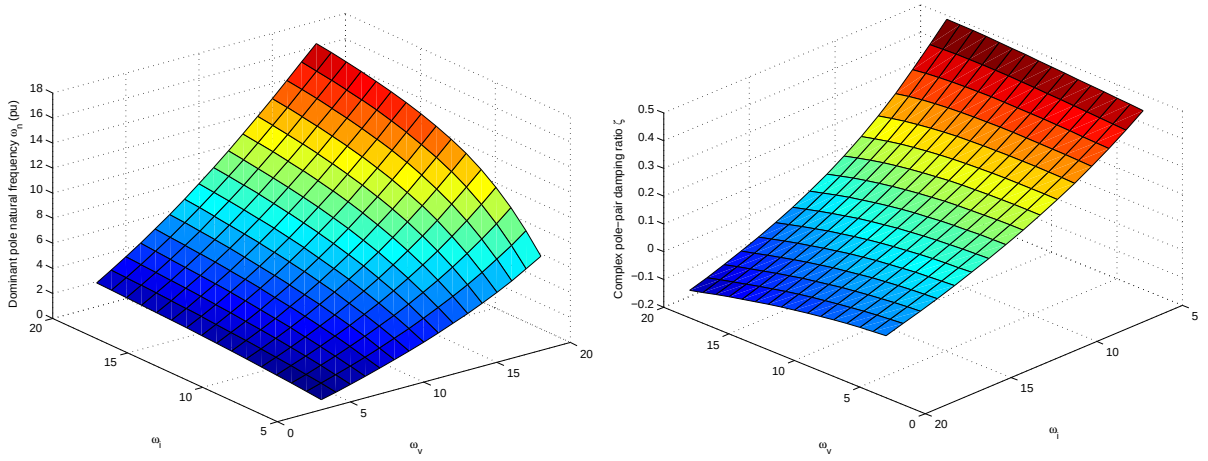


Figure 4.6: Pole contour of discretised VSI gain sweep. ω_i sweep from 5 to 20, $\omega_v = \frac{3}{4}\omega_i$, $L = 4\%$, $C = 10\%$, $T_s = \frac{2\pi}{160}$ (50Hz fundamental, 8kHz sample rate).

tem produces incomprehensible expressions. Whereas the continuous-time system closed-loop forward transfer function was not dependent on the resonant frequency of the LC filter, the discretised response is, as indicated by the '$\cos(T_s\omega_n)$' components in the transfer function.

Figure 4.6 shows pole contours for a gain sweep of $\omega_i = 5$ to 20. Unlike the continuous-time VSI which had two poles and was unconditionally stable, the discretised version becomes unstable with a gain of $\omega_i = 17.7$. Even with a relatively low gains of $\omega_i = 5$ and $\omega_v = 3.75$, the dominant real pole has a natural frequency of 1.03 while the complex pole-pair has a natural frequency of 28.2 with a damping ratio of 0.45. Unlike the discretised CSI which achieved a *greater* natural frequency for the dominant pole than the gain ω_i, the discretised VSI dominant pole not only has a much lower natural frequency (1.03pu) than the continuous-time VSI $\left(\sqrt{\omega_i\omega_v}\right)$, it is also has a lower damping ratio.

Figure 4.7 shows the effect of the two gains ω_i and ω_v on the dominant pole natural frequency and the complex pole-pair damping ratio. Figure 4.7a indicates that for a high ω_i the bandwidth is largely dominated by ω_v, while Figure 4.7b indicates that the damping ratio is mainly dominated by ω_i. Based on these observations, provided ω_i is not too low ($\omega_i > 8$), the bandwidth and



(a) Dominant pole natural frequency

(b) Complex pole-pair damping ratio

Figure 4.7: Discretised VSI natural frequencies and damping ratios for gains ω_i and ω_v. $L = 4\%$, $C = 10\%$, $T_s = \frac{2\pi}{160}$.

damping ratio can be selected almost independently of each other. However, the damping ratio for practical gains is bounded to below 0.5.

Previously the discretised CSI demonstrated a critically damped bandwidth as high as one ninth of the sample frequency. With a damping ratio of 0.3 the discretised VSI can only support a cutoff frequency of 11.4 ($\omega_i = 8, \omega_v = 18$), put into perspective this corresponds to 570Hz for a 50Hz system and one fourteenth (7%) of an 8kHz sample frequency. At these gains the response has a -45 degree phase shift by the 7th harmonic. As with the discretised CSI, for gains approaching the sample frequency the discretised VSI gains no longer correspond to the natural frequency or damping ratios derived for the continuous-time system.

The output impedance of the discretised VSI also changes. For the continuous-time system the output impedance for frequencies below the bandwidth frequency is proportional to the inverse of $\omega_i\omega_v$. The full third-order output impedance expression is given in Appendix F. The output impedance expression has the same poles as the forward transfer function.

Using the gains mentioned in the previous paragraph ($\omega_i = 8, \omega_v = 18$), which are the best achievable gains before the damping ratio becomes intolerably low, the output impedance response is shown in Figure 4.8. At the fundamental the inductive output impedance is 5.7%. As

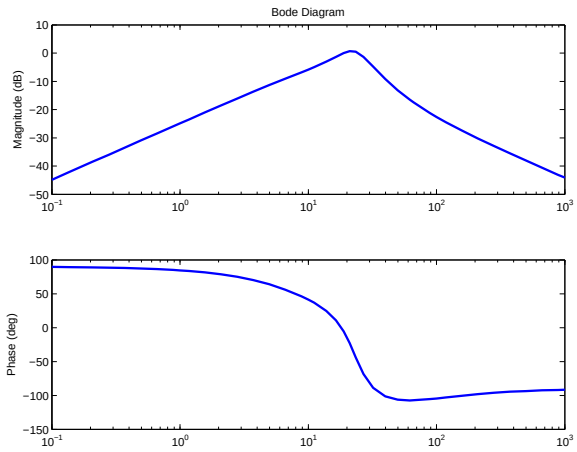


Figure 4.8: Discretised VSI example output impedance. $\omega_i = 8$, $\omega_v = 18$, $L = 4\%$, $C = 10\%$, $T_s = \frac{2\pi}{160}$.

expected, for high frequencies above the Nyquist ($\frac{1}{2T_s}$), the impedance is purely capacitive like the continuous-time system.

In high power systems with low switching frequencies, and therefore sampling frequencies when using regular sampled systems, the bandwidths required quickly approach the Nyquist limit of the controller. Discretised continuous-time controllers only achieve the continuous-time response when the Nyquist limit is high relative to the required bandwidths. As demonstrated in this section as the controller gains are increased the response of discretised controllers no longer match that of the continuous-time systems. The limitations of discretised continuous-time controllers as the sampling frequency is reduced provides motivation for better performing controllers that are specifically designed for discrete-time systems.

The primary issue with the discretised continuous-time controller is that the response of the system is dominated by the low frequency dominant pole, while the damping, and hence stability, of the system is dominated by the high frequency complex pole-pair.

In Section 4.2 it was concluded that the cascaded inductor current controller and capacitor voltage controller is an effective way of implementing a parallel VSI configuration. However, using current sourcing modules in parallel requires that the master module controlling the capacitor voltage propagates inductor current references to each slave module. In the continuous-time

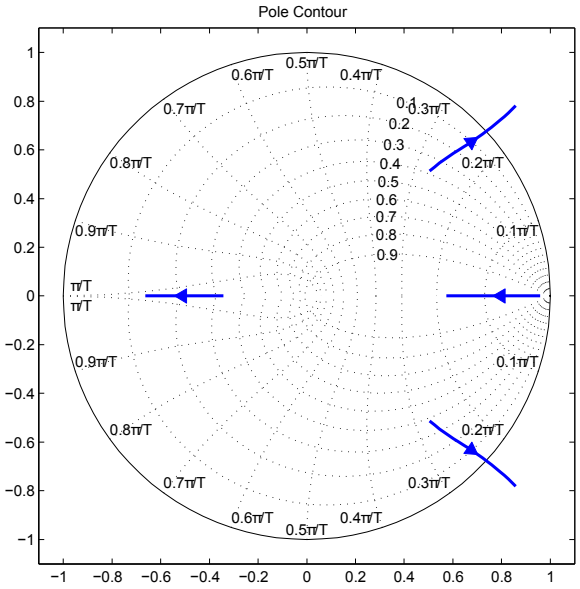


Figure 4.9: Pole contour of discretised VSI gain sweep with internal controller propagation delay. ω_i sweep from 5 to 20, $\omega_v = \frac{3}{4}\omega_i$, $L = 4\%$, $C = 10\%$, $T_s = \frac{2\pi}{160}$.

scenario this does not pose any issues, but in discrete-time systems a master module would need to propagate the reference to the slave modules in the same sample period to prevent additional loop delays affecting the response. Figure 4.9 shows the gain sweep from Figure 4.6 but with a sample period delay between the voltage control loop and the current control loop representing a propagation delay from a master voltage controller to a slave current controller. Compared to the Figure 4.6, Figure 4.9 has an additional pole, but more significantly, the lightly damped complex pole-pair has a lower stability margin. Further reasoning against paralleling modules in this manner is also detailed in [5] and discussed in Chapter 6.

Of course the discretised continuous-time controller detailed so far is by no means the only discretised continuous-time controller form. Due to the more intuitive nature of continuous-time systems many discretised controllers presented in literature are presented in continuous-time forms. Several methods for producing VSI systems are presented in the literature [15–21]. Common control elements such as PID controllers are often presented and analysed in closed loop as their continuous-time forms. Delays are also often approximated using first-order [18] or higher-order (Padé) continuous-time approximations.

4.3 DISCRETE DESIGNED CONTROLLERS

To overcome the limitations of discretised continuous-time control systems and due to the abundance of DSPs, discrete designed controllers have gained in popularity in recent decades. Direct discrete designs do not necessarily suffer from the performance issues associated with discretised continuous-time systems as the gains approach the Nyquist limit. Fundamentally discrete controllers are still controlling the output filter components. By incorporating the system delays in the controller design process, the controller may be able to offer greater performance over a continuous-time derived one.

Aside from mixed continuous and discrete systems mentioned in Section 4.2.1, the most common form of discrete designed controller is the Deadbeat form [22–30]. While deadbeat offers the best possible response achieveable with a discrete-time system, it does have some inherent limitations in practical applications, such as:

- Tight coupling to component values. While all controller responses have a dependency on component values, as confirmed in the literature, deadbeat has the tighest dependency on component values, limiting its applicability in practical applications where multiple components are used, such as LC filters.

- In applications where one or more of the component measured states is not available, such as the inductor current, the deadbeat realization can result in undesirable actuator ringing.

- By definition deadbeat respones is the fastest possible response for a discrete-time system, and therefore inherently does not offer the ability to tune the system which would otherwise allow the ability to forgo converter response for robustness.

Due to the practical limitations imposed by deadbeat control, this thesis focuses on high performance discretised controllers that offer configurable performance and robustness.

4.4 ROBUSTNESS

Creating a controller that is both robust to component variations while also achieving a high bandwidth is intrinsically difficult to achieve. High bandwidth controllers are typically designed for a specific output filter and load. When designing and evaluating high performance controllers the ability to trade off performance for robustness is a key requirement.

The discretised continuous-time VSI in Section 4.2.1, despite having a low stability margin, is relatively robust to component variations. Component variations of 10% have a less than 5% effect on the damping ratio, while the variations have a proportional effect on the forward bandwidth.

Although deadbeat controllers achieve the best response possible for a discrete-time controller, some of the literature shows that the controllers are not robust to component sensitivities [30]. The focus of the next chapter is to design a discrete-time controller that specifies the controller stability margin as part of the design process, allowing the designer to trade off performance for robustness.

4.5 SUMMARY AND DISCUSSIONS

This chapter started by introducing the fundamental ways of controlling voltage and current source inverters in continuous-time, and then continued by analysing the effects of discretising the same controllers as would be done in a digital control system.

The continuous-time controller forms displayed the characteristic responses, where both the control bandwidth and damping ratios are directly controllable. Both the CSI and VSI continuous-time configurations have no theoretical stability limits.

After discretisation, for low bandwidths the controllers exhibit a similar response to the continuous-time implementations, however, as the control bandwidth gains approach the discrete-time Nyquist limit, higher-order poles become lightly damped and eventually go unstable. The lightly

damped poles (and instability) impose undesirable bandwidth limitations. For instance, one of the examples demonstrated that a discrete-time VSI with a sampling frequency of 8kHz could only achieve a cut-off frequency of the 11th harmonic with a damping ratio of 0.3.

Given the constraint of discretised traditional controllers, the following chapter investigates a controller specifically designed for discrete-time that not only achieves a high bandwidth relative to the sample frequency, but is also robust to parameter and component variations.

Chapter 5

DISCRETE DIRECT DESIGN CONTROLLER

In Chapter 4 discrete-time controllers were introduced and as the bandwidth was increased the traditional, well known continuous-time derived approaches demonstrated stability limitations resulting in unacceptably low achievable response rates. The discretised VSI controller in Section 3.22 is flawed in that the response of the system is dominated by a low frequency dominant pole, while the damping is defined by a high frequency complex pole-pair. Later in Section 4.3, discrete designed controllers were introduced that have been purpose designed for discrete-time systems. Of these controllers, deadbeat control offers the optimal performance for a discrete-time controller, achieving the reference signal in the same number of sample delays as the order of the system being controlled (usually an output filter). Despite achieving the best performance possible, the controller's robustness is both sensitive to the actual filter component values and requires feedback of both the inductor current and capacitor voltage filter states. For many control systems robustness is of higher priority than response, and for each given application the ability to trade off response for robustness offers the greatest flexibility.

In this chapter a discrete direct design VSI controller is developed that through common design parameters allows the trade-off between the forward response bandwidth and the damping ratio of the complex poles (originally detailed in [31]). The controller is shown to achieve a high bandwidth to sample frequency ratio and is robust against component sensitivities. To aid in implementation the controller only requires capacitor voltage feedback and has a simple first-order form resulting in a third-order closed loop inverter. By automating the calculation of the

controller gains, either a bandwidth frequency or damping ratio is used as the primary design parameter for the controller, while the other is available as an output from the design process.

5.1 DESIGN CHOICES

For the controllers in Chapter 4 several key design requirements were defined that were based on the analysis and conclusions of the discretised VSI in Section 4.2.1. These included:

- Single-state feedback. Both the discretised VSI in Section 4.2.1 and the deadbeat controller in Section 4.3 have two state feedbacks. Given that the values of the output filter are known sufficiently well (within component value tolerances) each of the states can be derived using an observer on the output capacitor voltage. In power electronic systems, accurate, noise-free current sensors which operate over a wide frequency range are difficult to achieve. Therefore only the output capacitor voltage will be assumed to be available.

- Response specified by using the common response parameters, bandwidth (related to the dominant pole natural frequency) and the damping ratio. Previously the discretised continuous-time controller had used design parameters ω_i and ω_v to specify the response of the system, but the relationship of these parameters to the natural frequency and damping ratio was lost as the gains were pushed closer to the Nyquist frequency.

- Achieve a greater bandwidth and lower output impedance than the benchmark discretised continuous-time VSI controller in Section 4.2.1.

- No assumptions are made about the load. The inverter impedance alone defines the compatibility with different loads. The inverter impedance must be able to operate against common linear loads, including low impedance systems such as grids or machines, and non-linear loads.

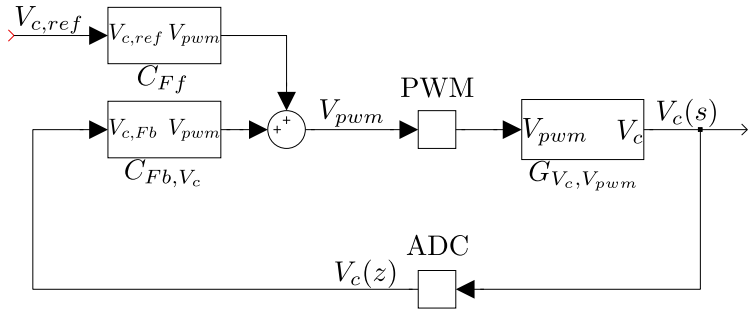


Figure 5.1: Discrete closed loop controller form.

- The controller should be relatively simple to implement in practical hardware. Sampling and processing delays and regular PWM are assumed.

5.2 POLE PLACEMENT DESIGN

The discrete controller uses constrained pole placement to achieve a high performance and robust voltage controller. Figure 5.1 shows the closed-loop controller with a single capacitor voltage feedback. $G_{V_c,V_{pwm}}$ represents the LC filter, and C_{Ff} and C_{Fb,V_c} represent the controller reference feed-forward and capacitor voltage feedback components respectively. Loop delays are included in the output filter discretisation process. The closed-loop forward transfer function is:

$$\frac{V_c(z)}{V_{c,ref}(z)} = H(z) = \frac{C_{Ff}(z)G_{V_c,V_{pwm}}(z)}{1 - C_{Fb,V_c}(z)G_{V_c,V_{pwm}}(z)} \tag{5.1}$$

where $G_{V_c,V_{pwm}}(z)$ is the ZOH discretised LC filter given in equation 3.22, and for clarity shown again below without any delays:

$$\frac{V_c(z)}{V_{pwm}(z)} = \frac{(z+1)(1-\cos(\omega_n T_s))}{z^2 - 2z\cos(\omega_n T_s) + 1} \tag{5.2}$$

$$\text{where} \quad \omega_n = \frac{1}{\sqrt{LC}} \tag{5.3}$$

Broken into their respective numerator and denominator parts, equation 5.1 becomes:

$$\frac{H_{num}(z)}{H_{den}(z)} = \frac{C_{Ff}(z)G_{V_c,V_{pwm},num}(z)C_{Fb,V_c,den}(z)}{G_{V_c,V_{pwm},num}(z)C_{Fb,V_c,num}(z) - G_{V_c,V_{pwm},den}(z)C_{Fb,V_c,den}(z)} \tag{5.4}$$

where the numerator and denominator parts are denoted by subscripts *num* and *den* respectively.

Using pole placement, the numerator and denominator of the controller components C_{Ff} and C_{Fb,V_c} are chosen to achieve the desired response. The first step in designing the controller is to specify the closed-loop poles of the system. The poles of the system affect both the forward response of the system and the output impedance. For this reason the controller feed-forward component $C_{Ff}(z)$ is assumed to not have any poles or zeroes that assist in stabilising the system. As expected, by examination of equation 5.4 the closed loop poles are determined by the filter and the controller feedback components.

As mentioned in Section 4.4 the most robust controller in regards to component sensitivities is one that would be entirely independent of the component values. Upon examination of equation 5.2, the zero $(z + 1)$ is independent of the filter component values. The first form of the controller feedback component C_{Fb,V_c} has a pole that cancels the $(z + 1)$ zero in the filter. With a single pole, the controller is first order, with the format as shown:

$$C_{Fb,V_c}(z) = \frac{k_2 z + k_1}{z + 1} \tag{5.5}$$

Substituting equations 5.2 and 5.5 into 5.1 with a single sample period delay (z^{-1}), the closed-loop third-order system is:

$$H(z) = \frac{z(z+1)\left(1 - \cos\left(\omega_n T_s\right)\right) C_{Ff}(z)}{z\left(z^2 - 2z\cos\left(\omega_n T_s\right) + 1\right) + \left(k_2 z + k_1\right)\left(1 - \cos\left(\omega_n T_s\right)\right)} \tag{5.6}$$

5.2.1 Gain selection

The three poles in equation 5.6 consist of one real pole p_0 and a complex pole-pair $p_{1,\Re}$ and $p_{1,\Im}$, such that:

$$0 = z\left(z^2 - 2z\cos\left(\omega_n T_s\right) + 1\right) + \left(k_2 z + k_1\right)\left(1 - \cos\left(\omega_n T_s\right)\right) \tag{5.7}$$

$$= (z - p_0)(z - p_{1,\Re} - jp_{1,\Im})(z - p_{1,\Re} + jp_{1,\Im}) \tag{5.8}$$

The three poles are functions of the gains k_1 and k_2 and the filter components. Of the three poles there is one relationship between the poles from equation 5.7 that is independent of k_1 and k_2:

$$p_0 = 2(\ p_{1,\Re} - \cos(\omega_n T_s)) \tag{5.9}$$

Given that the filter component variables L and C are typically fixed for a given application, a relationship between k_1 and k_2 and the three poles is required. The pole locations are chosen to achieve typical controller parameters such as the system's closed loop natural frequency ω_0 or damping ratio ζ.

The discretised VSI controller in Section 4.2.1 had a low frequency dominant real pole that limited the controller bandwidth, and a high frequency complex pole-pair that determined the damping ratio of the system. By equating the natural frequency of all three poles (ω_0), none of the poles' natural frequencies dominate and limit the controller bandwidth. Either the natural frequency or the damping ratio is chosen as the design parameter from which the remaining parameters and gains are derived.

The natural frequency and damping ratio are both parameters of continuous-time systems. The mapping $z = e^{sT_s}$ maps continuous-time poles and zeros to their discrete-time equivalents. Mapping the continuous-time expression for a complex pole-pair or zero-pair in equation 3.1 to

discrete-time gives:

$$z = e^{-T_s\zeta\omega_0}\left(\cos\left(\omega_0 T_s\sqrt{1-\zeta^2}\right) \pm j\sin\left(\omega_0 T_s\sqrt{1-\zeta^2}\right)\right) \tag{5.10}$$

Equating each pole of equation 5.8 with 5.10 results in the discrete VSI poles:

$$p_0 = e^{-\omega_0 T_s} \tag{5.11}$$

$$p_{1,\Re} = e^{-\omega_0 T_s\zeta}\cos(\omega_0 T_s\sqrt{1-\zeta^2}) \tag{5.12}$$

$$p_{1,\Im} = e^{-\omega_0 T_s\zeta}\sin(\omega_0 T_s\sqrt{1-\zeta^2}) \tag{5.13}$$

The natural frequency to damping ratio relationship can be found numerically from the relationships in equation 5.11, 5.12 and 5.13 and the pole-pole relationship 5.9, to give:

$$e^{-\omega_0 T_s\zeta}\cos(\omega_0 T_s\sqrt{1-\zeta^2}) = \cos(\omega_n T_s) - \tfrac{e^{-\omega_0 T_s}}{2} \tag{5.14}$$

where T_s is the sample period, ω_n is the LC filter resonant frequency defined in equation 5.2, ω_0 is the closed loop natural frequency of all the poles and ζ is the closed loop damping ratio of the complex pole-pair. Equation 5.14 indicates that the relationship between ω_0 and ζ is solely based on the filter natural frequency ω_n and the sample period T_s, and is independent of the controller gains k_1 and k_2.

The poles in equations 5.11, 5.12 and 5.13 are found by numerically solving 5.14, then the gains k_1 and k_2 are derived from equation 5.8 as:

$$k_1 = \frac{p_0(4\cos(\omega_n T_s)^2 - 4\cos(\omega_n T_s)a0 + {p_0}^2 + 4{p_{1,\Im}}^2)}{4(1-\cos(\omega_n T_s))} \tag{5.15}$$

$$k_2 = \frac{4 - 4\cos(\omega_n T_s)p_0 + 3{p_0}^2 - 4\cos(\omega_n T_s)^2 - 4{p_{1,\Im}}^2}{4(1-\cos(\omega_n T_s))} \tag{5.16}$$

The steps for the calculating the controller gains can be easily automated, allowing a damping ratio or natural frequency to be used as the controller design parameter.

5.2.2 Feed-forward response

To complete the controller the feed-forward component $C_{Ff}(z)$ must also be found. The feed-forward component can be any realisable transfer function, but unnecessary forward response delays should be minimised. The simplest approach is to define $C_{Ff}(z)$ as the gain that results in a closed-loop DC gain of 0dB:

$$C_{Ff}(z) = 1 - \frac{k_1 + k_2}{2} \tag{5.17}$$

Feed-forward transfer functions other than pure gains will affect the forward response so that it no longer matches the design parameters. The feed-forward transfer function allows a controller to have a different forward response from its output impedance. In certain applications it may be preferable to have a faster responding forward response at the expense of additional overshoot, while having a heavier damped and more stable output impedance.

5.2.3 Theoretical performance

From equation 5.14 the relationship between the attainable pole frequency and damping ratio can be found for a given filter natural frequency and sampling frequency.

Figure 5.2 shows the achievable cutoff frequency bandwidth for a given damping ratio and filter resonant frequency, normalised to the sample frequency. This plot shows that the achievable bandwidth decreases for both an increasing damping ratio and as the filter resonant frequency approaches the Nyquist frequency. In practical applications a low damping ratio and high filter resonant frequency (relative to the sample frequency) are not preferred. Low damping ratios result in greater overshoot and ringing, and high filter resonant frequencies result in greater

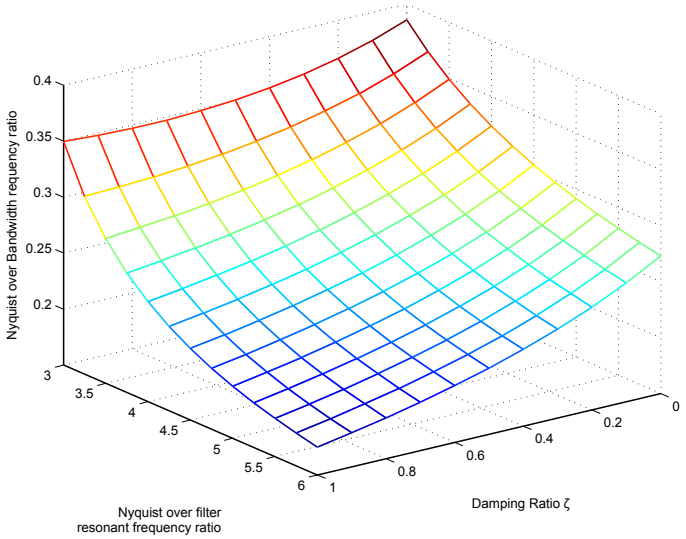


Figure 5.2: Plot of achievable bandwidth as a ratio of the sampling frequency, for a given damping ratio and filter resonant frequency (relative to the sampling frequency).

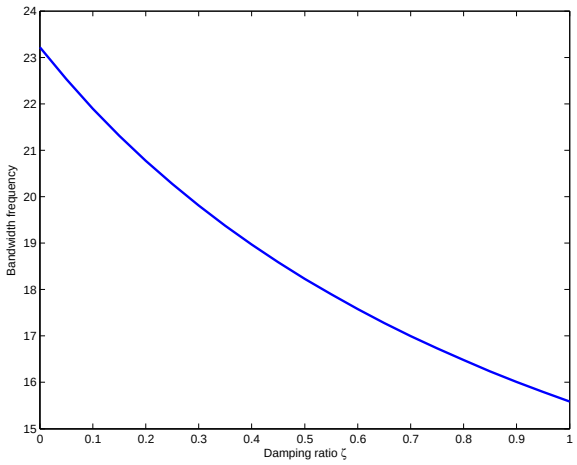


Figure 5.3: Plot of achievable bandwidth for a given damping ratio. $T_s = \frac{2\pi}{160}$, $L = 4\%$, $C = 10\%$.

output ripple.

As an example, an inverter with an 8kHz sampling frequency, 50Hz fundamental, 4% filter inductor and 10% filter capactior has a sampling to resonant frequency ratio of 5. Figure 5.3 shows the achieveable cutoff frequency for a given damping ratio and Figure 5.4 shows the actual poles for a damping ratio sweep for -0.1 to 1.0. For the discretised continuous-time VSI in Section 4.2.1 with the same filter components, and a damping ratio of 0.3, the 'best' achieveable cutoff-frequency was 11.4pu using gains $\omega_i = 8$ and $\omega_v = 18$. From Figure 5.3 a damping ratio of 0.3 results in a cutoff-frequency of 19.8pu, which is an increase of 74%.

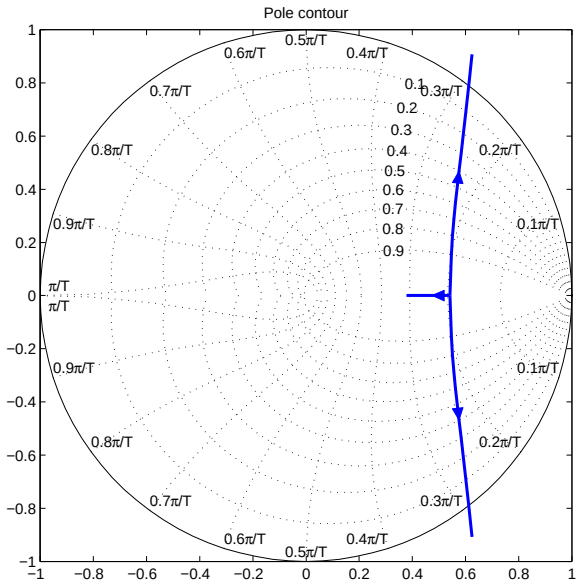


Figure 5.4: Pole contour for unloaded system, damping ratio ζ sweep from 1.0 to -0.1. $T_s = \frac{2\pi}{160}$, $L = 4\%$, $C = 10\%$.

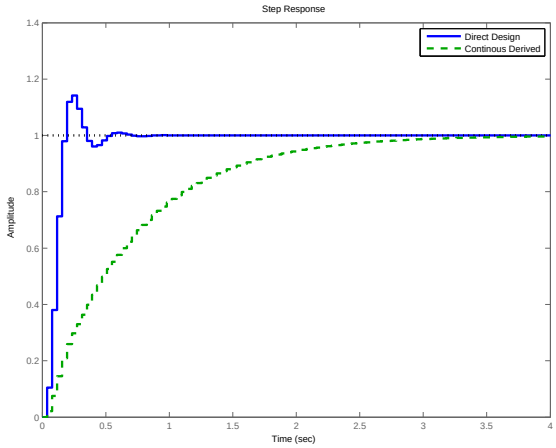


Figure 5.5: Step response of the proposed direct design controller and the benchmark discretised continuous-time controller. Both systems have a complex pole-pair damping ratio of 0.4. $T_s = \frac{2\pi}{160}$, $L = 4\%$pu, $C = 10\%$pu, $\omega_i = 6.1$, $\omega_v = \frac{3}{4}\omega_i$, damping ratio used as design parameter for direct design controller.

Previously the discretised continuous-time VSI could not achieve a dominant natural frequency above the fundamental with damping ratios greater than 0.5, whereas the direct design controller critically damped bandwidth ($\zeta = 1$) is still relatively high with a cutoff-frequency of 15.6pu.

Figure 5.5 shows the step response of the direct design controller compared to the discretised continuous-time-derived controller in Section 4.2.1. Given that the two controllers have significantly different bandwidths, the damping ratios of the complex pole-pair of each controller was

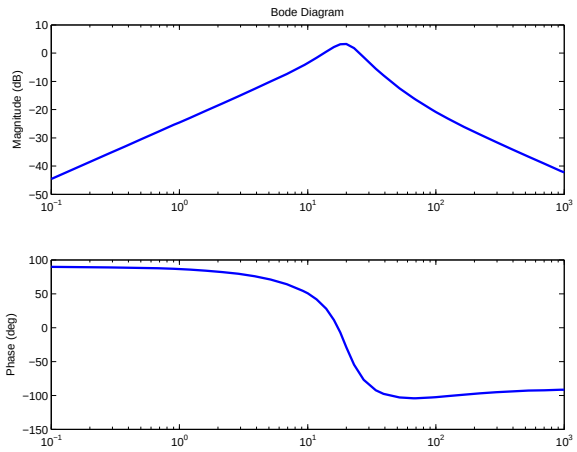


Figure 5.6: Direct design controller output impedance example. $T_s = \frac{2\pi}{160}$, $L = 4\%$, $C = 10\%$, damping ratio of 0.3 used as design parameter. Time scale is normalised frequency where a frequency of one corresponds to the fundamental.

equated. A damping ratio of 0.4 was chosen as it achieved adequate overshoot (less than 20%) and ringing for both controllers. Clearly visible in Figure 5.5 is that the direct design controller has a signifcantly faster response than the benchmark controller. The high frequency lightly damped complex pole-pair ($\zeta = 0.4$) is clearly visible in the direct design controller, evident as the ringing frequency. The lightly damped complex pole-pair in the benchmark controller is less evident as a result of the low frequency real pole that dominates the system response.

5.2.4 Output impedance

The discrete VSI output impedance is found in a similar manner to that of the discretised VSI in Section 4.2.1, and is derived in author's paper [31].

Using a damping ratio of 0.3 as the design parameter, Figure 5.6 shows an example output impedance. The output impedance has a typical inductive response up to the cutoff frequency, and a capacitive response as the frequency tends to infinity. From the figure the inductive impedance at the fundamental frequency is -24.5dB or 5.9%. The discretised VSI example with the same damping ratio had a similar output impedance. With a damping ratio of 0.5 the direct design controller has an impedance of 8%, while the discretised VSI has an output impedance of 16%, twice that of the direct design controller. This clearly indicates that for a poorly tuned

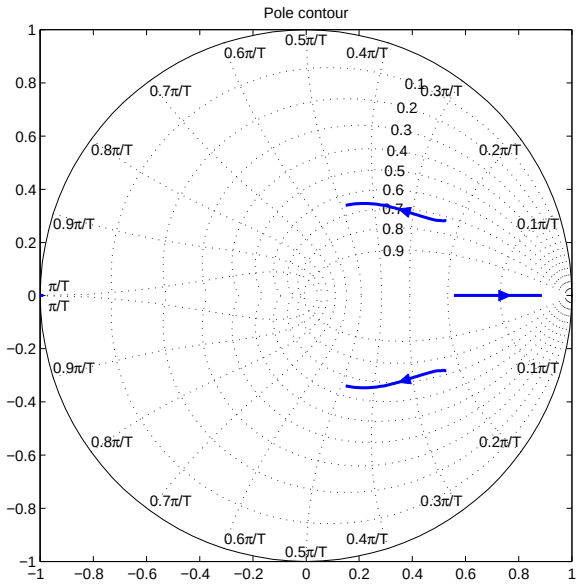


Figure 5.7: Pole contour for resistive load. Resistor impedance varied from 20pu down to 0.5. $T_s = \frac{2\pi}{160}$, $L = 4\%$, $C = 10\%$, designed with damping ratio of 0.7.

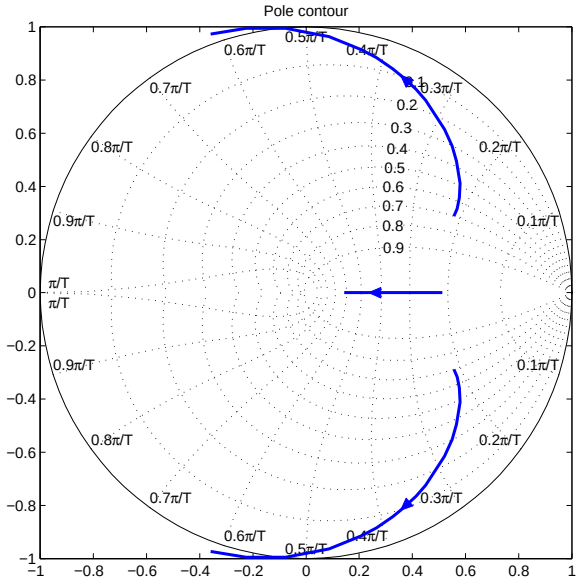


Figure 5.8: Pole contour for low impedance inductive load. Impedance varied from open circuit down to 0.5%. $T_s = \frac{2\pi}{160}$, $L = 4\%$, $C = 10\%$, designed with damping ratio of 0.7.

discretised VSI the output impedance will be significantly higher than that of the discrete direct design VSI.

Figures 5.7 and 5.8 show the effect on the system poles for purely resistive and inductive loads, respectively. The resistive loads figure illustrates that as the load increases the single real pole's natural frequency is reduced, lowering the system bandwidth, a common side-effect of controllers

that do not exhibit load compensation. The damping ratio of the complex pole remains relatively constant, dropping only slightly for large loads.

The inductive load pole contour is useful in determining how the controller performs under low impedance loads, including short circuit conditions, starting direct online (DOL) motors, or when coupled to a grid. Inductive loads have the effect of increasing the resonant frequency of the combined filter and load, which can lead to controller instability. From Figure 5.8 the controller becomes unstable for load impedances below 0.74%. In Figure 5.8 the unloaded filter has a natural frequency of 15.8pu, whereas the marginally stable combined filter and load has a natural frequency of 40pu. In grid-connected applications the use of a coupling impedance between the inverter and the grid provides an adequate minimum impedance to ensure stability.

Of particular importance when addressing robustness to loads is how the system performs with high-order loads. High-order systems typically have a response dominated by a single complex pole-pair, the worst are resonant loads with little or no damping. A common example is a power factor corrected induction machine. Power factor capacitors are sized according to the machine's magnetising inductance. The power factor capacitors then have the potential to resonate with both the magnetising inductance (at the fundamental) and the leakage inductance (at a high frequency). The low frequency resonance at the fundamental is well inside the controller bandwidth, but the high frequency resonance can be an issue. In an example setup where a motor has a 3pu magnetising inductance, the power factor capacitors will be 33%. The power factor capacitors and the series motor leakage and inverter impedance form a resonant pole-pair. Driven by the controller with a designed damping ratio of 0.4, the resonant pole-pair is sufficiently damped to a damping ratio of 0.24.

The issue of connecting to low impedance systems is further discussed in Chapter 6 where parallel-connected inverters are investigated.

5.3 PRACTICAL IMPLICATIONS

In Chapter 4 each of the controllers discussed exhibited characteristics that reduced their suitability in certain practical applications. Such limitations include robustness to component value sensitivities, inadequate output impedance, ability to limit currents and voltages for system protection, and the ability to accommodate delays. This section details some of the practical implications of the proposed controller and how they have been addressed.

5.3.1 Robustness

One of the key considerations when developing the discrete direct design VSI controller was for it to be robust. In practical applications the primary robustness considerations are the ability to be immune to component variations and to tolerate some level of noise in the feedback signals, including switching ripple.

Component value sensitivities

The effect of component variations depends solely on system poles as a function of the component values. System poles are a function of the resonant frequency ω_n of the LC filter. By definition of ω_n in equation 5.3, the inductor and capacitor have the same effect on the resonant frequency. Figure 5.9 illustrates the robustness of the controller with a $\pm 10\%$ filter inductor or capacitor variation. Typical component variations for inductors and capacitors are between 5 and 20%. As illustrated in the figure, the natural frequency of the poles vary between 12 and 24pu, while the damping ratio has a considerably lower deviation of 10%. From the figure a 10% lower LC product results in a lower natural frequency for the real pole of 12.4pu (originally 17pu), but a greater natural frequency of the complex pole-pair of 20.6pu. For a 10% greater LC product the real pole natural frequency is greater at 24pu, while the complex pole-pair natural frequency is 12.6pu. In each case the lower pole natural frequency becomes the dominant pole, effectively

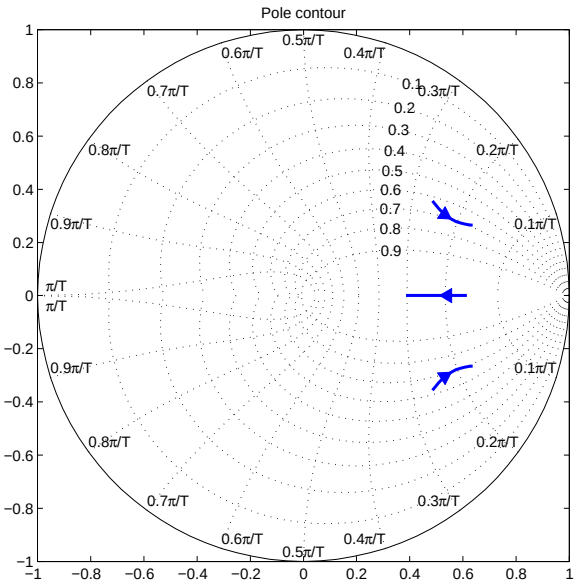


Figure 5.9: Pole contour for unloaded system illustrating component sensitivity. The LC product is varied by $\pm 10\%$. Nominal $L = 4\%$, $C = 10\%$. $T_s = \frac{2\pi}{160}$, designed with damping ratio of 0.7.

lowering the controller bandwidth. Fortunately, although component value variations result in a lower natural frequency for the dominant pole, due to the increasing separation of the pole natural frequencies, the bandwidth does not drop at a rate proportional to the natural frequency of the dominant pole.

Feedback sampling

In any practical application any signal in an industrial environment is likely to be exposed to noise. In the case of inverters the switching devices themselves are a source of noise, including the PWM switching frequency and high frequency noise from the high $\frac{dV}{dt}$ switching edges and high semiconductor $\frac{dI}{dt}$. Unfortunately it must be assumed that noise will couple into any feedback path.

Despite the apparent robustness of the proposed inverter, in its present form the controller has an incredibly high gain at the Nyquist frequency as a result of the pole at $z = -1$ in equation 5.5. Any high frequency noise in the capacitor voltage feedback signal will be amplified, resulting in an even noisier PWM reference signal. The severity of the high-gain high-frequency pole can be

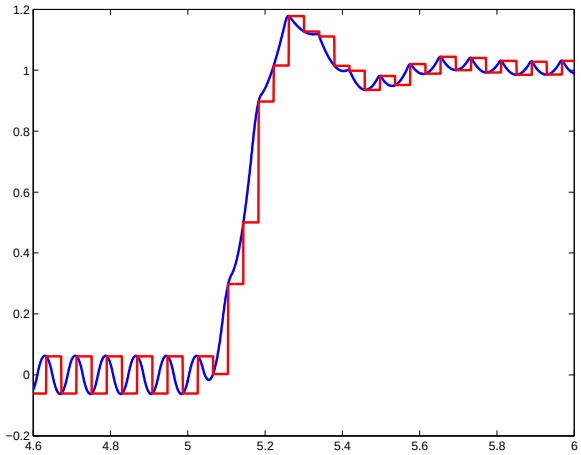


Figure 5.10: Step response of direct design controller with dual-edge sampled PWM with a whole sample period delay. Blue and red traces are actual and sampled capacitor voltages, respectively. $T_s = \frac{2\pi}{160}$, $L = 4\%$, $C = 10\%$, designed with damping ratio of 0.4, $k_1 = 1$, $k_2 = -0.23$, $k_3 = 0.65$, pole natural frequency $\omega_n = 18.3$pu. 1pu PWM reference corresponds to a 90% duty cycle.

reduced by sacrificing a small amount of bandwidth/stability margin by moving the $z = -1$ pole towards the origin. This is achieved by an additional control parameter k_3, changing equation 5.5 to:

$$C_{Fb,V_c}(z) = \frac{k_2 z + k_1}{z + k_3} \tag{5.18}$$

With the addition of k_3, the $z = -1$ zero in equation 5.2 is no longer cancelled and the system becomes fourth-order. When specifying the response of the controller, gains k_1 and k_2 are most conveniently derived by first assuming $k_3 = 1$ and calculating the gains as usual. A value for k_3 is then chosen that reduces the effect of noise amplification to a suitable level for a given application. Alternatively, mathematical solvers can also be used to solve the fourth-order system for the gains. By reducing k_3 from 1 to 0.65 the reduction in the cutoff frequency is less than 10% (< 2 for a system with a bandwidth of 20).

An unavoidable example of high frequency noise is in systems that sample the filter states at twice the switching frequency (regular PWM updating both the rising and falling edge). In fact without having a k_3 gain below 1 the controller with a dual-edge sampled PWM and a single sample period delay is not stable. Figure 5.10 shows a 1pu step response of the VSI with a k_3 gain of 0.65. Although stable the output shows excessive ripple. There is also a $\pm 22\%$ oscilation

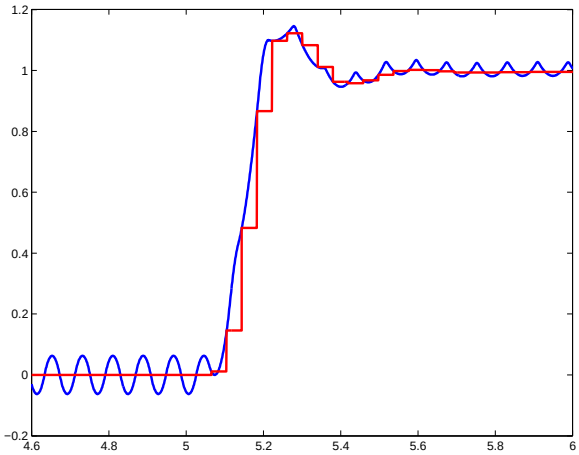


Figure 5.11: Step response of direct design controller with dual-edge sampled PWM with a half sample period delay. Blue and red traces are actual and sampled capacitor voltages, respectively. $T_s = \frac{2\pi}{160}$, $L = 4\%$, $C = 10\%$, designed with damping ratio of 0.4, $k_1 = 1.9$, $k_2 = -1.5$, $k_3 = 0.65$, pole natural frequency $\omega_n = 23$pu. 1pu PWM reference corresponds to a 90% duty cycle.

in the PWM reference signal at steady-state for an input reference of zero. Unfortunately the capacitor voltage ripple peaks align with the sample point when the sample delays are integer multiples of the sample period. By making the sample points 180 degrees out of phase with the PWM update points the switching ripple is eliminated in a similar manner to that of sampling inductor current as previously discussed in Section 3.6.1. Sampling 180 degrees out of phase with the PWM update points implies non-integer multiple delays of the sample period, therefore the original design assumption of a single sample period delay no longer holds and the gains must be modified to accommodate the different delay. The discretised LC filter with a fractional delay is:

$$H(s) = e^{-sT_d}\frac{1}{s^2LC+1} \tag{5.19}$$

$$H_{ZOH}(z) = \mathcal{Z}_{ZOH}\left\{\frac{1}{s^2LC+1}, T_d\right\} \tag{5.20}$$

$$= \frac{(z^2 - 2z\cos(\omega_n T_s) + 1) + (z-1)(\cos(\omega_n T_d) - z\cos(\omega_n(T_s - T_d)))}{z(z^2 - 2z\cos(\omega_n T_s) + 1)} \tag{5.21}$$

where T_d is the fractional delay of T_s and the ZOH operator takes the fractional delay as the second argument for the extended "Advanced Z transform".

Figure 5.11 again shows the step response of the controller with an actual PWM modulator, but with a half sample period delay rather than a whole sample period delay. In contrast to the example with a whole sample period delay shown in Figure 5.10, at steady-state there is no sampled output ripple and consequently the PWM reference signal has no oscillation either. In addition to the reduction in ripple, the small delay permits a greater natural frequency of the system poles, with an increase from 18.3pu to 23pu for this example.

5.3.2 Protection limits

As mentioned in Chapter 2 implementation hardware is constrained in many ways including the current each component can carry and the voltage it can tolerate. In addition to this PWM modulators can only generate ±1pu of the DC bus voltage. To ensure that the constraints for each component are not exceeded, control limits must be incorporated. Thankfully the discrete controller has no natural integrating effect which makes output voltage limiting as simple as a saturation block.

In the previous chapter the continuous-time VSI due to its cascaded nature of a capacitor voltage controller controlling an inductor current controller, current limits can be simply implemented by limiting the inductor current reference from the voltage controller. Unfortunately the proposed discrete controller does not have an intrinsic inductor current reference signal upon which inductor current limits can be implemented. A current limit however requires knowledge of the actual inductor current, which implies an additional sensor feedback. Despite the addition of an additional feedback signal, the current signal will only be used to compare against a saturation limit function. By only using the current feedback for saturation, any noise in the signal only affects the output when the current is outside the limits.

To provide current limiting an inductor current limiting function was added to the output of the discrete voltage controller before the PWM modulator as shown in Figure 5.12. Signals

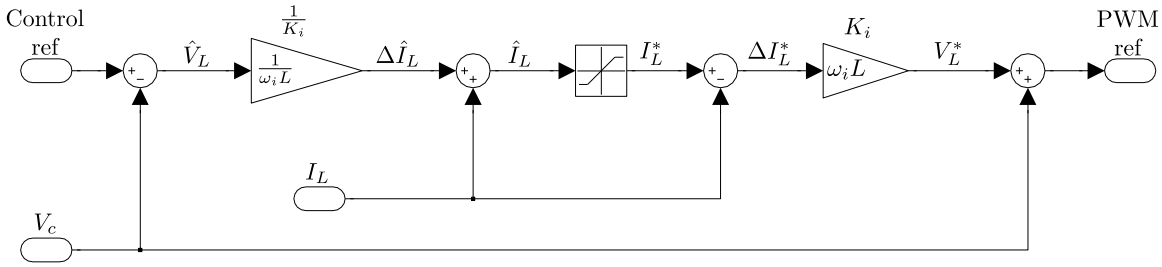


Figure 5.12: Discrete controller inductor current saturation.

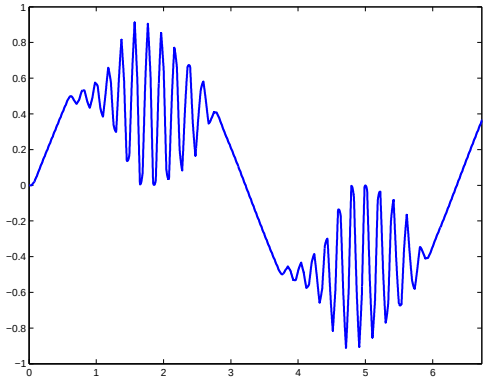


Figure 5.13: Example of uncontrolled filter oscillations during current limit. 1pu fundamental reference signal with a 1pu resistive load, inductor current limits set at ±0.5pu, current limit $\omega = 35$pu.

with a hat indicate calculated values for the next time step, while signals with a star indicate reference values for the present time step. The limiting function calculates what effect the controller reference signal will have on the inductor current $\Delta\hat{I}_L$ in the next time step which is then added to the measured inductor current to calculate the current in the next time step $\hat{I}_L$. The calculated current for the next time step is then saturated to the required limit. The output signal to the PWM module is then reconstructed from the saturated inductor current signal I_L^*.

The key consideration for the current limiting function in Figure 5.12 is the selection of the gain K_i, specifically its design parameter ω_i. The current limiting function effectively acts as an observer by calculating what the inductor current will be in the next time step. $\hat{V}_L$ is the calculated inductor voltage for the next time step and $\Delta\hat{I}_L$ is the expected inductor current change. To correctly calculate $\Delta\hat{I}_L$, K_i should accurately represent the inductor integrating effect $\frac{1}{sL}$, so for one time step ω_i should be $\frac{1}{T_s}$.

Although selecting ω_i to be $\frac{1}{T_s}$ accurately calculates the change in the inductor current over the

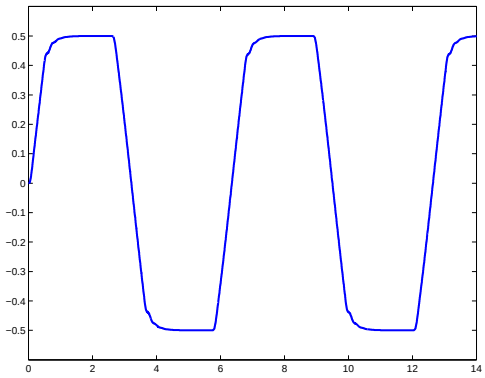


Figure 5.14: Example of clean operation during current limit. 1pu fundamental reference signal with a 1pu resistive load, inductor current limits set at ±0.5pu, current limit $\omega = 15$pu.

next time step, if the saturation block acts to limit the inductor current the PWM reference will be hard limited and the output filter will no longer be controlled. Figure 5.13 shows the effect of uncontrolled filter oscillations when $\omega_i = \frac{1}{T_s}$. In the figure the current limit is set at ±0.5pu while a 1pu resistive load attempts to draw close to 1pu current. Clearly evident are the uncontrolled filter oscillations when the current limit is in operation.

By choosing a lower value for ω_i than $\frac{1}{T_s}$ the response of the current limit is lowered slightly and the filter oscillations that were evident in Figure 5.13 are completely removed. Figure 5.14 shows the same example again but with $\omega_i = 15$pu. Clearly evident in this example, the filter oscillations have completely gone and the current is cleanly limited to 0.5pu. Unfortunately if the limit response ω_i is set too low relative to the sample rate the observer over-estimates the inductor current and the limit function may prematurely limit the current before the actual limit is reached.

5.3.3 Elimination of steady-state errors

In Section 4.2 integrators for DC systems and resonators for AC systems were discussed as a means of eliminating steady-state errors at chosen frequencies of interest (usually the fundamental). Steady-state errors can be removed by adding the output of an integrator or resonator operating on the voltage error to the control reference input. Anti-windup feedback is recom-

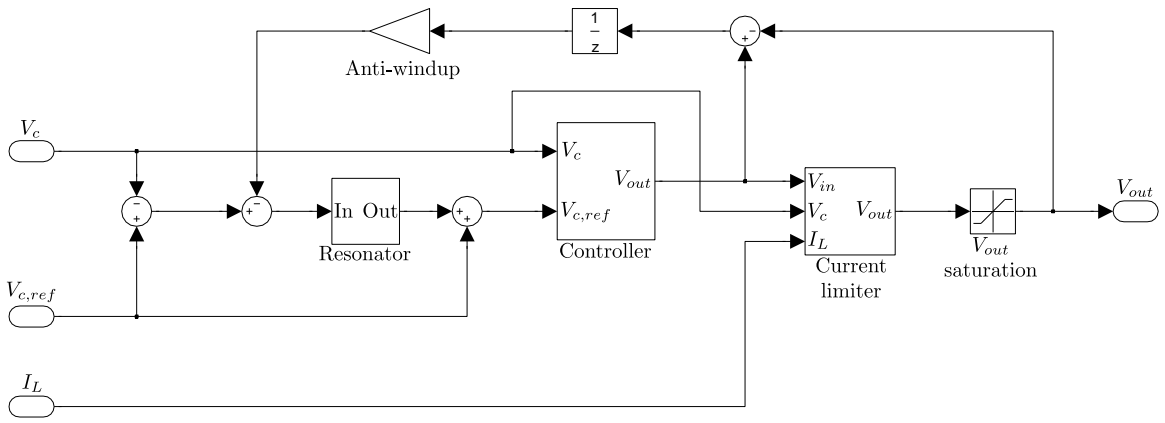


Figure 5.15: Complete discrete controller with resonator and current limiting.

mended in applications where the PWM reference may be limited.

5.4 PRACTICAL APPLICATION

The responses of both the proposed direct discrete controller and the discretised continuous-time controller have been confirmed both numerically in simulation and in practice on the test hardware platform. MATLAB Simulink confirmed the analytical results both in the simulation results and also through the use of the Simulink Linearization Analysis Toolbox. Details of the test hardware platforms are in Appendix G.

Figure 5.15 shows the complete controller used for testing, including the resonator, current limiting, and anti-windup feedback. Each signal represents an $\alpha\beta$ pair for three phase systems. When performing step and load responses the resonator was disabled to accurately represent the inverter output impedance.

To ensure current sharing between parallel modules conventional voltage droop that operates on the individual module's output current is used. In both simulation and hardware a droop of 1% is used. Simulations demonstrated negligible effect on the response of any of the control systems due to voltage droop. In hardware tests, tight component tolerances meant that the 1% droop provided adequate current sharing.

In both simulation and hardware a whole sample time delay was used with sampling at 8kHz

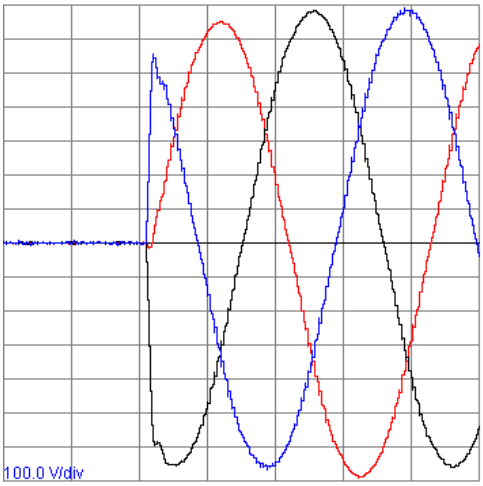


Figure 5.16: Open circuit 3ϕ voltage step response of discrete direct design controller. Step from $V_{ref} = 0\%$ to $V_{ref} = 100\%$ on sixteen module, 2MVA system. $T_s = \frac{2\pi}{160}$, $L = 4\%$, $C = 10\%$, $k_1 = 1$, $k_2 = -0.2$, $k_3 = 0.65$, damping ratio of 0.4 used as design parameter. V_c: 100V/div; time: 5ms/div.

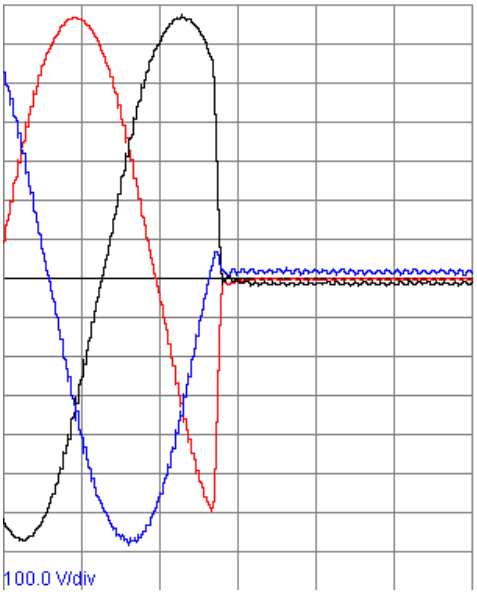


Figure 5.17: Open circuit 3ϕ voltage step response of discrete direct design controller. Step from $V_{ref} = 100\%$ to $V_{ref} = 0\%$ on sixteen module, 2MVA system. $T_s = \frac{2\pi}{160}$, $L = 4\%$, $C = 10\%$, $k_1 = 1$, $k_2 = -0.2$, $k_3 = 0.65$, damping ratio of 0.4 used as design parameter. V_c: 100V/div; time: 5ms/div. Note: the DC offset is due to the differential VTs used.

(4kHz dual-edge update PWM). To improve noise immunity a k_3 gain of 0.65 was used. The k_1 and k_2 gains were calculated for a damping ratio of 0.4.

Figures 5.16 and 5.17 show the open circuit step responses of the discrete direct design controller, for a 0 to 100% voltage reference step and a 100 to 0% reference step respectively. The tests were conducted on the largest test system of 1MVA, and a damping ratio of 0.4 was used as the

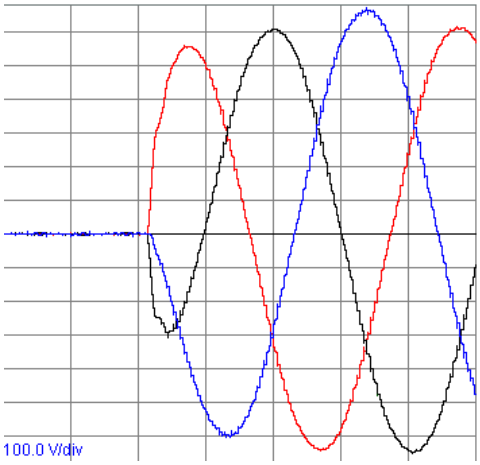


Figure 5.18: Open circuit 3ϕ voltage step response of discretised continuous-time controller. Step from $V_{ref} = 0\%$ to $V_{ref} = 100\%$ on a sixteen module, 2MVA system. $T_s = \frac{2\pi}{160}$, $L = 4\%$, $C = 10\%$, $\omega_i = 8$, $\omega_v = 6$. V_c: 100V/div; time: 5ms/div.

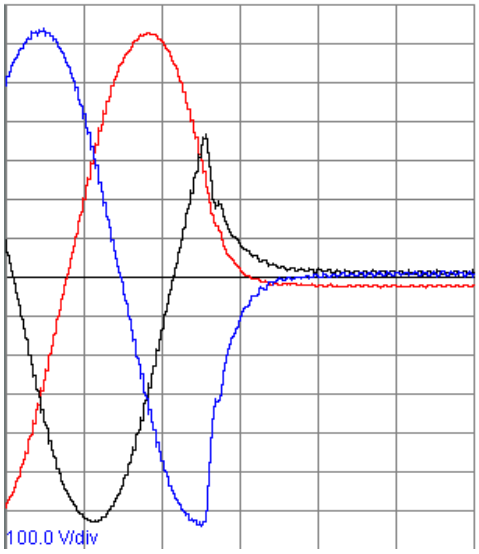


Figure 5.19: Open circuit 3ϕ voltage step response of discretised continuous-time controller. Step from $V_{ref} = 100\%$ to $V_{ref} = 0\%$ on a sixteen module, 2MVA system. $T_s = \frac{2\pi}{160}$, $L = 4\%$, $C = 10\%$, $\omega_i = 8$, $\omega_v = 6$. V_c: 100V/div; time: 5ms/div. Note: the DC offset is due to the differential VTs used.

control design parameter. The two responses exhibit a fast response with little overshoot, closely matching the 0.4 damping ratio design parameter. The small overshoot and ripple apparent in the step responses are approximately one third smaller than simulations predicted, attributed to resistive damping provided by the filter components.

Figures 5.18 and 5.19 show the same two step responses with the discretised continuous-time-derived controller. Compared to the discrete direct design step responses, the discretised continuous-

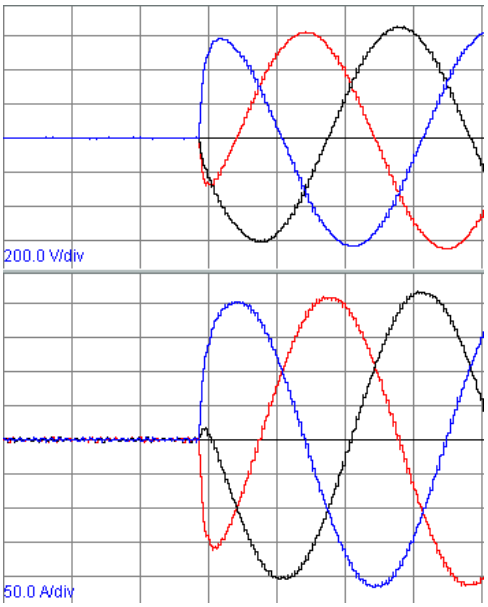


Figure 5.20: Step response of 3ϕ discrete direct design controller with 1pu resistive load, showing output voltage (top) and output current (bottom). Step from $V_{ref} = 0\%$ to $V_{ref} = 100\%$ on a three module, 125kVA system. $T_s = \frac{2\pi}{160}$, $L = 4\%$, $C = 10\%$, $k_1 = 1$, $k_2 = -0.2$, $k_3 = 0.65$, damping ratio of 0.4 used as design parameter. V_c: 200V/div; I_o: 50A/div; time: 5ms/div.

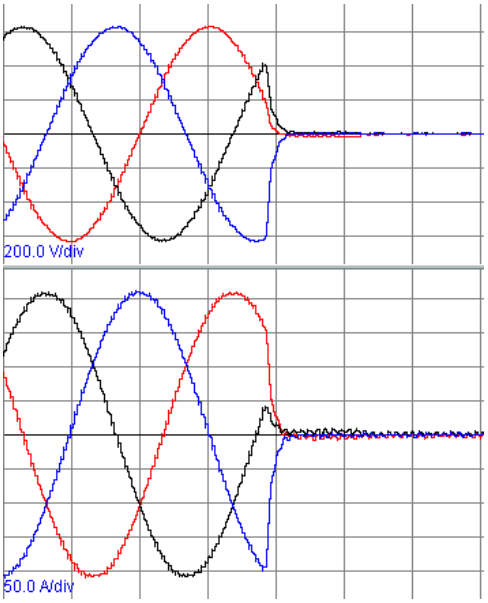


Figure 5.21: Step response of 3ϕ discrete direct design controller with 1pu resistive load, showing output voltage (top) and output current (bottom). Step from $V_{ref} = 100\%$ to $V_{ref} = 0\%$ on a three module, 125kVA system. $T_s = \frac{2\pi}{160}$, $L = 4\%$, $C = 10\%$, $k_1 = 1$, $k_2 = -0.2$, $k_3 = 0.65$, damping ratio of 0.4 used as design parameter. V_c: 200V/div; I_o: 50A/div; time: 5ms/div.

time controller step responses have a slower rolloff, matching the calculated 6pu dominant pole.

Figures 5.20 and 5.21 show the step responses of the discrete direct design controller with a 1pu resistive load, for a 0 to 100% voltage reference step and a 100 to 0% reference step respectively.

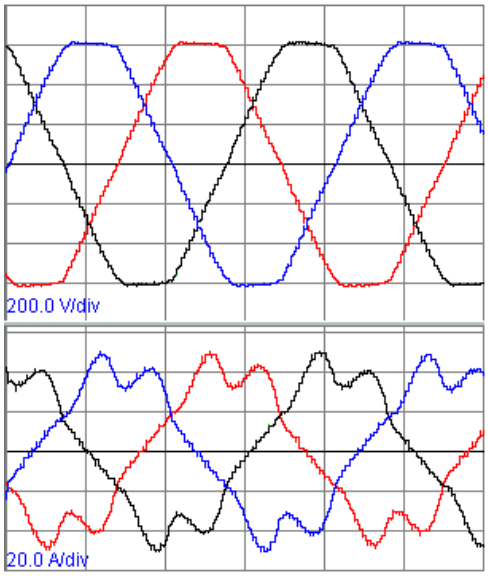


Figure 5.22: Voltage and current waveforms of 3ϕ discrete direct design controller with resistive and nonlinear load, showing line to line output voltage (top) and output current (bottom). 50% (RMS) resistive and 50% nonlinear load on a single 42kVA inverter module. Diode rectifier, cap and resistor with 3% line reactor used as nonlinear load. $T_s = \frac{2\pi}{160}$, $L = 4\%$, $C = 10\%$, $k_1 = 1$, $k_2 = -0.2$, $k_3 = 0.65$, damping ratio of 0.4 used as design parameter. V_c: 200V/div; I_o: 20A/div; time: 5ms/div.

The tests were conducted on the 125kVA hardware platform. The figures show a fast, clean response with no overshoot or ringing. The loaded system exhibited a 0.6% droop in output voltage, which correlates perfectly with the predicted fundamental output impedance calculation.

Figure 5.22 shows steady-state voltage and current waveforms of the discrete direct design controller with a diode rectifier nonlinear load. The voltage waveform (line to line) exhibits the increasingly common flat-top characteristic, often observed on low voltage distribution grid networks. The inverter impedance was calculated to be 7%.

5.5 SUMMARY AND DISCUSSIONS

When constructing high performance power inverter configurations which have a constrained switching frequency, achieving the best possible forward response and output impedance requires high performance controllers. As more control systems use discrete-time controllers, as the demand for performance increases in Chapter 4 discretised traditional continuous-time controllers

demonstrated non-ideal characteristics, resulting in reduced stability margins and reduced performance. Discrete-time controllers such as deadbeat control offer a high performance controller but inherently are not overly robust to component variations.

This chapter details a relatively simple to implement discrete-time controller using constrained pole-placement that offers the ability to trade off the response against the damping ratio. Through the use of an offline calculation the controller gains can be derived that achieve either a desired system-pole natural frequency or damping ratio. The controller demonstrates a high robustness to both component value variation and low impedance loads. Component value variations result in a shift of the system poles' natural frequency but have little effect on their damping ratio. The simple first order discrete design is not only relatively simple to implement in hardware, it only requires a single capacitor voltage feedback.

Further analysis of the controller uncovered potential issues that may arise in practical applications. Methods for reducing ripple, removing steady state errors and enforcing current limits are provided which are often required in practical applications. The controller performance and robustness has been confirmed on both monolithic and parallel configurations of up to 2MVA.

The high performance controller is the first component in constructing a high performance and high power grid-connected inverter system. Following the investigation of a high performance controller, the next chapter details the implications of paralleling inverters to achieve a scalable high power system.

Chapter 6

PARALLEL CONFIGURATIONS

6.1 INTRODUCTION

In Chapter 2 it was concluded that due to semiconductor device limitations the only practical way to increase an inverter's current capacity without sacrificing bandwidth is to parallel individual devices. In addition to the redundancy advantages discussed in Section 2.6, the various methods of paralleling individual inverters are numerous, and many different approaches have received significant attention in recent years.

In [5] regarding parallel system topologies, the definition of what constitutes a parallel system defines the paralleling mechanism as either passive or active. Passively paralleled systems are those in which load balancing relies entirely on the characteristics of the physical implementation, such as inter-module filter impedances and dead-times. In passive systems there is no differential change in the control reference as a result of module imbalance. Actively paralleled systems have some form of active balancing in the control loop. The control loop makes active adjustments for each parallel module to correct any imbalance.

This thesis expands on the work in [5] regarding actively controlled parallel inverter configurations. Specifically, active parallel inverters, each with their own separate controller, where each module receives the same output voltage reference signal from a master controller. In this manner the master controller treats the combined parallel modules as a single voltage source inverter. Each module is assumed to actively reduce or eliminate imbalance thus yielding a total

rated current equal to the sum of the individual module current ratings. In this manner any number of modules can be connected in parallel while the master module is only concerned with the total system current.

To ensure adequate current sharing between modules the resistive droop method has been employed in the parallel test hardware (Appendix G). This simple method is shown in Figure 6.2. Each module estimates its output current by subtracting the calculated filter capacitor current from the measured filter inductor current. In [5] the controller used was the benchmark discretised continuous-time controller described in Section 4.2.1.

In this chapter, the first section describes an analytical investigation into the instabilities that can occur with parallel arrays of inverters in a grid-connected configuration. First, the stability implications of parallel modules with LC filters are addressed, followed by the additional effects of using LCL filters. Both simulation and experimental results on the test hardware setup (Appendix G) confirm the findings. Having investigated the cause of the instabilities, methods to ensure stability are provided (originally detailed in [32]). The discrete direct design controller described in Chapter 5 is also examined and is shown to offer stability improvements over the discretised continuous-time controller.

Throughout the chapter the following convention with respect to indices is adhered to: for an n-module system an index i implies the subject module, and an index j implies each of the remaining $n-1$ identical modules. As an example Figure 6.1 shows the use of indexing for one module in a multi-module configuration. As suggested in Figure 6.1, for module one $G_{V_{c,i}V_{pwm,i}}$ is the component of the module one capacitor voltage ($V_{c,1}$) contributed by its own PWM voltage ($V_{pwm,1}$), and $G_{V_{c,i}V_{pwm,j}}$ is the component of $V_{c,1}$ contributed by the sum of the other PWM voltages ($\sum_{k=2}^{n} V_{pwm,k}$).

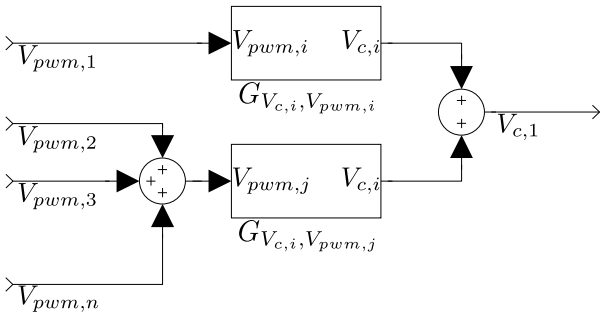


Figure 6.1: Indexing example for a n-module system showing module 1 capacitor voltage $V_{c,1}$ as a function of each PWM voltage

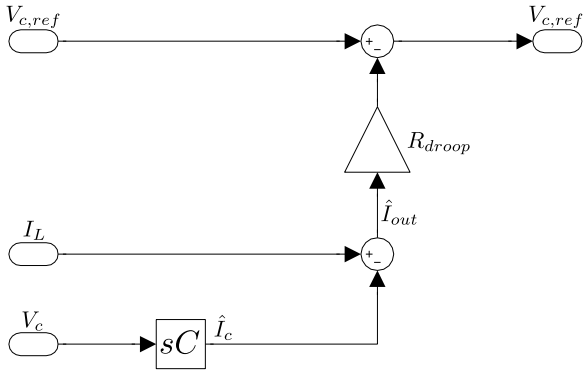


Figure 6.2: Resistive droop current sharing.

6.2 STABILITY ANALYSIS

Figure 6.3 shows the single-wire connection diagram for an actively paralleled, grid-connected, 2-level VSI. In practical applications there exists some form of coupling impedance L_c between each module. The coupling impedance may be purely a side effect of the geographical location of the inverters, or may be dominated by a deliberately inserted impedance. A parallel configuration is herein defined to be hard-coupled when the coupling impedance (line reactor) is zero ($L_c = 0$, LC filter with capacitors all tied together) and soft-coupled when there is a real coupling impedance ($L_c \neq 0$, LCL filter with independent capacitor voltages). Not shown is the master module which propagates the same output voltage reference signal to each module.

Small-signal stability is first investigated for a theoretical hard-coupled parallel configuration and then is expanded to the more practical soft-coupled configuration. A large amount of work has been done in the area of the stability of parallel grid-connected inverters [10,33–46], but due

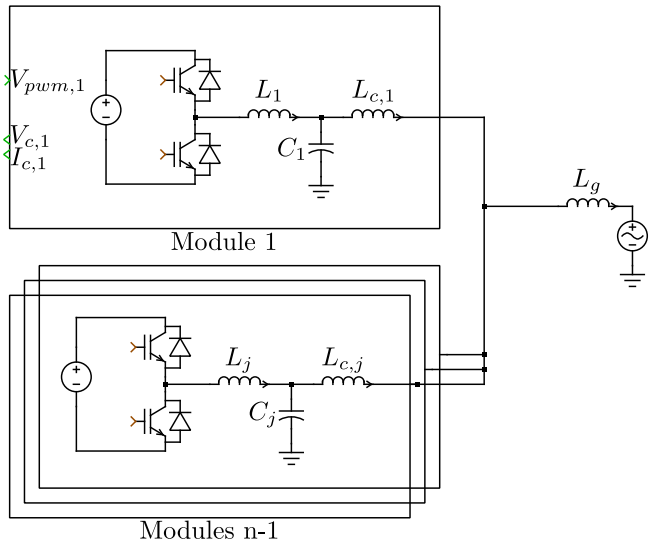


Figure 6.3: Soft-coupled Parallel VSIs.

to the complexity of parallel-connected systems they have only been investigated in continuous-time. To uncover the cause of the observed instability a small-signal analysis is performed in discrete-time. However, the complexity of analysing discrete-time inverters with low impedance loads is compounded when independently controlled inverters are connected in parallel [44–46].

The use of additional integrators (or AC resonators) is neglected for the stability analysis. For the small-signal stability analysis of the grid-connected VSI, the grid is treated as a low impedance (inductive) load. Typical grid-connect impedances range from a stiff grid scenario of less than 1% up to a weak grid of 20%. To achieve results independent of the number of modules, the grid load impedance L_g in Figure 6.3 is scaled by n such that $L_g = \frac{L_{g,per\ module}}{n}$.

The small-signal stability of an n-module system is defined by the pole locations of the closed-loop system. To determine the closed-loop system poles, the expression for the first module's capacitor voltage $V_{c,1}$ with respect to the voltage reference $V_{c,ref}$ is derived. In the following sections where non-identical modules are examined, the systems are disturbed by altering only the first module's parameters while using the specified nominal values for the remaining modules.

For the discretised continuous-time VSI in Section 4.2.1, the inverter is broken up into separate blocks for the controller and output filter, as shown in Figure 4.5. So far in this thesis only single

module inverters have been analysed and only a single module output filter and load has been discretised. For modular systems where the filter outputs are connected together, the entire combination of filters and loads must be discretised as a whole. In the hard-coupled scenario all the module capacitors are connected in parallel and therefore each controller senses the common capacitor voltage. The sensed capacitor currents are identical for identical capacitor values.

6.2.1 Hard-coupled parallel configuration

Firstly the output filter expressions as a function the PWM voltages must be obtained. Equating the capacitor and load currents in Figure 6.3 where $n-1$ of the modules have identical inductors L_j and module one has filter inductance L_1:

$$\frac{V_{pwm,1} - V_c}{sL_1} + \frac{\sum_{k=2}^{n} V_{pwm,k} - V_c}{sL} = V_c \left(nsC + \frac{1}{sL_g} \right) \tag{6.1}$$

Solving for V_c:

$$V_c(s) = \frac{(V_{pwm,1}(s)L + \sum_{k=2}^{n} V_{pwm,k}(s)L_1)L_g}{s^2 LL_1L_gCn + L_g(L + L_1(n-1)) + LL_1n} \tag{6.2}$$

$$V_c(s) = G_{V_c,V_{pwm,i}} V_{pwm,i} + G_{V_c,V_{pwm,i}} V_{pwm,j} \tag{6.3}$$

The capacitor currents are derived as:

$$I_{c,i}(s) = \frac{V_{c,i}(s)}{Z_c} = sCV_{c,i}(s) \tag{6.4}$$

For an identical module system where L_1 to $L_j = L$ and $V_{pwm,1} = V_{pwm,i}$, substituting into equation 6.2 produces:

$$V_c(s) = \frac{\sum_{k=1}^{n} V_{pwm,k}(s)L_g}{n(s^2 LL_gC + L_g + L)} \tag{6.5}$$

As each controller samples the same common capacitor voltage each controller produces the

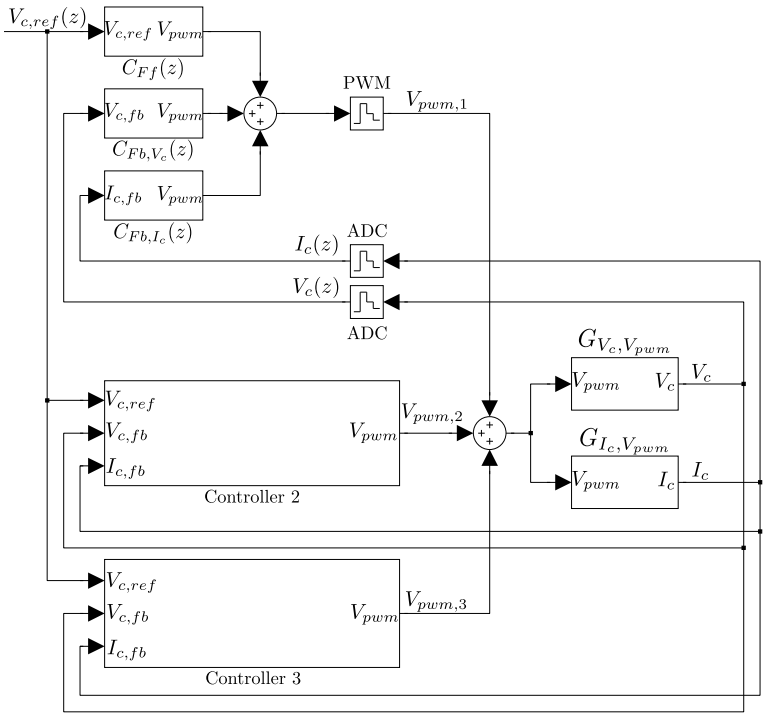


Figure 6.4: Identical 3 module hard-coupled parallel configuration. Module 1 controller unmasked.

same PWM reference V_{pwm}, and therefore $V_{pwm,i} = V_{pwm,j}$.

The discretised PWM to capacitor voltage transfer function (demonstrated in Section 3.4.2) for identical parallel filters in equation 6.5 is:

$$G_{V_c,V_{pwm}}(z) = \frac{L_g(z+1)\left(1-\cos\left(T_s\sqrt{\frac{L_g+L}{LL_gC}}\right)\right)}{n(L_g+L)\left(z^2-2z\cos\left(T_s\sqrt{\frac{L_g+L}{LL_gC}}\right)+1\right)} \tag{6.6}$$

Compared to the discretised LC filter in Section 3.4.2 which has a single resonant frequency of $\frac{1}{\sqrt{LC}}$, the parallel grid-coupled filters also have a single resonant frequency of $\sqrt{\frac{L_g+L}{LL_gC}}$. Although the natural frequency is dependent on the grid impedance L_g, the system order remains the same.

Combining the discretised filter components and closing the loop produces the capacitor voltage

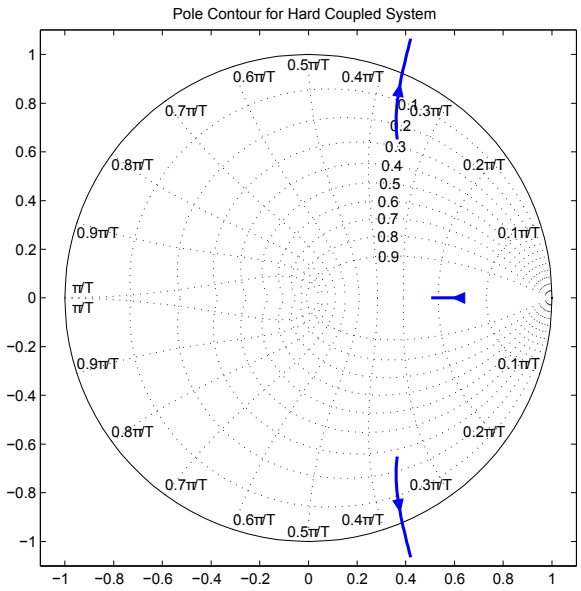


Figure 6.5: Pole contour of hard-coupled system with ω_i gain sweep from 5 to 20pu. $T_s = \frac{2\pi}{160}$pu, $L = 4\%$pu, $C = 10\%$pu, $L_g = 5\%$pu, $\omega_v = \frac{3}{4}\omega_i$, identical module system.

as a function of the input reference:

$$G_{V_c,V_{pwm}} = G_{V_c,V_{pwm},i}(z) + G_{V_c,V_{pwm},j}(z) \tag{6.7}$$

$$G_{I_c,V_{pwm}} = G_{I_c,V_{pwm},i}(z) + G_{I_c,V_{pwm},j}(z) \tag{6.8}$$

$$\frac{V_c(z)}{V_{c,ref}(z)} = \frac{C_{Ff}C_{Fb,V_c}G_{V_c,V_{pwm}}}{1-(C_{Fb,V_c}G_{V_c,V_{pwm}} + C_{Fb,I_c}G_{I_c,V_{pwm}})} \tag{6.9}$$

From equation 6.9 it can be seen that for a hard-coupled parallel configuration of identical inverters there is no longer any dependency on the number of parallel modules, n. This provides the likely conclusion that n *perfectly identical* modules with the same input reference are mathematically equivalent to one large inverter, n times the size of an individual module.

A controller gain frequency ratio of $\omega_v = \frac{3}{4}\omega_i$ was chosen as a benchmark gain ratio as it results in a damping ratio of 0.6 for the continuous-time controller (Section 4.2, equation 4.5). Figure 6.5 shows the discretised hard-coupled VSI for a gain sweep of ω_i from 5pu to 20pu. The hard-coupled configuration becomes unstable at $\omega_i = 14.6$pu. This sets a benchmark for the discretised continuous-time controller parallel configuration.

The system expression is now expanded to accommodate non-identical modules, where the individual filter component values are subtly different due to practical tolerances.

For a non-identical system L_1 is unique. The capacitor voltage functions in equation 6.3 become:

$$G_{V_c,V_{pwm,1}}(s) = \frac{LL_g}{s^2LL_1L_gCn + L_g(L + L_1(n-1)) + LL_1n} \tag{6.10}$$

$$G_{V_c,V_{pwm,j}}(s) = \frac{(n-1)L_1L_g}{s^2LL_1L_gCn + L_g(L + L_1(n-1)) + LL_1n} \tag{6.11}$$

with respective capacitor currents:

$$G_{I_c,V_{pwm,1}}(s) = sCG_{V_c,V_{pwm,1}}(s) \tag{6.12}$$

$$G_{I_c,V_{pwm,j}}(s) = sCG_{V_c,V_{pwm,j}}(s) \tag{6.13}$$

Discretising the capacitor and current functions produces:

$$G_{V_c,V_{pwm,1}}(z) = \mathcal{Z}_{ZOH}(G_{V_c,V_{pwm,1}}(s)) \tag{6.14}$$

$$G_{V_c,V_{pwm,j}}(z) = \mathcal{Z}_{ZOH}(G_{V_c,V_{pwm,j}}(s)) \tag{6.15}$$

$$G_{I_c,V_{pwm,1}}(z) = \mathcal{Z}_{ZOH}(G_{I_c,V_{pwm,1}}(s)) \tag{6.16}$$

$$G_{I_c,V_{pwm,j}}(z) = \mathcal{Z}_{ZOH}(G_{I_c,V_{pwm,j}}(s)) \tag{6.17}$$

Closing the loop, the non-identical module expressions are:

$$G_{V_c,V_{pwm}} = G_{V_c,V_{pwm,1}} + G_{V_c,V_{pwm,j}} \tag{6.18}$$

$$G_{I_c,V_{pwm}} = G_{I_c,V_{pwm,1}} + G_{I_c,V_{pwm,j}} \tag{6.19}$$

$$\frac{V_{pwm,1}}{V_{c,ref}} = \frac{C_{Ff}}{1 - C_{Fb,V_c}G_{V_c,V_{pwm}} + C_{Fb,I_c}G_{I_c,V_{pwm}}} \tag{6.20}$$

$$\frac{V_{c,1}}{V_{c,ref}} = \frac{V_{pwm,1}}{V_{c,ref}}G_{V_c,V_{pwm}} \tag{6.21}$$

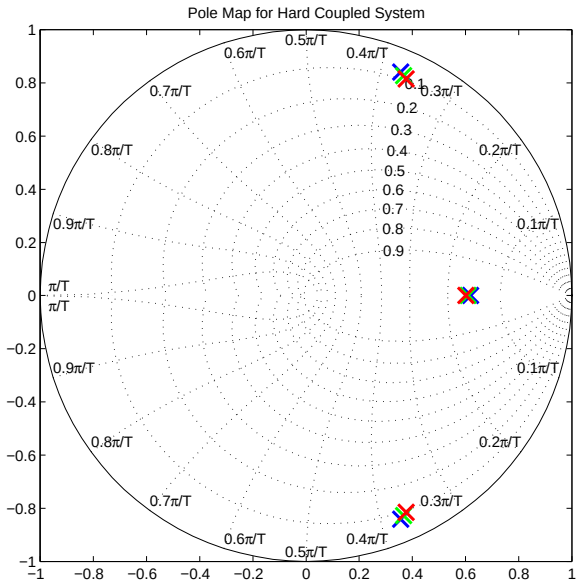


Figure 6.6: Pole map of hard-coupled system demonstrating component sensitivities by varying module one inductor. $T_s = \frac{2\pi}{160}$pu, $L = 4\%$, $C = 10\%$, $L_g = 5\%$, $L_1 = L \pm 10\%$, $\omega_i = 11$pu, $\omega_v = \frac{3}{4}\omega_i = 8.25$, three module system.

The poles of the non-identical system are defined by the denominator of equation 6.20. From equations 6.10 and 6.11 the filter equations are still only second order like the single module system (equation 3.17).

Figure 6.6 illustrates the effect of component sensitivities in a three module system by varying L_1. Increasing the number of modules reduces the effect of component variations. Hard-coupled configurations do not pose any additional stability implications compared with an individual module. In fact, more modules helps to average out component sensitivities.

6.2.2 Soft-coupled parallel configuration

The soft-coupled configuration assumes a non-zero coupling impedance $L_c \neq 0$ in Figure 6.3. With the addition of L_c equations 6.7 and 6.8 are no longer valid, and the individual module capacitor voltages and currents must be resolved. Figure 6.7 shows the closed-loop configuration for a three module soft-coupled parallel configuration where each module is identical. Note that Figure 6.7 does not show the blocks for the respective capacitor current feedbacks.

The module capacitor voltages are derived in a similar manner to the hard-coupled configuration,

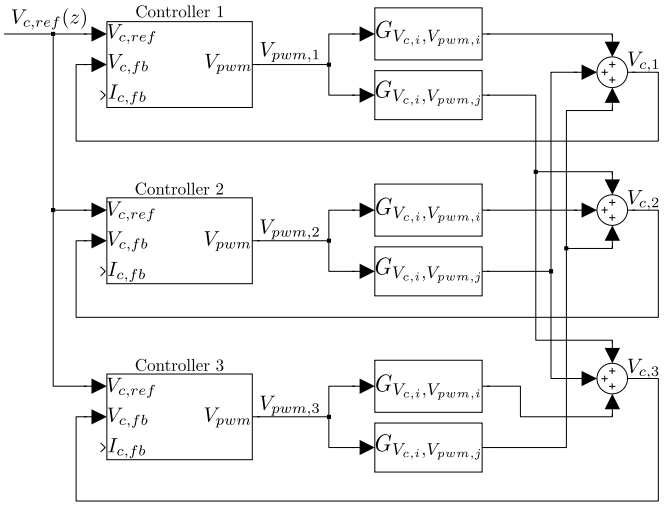


Figure 6.7: Soft-coupled parallel system with three modules. Note that the functions for the capacitor currents are not shown but are of the same form as the capacitor voltage functions.

except that there is no longer one common capacitor voltage, and, as a result, each controller no longer produces the same PWM reference $V_{pwm,i}$. For a configuration where each filter is identical, the continuous-time transfer function for the module capacitor voltage as a function of its own PWM voltage $G_{V_{c,i}V_{pwm,i}}(s)$ is:

$$G_{V_{c,i}V_{pwm,i}}(s) = \frac{V_{c,i}(s)}{V_{pwm,i}(s)} = \frac{s^2 nL_c LC(L_c + L_g) + nL_c(L + L_c + L_g) + LL_g}{n(s^2 LCL_c + L + L_c)(s^2 LC(L_c + L_g) + L + Lc + L_g)} \tag{6.22}$$

and the module capacitor voltage as a function of *every other* PWM voltage $G_{V_{c,i}V_{pwm,j}}(s)$ is:

$$G_{V_{c,i}V_{pwm,j}}(s) = \frac{V_{c,i}(s)}{V_{pwm,j}(s)} = \frac{LL_g}{n(s^2 LCL_c + L + L_c)(s^2 LC(L_c + L_g) + L + Lc + L_g)} \tag{6.23}$$

Respective capacitor current expressions are obtained with equation 6.4.

Closing the loops in Figure 6.7 for an n-module parallel configuration produces the module one

capacitor voltage $V_{c,1}$ as a function of the reference voltage. Defining

$$H_1 = G_{V_{c,i}V_{pwm,i}}(z) \tag{6.24}$$

$$H_2 = G_{V_{c,i}V_{pwm,j}}(z) \tag{6.25}$$

$$H_{1I} = G_{I_{c,i}V_{pwm,i}}(z) \tag{6.26}$$

$$H_{2I} = G_{I_{c,i}V_{pwm,j}}(z) \tag{6.27}$$

The complete closed-loop transfer function for an individual module $V_{c,i}(z)$ as a function of $V_{c,ref}(z)$ is given as:

$$\frac{V_{c,i}(z)}{V_{c,ref}(z)} = \frac{-C_{Ff}(H_1+(n-1)H_2)(C_{Fb,V_c}(H_1-H_2)+C_{Fb,I_c}(H_{1I}-H_{2I})-1)}{(C_{Fb,V_c}(H_1-H_2)+C_{Fb,I_c}(H_{1I}-H_{2I})-1)(C_{Fb,V_c}(H_1-H_2)+C_{Fb,I_c}(H_{1I}-H_{2I})-1+n(C_{Fb,V_c}H_2+C_{Fb,I_c}H_{2I})} \tag{6.28}$$

The first observation to be made for a perfectly identical system is that further pole-zero cancellations can be made in equation 6.28. The two factors in the denominator that each contribute a pole-pair are:

$$Factor_1 = (C_{Fb,V_c}(H_1-H_2)+C_{Fb,I_c}(H_{1I}-H_{2I})-1) \tag{6.29}$$

$$Factor_2 = (C_{Fb,V_c}(H_1-H_2)+C_{Fb,I_c}(H_{1I}-H_{2I})-1+n(C_{Fb,V_c}H_2+C_{Fb,I_c}H_{2I}) \tag{6.30}$$

A further cancellation of the first factor produces:

$$\frac{V_{c,i}(z)}{V_{c,ref}(z)} = \frac{-C_{Ff}(H_1+(n-1)H_2)}{(C_{Fb,V_c}(H_1-H_2)+C_{Fb,I_c}(H_{1I}-H_{2I})-1+n(C_{Fb,V_c}H_2+C_{Fb,I_c}H_{2I})} \tag{6.31}$$

Worth noting is that for a perfectly identical *hard-coupled* system where the load $L_{g,load}$ is the sum of the coupling impedance and load of a soft-coupled system ($L_{g,hard} = L_{g,soft} + L_c$), the

response expressions are the same.

For the non-identical configuration, module one has a unique coupling impedance $L_{c,1}$. Unlike the identical module scenario, the expressions for each capacitor voltage (and respective capacitor current) shown in Figure 6.7 must be further expanded to take into account the effect of $L_{c,1}$. As only module one is unique, the capacitor voltage expressions are expanded to be with respect to that module's PWM voltage, module one's PWM voltage and then every other module's PWM voltage. The index notation given at the start of the chapter in Figure 6.1 is again used, but as module one is not identical to the remaining modules its specific index is used. Subscript j refers to the remaining $(n-2)$ modules and $i \neq 1$. The non-identical configuration capacitor voltage expressions are:

$$H_1 = G_{V_{c,1}V_{pwm,1}}(z) \tag{6.32}$$

$$H_2 = G_{V_{c,1}V_{pwm,j}}(z) \tag{6.33}$$

$$H_3 = G_{V_{c,i}V_{pwm,1}}(z) \tag{6.34}$$

$$H_4 = G_{V_{c,i}V_{pwm,i}}(z) \tag{6.35}$$

$$H_5 = G_{V_{c,i}V_{pwm,j}}(z) \tag{6.36}$$

The full equations for each of the capacitor output voltage transfer functions for equations 6.32 to 6.36 are given in Appendix H.

Figure 6.8 shows the poles of a non-identical configuration scenario. The coupling impedance and load impedance sum are the same as Figure 6.6. When the modules are not exactly identical $Factor_1$ (equation 6.29) of equation 6.28 no longer cancels, and in the present example manifests as the pole-zero pairs just outside of the unit circle. Not only do the pole-zero pairs not cancel, but the same gains used in a hard-coupled system have a higher stability margin than in a soft-coupled system. Figure 6.8 shows the additional pole-zero pairs are outside the unit circle

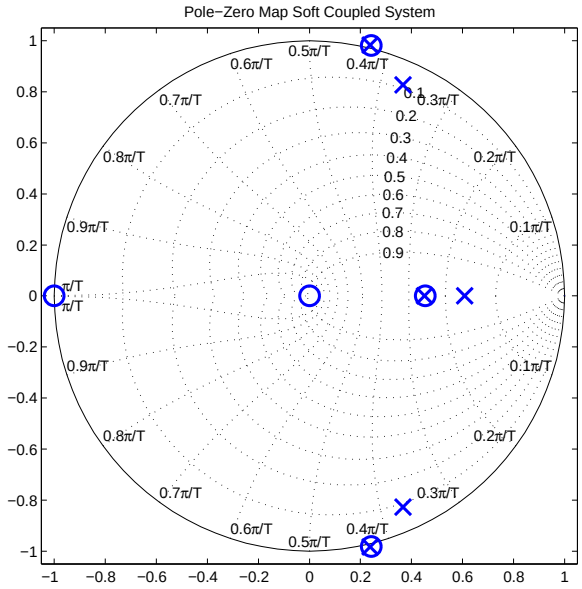


Figure 6.8: Pole-zero map of soft-coupled system varying module one coupling impedance $L_{c,1}$. $T_s = \frac{2\pi}{160}$, $L = 4\%$, $C = 10\%$, $L_c = 2\%$, $L_{c,1} = 0.95L_c$, $L_g = 3\%$, $\omega_i = 11$, $\omega_v = \frac{3}{4}\omega_i = 8.25$, three module system.

Table 6.1: Hard and soft-coupled parallel stability margin

Hard-coupled	Soft-coupled
$\omega_i = 14.6$pu, $\omega_v = 10.9$pu	$\omega_i = 10.6$pu, $\omega_v = 7.9$pu

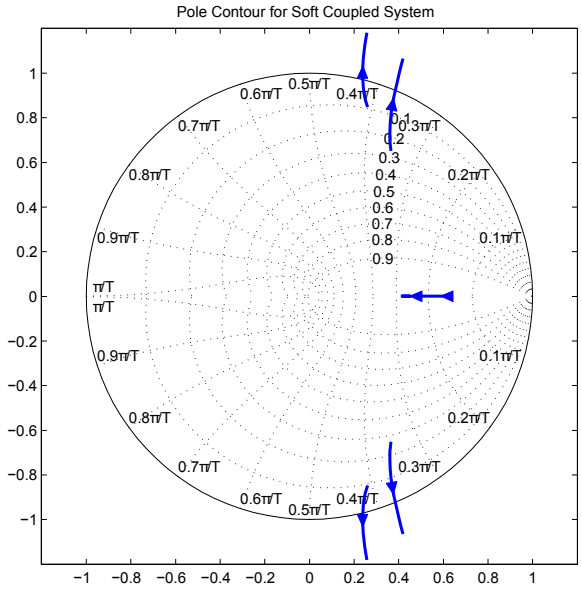


Figure 6.9: Pole contour of soft-coupled system with ω_i gain sweep from 5 to 20pu. $T_s = \frac{2\pi}{160}$, $L = 4\%$, $C = 10\%$, $L_c = 2\%$, $L_{c,1} = 0.95L_c$, $L_g = 3\%$, $\omega_v = \frac{3}{4}\omega_i$, three module system.

causing instability. For the parameters in Figure 6.8, the soft-coupled system is unstable with the same gains as the stable hard-coupled system example in Figure 6.6.

Figure 6.9 shows the pole contour of a non-identical parallel configuration with a load impedance. The same contours exist that are in the hard-coupled system example in Figure 6.5, but the additional complex pole-pair $Factor_1$ lowers the soft-coupled system's stability margin. Table 6.1 shows the stability margin gains for a hard-coupled system against a soft-coupled system. The hard-coupled system achieves a 37% greater maximum gain than the soft-coupled system.

The soft-coupled instability, by definition, requires a minimum of two parallel modules. The greatest change in gain margin is between a system with two modules and three modules. Displaying the effect of varying the number of modules is difficult as the stability margin only varies by approximately 3% (between two and an infinite number of modules and with module parameters specified in Figure 6.9).

The unstable poles in Figure 6.8 correspond to $Factor_1$ that numerically cancel when all of the modules are perfectly identical. Algebraic simplification of $Factor_1$, and with the continuous-time components for analysis clarity produces the following expression:

$$Factor_1 = \frac{(C_{Fb,V_c} + C_{Fb,I_c} sC)L_c - (s^2 LCL_c + L + L_c)}{s^2 LCL_c + L + L_c} \tag{6.37}$$

Upon inspection of $Factor_1$ above it is evident that the unstable poles are only dependent on the LCL filter values and the controller, not the load. This key finding suggests that the stability of soft-coupled parallel configurations is entirely specified by the inverter components and is, thankfully, immune to customer loads, as this means that it can be prevented at implementation.

The stability findings have so far shown that as the coupling impedance L_c decreases, so too does the system damping ratio, lowering the stability margin to the point where it becomes unstable. Furthermore, as the coupling impedance decreases the natural frequency of the poles increases, tending to infinity.

To determine the effect of filter component damping it is introduced into the capacitor voltage and current expressions in equations 6.22 and 6.23. Figure 6.10 shows the effect on the unstable

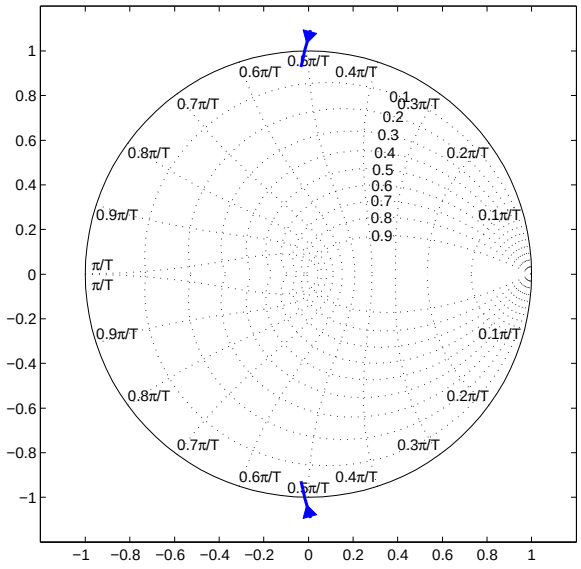


Figure 6.10: Pole contour of soft-coupled system varying coupling impedance L_c Q-factor from infinite down to 1. $T_s = \frac{2\pi}{160}$, $L = 4\%$, $C = 10\%$, $L_c = 1\%$, $\omega_i = 11$, $\omega_v = \frac{3}{4}\omega_i = 8.25$, three module system.

pole-pair of a low coupling impedance with a decreasing Q-factor. This confirms the practical findings that parallel configurations with negligible coupling impedances (well below 1%) are unlikely to become unstable.

To prevent instability in parallel configurations there is a minimum or maximum coupling impedance between parallel modules that prevents instability for a given controller. This imposes the following limitations:

- Firstly stability is dependent on the controller and its associated response. For a given system defining the coupling impedance to be a particular value requires that the controller response does not vary over the lifetime of that hardware. This may limit responses required for certain load types, limiting against theoretical use of the system with certain loads.

- Secondly, the impedance value that ensures stability for the parallel configuration may be unsuitable as a coupling impedance with certain loads. For example, an application may require a certain coupling impedance between the load and the inverter, but the impedance value required may conflict with the stability requirements. The previous unstable pole-

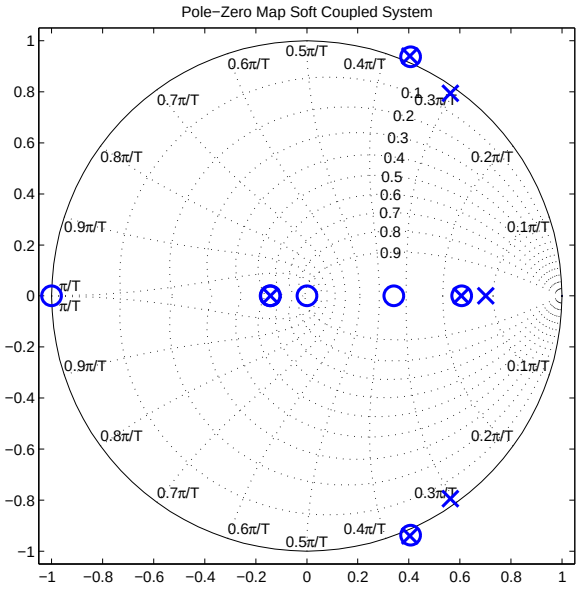


Figure 6.11: Pole-zero map of soft-coupled system varying module one coupling impedance $L_{c,1}$. $T_s = \frac{2\pi}{160}$, $L = 4\%$, $C = 10\%$, $L_c = 2\%$, $L_{c,1} = 0.95L_c$, $L_g = 3\%$, $\omega_i = 11$, $\omega_v = \frac{3}{4}\omega_i = 8.25$, three module system.

contour figures in this section are examples of this. The 2% coupling impedance is required to prevent resonance with grid capacitors (such as power factor correction) but in the scenario presented the system is unstable.

In applications where the load requires a minimum coupling impedance it may be logistically impractical to use a large bulk coupling impedance instead of a distributed, modular coupling impedance.

6.2.3 Experimental results

In addition to instabilities experienced on hard-coupled parallel configurations with two to 16 module configurations, the stability implications of soft-coupled parallel configurations were confirmed against the theoretical predictions on the three module 100kVA test system (Appendix G). Due to hardware constraints, the capacitor current state feedback is approximated using an observer (discrete-time lead filter) on the capacitor voltage, rather than sensing the actual current. An additional real pole is created, but stability effects are similar to actual current sensing. Figure 6.11 shows the poles and zeros of the system in Figure 6.8 but with a

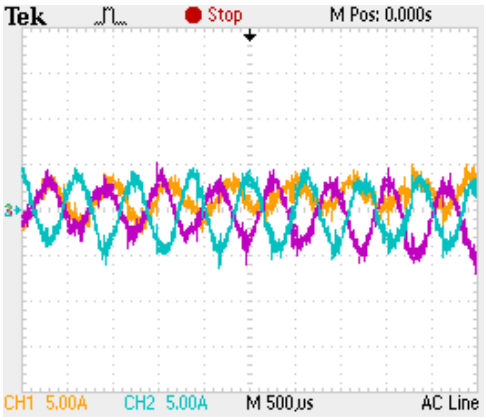


Figure 6.12: Marginally unstable soft-coupled output current. $\omega_i = 10.5$, $\omega_v = 7.9$.

Table 6.2: Soft-coupled stability margin

	ω_i (pu)	ω_v (pu)	Oscillation frequency (pu)
Theoretical	10.6	7.9	29.6
Simulation	10.4	7.8	29
Practical	10.5	7.9	28

capacitor current observer. In all scenarios, a lead filter cutoff frequency of 25pu is used as it provides a similar stability margin as the actual capacitor current feedback method, with the additional poles and zeros created shown in Figure 6.11.

To provide current balancing in both simulation and hardware tests a resistive droop of 1% is used. Simulations demonstrated that the droop has almost no effect on the parallel module stability margin. Both the simulation and hardware have internal current limits of ±2pu, implemented in the controller inductor current loop.

The grid impedance was measured to be approximately 4% relative to a single module current rating. The inverter nominal passive component values are within tolerance of measurement error of the values used in simulation: $T_s = \frac{2\pi}{160}$, $L = 4\%$, $C = 10\%$, and $L_c = 2.3\%$. Component tolerance variations of up to 10% provided adequate variation between module inductances to induce soft-coupled instability.

Figure 6.12 shows the soft-coupled output current for marginally unstable gains and that the instability point matches the expected gains as derived in Section 6.2.2. Table 6.2 illustrates the

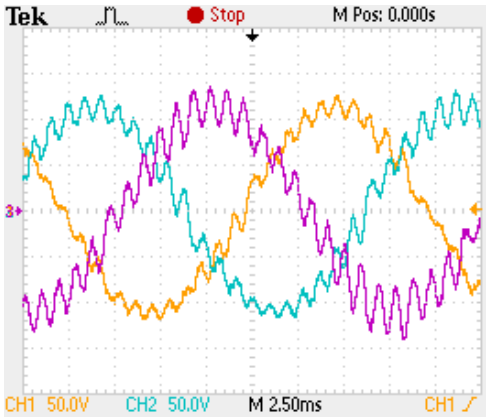


Figure 6.13: Marginally unstable hard-coupled configuration output voltage. $\omega_i = 14.4$, $\omega_v = 10.8$.

predicted and measured gains at the point of instability. The measured results demonstrate a close correlation to within 2% of the predicted unstable gains.

Figure 6.13 shows the hard-coupled output voltage for marginally unstable gains. Similar to the soft-coupled configuration, the hard-coupled stability margin gains match the theoretical and simulation results to within 2%.

Although systems with no coupling impedance do not suffer from the parallel connection stability issue at all, any modular system with separate capacitors (rather than one n-times bulk capacitor) will have *some* coupling impedance. Of the hard-coupled systems tested, none exhibited any stability margin limitations as suggested by the findings. The likely reason being that low-valued impedances such as cabling and bus-bars typically have a decreasing Q-factor (quality factor) for increasing frequency. Typically for inductors with iron laminations the Q-factor would be expected to decrease significantly with frequencies in the kilohertz range.

6.3 DIRECT DESIGN CONTROLLER

The initial motivation to investigate the stability implications of parallel connected inverters was from instabilities experienced on the parallel experimental configuration in Appendix G with the discretised continuous-time controller in Section 4.2.1. In the previous section the cause of soft-

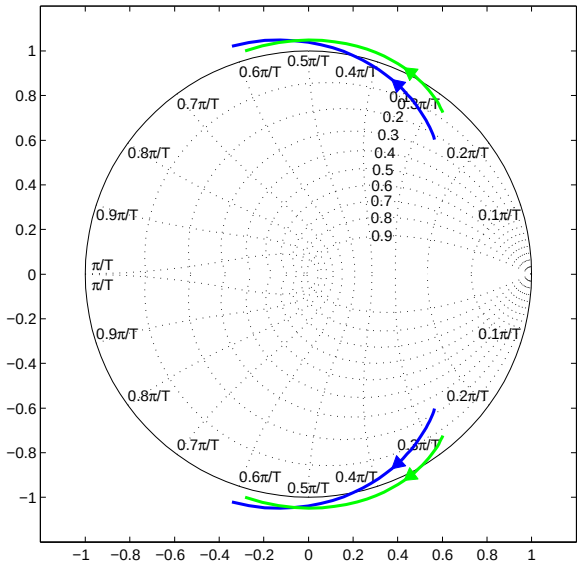


Figure 6.14: Soft-coupled pole-contour of stability-governing poles, for a coupling impedance L_c sweep from 10% down to 0.5%. Green contours are for the discretised continuous-time controller, and blue contours are for the discrete direct design controller. $T_s = \frac{2\pi}{160}$, $L = 4\%$, $C = 10\%$, discretised controller parameters: $\omega_i = 11$pu, $\omega_v = \omega_i \frac{3}{4}$pu. Direct discrete controller parameters: $k_3 = 0.65$, 0.4 damping ratio design parameter.

coupled parallel module instability was determined to be governed purely by the LCL filter and the controller. The response of a given controller directly relates to the maximum and minimum coupling impedance that will cause instability in soft-coupled parallel systems. This section details the use of the discrete direct design controller detailed in Chapter 5, and how its response affects the stability of soft-coupled systems.

The discrete direct design controller in the previous chapter demonstrated improved performance as a stand-alone monolithic controller, so a key consideration is the impact the controller has on the soft-coupled instabilities. Figure 6.14 shows a theoretical pole-contour of only the poles that govern the soft-coupled stability (equation 6.29), for both controllers with a coupling impedance sweep. From the figure, the direct design controller demonstrates a greater stability margin for a given coupling impedance. This finding is consistent with the experimental results.

6.4 SUMMARY AND DISCUSSIONS

Parallel and series inverter configurations allow high power and performance inverter configurations that exceed the individual device constraints presented in Chapter 2. Actively paralleled VSI configurations individually control each inverter to ensure that it current-shares appropriately, avoiding the need for derating. Due to the actively paralleled nature, each module looks like an independent low impedance load to the other modules. In applications where a discrete-time controller is used, the low impedance interconnections can be a source of instability.

This chapter described the potential instabilities observed in soft-coupled parallel VSIs. The instability is shown to be independent of the external load connected, and by choosing appropriate filter values and controller types the instability can be adequately prevented. In scenarios where the filter component values are fixed, only the controller can prevent instability. However, the primary reason for using parallel configurations is so that high bandwidth controllers and devices can be used, therefore sacrificing any performance in the controller to ensure stability is undesirable.

As the soft-coupled instability is directly related to the filter components and the controller, several implementation recommendations can be made. Soft-coupled systems that have either close to zero coupling impedance or a relatively high coupling impedance (typically greater than 10%) have been demonstrated to be stable with sub-optimal controllers. Given that in most applications where LCL filters are used the secondary L coupling impedance is typically to prevent potential high frequency resonance between the load (often a grid) and the filter capacitor C, and for this reason the inductance can be quite low (a few percent). To prevent possible soft-coupled instability it is recommended to use a bulk monolithic coupling impedance rather than modular ones. Despite violating the redundancy aspect of individual coupling impedances, inductors (like transformers) seldom fail. In applications where the parallel system is connected to the load via a transformer, the transformer may be able to provide sufficient impedance, such

that a separate coupling impedance is not necessary.

The discrete direct design controller developed in Chapter 5 has been tested against the benchmark discretised continuous-time controller and has demonstrated an improved stability margin. The direct design controller has been shown to ensure stability over a wider range of coupling impedance values than that achievable with the benchmark controller. Future research into designing a controller that specifically targets the cause of the instabilities shown in this chapter has the potential to offer a greater level of stability than just standard VSI designs.

By following the recommended implementation recommendations concluded in this chapter, a scalable grid-connectible inverter system can be constructed that offers the high bandwidth response of a single lower-power inverter, but at higher power levels. The next chapter follows on from this one by looking at how high power inverter configurations interact with other sources and loads on grids.

Chapter 7

GRID CONNECTION

7.1 INTRODUCTION

The flexibility and availability of inverters has resulted in a rapidly increasing number of grid-connected applications. Half a century ago thyristor inverters began being used in grid-connected applications for DC power transmission. Since then inverters are now used in grid-connected applications as loads and sources ranging from watts to gigawatts. Not surprisingly, as the number of grid-connected applications and systems grows, so too does the complexity of analysing interconnected systems. With the number of publications regarding grid stability risks due to an increasing penetration becoming commonplace [47, 48], there is a strong desire to find methods for analysing complex systems. This chapter investigates methods of controlling and analysing sources and loads in grid-connected applications.

Herein a 'grid-connected' inverter is defined as any inverter that forms part of a network of sources and loads. Any source or load output impedance is a linearisation of how it interacts with the grid. A grid's apparent size, regarding the number of connected sources and loads and their power, is arbitrary. Stiff grids represent a low impedance to source or load, whereas weak grids may have a relatively large impedance.

The grid impedance determines how a connected load or source is able to influence the voltage at the common point of coupling. Depending on the application, from a source or load point-of-view a grid may have little or no back EMF, in which case the device connected is likely to

be the source responsible for the frequency and voltage of the grid. A grid impedance also has no bounds on its complexity, herein referred to as its system order (the number of poles for a linear system). A 'simple' grid may be a nominal resistive load, whereas a complex grid may be a high-order combination of linear and non-linear impedances.

This chapter first examines the control methods commonly used with grid-connected devices and how they apply to grid-connected inverter systems. Having introduced how inverters can connect to grids and how power is transferred to or from a grid, the common historical analytical techniques used to gauge grid stability and robustness are reviewed and applied to grid-connected inverter applications. Due to the limitations found with existing traditional analytical techniques when applied to grid-connected inverters, a graphically-assisted application of the Nyquist stability criterion is introduced that indicates how individual loads and sources contribute to closed-loop system poles, and therefore stability and robustness. The graphical analysis technique is not limited to loads and sources of a particular order, and can also be used with systems that have delays.

Two examples of the graphical technique for determining the stability of complex source and load types are provided. The first example identifies the cause of instability for a cascaded VSI and CSI micro-grid system. The analysis technique is further expanded to multiple-input multiple-output (MIMO) systems and identifies potential instability for a VSI running an induction machine. Both examples are confirmed on the parallel module test system described in Appendix G.

7.2 COMMON METHODS

Grid-connected systems, including inverters, can operate in either voltage sourcing or current sourcing modes. System designers can choose either voltage sourcing systems to provide a low impedance to setup a nominal grid voltage and frequency, or current sourcing systems where a

stiff grid already exists. In addition to sourcing either a fixed voltage or current, either scheme may receive a reference from a real or reactive power controller.

To analyse grid-connected systems the common methods of power sharing between sources are briefly reviewed. Voltage sourcing systems typically use the voltage and frequency droop method to control their power flow. A brief review of the commonly used voltage and frequency droop method is given in [49] and Appendix I. For a predominantly reactive grid impedance the voltage sourcing device frequency and voltage are defined as:

$$\omega = \omega_{rated} - m_{\omega}(P_{rated} - P) \tag{7.1}$$

$$V_{out} = V_{out,rated} - m_V(Q_{rated} - Q) \tag{7.2}$$

where the m coefficients represent the droop factors, and each device is defined as having similar ω and V ratings.

The voltage and frequency droop methods are used by all synchronous generators to provide real and reactive power sharing. Grid-connected inverter systems often use the same principles to provide PQ control and comply with other voltage sources on a grid. Most rotating machine loads and sources appear as voltage sources behind a transient impedance.

Unlike voltage-sourcing systems, current-sourcing inverters can only change the voltage or frequency by sourcing or sinking current against an impedance or inertia, respectively. In applications where the size of the inverter is no longer tiny in comparison to the voltage sourcing devices, current sourcing systems can have adverse effects on grid sources. On grids where the voltage and frequency are predominantly controlled by synchronous machines, it is imaginable that exceptionally large current sourcing loads or sources could destabilise the generators, resulting in grid instability or collapse. This is one of the areas of analysis that is useful. Current controllers require additional control loops to offer voltage and frequency support. On the contrary, if the voltage collapses a constant power CSI will draw more current, further collapsing

the voltage. This is further explored in the following section regarding grid synchronisation.

7.2.1 Inverter Impedance

As detailed in Chapter 2, a perfect VSI would have zero output impedance. In micro-grid applications where frequency and voltage droop are not used, 'ideal' inverter impedances are typically preferred. These are usually applications with single sources or where other sharing mechanisms are employed, however, if frequency and voltage droop is used for load sharing on a grid not only must the inverter be compliant in order to share, the droop mechanisms also require a particular grid impedance and inertia to work with (refer Appendix I). In Chapter 5 the high performance direct design controller achieved an output impedance as low as 6% at the fundamental, whereas a typical generator impedance ranges between 20 to 150%. In order to achieve the same characteristics as generators on a common grid, an additional grid-coupling impedance may need to be added to the inverter.

In grid-connected inverter applications a fixed coupling impedance is typically used to reduce ripple and to prevent high frequency currents being sourced by the inverter's filter capacitors (LCL filters) in the presence of grid voltage distortion. The coupling impedance is typically in the range of a few percent, commonly implemented as either a small inductor or as part of the connection transformer.

When additional impedance is required a 'synthetic' impedance can be emulated in the inverter controller that is effective up to its cutoff frequency (bandwidth). This can be implemented in a similar manner to the resistive droop method shown in Figure 6.2 in Chapter 6. In the case of a VSI, an inductive impedance sL is implemented as a lead term since a pure derivative is impractical. An inverter can therefore effectively create a synthetic impedance if its bandwidth is sufficiently greater than the fundamental.

Figure 7.1 shows the effect on the output impedance of the direct design controller in Chap-

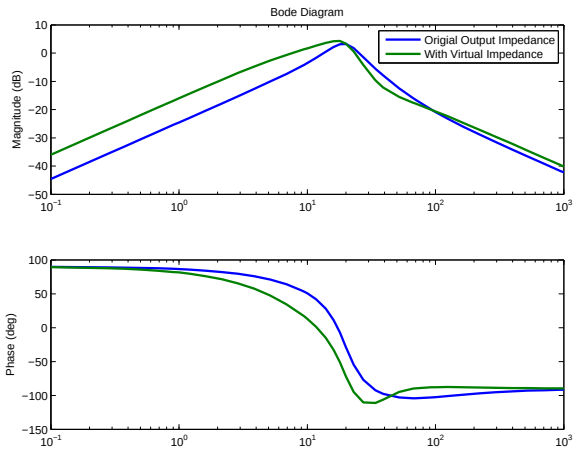


Figure 7.1: Bode plot of Direct Design controller in Chapter 5 with and without virtual 10% inductive impedance. $T_s = \frac{2\pi}{160}$pu, $L = 4\%$pu, $C = 10\%$pu, controller designed with damping ratio of 0.4, bilinear lead filter cutoff frequency of 10pu.

ter 5 with a virtual 10% inductive impedance. A bilinear-lead filter is used to approximate the inductive response based on the inverter output current. From the figure there is an evident impedance increase for frequencies below the 20pu cutoff frequency. At the fundamental the output impedance magnitude is exactly 10% greater with only a 5 degree phase shift.

7.3 GRID SYNCHRONISATION

In grid-connected applications control of individual d and q components are required as they directly correspond to real and reactive power. The rotating reference frame transformations (detailed in Section 3.3.4) require a Phase Locked Loop (PLL) synchronised to the grid voltage in order to align to the real and imaginary components. In a grid-connected system where frequency droop is used as a sharing mechanism, the response of the PLL to frequency changes will affect how the inverter performs dynamically. If the PLL phase leads or lags the actual grid voltage phase then the controller's observed real and imaginary components will be incorrect.

The PLL model is detailed in Section 3.3.4 and shown in Figure 3.4. In an inverter application the PLL is typically synchronised to the voltage at the inverter terminals. To determine the effect of the PLL on an inverter its response must be derived. In Figure 3.4 the input reference is a signal in the $\alpha\beta$ frame, however, it is desirable to model everything in either the $\alpha\beta$ frame

or the *dq* frame. To analyse the dynamic effect of the PLL on an inverter, an expression of the inverter's observed voltage as a function of the sensed voltage is derived.

An expression for the PLL is achieved by linearising its feedback loop. The PI controller and frequency integrator are simple linear blocks, but the $e^{-j\theta}$ coordinate transform is non-linear and is linearised around the nominal operating frequency. To linearise the $e^{-j\theta}$ transform the sin and cos components are eliminated by assuming that for small $\Delta\theta$ that $\sin(\Delta\theta) = \theta$ and $\cos(\Delta\theta) = 1$. In the $\alpha\beta$ frame the voltage vector angle θ will be revolving at a rate of the fundamental frequency (during steady state) and will thus violate the requirement that $\Delta\theta$ is close to zero. Modelling the PLL in *dq* frame results in a $\Delta\theta$ that only varies with transients, satisfying the linearisation requirements.

The PLL voltage expression is defined as a multiple-input multiple-output (MIMO) transfer function matrix that results in the inverter voltage $\underline{E}_c$ as a function of the actual line voltage $\underline{E}$, both in the *dq* frame. To achieve this, an expression for $\Delta\theta$ as a function of $\underline{E}$ is first derived. The relationship between the actual line voltage and the PLL inverter reference voltage is:

$$\underline{E}_c = e^{-j\Delta\theta}\underline{E} = (\cos(\Delta\theta) - j\sin(\Delta\theta))\underline{E} \tag{7.3}$$

$$\cong (1 - j\Delta\theta)(E_0 + \Delta\underline{E}) \tag{7.4}$$

$$\cong E_0 - j\Delta\theta E_0 + \Delta\underline{E} \tag{7.5}$$

The nominal grid voltage by definition has no imaginary part, so E_0 is a real scalar.

The PLL aligns to the real component of the voltage by zeroing the imaginary part. Therefore the PLL PI controller output is:

$$\Delta\omega = (0 - \Im\{\Delta\underline{E}_c\})F_{PLL}(s) \tag{7.6}$$

where $F_{PLL}(s)$ is the PI controller transfer function and is typically $F_{PLL}(s) = k_{pp}\left(1 + \frac{k_{pi}}{s}\right)$.

The imaginary component of $\Delta\underline{E}_c$ is:

$$\Im\{\Delta\underline{E}_c\} = \Im\{\Delta\underline{E}\} - \Delta\theta E_0 \tag{7.7}$$

The angle $\Delta\theta$ is found by integrating $\Delta\omega$ in equation 7.6. Closing the loop and solving for $\Delta\theta$:

$$\Delta\theta = G_{PLL}(s)\Im\{\Delta\underline{E}\} \tag{7.8}$$

where $G_{PLL}(s)$ is:

$$G_{PLL}(s) = \frac{k_{pp}(s + k_{pi})}{s^2 + E_0 k_{pp} s + E_0 k_{pp} k_{pi}} \tag{7.9}$$

Substituting into the inverter voltage expression in equation 7.4 results in the inverter voltage as a function of the grid voltage, expressed as a matrix:

$$\Delta\underline{E}_c = \begin{bmatrix} 1 - E_0 G_{PLL}(s) & 0 \\ 0 & 1 \end{bmatrix} \Delta\underline{E} \tag{7.10}$$

The result above indicates that the PLL angle is only affected by changes in the out-of-phase (d axis) voltage component, as result of a dynamic voltage phase shift.

Measured currents are also affected by the PLL synchronisation to the grid voltage. However, the nominal current I_0 is not strictly real. In matrix form, a measured current $\Delta\underline{I}_c$ as a function of the actual current $\Delta\underline{I}$ is:

$$\Delta I_c = \Delta I - \begin{bmatrix} -I_{0,q} G_{PLL}(s) & 0 \\ I_{0,d} G_{PLL}(s) & 0 \end{bmatrix} \Delta E \tag{7.11}$$

where I_0 is the nominal dq current.

Inspection of $G_{PLL}(s)$ in equation 7.9 indicates that the PLL has a simple second order low-pass

response. If the linearisation assumptions are not met ($\Delta\theta$ close to zero) then the response may deviate from $G_{PLL}(s)$.

The PLL is an example of a unsymmetrical function in the dq axis that can affect a grid-connected inverter's response. It will act to increase the system order when included in the inverter response.

7.4 STABILITY ANALYSIS OF COMPLEX SYSTEMS

As the interconnection of different sources and loads on power grids increases, so too does the complexity of analysing the stability and the response of grids. The complexity of analysing a particular grid is increased by the type of source or load that is connected, and also by the location and associated connection impedance. When analysing an interconnected system the first and foremost concern is stability, which is governed by the poles of the system. When determining the stability and response of a system, a trade-off is made between the use of different analysis techniques against the level of detail in which the system is described.

To analyse the stability and response of a system, simulation with a given set of parameters is often the most popular approach. Simulations can often accommodate the greatest complexity of any analytical technique, but in addition to the large computational effort required, each simulation iteration results only in the response of the system with a fixed set of parameters. For this reason simulation is often used prior to the final implementation. With systems that can be appropriately linearised, eigenvalue analysis for a set of system parameters is also applicable. Although simulation and more detailed approaches [50] can suitably determine the stability of a system, they only do so using the closed-loop expression. Closed-loop analysis can offer insight into how each closed-loop pole affects the system stability, but they do not provide information about the detail that each separate component of a system (sources and loads) contributes, and in what way it affects system stability and response.

Ideally when analysing interconnected systems, it is preferable to get a sense of which part of each source and load contributes to each eigenvalue. The complexity of the system is defined as the order of the closed-loop system (the sum of the orders of the sources and loads). In earlier chapters low order systems (typically less than three) have been analysed using traditional pole-zero analysis. Typically most interconnected systems, such as grids, include sources and loads that are quite complex, resulting in a closed-loop system that is too complex (typically fourth order or greater) to be comprehensible. Discrete-time systems further reduce the ability to intuitively analyse systems.

To analyse systems with a high complexity there are several traditional methods that can be used for certain scenarios. To date, the complex torque coefficients and passivity theory methods attempt to provide a means of evaluating high-complexity systems by deriving expressions for the system damping over a given frequency range. These methods have been used for decades to analyse subsynchronous torsional oscillations of machines [51] and HVDC systems [52]. Recent publications [53, 54] that have looked at issues of grid-connected inverter systems have looked at an inverter's impedance effective damping to predict potential instability. Although these approaches present methods for determining undamped or lightly damped regions, not only do they not work for some common systems (as documented in [54]), they are still unable to separately show how each source and load in a system contributes to the closed-loop response.

This section first demonstrates and collates existing work regarding the short-comings of the complex torque coefficients and passivity methods for both analysing the closed-loop response and how individual components contribute to the overall response of power electronic systems (originally detailed in [55]). Having established limitations of existing techniques, an intuitive Nyquist Stability Criterion application is presented that, using only the individual frequency response plots of the two components (sources and/or loads) to be interconnected, shows how each component contributes to the final closed-loop system poles. By using the frequency response

(common Bode responses), the graphical application is capable of handling some nonlinear elements, such as delays, that affect the phase. The technique is used to demonstrate stability implications with a VSI acting as a local grid with a CSI load. The technique is then expanded to multiple-input multiple-output (MIMO) systems, such as asymmetric three-phase systems. An example with a VSI acting as a local grid which includes an induction machine as a load is then given.

7.4.1 Complex loads and sources

For the inverters analysed in Chapters 4 and 5, the highest order system was a third-order discrete VSI. The continuous-time expressions for the closed-loop inverters are one order lower due to the lack of delays. This was also without the effect of integrators (or resonators), a virtual output impedance (Section 7.2.1), or any other practical implications such as anti-aliasing filters. In Chapter 6 soft-coupled parallel inverters were analysed which were fourth-order, and adding a resonator would further increase the system complexity to sixth-order.

A further assumption was made that both axes in three-phase systems (dq or $\alpha\beta$) were symmetric, and therefore invertible. In real/reactive power controllers the individual dq axes can be controlled separately, requiring that the MIMO system be analysed using transfer function matrices, further increasing the complexity. The PLL in Section 7.3 is an asymmetric MIMO system. When analysing grid-connected sources and loads, their impedance may be modelled in either continuous or discrete-time.

7.4.2 Traditional analysis techniques

Since 1982 the complex torque coefficients method [56, 57] has been employed to find potential oscillation frequencies in power grids, and previous to 1982 similar concepts defining damping torque had been in use [52]. The method has been attractive for both its simplicity in application

and its extension from the original application with rotating machines to HVDC systems and others [52, 58].

Application of the complex torque coefficients method to generalised systems expressed in terms of transfer functions is relatively straight forward. In an example multi-mass shaft scenario (as detailed in [54], Section II) for a closed-loop system, where $k_m(s)$ and $k_e(s)$ are mechanical and electrical transfer functions respectively, defined as:

$$\Delta T_e = -k_m(s)\Delta\delta \tag{7.12}$$

$$\Delta T_e = k_e(s)\Delta\delta \tag{7.13}$$

and where $\Delta\delta$ and ΔT_e are the perturbations in the generator rotor angle and electrical torque respectively.

The closed-loop system becomes

$$(k_m(s) + k_e(s))\Delta\delta = 0 \tag{7.14}$$

and the system is therefore stable if all the roots of $k_m(s) + k_e(s) = 0$ are on the left hand side of the complex plane. The complex torque coefficients method then defines stability based on the frequency response of $k_m(s)$ and $k_e(s)$ by substituting $s = j\omega$ and separating the real and imaginary parts, as shown in [54], such that

$$k_m(j\omega) = K_m(\omega) + j\omega D_m(\omega) \tag{7.15}$$

$$k_e(j\omega) = K_e(\omega) + j\omega D_e(\omega) \tag{7.16}$$

$K_m(K_e)$ and $D_m(D_e)$ are called the mechanical (electrical) spring and damping constants respectively. The complex torque coefficients method defines the frequencies of the oscillatory

modes as the roots of $K(\omega) = K_m(\omega) + K_e(\omega) = 0$, and an oscillatory mode of frequency ω is stable if $D(\omega) = D_m(\omega) + D_e(\omega)$ is positive [54].

In [59] a technical proof for the complex torque coefficients method was presented. The technical proof provides a important insight into the stability conditions that the complex torque coefficients method provides, in that the theorem does not account for instances where the Nyquist curve crosses the negative real axis to the left of -1 but yet not encircle -1, and that the method will not *perfectly* identify torsional resonant frequencies. The issues with the complex torque coefficients method were initially demonstrated in [54] which show that the method only deals with roots that appear in complex conjugate form (not real ones), and [58] shows that the method is not valid for a multi-machine power system (rather than a single machine on an infinite bus). Although [59] justifiably states that the issues presented are unusual scenarios, in applications with electronic inverters these scenarios may well be encountered.

In the previous chapters, discretising and/or adding a coupling impedance will introduce real roots, preventing effective use of the complex torque coefficients method. Regardless of this, the investigation of inverters on an infinite bus is trivial. Practical scenarios are concerned with the stability of these systems with grid-type loads, such as rotating machines. Examples of the shortcomings are given in [54], where the method fails when applied to the standard IEEE Benchmark System [60].

A similar approach to the complex torque coefficients method is the use of passivity and dissipative systems analysis as applied to continuous-time systems (sources and loads) [61,62]. Passivity defines a conservative requirement for the stability of a system [63]. The conditions for a system to be passive is that the system must have no unstable poles (positive real in continuous-time). Marginally stable systems with all poles on the imaginary axis are acceptable. Passivity determines an effective electrical damping frequency response for any system, including power electronic systems [53]. Unfortunately the damping frequency response is not able to predict

the poles of a closed-loop system, rendering it suitable only as a guide when determining how a source or load will behave when it is incorporated into a larger system (effectively closing the impedance/admittance loop).

Despite their advantages in certain applications, the complex torque coefficients method and passivity are unable to be used to predict how two systems will interact and how each one will contribute to the closed-loop stability for more general scenarios.

7.4.3 Graphical analysis technique

Given the limitations of existing analytical techniques to examine how two systems will interact and whether the closed-loop system is stable, a Nyquist application technique which is derived from fundamental principles, is proposed that overcomes these shortcomings. The technique is a variation on the Middlebrook criterion [64] as it separately examines the respective impedances.

The graphical technique is based on the Bode/Nyquist stability criteria for determining closed-loop stability from an open-loop system. To review; for an open-loop stable scenario a system ($G(s)$) will be stable in closed-loop negative feedback ($H(s)$) if the open-loop gain is less than one (0dB) for any frequency where the phase is -180 degrees. For more complex systems the system is only unstable if the Nyquist curve *encircles* the -1 point (0dB, -180 degrees).

In the following analysis it is assumed that the two systems being analysed are open-loop stable. In grid applications this is typically an acceptable assumption to make, however the Nyquist stability criterion used herein works with open-loop unstable systems.

The closed-loop response of two cascaded systems, such as an impedance followed by an admittance, is:

$$G(s) = Y_{load}(s)Z_{source}(s) \tag{7.17}$$

The Bode magnitude and phase responses are found by evaluating the open-loop system at

$s = j\omega$, such that:

$$|G(j\omega)| = \sqrt{\Re\{G(j\omega)\}^2 + \Im\{G(j\omega)\}^2} \tag{7.18}$$

$$\angle G(j\omega) = \tan^{-1}\left(\frac{\Im\{G(j\omega)\}}{\Re\{G(j\omega)\}}\right) \tag{7.19}$$

The magnitude and phase responses for the complete open-loop system $G(s)$ can be rewritten as functions of the individual responses of $Y_{load}(s)$ and $Z_{source}(s)$:

$$|G(j\omega)| = |Y_{load}(j\omega)||Z_{source}(j\omega)| \tag{7.20}$$

$$\angle G(j\omega) = \angle Z_{load}(j\omega) + \angle Y_{source}(j\omega) \tag{7.21}$$

The stability of two cascaded systems in closed-loop negative feedback can be determined by superimposing the two individual magnitude and phase responses, search for critical frequencies where the phase responses sum to -180 degrees, and finally check if any of the magnitudes at the critical frequencies sum (in dB) to be greater than 0dB. In addition to absolute stability, gain and phase margins can be intuitively found. The process of finding frequencies with a phase shift of -180 degrees and then checking the gain at those frequencies may be automated using scripting languages such as MATLAB. Although the method is relatively simple, it clearly illustrates how two cascaded systems each contribute to the closed-loop stability. In the presented scenarios to follow it is worth noting that each of the open-loop systems are stable, which is typically a valid assumption for grid-connected systems.

By using traditional Bode frequency responses the technique is not strictly limited to simple linear continuous-time transfer functions. Responses may be a mix of continuous and discrete-time. Non-linear elements that can be characterised by magnitude and phase responses, such as delays in both continuous ($e^{-s\tau}$) and discrete (z^{-n}) time may also be used.

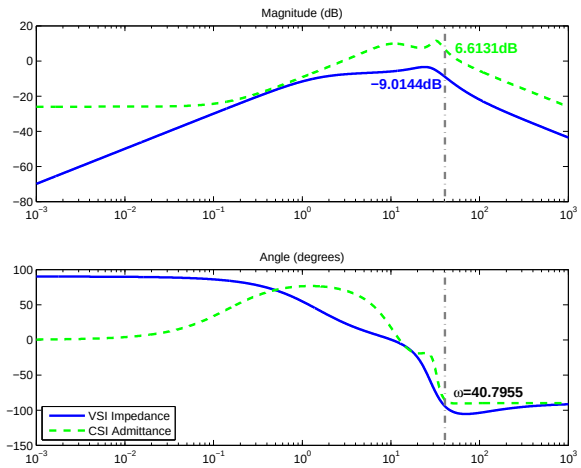


Figure 7.2: Discrete CSI admittance and VSI impedance responses. VSI: $T_s = \frac{2\pi}{160}$pu, $L = 4\%$pu, $C = 10\%$pu, $\omega_i = 6$pu, $\omega_v = \frac{3}{4}\omega_i$. CSI: $T_s = \frac{2\pi}{160}$pu, $L = 4\%$pu, $C = 10\%$pu, $L_c = 2\%$pu, $\omega_i = 6$pu, $R_{damping} = 5\%$.

Application Example

To illustrate the analysis technique, the first example is of the benchmark discretised VSI detailed in Section 4.2.1 acting as an AC grid source, with a CSI as a load. Both of the inverters are modelled in the stationary reference frame and are symmetric in the $\alpha\beta$ paths with no cross-coupling components. The superimposed Bode responses of the discretised VSI impedance and CSI admittance with a typical set of parameters are shown in Figure 7.2.

For the responses in Figure 7.2, the vertical dashed line shows the single frequency (40.8pu) where the responses have a combined phase shift of -180 degrees. The total gain margin is 2.4dB $(0 - (6.6 - 9.0))$ so the closed-loop system is stable for the specified parameters.

Figure 7.3 again shows the system from Figure 7.2, but the voltage controller has a two-thirds higher bandwidth parameter ($\omega_i = 10$ rather than 6). By again examining the frequencies where the responses have a combined phase shift of -180 degrees, the closed-loop stability can be determined. The vertical solid red line in the figure indicates frequencies where there is a -180 degrees phase shift and the closed-loop system is unstable.

At the frequency where the system is unstable in Figure 7.3 it is observed that the cause of the instability is the significant phase lags and the high gains of the two systems that occur around

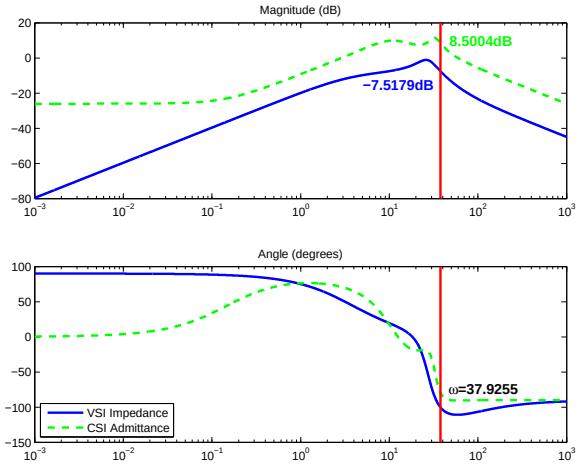


Figure 7.3: Discrete CSI admittance and VSI impedance responses. VSI: $T_s = \frac{2\pi}{160}$pu, $L = 4\%$pu, $C = 10\%$pu, $\omega_i = 10$pu, $\omega_v = \frac{3}{4}\omega_i$. CSI: $T_s = \frac{2\pi}{160}$pu, $L = 4\%$pu, $C = 10\%$pu, $L_c = 2\%$pu, $\omega_i = 6$pu, $R_{damping} = 5\%$.

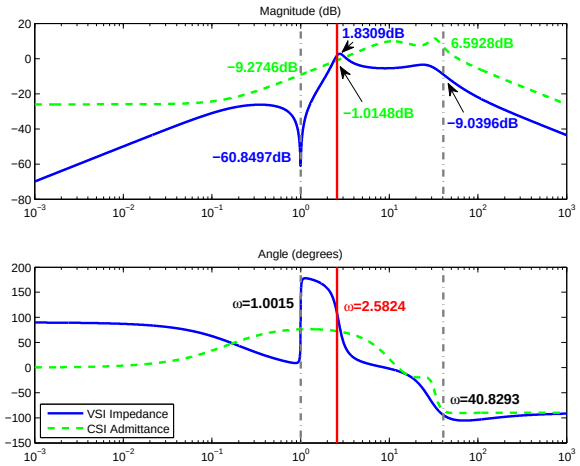


Figure 7.4: Discrete CSI admittance and VSI impedance responses with PR VSI controller. VSI: $T_s = \frac{2\pi}{160}$pu, $L = 4\%$pu, $C = 10\%$pu, $K_r = 2$pu, $\omega_i = 6$pu, $\omega_v = \frac{3}{4}\omega_i$. CSI: $T_s = \frac{2\pi}{160}$pu, $L = 4\%$pu, $C = 10\%$pu, $L_c = 2\%$pu, $\omega_i = 6$pu, $R_{damping} = 5\%$.

the fortieth harmonic, which in turn are a side-effect of the controller delays and the inverter filter resonances. This is an important observation as the ω_i bandwidth of 10 and 6pu for the VSI and CSI respectively, are relatively low compared to the sampling frequency of 8kHz. Had the system been modelled in continuous-time, as is often done for power inverters (as demonstrated in [12, 13, 51, 53]), the cause and gain limitations would not have been identified as the poles in question would not be present. The graphical technique allows complex systems in both continuous and discrete-time to be analysed without having to make simplifications that may hide potential instabilities.

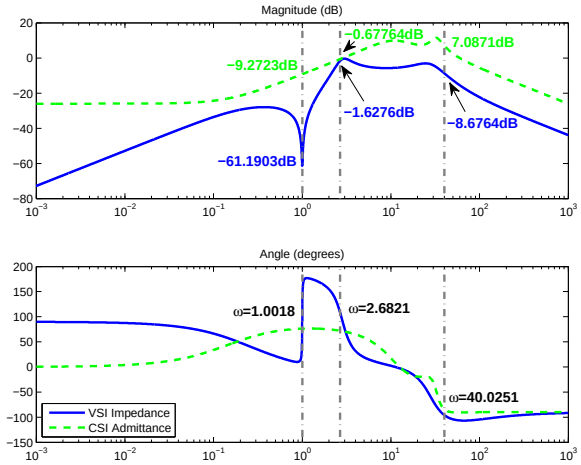


Figure 7.5: Discrete CSI admittance and VSI impedance responses with PR VSI controller. VSI: $T_s = \frac{2\pi}{160}$pu, $L = 4\%$pu, $C = 10\%$pu, $K_r = 2$pu, $\omega_i = 7$pu, $\omega_v = \frac{3}{4}\omega_i$. CSI: $T_s = \frac{2\pi}{160}$pu, $L = 4\%$pu, $C = 10\%$pu, $L_c = 2\%$pu, $\omega_i = 6$pu, $R_{damping} = 5\%$.

In the next example a resonator is added to the VSI capacitor voltage controller. Figures 7.4 and 7.5 show the responses of the cascaded VSI and CSI microgrid with the addition of a resonator at the fundamental frequency. The system without a resonator in Figure 7.2 is stable, but becomes unstable with the addition of a resonator in Figure 7.4. Figure 7.5 illustrates that the system is stable when the VSI parameter ω_i is *increased* from 6 to 7pu.

7.4.4 MIMO systems

So far the analysis has focused on single wire or single input single output (SISO) systems. As a result, three-phase analysis has been restricted to systems where both the source impedance and load admittance are symmetric and independent (no cross-coupling) in both axes (dq or $\alpha\beta$).

In addition to real and reactive power control, electrical machines are asymmetric in the dq axis due to the electrical torque being perpendicular to the magnetic flux. As a result of separate d and q axes in controllers, linearised transfer functions for asymmetric systems are typically expressed as complex transfer functions or expanded to transfer function matrices [12,65]. Three phase electrical systems typically have two axes and therefore have 2×2 transfer function matrices. These systems are therefore multiple input multiple output (MIMO) and the proposed single closed-loop analysis technique is no longer applicable.

The proposed technique can be extended to MIMO systems by the use of the Generalised Nyquist criterion [66]. The Nyquist stability criterion is often extended to MIMO systems through the use of Gershgorin bands, which assist in finding critical gains which govern gain and phase margins for closed-loop systems [67]. The generalised Nyquist stability criterion approach to MIMO systems is achieved via inspection of the transfer function matrix eigen values.

In the general MIMO case where the input and output have N-channels, $\mathbf{G}(s)$ is a $N \times N$ transfer function matrix such that

$$\mathbf{G}(s) = \begin{bmatrix} G_{11}(s) & G_{12}(s) & \cdots & G_{1N}(s) \\ G_{21}(s) & G_{22}(s) & \cdots & G_{2N}(s) \\ \cdots & \cdots & \ddots & \cdots \\ G_{N1}(s) & G_{N2}(s) & \ldots & G_{NN}(s) \end{bmatrix} \tag{7.22}$$

For space vector variables as input and output signals (a special case where $N = 2$), the notation for a transfer function matrix in dq is defined as

$$\mathbf{G}(s) = \begin{bmatrix} G_{dd}(s) & -G_{qd}(s) \\ G_{dq}(s) & G_{qq}(s) \end{bmatrix} \tag{7.23}$$

where the negative sign of element (1,2) is chosen to conform with the complex vector definition. Similar expressions are valid for $\alpha\beta$ systems. Although specified as continuous-time systems, the same approach also applies to discrete systems.

The generalised Nyquist theorem for MIMO systems compared to SISO systems defines multiple complex contours, where each contour is an eigen value $\lambda_i(s)$ of $\mathbf{G}(s)$, evaluated at $s = j\omega$. The eigen values $\lambda_i(s)$ are often not linear, but are still functions of s, calculated as:

$$0 = det(\lambda \mathbf{I}_N - \mathbf{G}(s)) \tag{7.24}$$

As expected the generalised Nyquist theorem simplifies for SISO systems, as the eigen value for a single transfer function $\mathbf{G}_1(s)$ is itself. For space vector systems where $N = 2$ there are two eigen values. The Nyquist criterion for stability requires $Z = P + N$, where P is the number of open-loop unstable poles of $\mathbf{G}(s)$, N is the combined number of times the Nyquist contours encircle -1 clockwise, and Z is the number of positive real poles of the closed-loop system. Examples of automating MIMO Nyquist analysis techniques are given in [68].

The open-loop transfer function matrix $\mathbf{G}(s)$ for an electrical system consists of an impedance and admittance transfer function matrix in equation 7.17. Therefore, to determine how each impedance and admittance contributes to the closed-loop stability, it must be possible to isolate the two eigenvalues $\lambda_1(s)$ and $\lambda_2(s)$ as functions of the respective impedance and admittance. It is case of isolating the various parts from each source and load that influence each eigenvalue. Substituting equation 7.17 into 7.24, where $\mathbf{G}(s)$ is a 2×2 transfer function matrix, in order to be able to separate the eigenvalues one of the transfer function matrices (either $Y_{load}(s)$ or $Z_{source}(s)$) must have zero entries for both $G_{dd}(s)$ and $G_{qq}(s)$ *or* both $G_{dq}(s)$ and $G_{qd}(s)$ (diagonal or antidiagonal). Despite the limitation, simplified systems that satisfy this condition can often be found.

Application Example

An example MIMO configuration is an induction machine with an appropriate source. Without loss of generality, the analysis of induction machines is limited to machines with a shorted rotor, primarily squirrel cage machines (SCIMs). Induction machines commonly have lightly damped subsynchronous poles which have been observed to become unstable at certain operating frequencies [69].

Induction machines have a symmetric electric component and an asymmetric torque producing component. Despite their non-linear nature, mature linearised transfer functions give reliable

results at given operating points as initially described in [65]. Linearised admittance expressions for an induction machine in the rotating reference frame from [65] are:

$$\Delta\mathbf{V} = \mathbf{Q}\Delta\mathbf{I} + \mathbf{S}\Delta\omega \tag{7.25}$$

where

$$\Delta\mathbf{V} = [\Delta\underline{V_s}, 0]^T \tag{7.26}$$

$$\Delta\mathbf{I} = [\Delta\underline{I_s}, \Delta\underline{I_r}]^T \tag{7.27}$$

$$\Delta\boldsymbol{\omega} = [\Delta\omega, \Delta\omega_s]^T \tag{7.28}$$

$$\mathbf{Q} = \begin{bmatrix} L_s(s+j\omega_0)+R_s & L_m(s+j\omega_0) \\ L_m(s+j\omega_{s0}) & L_r(s+j\omega_{s0})+R_r \end{bmatrix} \tag{7.29}$$

$$\mathbf{S} = \begin{bmatrix} j(L_s\underline{I_{s0}}+L_m\underline{I_{r0}}) & 0 \\ 0 & j(L_r\underline{I_{r0}})+L_m\underline{I_{s0}}) \end{bmatrix} \tag{7.30}$$

and mechanical expressions:

$$\Delta m_e = L_m\Im\{\underline{I_{s0}}\underline{\Delta I_s^*} + \underline{I_{r0}^*}\underline{\Delta I_s}\} \tag{7.31}$$

$$m_e = m_1 + \tfrac{J}{N_p}s\omega_r \tag{7.32}$$

Variables are defined in Table 7.1 and subscript "0" denotes operating point values.

From the above expressions a 2×2 transfer function matrix for the dq motor admittance $\mathbf{Y}_{load}(s)$ can be obtained. Due to the asymmetric torque coupling in equation 7.31, all four of the elements in $\mathbf{Y}_{load}(s)$ are unique.

Due to the vastly different time constants of the electrical and the mechanical components

of the machine, the frequencies of the poles and zeros of the transfer function matrix can be treated as being relatively independent, and the stability can be analysed in two parts. For high frequency analysis (above the fundamental) of the machine with an inverter, the high frequency response of the machine is governed purely by the electrical components. By neglecting the mechanical response the machine transfer function matrix becomes symmetric and the simpler SISO analysis technique can be used. For responses at and below the fundamental, such as inverter integrators (or resonators at the fundamental), the electrical and mechanical responses must both be considered.

As the full electrical and mechanical admittance transfer function matrix of an induction machine is asymmetric, the analysis method constrains the controller impedance to be either diagonal or antidiagonal. The discretised VSI is again used as the grid source. For the low frequency stability only the low frequency (subsynchronous) response of the VSI is required, which is inductive (Section 4.2). The continuous-time low frequency impedance of the VSI in Section 4.2 is $\frac{s}{C\omega_i\omega_v}$. Frequency shifted to the rotating frame, s is substituted with $s - j\omega_0$, and as only the low frequency response is of interest, the dynamic element s is dropped, simplifying the inverter response to $\frac{-j\omega_0}{C\omega_i\omega_v}$. Provided the inverter gains (and therefore bandwidth) are above the fundamental frequency, the only low frequency response of the VSI is an integrating component

Table 7.1: Induction machine variables

L_m	Magnetising inductance
L_s	Stator leakage
L_r	Rotor leakage
R_s	Stator resistance
R_r	Rotor resistance
ω	Synchronous frequency
ω_s	Slip frequency
ω_r	Rotor frequency
N_p	Number of pole pairs
J	Rotor inertia
m_e	Electrical torque
m_1	Load torque

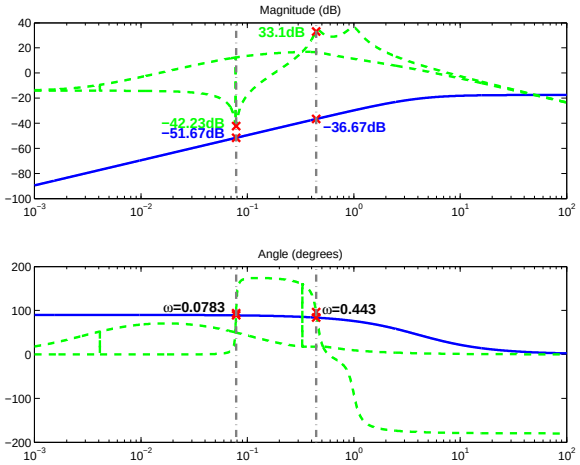


Figure 7.6: Induction machine with simplified VSI model. Induction machine: $\omega = 1$pu, $\omega_s = 0$ (no load), $L_m = 5$pu, $L_s = L_r = 5.075$pu, $R_s = R_r = 15\%$, $J = 47$ ($\sim$100ms response for 50Hz machine), $N_p = 1$ pole-pair. VSI: $L = 4\%$pu, $C = 10\%$pu, $\omega_i = 10$pu, $\omega_v = \frac{3}{4}\omega_i$, K_{int}=4.

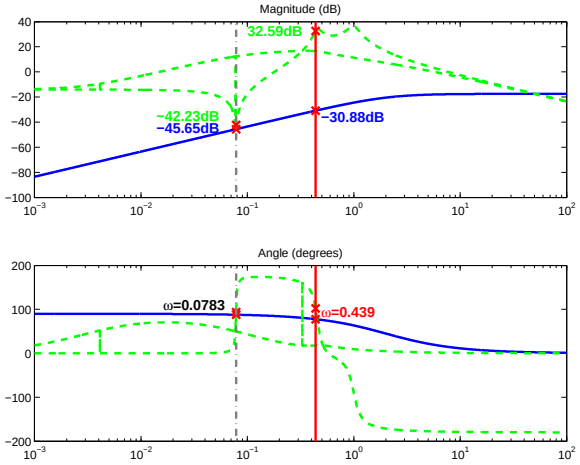


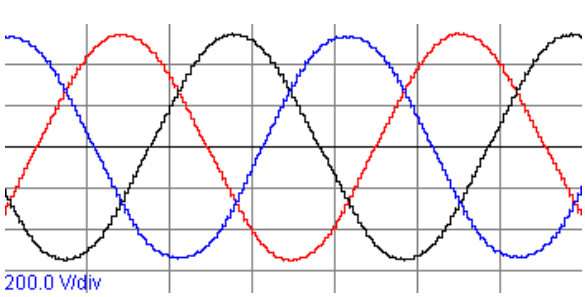
Figure 7.7: Induction machine with simplified VSI model. Induction machine: $\omega = 1$pu, $\omega_s = 0$, $L_m = 5$pu, $L_s = L_r = 5.075$pu, $R_s = R_r = 15\%$, $J = 47$pu, $N_p = 1$ pole-pair. VSI: $L = 4\%$pu, $C = 10\%$pu, $\omega_i = 10$pu, $\omega_v = \frac{3}{4}\omega_i$, K_{int}=2.

on the output voltage to eliminate steady-state errors. The VSI output impedance with an integrator in dq becomes:

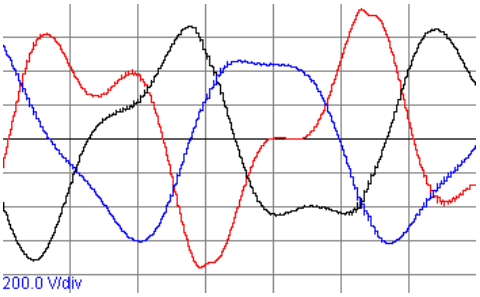
$$\mathbf{Z}_{VSI}(s) = \begin{bmatrix} 0 & -\frac{\omega_0 s}{C\omega_i\omega_v(s+K_{int})} \\ \frac{\omega_0 s}{C\omega_i\omega_v(s+K_{int})} & 0 \end{bmatrix} \tag{7.33}$$

where K_{int} is the integrator gain.

Figures 7.6 and 7.7 show the transfer function matrix eigenvalue Bode plots of a typical induction machine connected to the simplified VSI model with integrator. The 2×2 transfer function



(a) Stable with VSI $\omega_i = 7$pu.



(b) Unstable with VSI $\omega_i = 6$pu.

Figure 7.8: Onset of VSI and CSI voltage instability. VSI PR controller parameters: $\omega_v = \frac{3}{4}\omega_i$pu and $K_r = 2$pu. CSI $\omega_i = 6$pu.

matrix for the induction machine is in Appendix J. In Figure 7.6 the system with a VSI integrator gain K_{int} of 4pu is stable, whereas Figure 7.7 shows the system with an integrator gain of 2pu is unstable at a frequency of 0.4pu. It is worth noting that the system with an integrator gain of 0 (no integrator) is also stable. These results illustrate that the interactions from VSI integrators have the potential to excite low frequency lightly damped poles and result in instability.

In addition to the graphical technique, eigen value analysis has numerically confirmed the stability conditions found for Figures 7.6 and 7.7.

7.4.5 Hardware Results

The 125kVA parallel test hardware described in Appendix G has been used to confirm the findings for the VSI/CSI instability and VSI/SCIM instability.

The test system was first configured as a cascaded VSI and CSI as detailed in Section 7.4.3. One of the modules was configured as a VSI creating a three phase microgrid, while another was configured as a CSI with a DC bus voltage controller to maintain the DC bus. An additional module was configured as a rectifier to provide a DC bus for the VSI. The stability bounds for the simplified integral controller in Section 7.4.3 matched the gains found in Figures 7.4 and 7.5 to within 10% of the specified stable/unstable gains. Figure 7.8b shows the system voltage

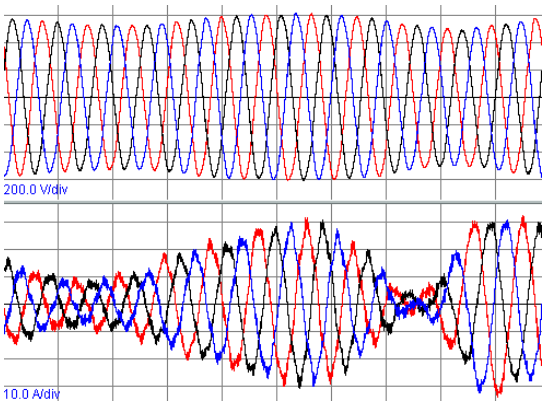


Figure 7.9: VSI and induction machine instability on test system. VSI PR controller gains: $\omega_i = 5$pu, $\omega_v = \frac{3}{4}\omega_i$pu and $K_r = 2$pu. Measured machine parameters: $\omega = 1$pu, $\omega_s = 0$, $L_m = 3$pu, $L_s = L_r = 3.08$pu, $R_s = R_r = 3.3\%$, $J = 180$pu (∼400ms).

becoming unstable when the VSI current gain ω_i is 6pu, where before it had been stable with a gain of 7pu in Figure 7.8a. The waveform in Figure 7.8b shows the fundamental 50Hz with the unstable 2.6pu frequency superimposed, as predicted in Figure 7.4.

For the MIMO analysis a 40A squirrel cage induction machine was connected to a VSI module. The transfer function matrix for the induction machine is provided in Appendix. J. Given the machine parameters, the stability of a VSI with a proportional-resonant controller running the motor was examined using the proposed graphical technique. The analysis predicted that the VSI running the motor at 50Hz would be unstable with a resonator gain below 0.2pu. When tested the system became unstable with a resonator gain below 0.3pu. Figure 7.9 shows the onset of the instability shortly before the system tripped on overcurrent. The graphical analysis specified the unstable frequency to be 0.14pu which is within 10% of the observed oscillation period in Figure 7.9.

7.5 SUMMARY AND DISCUSSIONS

As the number of different types of grid-connected devices increases so too does the complexity of analysing complex grids. From small micro-grids with only one source and one load, up to complex combinations, analysing grids has become increasingly difficult. Until recent years the

grid size problem has been manageable as the dominant devices have been of a particular type, typically large synchronous machines. While traditional synchronous machines have an intrinsic power sharing mechanism, power electronic systems do not.

In applications where grid-connected devices are capable of having an influence on the grid stability, system analysis must be performed. For traditional scenarios, such as rotating machines and infinite grids, the complex torque coefficients method and passivity analysis are adequate for determining system stability, however, for other complex scenarios they have been shown to be inadequate.

A graphical Nyquist stability criterion application that illustrates how the individual responses of interconnected complex sources and loads affect the total closed-loop stability has been developed. The graphical technique is used to indicate how individual impedance responses contribute to the closed-loop system poles. It provides insight as to how each of the two systems contribute to a given pole's gain or phase margin, allowing conclusions to be drawn as to how either one or both of the systems may be modified (for example changing gains or configuration) to affect the damping of particular poles.

The chapter concluded by further expanding the graphical technique to asymmetric multiphase systems, such as machines and complex electronic systems commonly found in grid-connect scenarios. An example is provided that successfully identified an instability for an induction machine driven by a VSI operating at full speed (50Hz). The analysis identified instability if the VSI integral gain was below 0.2pu. Experimentally the system became unstable with a gain of 0.3pu, showing a close correlation to the theoretical analysis.

Chapter 8

DISCUSSION AND CONCLUSION

The use of inverters in industry and grid-connect applications is growing at a rapid rate due to the availability of high performance and high power switching devices. Applications such as UPSs, dynamic voltage restorers, STATCOMs, frequency converters, and grid-connect resources all require both high performance and high power inverters. The IGBT is currently the state of the art device for achieving the inverter performance for particular applications, and in parallel or series configurations can provide the required power scaling. Mass-manufacture of massively-paralleled systems also has the inherent advantage of high system reliability.

The IGBT alone, however, is not the only bottleneck to achieving a high performance inverter. The choice of inverter controller is crucial in achieving the required performance given the associated inverter constraints. Unavoidable delays introduced by PWM and digital controller processing and sampling delays impose performance and stability limits. The use of PWM output filters and the paralleling of multiple power devices also has implications on the controller. Unfortunately, as the inverter bandwidth requirements approach the inverter switching and sampling frequency, traditional continuous-time derived controllers are only able to support a relatively low bandwidth.

Conflicting with the requirement of increasing the controller bandwidth is the controller sample frequency and delays. For low bandwidth to sample frequency ratios, discretised traditional continuous-time controllers exhibit a characteristic response, but as the controller bandwidth gains approach the discrete-time Nyquist limit, the stability margin rapidly decreases. For

example, down to a minimally-operable damping ratio of 0.3, a discretised continuous-time VSI controller sampling at 8kHz had a bandwidth to sample frequency ratio of 15 (bandwidth of the 11th harmonic). The limited achievable bandwidth becomes the primary driver for improved discrete-time controllers that can potentially offer greater bandwidth.

In Chapter 5 a discrete direct-design VSI controller is developed to overcome the limitations of traditional continuous-time derived controllers. The design uses constrained pole-placement that offers design-time ability to trade off the converter bandwidth against the respective damping ratio. The controller implementation is inherently simple, requiring only the capacitor voltage feedback, while also being robust to component value variations. A practical example on a 2MW system with an 8kHz sample frequency demonstrated a significantly improved controller bandwidth up to the 23rd harmonic while maintaining a damping ratio of 0.4.

The second part of developing a high performance controller for high power systems is ensuring suitability when paralleling multiple inverter modules to achieve a greater output power than individual device limits. Actively paralleling ensures that each module current-shares, however, potential instabilities were shown to exist depending on the controller and inverter filter. In applications where the filter values are fixed, different controller types can be used to ensure the prevention of instability. The source of the instability was shown to be related to the inter-module coupling impedance, either as a parasitic impedance between modules, or from intentional coupling inductances.

The worse case scenario is when the inter-module coupling impedance is around a few percent. To prevent the potential instability two options are offered: sacrifice the redundancy aspect of inter-modular coupling impedances and use a bulk monolithic coupling impedance, or use a controller that offers greater stability. Pole contours demonstrated that the discrete direct design controller developed in Chapter 5 offers an improved stability margin over the traditional continuous-time derived controllers.

Following the development of a high bandwidth and high power inverter system suitable for the applications introduced in the introduction, techniques for controlling and analysing grid-connected systems were reviewed and developed. As a the number of grid-connected applications and systems grows, so too does the complexity of analysing the numerous permutations. Whereas traditional grid-connected sources and loads were typically sub-cyclic systems such as rotating machines, large inverter systems with sub-millisecond performance are increasingly being coupled to the grid.

The method for analysing grid-connected systems is via their effective impedance. A grid impedance has no bounds on its complexity, its frequency response, and may possibly be non-linear, however, it is still important to be able to perform system analysis to ensure grid stability. When analysing grid-connected inverter systems, traditional analysis methods such as as the complex torque coefficients methods and passivity analysis no longer work when the underlying assumptions they were built on are invalidated. The assumptions made in these traditional analysis techniques are often valid for traditional sources and loads, such as rotating machines, but inverter systems are often not constrained in the same way.

A graphical Nyquist stability criterion application has been developed that illustrates how the individual responses of interconnected complex sources and loads affect the total closed-loop stability, as required for grid-connected systems. The application focuses on identifying how individual impedance responses contribute to the closed-loop system gain margin or phase margin, and in effect, stability. This allows the designer to identify incompatibilities with certain source or load combinations, and for conclusions to be drawn as to how either of the interconnected systems may be modified to affect the stability. The graphical application is demonstrated to be effective at analysing asymmetric multiphase systems, such as motors, operating with inverters.

The combination of high performance inverter controller development, the ability to parallel inverters to achieve power scaling, and analysis techniques for grid-connected systems achieves

the overarching goal of developing high performance and high power grid-connected inverter systems.

8.1 FUTURE WORK

A number of areas have been identified to progress this research further, specifically in the high performance inverter design and grid analysis.

Many grid-connect applications make use of either VSI or CSI modes, and may even have to transition between the two. Such an example may be a distributed storage system that at times may need to be a rectifier (CSI) and at other times a voltage and frequency source (VSI). Following the development of a high performance discrete direct-design VSI controller, either a CSI controller could be developed using similar techniques, or even more useful may be the development of a unified VSI and CSI controller. Such controller would be configurable to be a VSI with a source impedance or a CSI with a shunt admittance, and the ability to seamlessly transition between the two.

Upon applying the graphical analysis technique developed in Chapter 7 a potential subcyclic incompatibility between inverters and induction machines was identified that raised questions as to other potential incompatibilities with other inverter applications. At present the industry-practice method for analysing grids is through the use of time-domain simulations that show binary stability, however, by applying the graphical analysis technique to ensure stability then gain margins and potential instabilities could be uncovered.

Appendix A

DEVICE THERMAL RATING

To compare devices a set of typical operating conditions are defined. A fixed heatsink temperature will be assumed that maintains a device case temperature of 90°C. This value is has been chosen as a typical value for a moderate cost air-forced heatsink. The junction temperature is taken as 125°C as this is the typical maximum operating temperature for a Silicon power device. For determining the switching and conduction losses the voltage across the device will be taken at the manufacturers recommended switching voltage. This provides a typical voltage headroom for the device to operate within its maximum blocking voltage. The RMS device current will be taken as the device rating.

The conduction loss is fixed for a given device current rating and its respective parameters. For IGBTs and Thyristors it consists of a $I^2 \cdot R$ and $V_{ce,sat} \cdot I$ loss. For MOSFET devices it is simply an $I^2 \cdot R$ loss. The modulation depth will be assumed for a maximum sine wave ($1/\sqrt{2} = 0.707$). Given the conduction losses the switching losses and hence maximum switching frequency can be calculated. For a given device the following calculations are used to determine the maximum switching frequency:

$$P_{loss,max} = \frac{125°\text{C} - 90°\text{C}}{R_{th(j-c)}} \tag{A.1}$$

$$V_{bus} = 0.7V_{rated} \tag{A.2}$$

$$P_{loss} = P_{loss,igbt,conduction} + P_{loss,diode,conduction} + P_{loss,igbt,switch} + P_{loss,diode,switch} \tag{A.3}$$

$$P_{loss,igbt,conduction} = V_{ce,sat}I_{rated}\sqrt{2}(\frac{1}{2\pi} + \frac{1}{8\sqrt{2}}) + 2R_{terminal-chip}I_{rated}^2(\frac{1}{8} + \frac{1}{3\pi\sqrt{2}}) \tag{A.4}$$

$$P_{loss,diode,conduction} = V_{ce}I_{rated}\sqrt{2}(\frac{1}{2\pi} - \frac{1}{8\sqrt{2}}) + 2R_{terminal-chip}I_{rated}^2(\frac{1}{8} - \frac{1}{3\pi\sqrt{2}}) \tag{A.5}$$

$$P_{loss,igbt,switch} = f_{switch}E_{sw}\frac{\sqrt{2}}{\pi} \tag{A.6}$$

$$P_{loss,diode,switch} = f_{switch}E_{rr}\frac{\sqrt{2}}{\pi} \tag{A.7}$$

$$\tag{A.8}$$

where $R_{th(j-c)}$ is the junction-case thermal resistance.

Appendix B

MTBF OF REDUNDANT INVERTER SYSTEMS

In inverter array configurations the MTBF is typically derived for the individual modules. The final system MTBF depends on the ability to provide redundancy in the event of a module failure. Without module redundancy where the failure of one module is a failure of the entire array, the MTBF of N modules, each with an MTBF of $MTBF_m$, is:

$$MTBF_{sys} = \frac{MTBF_m}{N} \tag{B.1}$$

The decrease in the system MTBF with N immediately exceeds any reliability gains achievable with mass-manufacturing. In fact, the it provides a strong argument against inverter arrays. The only way to improve the MTBF is to provide module redundancy. Redundancy can be provided by either installing additional capacity, or if possible, reduce the system capacity. In some applications, such as Statcoms and frequency converters, a reduced capacity is often preferred over complete failure.

For systems that a constant failure rate, the system failure rate for redundant systems can be

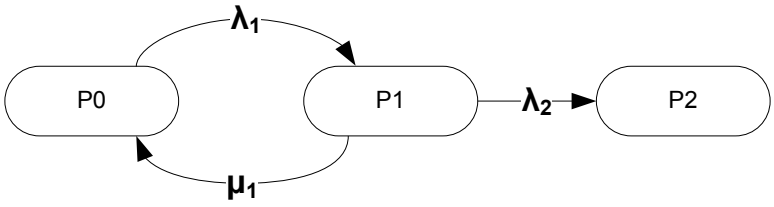


Figure B.1: Markov state transition diagram.

calculated using Markov chains. The Markov assumption implies that a system is memoryless (constant failure rate with time). The failure of individual modules is defined as a change of state. States that result in system failure are known as absorbing states, while ones that allow the system to continue operating are non-absorbing. The Markov transfer matrix for determining the system failure is:

$$P = \left[\begin{array}{c|c} I & 0 \\ \hline R & Q \end{array}\right] \tag{B.2}$$

where I is the identity matrix, 0 is the zero matrix, R is the non-absorbing to absorbing transitions, and Q is the non-absorbing to non-absorbing transitions.

The system MTBF is found by first computing the fundamental matrix $\Phi = (I - Q)^{-1}$, then summing the elements of the row corresponding to state zero.

For an inverter array configuration with one redundant module the state diagram for the Markov chain is shown in Figure B.1. State $P0$ is when all modules are operational (zero failures), $P1$ is when one of the modules has failed, and $P2$ is when two or more modules have failed and the system is no longer operational. The state transitions λ_1 and λ_2 are the failure rates from the respective states, while μ_1 is the repair rate (if applicable). The system MTBF depends on if a failed module can be repaired (μ_1), preventing system outages. MTBFs for systems with and without module repair will be investigated.

B.1 MTBF OF SYSTEMS WITHOUT MODULE REPAIR

For systems without module repair μ_1 in Figure B.1 is zero. For a system in state k (k failures), the probability of moving from state k to $k + 1$ is the probability of a single failure among the remaining $N - k$ units:

$$P(S_k \to S_{k+1}) = (N - k)\lambda(1 - \lambda)^{N-k-1} \tag{B.3}$$

Given that $\lambda \ll 1$:

$$P(S_k \to S_{k+1}) \simeq (N-k)\lambda \tag{B.4}$$

Therefore in Figure B.1 from $P0$ to $P1$ $k = 0$ so $\lambda_1 = N\lambda$, and from $P1$ to $P2$ $k = 1$ so $\lambda_2 = (N-1)\lambda$. Without module repairs there is no way of going back to states with less failures. The Markov matrix is constructed as defined in equation B.2 as:

$$P = \left[\begin{array}{c|cc} 1 & 0 & 0 \\ \hline (N-1)\lambda & 1-(N-1)\lambda & 0 \\ 0 & N\lambda & 1-N\lambda \end{array}\right] \tag{B.5}$$

The fundamental matrix is then found by computing $\Phi = (I-Q)^{-1}$:

$$\Phi = \begin{bmatrix} \frac{1}{(N-1)\lambda} & 0 \\ \frac{1}{(N-1)\lambda} & \frac{1}{N\lambda} \end{bmatrix} \tag{B.6}$$

Summing the elements of the row corresponding to the state zero and substituting λ for the reciprocal of the MTBF $\frac{1}{M_m}$:

$$MTBF_{sys} = \sum_{k=0}^{1} \Phi_{0,k} = \frac{1}{(N-1)\lambda} + \frac{1}{N\lambda} \tag{B.7}$$

$$= \frac{2N-1}{N(N-1)} M_m \tag{B.8}$$

From equation B.8, for a large N system the MTBF converges to $\frac{2MTBF_m}{N}$, effectively only doubling the MTBF of a non-redundant system.

B.2 MTBF OF SYSTEMS WITH MODULE REPAIR

For systems where failed modules can be repaired, the repair rate μ_1 in Figure B.1 is defined as the reciprocal of the repair time R_m. In this instance the Markov matrix is:

$$P = \left[\begin{array}{c|cc} 1 & 0 & 0 \\ \hline (N-1)\lambda & 1-((N-1)\lambda+\mu_1) & \mu_1 \\ 0 & N\lambda & 1-N\lambda \end{array}\right] \tag{B.9}$$

The fundamental matrix is:

$$\Phi = \begin{bmatrix} \frac{1}{(N-1)\lambda} & \frac{\mu_1}{N(N-1)\lambda^2} \\ \frac{1}{(N-1)\lambda} & \frac{(N-1)\lambda+\mu_1}{N(N-1)\lambda^2} \end{bmatrix} \tag{B.10}$$

The system MTBF is again found by summing the elements of the row corresponding to zero, substituting λ for the reciprocal of the MTBF $\frac{1}{M_m}$, and substituting μ_1 for $\frac{1}{R_m}$:

$$MTBF_{sys} = \sum_{k=0}^{1} \Phi_{0,k} = \frac{1}{(N-1)\lambda} + \frac{(N-1)\lambda+\mu_1}{N(N-1)\lambda^2} \tag{B.11}$$

$$= \frac{((2N-1)R_m + M_m)M_m}{N(N-1)R_m} \tag{B.12}$$

$$M_m \gg R_m \Rightarrow \quad MTBF_{sys} \simeq \frac{{M_m}^2}{N(N-1)R_m} \tag{B.13}$$

Equation B.13 suggests that regardless of N, a repairable redundant system has a system MTBF that is proportional to the square of a system without repairable redundancy. For module MTBF figures in the hundreds of thousands of hours—as is common with industrial equipment—this results in an MTBF in the tens of millions of hours! Of course to achieve this the rest of the system (power supplies, high level controllers etc) must also have an MTBF this high, and secondly that in *every* instance of a module failure that it did not result in a coupled failure, such as an explosion in one module taking out a second. In practice these conditions are not achievable, however, it does emphasise the fact that redundant repairable modules do offer an

exceptionally high MTBF.

Appendix C

APPLICATION OF Padé APPROXIMATIONS AND THE LAMBERT W FUNCTION

Figure C.1 shows a continuous-time closed-looped system with a feedback transport delay. The closed-loop transfer function for the system $H(s)$ is given as:

$$H(s) = \frac{G(s)}{1 + G(s)e^{-s\tau}} \tag{C.1}$$

Figure C.2 shows a Nyquist plot of equation C.1 where $G(s) = \frac{1}{s}$ and $\tau = 1.5$, where:

$$H(s) = \frac{1}{s + e^{-1.5s}} \tag{C.2}$$

Figure C.2 indicates the system is stable with a gain margin of 0.401dB. A second and third order Padé approximation results in a gain margin of 0.47dB and 0.402dB respectively, confirming the close correlation claimed. The expression for equation C.1 with a second-order Padé approximation is:

$$H(s) = \frac{s^2 + 4s + 5.33}{(s + 4.95)(s^2 + 0.0516s + 1.08)} \tag{C.3}$$

And a third order Padé:

$$H(s) = \frac{(s + 3.10)(s^2 + 4.90s + 11.5)}{(s^2 + 0.0439s + 1.07)(s^2 + 6.96s + 33.3)} \tag{C.4}$$

Evaluating the closed-loop system $H(s)$ using the Lambert W function, the poles of equation C.2

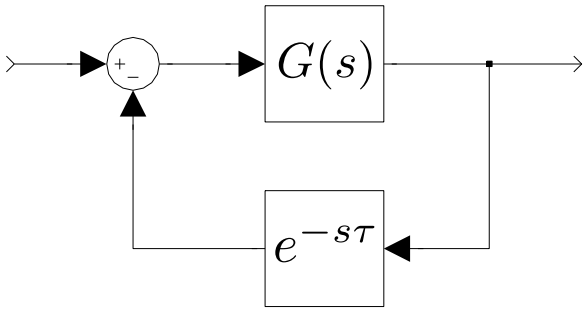


Figure C.1: Continuous-time closed-loop system with feedback delay.

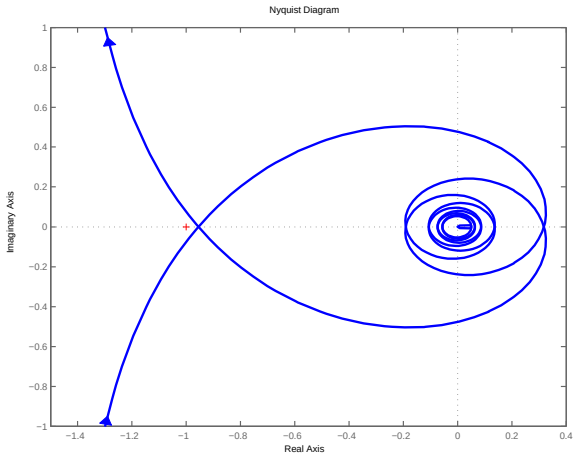


Figure C.2: Nyquist plot of system with $G(s) = \frac{1}{s}$ open loop response and propagation delay of $\tau = 1.5$.

are:

$$s = \frac{W(-\tau)}{\tau} \tag{C.5}$$

The Lambert W is a multivalued function and each pole of equation C.2 can be found by choosing the appropriate Lambert W index. The dominant pole of equation C.5 where $\tau = 1.5$ is $s = -0.2186 \pm j1.033$ which has a damping ratio of $\zeta = 0.021$.

Appendix D

ZERO ORDER HOLD RESPONSE

The continuous-time ZOH response is defined as

$$H_{ZOH}(s) = \frac{1 - e^{-sT_s}}{sT_s} \tag{D.1}$$

The ZOH phase response is

$$\begin{aligned}
\angle H_{ZOH}(s) &= \angle\left(\frac{1 - e^{-sT_s}}{sT_s}\right) && \text{(D.2)}\\
\text{substituting } s = j\omega \Rightarrow \quad &= \angle\left(\frac{1 - \cos(\omega T_s) + j\sin(\omega T_s)}{sT_s}\right) && \text{(D.3)}\\
&= \tan^{-1}\left(\frac{\sin(\omega T_s)}{1 - \cos(\omega T_s)}\right) - \frac{\pi}{2} && \text{(D.4)}\\
&= \tan^{-1}\left(\frac{1}{\tan(\frac{\omega T_s}{2})}\right) - \frac{\pi}{2} && \text{(D.5)}\\
&= -\frac{\omega T_s}{2} && \text{(D.6)}
\end{aligned}$$

This is in contrast to a single unit delay which has a phase response of $-\omega T_s$.

The ZOH magnitude is

$$
\begin{aligned}
|H_{ZOH}(s)| &= \left|\frac{1-e^{-sT_s}}{sT_s}\right| && \text{(D.7)}\\
\text{substituting } s=j\omega \Rightarrow \quad &= \frac{\sqrt{(1-\cos(\omega T_s))^2+\sin^2(\omega T_s)}}{\omega T_s} && \text{(D.8)}\\
&= \frac{\sqrt{2}}{\omega T_s}\sqrt{1-\cos(\omega T_s)} && \text{(D.9)}\\
&= \frac{2}{\omega T_s}\sin\left(\frac{\omega T_s}{2}\right) && \text{(D.10)}\\
&= \operatorname{sinc}\left(\frac{\omega T_s}{2\pi}\right) && \text{(D.11)}
\end{aligned}
$$

In (D.11) the sinc function is the normalised sinc function where $\operatorname{sinc}(\theta)=\frac{\sin(\pi\theta)}{\pi\theta}$.

Appendix E

INTEGRAL SQUARED ERROR AND INTEGRAL ERROR SQUARED

ISE is calculated as:

$$ISE = \int_0^\infty \{e(t)\}^2 \, dt \tag{E.1}$$

Analytic solutions for low-order systems are easily attainable, but rapidly become difficult to find for systems above the second-order. Applied to a first-order system $\frac{\omega_i}{s+\omega_i}$ with a unit step $\left(\mathcal{L}\{u(t)\} = \frac{1}{s}\right)$, the ISE is

$$\begin{aligned} ISE &= \int_0^\infty \left\{1 - \mathcal{L}^{-1}\left\{\frac{\omega_i}{s+\omega_i}\frac{1}{s}\right\}\right\}^2 dt && \text{(E.2)} \\ &= \int_0^\infty \left\{e^{-\omega_i t}\right\}^2 dt && \text{(E.3)} \\ &= \frac{1}{2\omega_i} && \text{(E.4)} \end{aligned}$$

As expected, the ISE decreases for a higher gain ω_i.

The ISE for an arbitrary second-order system $H(s)$ can be shown to be

$$\begin{aligned} H(s) &= \frac{\omega_n^2}{s^2 + 2s\omega_n\zeta + \omega_n^2} && \text{(E.5)} \\ ISE(H(s)) &= \frac{4\zeta^2 + 1}{4\omega_n\zeta} && \text{(E.6)} \end{aligned}$$

Where ω_n is the natural frequency and ζ is the damping ratio.

IAE is calculated as

$$IAE = \int_0^\infty |e(t)|\, dt \tag{E.7}$$

For the same example first-order system used above, the IAE can be shown to be $IAE = \frac{1}{\omega_i}$.

Appendix F

DISCRETISED CONTINUOUS-TIME VSI EXPRESSIONS

Discretised continuous-time VSI controller as shown in Figure 4.5. The controller and filter blocks are:

$$G_{V_c,V_{pwm}}(z) = \frac{(z+1)(1-\cos(\omega_n T_s))}{z^2 - 2z\cos(\omega_n T_s) + 1} \tag{F.1}$$

$$G_{I_c,V_{pwm}}(z) = \frac{C(z-1)\omega_n \sin(\omega_n T_s)}{z^2 - 2z\cos(\omega_n T_s) + 1} \tag{F.2}$$

$$C_{Ff}(z) = \omega_i \omega_v LC \tag{F.3}$$

$$C_{Fb,V_c}(z) = 1 - \omega_i \omega_v LC \tag{F.4}$$

$$C_{Fb,I_c}(z) = -\omega_i L \tag{F.5}$$

Substituting these into (4.15) and inserting a single sample period delay to the feedback paths, the closed loop forward transfer function is:

$$\frac{V_c(z)}{V_{c,ref}(z)} = \frac{\omega_i \omega_v LC(z+1)(1-\cos(\omega_n T_s))z}{(z^2 - 2z\cos(\omega_n T_s)+1) - (1-\omega_i\omega_v LC)(z+1)(1-\cos(\omega_n T_s)) + \omega_i LC\omega_n \sin(\omega_n T_s)(z-1)} \tag{F.6}$$

The expression for the output impedance transfer function is:

$$\frac{V_c(z)}{I_{out}(z)} = \frac{G_{V_c,I_{out}} + C_{Fb,I_c}(G_{V_c,V_{pwm}}G_{I_c,I_{out}} - G_{I_c,V_{pwm}}G_{V_c,I_{out}})}{1 - (C_{Fb,V_c}G_{V_c,V_{pwm}} + C_{Fb,I_c}G_{I_c,V_{pwm}})} \tag{F.7}$$

The two filter expressions for V_c and I_c with respect to I_{out} are:

$$G_{V_c,I_{out}}(z) = \frac{L(z-1)\omega_n \sin(\omega_n T_s)}{z^2 - 2z\cos(\omega_n T_s) + 1} \tag{F.8}$$

$$G_{I_c,I_{out}}(z) = \frac{LC(z-1)\omega_n^2(z - \cos(\omega_n T_s))}{z^2 - 2z\cos(\omega_n T_s) + 1} \tag{F.9}$$

Substituting into (F.7) and inserting a single sample period delay to the feedback paths, the closed loop output impedance transfer function is:

$$\frac{V_c(z)}{I_{out}(z)} = \frac{L\omega_n z(z-1)(\sin(\omega_n T_s) - \omega_i LC\omega_n + \omega_i LC\omega_n \cos(\omega_n T_s))}{(z^2 - 2z\cos(\omega_n T_s) + 1) - (1 - \omega_i\omega_v LC)(z+1)(1-\cos(\omega_n T_s)) + \omega_i LC\omega_n \sin(\omega_n T_s)(z-1)} \tag{F.10}$$

Appendix G

TEST HARDWARE

Three parallel-connected inverter configurations were used for evaluation and validation of control models developed. Each of the hardware configurations were built up using either full rating or scaled 480V, 150A, 125kVA 3-phase inverter modules. Each module has configurable LC or LCL output filters; inductor current, capacitor voltage and output current feedback; 4kHz IGBT switch stack; and an 8kHz-sampling DSP controller. The modules receive voltage or current references from a master DSP once per sampling period. The master DSP has its own set of point of common coupling voltage and current sensors. Rapid testing was achieved by using code generation tools as detailed in Section 3.6.2.

Two selectable operating modes are available for each module. A typical application is a current controlled rectifier which controls the DC bus in one set of modules, and an output inverter in the other set of modules. The modules can have paralleled or independent DC buses and outputs.

Three hardware configurations were used with modules of different ratings. When a module was scaled from the original 125kVA rating, the filter components and feedback scaling was adjusted accordingly. The configurations used were:

- A single low power (1% power, 48V, 15A) module to allow rapid testing in an office environment. Connected to high current DC supply and various load configurations.

- Three pairs of one third current modules (50A) fed from 100kVA 480V supply, shown in

(a) 125kVA system made up of three pairs of 50A modules

(b) 2MVA system made up of sixteen pairs of 150A modules

Figure G.1: Test hardware.

Figure G.1a. A wide range of loads were available including inductive, capacitive and resistive combinations. Partially rated induction machine and diode rectifier loads were also available.

- Sixteen pairs of 150A modules fed from a 1MVA supply, shown in Figure G.1b. Due practical constraints it was not possible to provide full resistive loading.

Appendix H

NON-IDENTICAL SOFT-COUPLED PARALLEL EXPRESSIONS

The continuous-time expressions for the capacitor voltage transfer functions in equations 6.32 to 6.36 are:

$$H_1 = G_{V_{c,1}V_{pwm,1}}(s) = \frac{L_{c,1}(Eb-(n-1)LL_gL_{c,1})}{EE_1b-LL_g(EL_c-(n-1)E_1L_{c,1})} \tag{H.1}$$

$$H_2 = G_{V_{c,1}V_{pwm,j}}(s) = \frac{L_{c,1}LL_cL_g}{EE_1b-LL_g(EL_c-(n-1)E_1L_{c,1})} \tag{H.2}$$

$$H_3 = G_{V_{c,i}V_{pwm,1}}(s) = G_{V_{c,1}V_{pwm,j}}(s) \tag{H.3}$$

$$H_4 = G_{V_{c,i}V_{pwm,i}}(s) = \frac{L_c(EE_1b-EL_gL_cL-(n-2)L_lL_{c,1}LE_1)}{E(EE_1b-LL_g(EL_c-(n-1)E_1L_{c,1}))} \tag{H.4}$$

$$H_5 = G_{V_{c,i}V_{pwm,j}}(s) = \frac{L_cLL_gL_{c,1}E_1}{E(EE_1b-LL_g(EL_c-(n-1)E_1L_{c,1}))} \tag{H.5}$$

where E and E_1 are the identical and unique filter expressions respectively, and b determines the output current sharing, given as:

$$E = s^2LCL_c+L_c+L \tag{H.6}$$

$$E_1 = s^2LCL_{c,1}+L_{c,1}+L \tag{H.7}$$

$$b = nL_{c,1}L_c+L_g(L_c+(n-1)L_{c,1}) \tag{H.8}$$

Expressions for the individual capacitor currents are are found by applying equation 6.4 in Section 6.2.1. Each of the expressions for the capacitor voltages and currents are discretised using either the regular Z-transform for integer feedback delays or the Advanced Z-transform

when fractional feedback delays are used. The discretised capacitor voltage expressions are labelled $H_1(z)$ through to $H_5(z)$, with a subscript i to denote the respective discretised capacitor current expressions.

The closed-loop expressions for the module PWM voltages as a function of the input reference voltage $G_{V_{pwm,1}V_{c,ref}}$ and $G_{V_{pwm,i}V_{c,ref}}$ are given below. Without loss of generality the equivalent capacitor current expressions are left out for clarity.

$$G_{V_{pwm,1}V_{c,ref}} = \frac{C_{Ff}(C_{Fb}(H_4 + (n-2)H_5 - (n-1)H_2) - 1)}{{C_{Fb}}^2((n-1)H_2H_3 - H_1H_4 - (n-2)H_1H_5) + C_{Fb}(H_4 + H_1 + (n-2)H_5) - 1} \tag{H.9}$$

$$G_{V_{pwm,i}V_{c,ref}} = \frac{C_{Ff}(C_{Fb}(H_1 - H_3) - 1)}{{C_{Fb}}^2((n-1)H_2H_3 - H_1H_4 - (n-2)H_1H_5) + C_{Fb}(H_4 + H_1 + (n-2)H_5) - 1} \tag{H.10}$$

In the interest of stability the above expressions provide the closed-loop system poles. More appropriate system outputs such as capacitor voltages or output currents can be obtained via substitution with the filter expressions H_1 through to H_5.

Appendix I

POWER SHARING BETWEEN GRID-CONNECTED SOURCES

As a result of the predominantly inductive coupling between grid-connected sources, real and reactive power sharing is achieved by actively drooping the frequency in response to increased power flow, and drooping the voltage in response to increased reactive power flow, respectively. For a single complex EMF source $\underline{U_s}$ and operating into a grid with voltage $\underline{U_g}$ and impedance $\underline{Z}$, the power flowing into the grid is described as:

$$\begin{aligned} P + jQ &= \underline{S} = \underline{U_s}\underline{I^*} = \underline{U_s}\left(\frac{\underline{U_s} - \underline{U_g}}{\underline{Z}}\right)^* && \text{(I.1)} \\ &= U_s\left(\frac{U_s - U_g e^{j\delta}}{Z e^{-j\theta}}\right) && \text{(I.2)} \\ &= \frac{U_s^2}{Z}e^{j\theta} - \frac{U_s U_g}{Z}e^{j(\theta+\delta)} && \text{(I.3)} \end{aligned}$$

where δ is known as the power angle.

Therefore the real and reactive power flowing into the grid (out of the source) are:

$$\begin{aligned} P &= \frac{U_s^2}{Z}\cos(\theta) - \frac{U_s U_g}{Z}\cos(\theta+\delta) && \text{(I.4)} \\ Q &= \frac{U_s^2}{Z}\sin(\theta) - \frac{U_s U_g}{Z}\sin(\theta+\delta) && \text{(I.5)} \end{aligned}$$

Substituting $Ze^{j\theta} = R + jX$ into equations I.4 and I.5, and rearranging results in:

$$U_s \sin(\delta) = \frac{XP - RQ}{U_s} \tag{I.6}$$

$$U_s - U_g \cos(\delta) = \frac{RP + XQ}{U_s} \tag{I.7}$$

For grid impedances where $X \gg R$, R may be eliminated. Also, if the power angle δ is small, then $\sin(\delta) = \delta$ and $\cos(\delta) = 1$. Equations I.6 and I.7 become:

$$\delta \cong \frac{XP}{U_g U_s} \tag{I.8}$$

$$U_g - U_s \cong \frac{XQ}{U_g} \tag{I.9}$$

These two relationships confirm that for predominantly inductive grid and small power angles, that the power angle depends on P, whereas the voltage difference depends on Q.

In all modern power grids this technique is exploited by the synchronous rotating machines used for generation. An increased power flow demands an increased electromechanical torque, which causes the rotor to decelerate. This effect propagates through all the sources on a grid, resulting in load sharing. The mechanical torque may then be increased to restore any effective frequency droop. Grid voltage regulation works in a similar manner by actively controlling the amount of VARs sourced or sunk by a generator (its excitation) the voltage at the common point of coupling can be controlled.

Appendix J

INDUCTION MACHINE TRANSFER FUNCTION MATRICES

Example induction machine transfer function matrix elements for motor in Chapter 7, Figures 7.6 and 7.7:

$$G_1(s) = \frac{6.72(s-0.033)(s-0.00023)(s^2+0.24s+0.063)}{(s+0.10)(s^2+0.094s+0.055)(s^2+0.21s+0.99)} \tag{J.1}$$

$$G_2(s) = \frac{6.72(s+0.0030)(s^2+0.10s+0.054)}{(s+0.10)(s^2+0.094s+0.055)(s^2+0.21s+0.99)} \tag{J.2}$$

$$G_3(s) = \frac{-6.72(s+0.098)(s^2+0.0037s+0.0016)}{(s+0.10)(s^2+0.094s+0.055)(s^2+0.21s+0.99)} \tag{J.3}$$

$$G_4(s) = \frac{6.72(s+0.24)(s+0.00017)(s^2-0.036s+0.011)}{(s+0.10)(s^2+0.094s+0.055)(s^2+0.21s+0.99)} \tag{J.4}$$

where machine transfer function matrix is:

$$\mathbf{G}(s) = \begin{bmatrix} G_1(s) & G_2(s) \\ \\ G_3(s) & G_4(s) \end{bmatrix} \tag{J.5}$$

Transfer function matrix elements for example motor in Figure 7.9:

$$G_1(s) = \frac{6.33(s+0.34)(s+0.068)(s+0.012)(s+0.011)}{(s+0.20)(s^2+0.21s+0.028)(s^2+0.42s+0.96)} \tag{J.6}$$

$$G_2(s) = \frac{6.33(s+0.011)(s^2+0.21s+0.026)}{(s+0.20)(s^2+0.21s+0.028)(s^2+0.42s+0.96)} \tag{J.7}$$

$$G_3(s) = \frac{-6.33(s+0.21)(s^2+0.011s+0.0013)}{(s+0.20)(s^2+0.21s+0.028)(s^2+0.42s+0.96)} \tag{J.8}$$

$$G_4(s) = \frac{6.33(s+0.41)(s+0.0054)(s^2+0.011s+0.0013)}{(s+0.20)(s^2+0.21s+0.028)(s^2+0.42s+0.96)} \tag{J.9}$$

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