Integrated Combined Amplifiers for Planar Circuits

(Invited paper)

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Abstract - **Integrating amplification with power combining allows components to be eliminated thereby reducing system size. Recently there has been much interest in reducing size of planar circuit components that use transmission lines, and therefore, combining strategies that employ transmission elements can leverage on these miniaturization techniques to further reduce system size. In this paper we explore the dual-fed distributed power amplifier and a variant that uses periodic loops of transmission lines.**

I. INTRODUCTION

An important application of N-way power dividers is combining N identical amplifiers to achieve an output power N times that of a single transistor. Fig. 1 shows the basic schematic of an N-way combining power amplifier. Two N-way combiners are required: one to equally distribute the input signal amongst the N transistors and another to combine the signals from the transistor outputs. The transverse width of the amplifier is W, and the longitudinal lengths of the divider, transistors and combiner are L_d, L_t and L_c respectively. Lengths L_d and L_c include lengths of transmission lines between the transistors and the two dividers to ensure equal phasing of the transistors. The transverse width W is proportional to N.

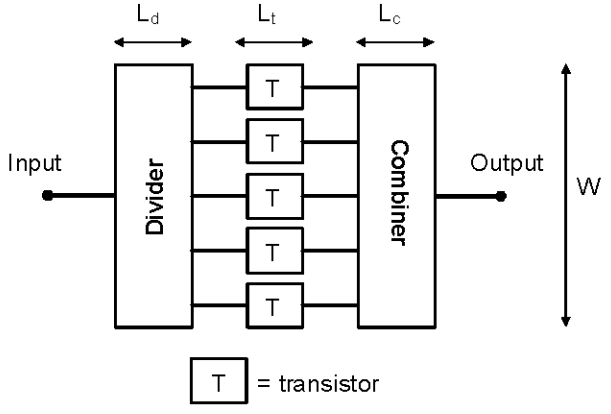

Fig. 1. N-way combined power amplifier block diagram

Experience has shown that corporate power combiners constructed from 2-way dividers [1] are most suitable for the combined amplifier application as they have their output ports located in a straight line. Such dividers however have lengths proportional to the logarithm of N. Tapered line and sectoral power dividers can be used, but like the corporate power divider, their lengths increases with N.

It is common to integrate circuits and components on the same substrate. But as each circuit or component is designed in isolation with little regard to their end application, integration often simply comprises physical placement of components on the same substrate. Though, for on-chip power combining for high-power FETs and power amplifier output stages, dividers are designed to perform impedance transformation [2]. On the other hand, the integrated active antenna concept aims to do more than simply place circuits and components on the same substrate; planar antennas are designed to perform transistor output matching and harmonic termination as well as radiation [3]. A single antenna can also be used to combine transistors [4]-[7].

It is the purpose of this work to consider planar power divider structures that form an integral part of the amplifier (and of course can be integrated on the same substrate). This approach means that individually designed N-way power dividers can be dispensed with thereby reducing circuit size. Such dividers would ideally have longitudinal lengths that are small and independent of N. Whereas it is reasonable to accept that the combined amplifier transverse width, W, will be proportional to N. The distributed amplifier is an example of an N-way combined amplifier that has these structural features. However, although conventional distributed amplifiers achieve broad bandwidth, they have very low efficiency. Tapering of the input and output lines of the distributed amplifier can be used to direct transistor output power to the load [8], but the level of combining (N) is limited.

The extended resonance amplifier [9], the dual-fed distributed amplifier [10], and the distributed active transformer [11] offer alternative approaches to efficient integrated combined amplifiers. The former two methods have a longitudinal length largely independent of N, whereas the later method uses an entirely different approach to feed the transistors. The dual-fed distributed amplifier integrates FETs

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in much the same manner that conventional distributed amplifier and their uniform divider and combiner structures lend themselves to method further miniaturization. It is the dual-fed distributed amplifier that is central to this paper.

Section II will describe the basic principles of the dual-fed distributed amplifier, section III describes dual-fed distributed amplifier realizations including modifications to achieve further improve performance and compactness. Section IV will introduce a variant of the dual-fed distributed amplifier that uses periodic loop structure in place of transmission lines.

II. Dual-Fed Distributed Amplifier Principles

The dual-fed distributed amplifier was originally proposed as far back as 1988 as an approach to make better use of the transistors [12]. More recent activity concentrated on efficient power combining and utilization of the transistors [10][13]. A basic schematic of an optimum 4-FET dual-fed distributed amplifier is shown in Fig. 2.

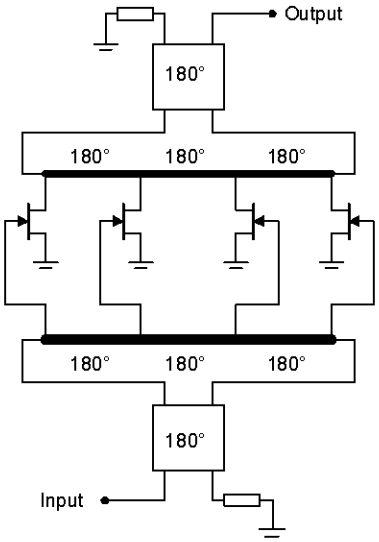

Fig. 2. Dual-fed distributed amplifier combining 4 FETs

The midpoint of the gate and drain transmission line are effectively short-circuited to ground and allows the dual-fed distributed amplifier to be split into a pair of single-ended dual-fed distributed amplifiers which can be combined using a pair of quadrature couplers to achieve matched input and output ports [14][15]. The single-ended dual-fed distributed amplifier can be designed for efficient operation [15], and an N-way single-ended dual-fed distributed amplifier is shown in Fig. 3. Dual-feeding in this amplifier occurs by virtue of the short-circuit terminations of both the gate and drain lines which are also useful for FET biasing.

An important attribute of the dual-fed distributed amplifiers shown in Fig. 2 and Fig. 3 is that all transistors are equally driven, drive into identical loads, and are equally utilized. Dual-feeding also provides some compensation for losses in the gate and drain lines [13]. With reference to Fig. 3, it can be shown that the load impedance for each FET is zero at even harmonics, and NZ_L at the fundamental and odd harmonics [16]. The drain line characteristic impedance Z_{0D} is normally equal to Z_L (at the fundamental) to maximize bandwidth.

III. Dual-Fed Distributed Amplifier Realizations

A balanced amplifier comprising a pair optimum 2-FET single-ended dual-fed distributed amplifier was designed for operation at 1.8 GHz and achieved an efficiency of 37 % under class-A conditions [17] and 50 % under class-B conditions [18]. In both cases, the output power was 25 dBm, and the gain was 9.3 dB and 7.3 dB under class-A and class-B conditions respectively [18]. Class-B operation is possible due to the inherent short-circuit loading of the FETs at even harmonics [18]. This amplifier had matched input and output ports.

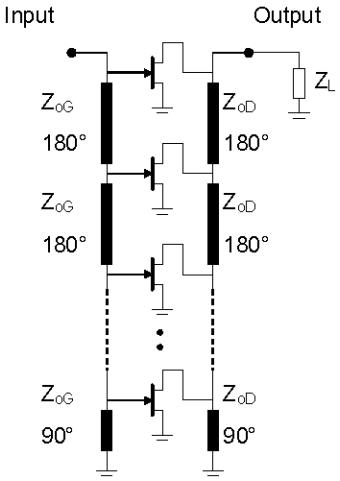

Fig. 3. N-way single-ended dual-fed distributed amplifier.

Class-F operation of FETs is possible at microwave frequencies and requires the presence of odd-harmonics [19]. The single-ended dual-fed distributed amplifier can be modified to achieve the right conditions under which class-F operation can take place and yet no harmonics appear at the output. Namely, Z_L is resistive at the fundamental and infinite at odd-harmonics, and that the output matching network contains odd-harmonic traps [16]. A 2-FET class-F single-ended distributed amplifier operating at 1.8 GHz achieved an efficiency of over 70 % at an output power of 22 dBm and had a gain of 8 dB [20].

The transmission line lengths between FETs are nominally 180° and the gate and drain lines are terminated by 90° short-circuit stubs. FET input and output capacitances mean that these line lengths need to be shortened [21] to maintain correct phasing of the FETs [17]. Although shortening of the transmission lines is desirable, bandwidth is also reduced [22]. An alternative approach is to implement the gate and drain

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lines with artificial transmission lines. Using this approach, not only is the transverse width, W, reduced, the FET input and output capacitances are absorbed into the artificial transmission line structure without reducing bandwidth [22]. Fig. 4 shows the photograph of 3-FET single-ended dual-fed distributed amplifier that operates at 1.8 GHz. This amplifier achieved and output power of 23 dBm over an 11 % bandwidth and over 35 % efficiency over a 15 % bandwidth [22]. Another approach to reduce size is to use the metamaterial approach to realize finite length zero-phase shift transmission lines [23]. This has the added bonus of increasing bandwidth [23].

Recently, optimum single-ended dual-fed distributed amplifiers have been used to implement the main and peaking amplifiers of a Doherty amplifier [24][25].

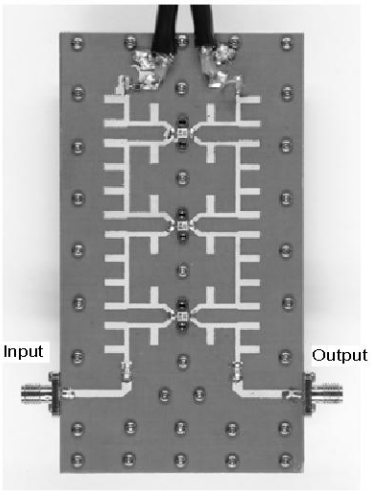

Fig. 4. 3-FET 1.8 GHz single-ended dual-fed distributed amplifier that uses artificial transmission lines [22]

IV. Combining of FETs Using Periodic Loop Structures

One of the drawbacks of the optimum dual-fed distributed amplifier is that the load seen by the FET is N times the amplifier load impedance. For power FETs, a low value of load impedance is required and hence the amplifier load impedance would be prohibitively low. Preferably, a combiner should present the power FET a load impedance that is the amplifier load impedance divided by N. In this way, a low impedance can be obtained from an external 50 Ω amplifier load. Fork power dividers operate on this principle.

Fig. 5 shows the schematic of the proposed new type of dual-fed distributed amplifier that uses a periodic loop combining structure in place of the drain transmission line. The FET gates are fed similar to a pair of 2-FET single-ended dual-fed distributed amplifiers but with a 180° hybrid feeding these. In the periodic loop combining structure, the characteristic impedance of all the transmission line elements are identical and equal to Z_{0C}. Simulations have shown that the load impedance presented to each FET are all equal to Z_{0C}^2/NZ_L where Z_L is the amplifier load impedance. Importantly, the FET load impedance is inversely proportional to N, and similar to the dual-fed distributed amplifier, the longitudinal length of the combiner is independent of N.

An amplifier operating at 2 GHz employing four Eudyna FLC057WG GaAs FETs is now considered. For such a FET, the optimum load is 33 Ω when a 3.6 V drain supply is used. If Z_L is 50 Ω, then Z_{0C} = 81 Ω which is feasible. Shunt inductors were used to parallel resonate the FET input and output at 2 GHz.

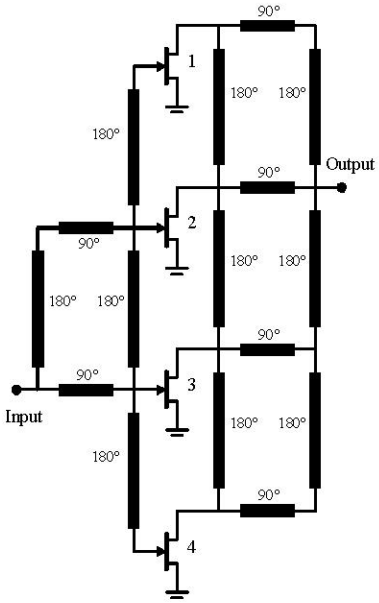

Fig. 5. Schematic of a 4-FET amplifier using a periodic loop combiner at the output of the amplifier

Harmonic balance simulations were used to assess the feasibility of the amplifier. The FETs were represented by a nonlinear circuit model and included parasitics, whose parameters were obtained using the data sheet DC I/V data and S-parameters.

Simulated load lines indicated that the load impedances seen by the FETs at 2 GHz were identical and optimum for class-A operation. Fig. 6 shows the loadlines at 1.85 GHz.

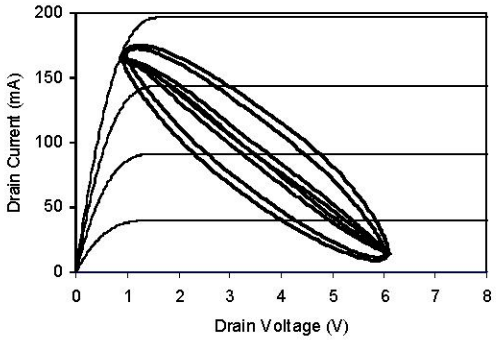

Fig. 6. Simulated loadlines for the 4-FET power amplifier at 1.85 GHz

Fig. 7 shows the simulated transfer characteristics at 2 GHz as a function of input power. The output power and efficiency

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at compression are consistent with theoretical expectations for the FETs operated from a 3.6 V supply voltage. Other simulations showed that the gain is flat over 500 MHz or 25 % bandwidth and even harmonic suppression is obtained.

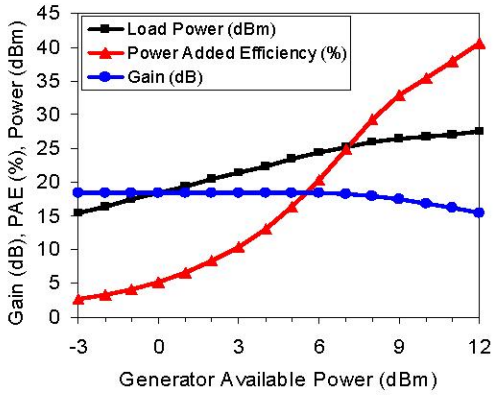

Fig. 7. Simulated large-signal transfer characteristics as a function of input generator power for the 4-FET power amplifier at 2 GHz

The input power divider and output combiner comprise transmission lines and artificial transmission line methods can be used to reduce size, fill the space of loops, and absorb FET input and output capacitances [22].

V. Conclusion

In this paper we have examined combined power amplifiers that integrate the input divider and output combiner functions as part of the amplifier circuit thereby obviating the need for extra power dividers and interconnecting lines. These amplifiers were the: (i) dual-fed distributed amplifier, and (ii) a new type of amplifier that comprises a periodic loop combining structure. Both amplifiers have a longitudinal length independent of N the number of transistors to be combined. Their composition makes them amenable to miniaturization using artificial transmission line methods which can be used to absorb transistor input and output capacitances into the divider and combiner structures. In both cases, even harmonic suppression occurs. The load presented to the transistors is proportional to N for the dual-fed distributed amplifier, and inversely proportional to N for the proposed amplifier. The former amplifier is evolved whist further investigations are needed for the later amplifier.

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