Power Electronic Control of a Partial Core Transformer

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Abstract

The research programme at the University of Canterbury includes the development and applications of partial core inductors and transformers for high voltage testing of generator insulation. Unlike a conventional full core transformer, a partial core transformer has no limbs and yokes. A partial core transformer is a compromise between a full core and coreless transformer. It is superior to its full core counterpart as far as cost, weight and ease of transportation are concerned.

Partial core transformers have a low magnetising reactance and hence draw a high magnetising current. This characteristic makes them a perfect fit in applications where the load is capacitive in nature, such as a.c. power frequency high voltage testing of generator insulation and cable testing etc.

The work carried out for this thesis focuses on automatically controlling the amount of reactive power on the supply side of a partial core transformer. The considered design includes a third winding around the existing two windings. A power electronic controller is connected to the third winding, which modifies the VAr absorption characteristics of the magnetically coupled supply winding.

Two options are considered to achieve continuous reactive power control in the partial core transformer as explained below.

First, a thyristor controlled reactor (TCR) is proposed as the VAr controller. It is modelled using PSCAD/EMTDC software. Simulations reveal the design criteria, overall performance and the limitations of the suggested proposal. The TCR connected tertiary winding takes the capacitive burden of the supply. The model demonstrates the ability of the automatically controlled TCR to provide a continuous

variation of reactive power without significant under or over compensation. This feature limits the supply current to its real component only, so the supply provides only the losses of the system.

Second, a voltage source converter is considered as the VAr controller. This is modelled in PSCAD/EMTDC and a hardware prototype is designed and built. Based on the analysis, the control algorithm (including a digital PI controller) is implemented using an 8 bit micro-controller, PIC18LF4680. The prototype is tested in the laboratory for both active and inductive load conditions as seen from the supply side. Performance of the hardware prototype is discussed in detail.

The PSCAD/EMTDC model and the hardware prototype successfully demonstrate the feasibility of a STATCOM controlled partial core transformer. The proposed system is capable of compensating a wide range of capacitive loads as compared with its TCR counterpart.

It is proved that the system is very robust and remains dynamically stable for a large system disturbance such as change in load from full capacitive to inductive and vice versa[1]. This confirms that the system is capable of providing continuous VAr control.

[1] As seen by the STATCOM

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Technical papers published during Master of Engineering

- Vijay Bendre, Pat Bodger, Alan Wood, "**Towards a practical partial core transformer - compensation of reactive power requirements with a VSC**," the IASTED International Conference on Power and Energy Systems, Botswana, Africa, September 8-10, 2008.

- Vijay Bendre, Wade Enright, Simon Bell, Pat Bodger, "**Field Experiences Using a Prototype Open Core Resonating Transformer for A.c. High Potential Testing of Hydro-generator Stators**," TechCon 2008, Sydney, Australia, 1-2 April 2008.

- Pat Bodger, Wade Enright, Simon Bell, Vijay Bendre, "**Partial Core Transformers for HV Testing and Power Supplies,**" TechCon 2008, Sydney, Australia, 1-2 April, 2008.

- Vijay Bendre, Wade Enright, Simon Bell, Pat Bodger, "**A.c. High Potential Testing of Large Hydro-generator Stators Using Open Core Transformers,**" 15th International High Voltage Symposium, Slovenia, August 27-31, 2007.

- Vijay Bendre, Pat Bodger, Alan Wood, "**Thyristor Controlled Three Winding Transformer as a Static VAr Compensator,**" presented at EEA-2007 conference, Auckland, June 15-16, 2007.

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Chapter 1

Introduction

1.1 A full core transformer

A transformer is a stationary apparatus which transforms electric power in one circuit into electric power of the same frequency in another circuit at a different voltage [1]. A conventional single phase power transformer has two windings separated electrically but linked magnetically by a path of low reluctance i.e. through a closed or full core of ferromagnetic material, as shown in Figure 1.1. Generation of a high core flux density using a relatively low magnetising current is possible because of the high permeability of the ferromagnetic core. Transformer designs with high voltages per turn for the windings are possible due to the ferromagnetic core, which minimises the lengths of the winding material used and hence lowers the copper losses [2]. These features cannot be accomplished in a cost effective, light weight, coreless transformer. The percentage magnetising current in a coreless transformer is a much higher percentage of its total current rating.

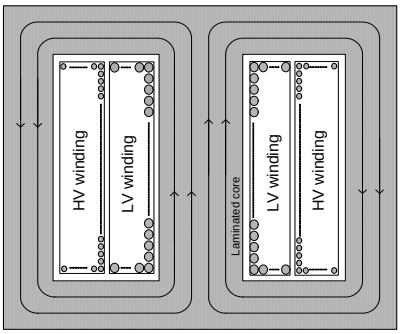


Figure 1.1: A full core transformer

1.2 Introduction to a partial core transformer

A compromise between a full core and coreless transformer is a partial core transformer. It consists of a laminated ferromagnetic central core around which the primary and the secondary windings are wound. The outer limbs and the yokes are absent as shown in figure 1.2.

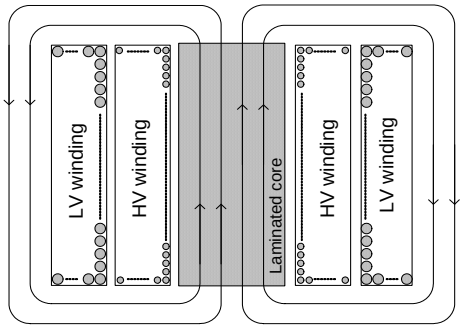


Figure 1.2: A partial core transformer

Partial core transformers have different characteristics from full core transformers as the flux path is a combination of steel and air. Keeping all other parameters constant such as supply voltage, cross sectional area and number of turns on the excitation, the theoretical flux density is the same for both a full core and a partial core transformer. In the case of a partial core transformer, the flux path reluctance is much higher, leading to a lower magnetising reactance and higher magnetising current. However, it has better magnetisation than a coreless transformer and maintains the leakage flux at an acceptable level. This also means that the overall weight and volume of the partial core units can be significantly reduced. They are also easy to manufacture [3, 4].

1.2.1 High voltage partial core resonant transformer

Partial core transformers are better suited to applications such as supplying capacitive loads, and/or where factors such as cost, size and ease of transportation are critical. Since 2002, the University of Canterbury has designed, built and

developed partial core transformers [5-8]. One of the most significant results is the development of a high voltage (HV) partial core resonating transformer for a.c. power frequency testing of a hydro-generator.

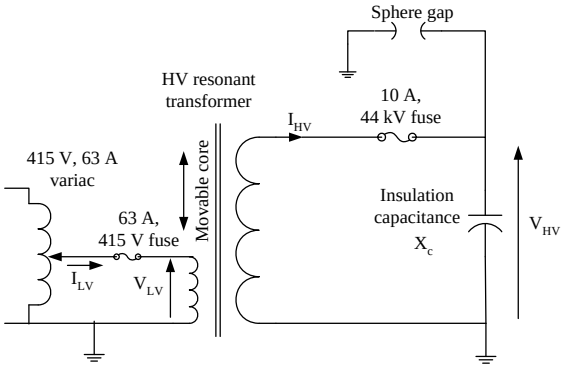


Figure 1.3: Circuit diagram for performing HV power frequency test with only a HV partial core resonating transformer

Figure 1.3, shows the circuit diagram for performing an a.c. high potential test at power frequency by a high voltage partial core resonant transformer. In order to limit the supply current to its real component only, the generator insulation capacitance (X_c) is resonated with the magnetizing reactance (X_m) of the partial core transformer by manually adjusting its central core. Figure 1.4 shows a light utility vehicle transporting the HV partial core resonating transformer. Many of the hydro-generators in the South Island of New Zealand have been tested by using this transformer [9, 10].

Figure 1.4: A light utility vehicle transporting the dry type partial core resonating HV transformer

1.3 Research objectives

Manual position adjustment of the core has some limitations due to the involvement of large magnetic forces, necessary proximity of the operator to the high voltage and the possibility of under or over compensation. In order to overcome these problems, there is a need for a means of continuous control of reactive power.

With this objective, a third winding is proposed around the already existing two windings, along the direction of the main field flux. Due to magnetic coupling, an e.m.f. will be generated in the third winding. A controller can be put on the third winding which is responsible for modifying the VAr absorption characteristics of that winding for compensating the capacitive VArs required by the HV winding [11]. This will limit the supply current. Two independent strategies have been proposed for limiting the magnitude of current drawn from the supply side, namely

1. Applying a thyristor controlled static VAr compensator to the third transformer winding.

2. Applying a single phase voltage source converter (VSC) based static compensator (STATCOM) to the third transformer winding.

The first proposed scheme works only if a load seen by the supply side is capacitive in nature. Application of a switched capacitor bank may need a.c. capacitors with a large energy storage capacity, which are expensive and bulky. This option does not offer continuous VAr control. A VSC based STATCOM overcomes limitations of both the VAr compensating schemes. These converters are able to use electrolytic capacitors, this is a much cheaper and cost effective option rather than going for a.c. capacitors. A VSC based STATCOM provides both capacitive and inductive VArs. This enables a range of loads to be compensated by the system. A partial core transformer can be used like a full core transformer with the employment of the

second strategy, although significant current will be required to flow in the third transformer winding.

1.4 Outline of the thesis

The performance of a TCR application to a three winding partial core transformer is evaluated by simulating the proposed scheme using PSCAD/EMTDC software. Hardware prototype of a single phase VSC based STATCOM is designed, built and tested in the laboratory for evaluating its performance.

Chapter 2 describes previous work carried out on partial core machinery in the University of Canterbury. The partial core machines designed, developed and built for applications such as high voltage resonant inductor and transformer for a.c. power frequency high voltage testing of a generator insulation, high current transformer for testing current transformers, high temperature superconducting transformer etc.

Chapter 3 introduces the thyristor controlled three winding transformer. Parameters of the selected single phase three winding transformer are determined by performing open and short circuit tests on it. The system is modelled and simulated using PSCAD/EMTDC software for evaluating its performance and limitations.

Chapter 4 covers the theory, modelling, analysis and design of a single phase VSC based STATCOM. The chapter also illustrates the design criteria for implementing a proportional- integral (PI) based closed loop automatic control system. The scheme is modelled in PSCAD/EMTDC software for verifying dynamic as well as steady state performance of the system.

Chapter 5 describes the development of the controller board built to implement the proposed automatic control system. The hardware and methodology used for the accurate measurement of the reactive component of the supply current is presented.

Chapter 6 explains the design and development of the power circuit. The power circuit consists of an IGBT based 'H' bridge inverter, driver circuits, snubber circuit, a current limiting series inductor to be inserted in the tertiary winding, a capacitor on the d.c. side of the VSC etc.

Chapter 7 explains the control algorithm developed for programming the micro-controller, PIC18LF4680. The micro-controller is responsible for generation of a sinusoidal pulse width modulated waveform (SPWM) and synchronising it with the supply voltage waveform, data acquisition, A/D conversion, performing the mathematical operations, and shifting the SPWM waveform earlier or later with respect to the supply voltage waveform to achieve the required VAr compensation on the supply side.

Chapter 8 demonstrates the performance of the prototype built for a range of load conditions.

Chapter 9 presents conclusions drawn from the research effort and discusses possible future work related to both the schemes proposed.

Chapter 2

Previous work on partial core systems

2.1 Overview

In the previous chapter, the partial core transformer was introduced. This chapter describes the previous work carried out at the University of Canterbury in the area of partial core machinery.

2.2 Research carried out on partial core transformers

2.2.1 Generator Insulation Testing

2.2.1.1 Overview of high potential tests

When generator stators are rewound or undergo major repairs, there is often a desire to perform a high potential test. These tests can be completed using d.c., very low frequency or power frequency a.c. test voltages. A.c. high potential tests are becoming more popular due to their superiority in many aspects over the alternatives. A.c. high-potential testing stresses the components of generator insulation in a manner more similar to normal service, except at higher a.c. voltages and in a non-induced or non-graded manner. Under a.c. conditions the amount of current drawn by the insulation capacitance depends in part on the physical dimensions of the stator winding.

As shown in Table 2.1, some of the hydro-generators in New Zealand have large values of stator insulation capacitance.

Table 2.1: Hydro-generators tested in New Zealand with their insulation capacitances

Generator rating	Test voltage kV	Insulation capacitance µF	Calculated kVAr	Calculated charging current at 230 V[1] A
2.35 MVA, 6.6 kV	14.2	0.084	5.32	23
8.82 MVA, 6.6 kV	14.2	0.217	13.8	60
55.55 MVA, 11 kV	13.8	0.234	14	61
88.9 MVA, 11 kV	23	0.422	70.1	305
120 MVA, 15.4 kV	20	0.75	94.2	409
40 MVA, 11 kV	23	0.57	94.7	412
135 MVA, 13.8 kV	32	1.05	338	1468

In most of the cases, the charging current required cannot be supplied by the power station local services without compensation. To overcome this problem, resonant systems are most popular among companies offering HV test equipment. Series and parallel resonant test systems are common for a.c. high-potential tests on generator insulation, so that under resonant conditions the energy absorbed at any instant by one reactive element is exactly equal to that released by another reactive element within the system. This self sustaining resonant system requires much less current from the power station distribution board.

Most of the expensive and heavy resonant testing systems employ full core electromagnetic machinery such as double shielded isolation transformers, voltage regulators, excitation transformers and high voltage reactors. Such machines can reach multiple tons in mass. Transportation of this heavy equipment is also expensive, especially when a hydro-generator is located remotely. These difficulties can discourage generator owners and force them to undertake a d.c. test. Some of the companies try to optimize size and weight considerations by increasing the frequency of the supply from d.c. to Very Low Frequency (V.L.F.), but this technique suffers from many of the criticisms already noted for the d.c. test [10].

[1] Charging current without considering any losses and assuming an ideal HV transformer ratio

2.2.1.2 Resonant Inductor

In 2002, a partial core HV inductor was designed and built in order to perform an a.c. high-potential test on a 40 MVA, 11 kV North Island hydro-electric power station generator. As shown in figure 2.1, the partial core inductor was connected in parallel with the generator insulation. The generator insulation capacitance can be resonated with the inductive reactance of the partial core inductor by using taps provided [9]. The final high potential test of the generator was conducted at 23 kV for one minute. The test set up is shown in figure 2.2.

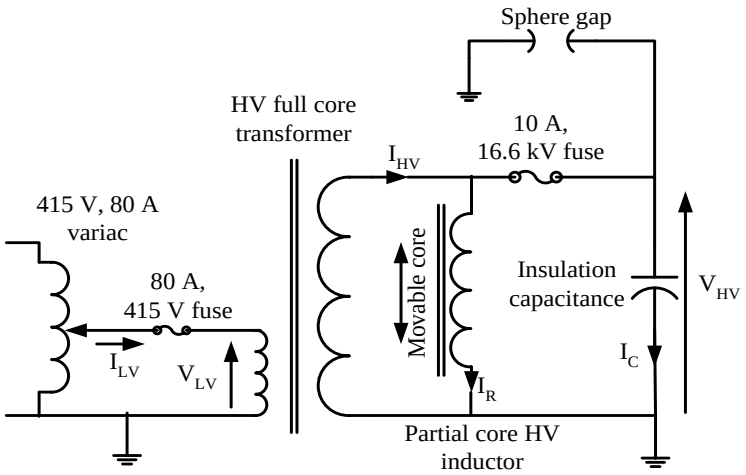


Figure 2.1: Circuit diagram for performing HV power frequency test with a partial core resonating inductor

The generator stator insulation was measured at 0.56 μF which corresponds to 5700 Ω. Under test, the stator insulation drew 4.1 A at 23 kV. The partial core resonant inductor actually over compensated the stator capacitance.

The supply current was reduced to 0.75 A, considerably below that which would have been necessary without the inductor in circuit. Thus a VA gain of 5.5 from the supply to the load was obtained. VA gain can be defined as the ratio of apparent power (VA) available on the output side of a transformer to the input VA supplied.

This permitted the use of a lower VA rating HV test supply transformer and variac, with smaller supply station and protection concerns [3].

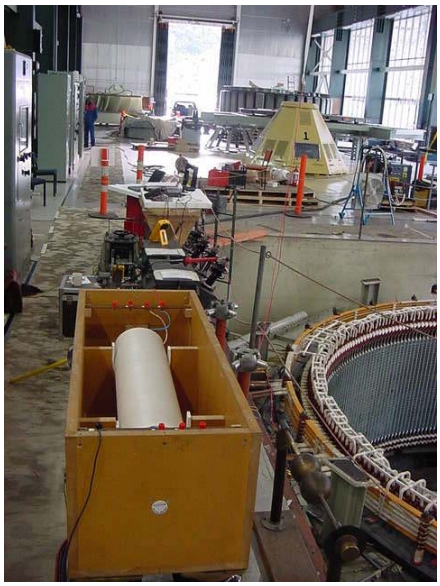


Figure 2.2: Test location for the partial core resonant inductor

2.2.1.3 HV Partial core resonating transformer

In the case of a conventional transformer, the LV winding is wound on the inside next to the core, to reduce its length and hence the copper losses due to its relatively high current. A partial core resonant transformer has the LV wound around the HV winding. The LV winding acts a shield and prevents the HV winding from electric field coupling to grounds external to the transformer and thus the probability of corona from the windings is significantly reduced [3].

A HV partial core resonating transformer was first applied to test a 135 MVA, 13.8 kV hydro electric power station in the South Island of New Zealand. It was designed for a 334 kVAr capacitor load to perform the power frequency high voltage test at 31.5 kV. In practice, the resonant transformer used was to supply 36.5 kV to an initial batch of installed stator bars at 0.49 μF, which is equal to a capacitive load of 205 kVAr. Under flashover situations, the transformer proved its electrical and mechanical integrity.

In a follow up test, it is required to test each complete phase of the generator stator of 1.06 μF at 32 kV for one minute. The resonant inductor described in 2.1.2 was inserted in parallel with the resonant transformer. This high voltage testing assembly, as shown in figure 2.3, achieved a resonance of 340 kVA while drawing only 70 A from a single phase 415 V supply. The output to supply VA ratio was 11 [3].

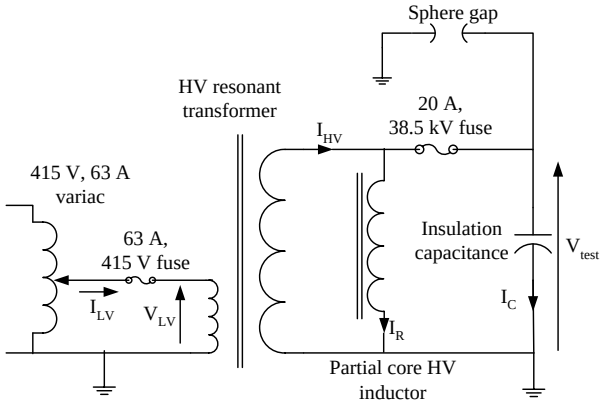


Figure 2.3: Complete stator phase test with HV resonant transformer and inductor, both designed using partial core technology

Many of the hydro-generators in New Zealand were successfully tested with this compact HV resonant testing kit which weighs approximately 300 kg [3-5]. This has replaced a full core HV resonant testing kit weighing around 6 tonnes as shown in Figure 2.4.

Figure 2.4: Partial core HV resonant transformer in front of conventional full core high voltage testing kit (full core excitation transformer and inductors)

2.2.2 High Current Transformer

Primary current injection is employed for testing current transformers and related equipment on power transmission and distribution metering and protection systems. Traditional high current transformers are bulky and heavy, hence they have limitations on the locations they can be placed in. This results in extra secondary cable lengths. With the low voltage, high current output characteristic of these transformers, the voltage drop in the cable is usually the limiting factor of the output current. A compact, lighter transformer can be placed close to the equipment under test, decreasing the effect of cable voltage drop, which results in the availability of higher current.

As shown in figure 2.5, a partial core high current transformer was designed and built for the purpose [8]. It weighted 39 kg. It is suitable for 4000 A continuously or 11000 A peak. Although the continuous rating met the specifications of a conventional transformer used for the purpose (weighing 147 kg), the peak current was limited due to excessive eddy current heating at the terminals of the secondary winding. The heating problem may be solved by laminating these terminations [3].

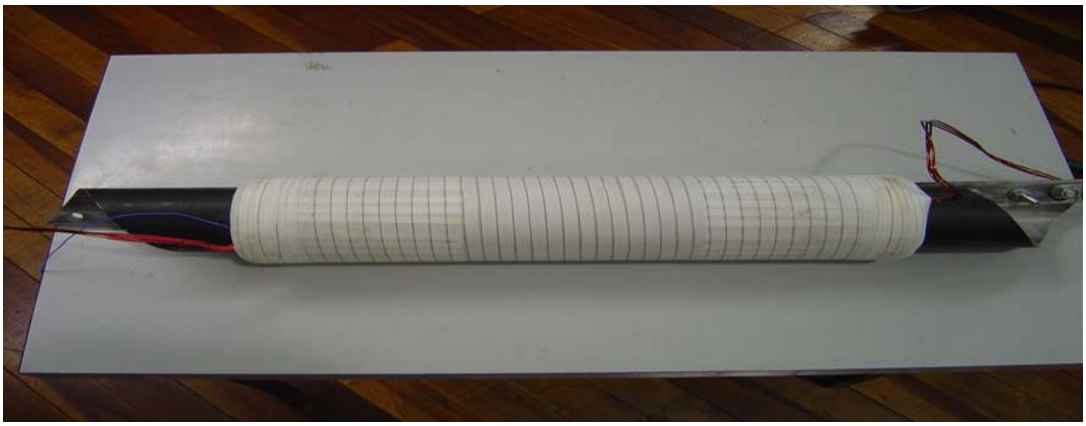


Figure 2.5: High current test transformer

2.2.3 High Temperature Superconducting (HTS) Transformer

A prototype of a single phase, 15 kVA, 230/115 V, partial core HTS transformer was designed and built. The rated primary current for the transformer is 65.22 A.

The typical first generation HTS tape from American Superconductors has cross sectional dimensions of 4.1 mm by 0.305 mm. This means the effective tape area is 1.25 mm^2. This gives the current density of 52.15 A/mm^2. It has a minimum bend radius of 70mm.

The construction of the transformer was such that the core operates at normal temperatures while the windings were immersed in liquid nitrogen. The complete assembly was placed inside a double skinned/vacuum or permulite composite tank that provided insulation to the outside. The ends of the three windings made were accessible to allow variable location of the primary and secondary windings, and also to allow alternative two winding and autotransformer configurations.

The winding terminals were connected to the copper leads and brought out to terminals through a gaseous nitrogen headspace which cooled the leads. This reduced the conduction of heat from the outside into the liquid nitrogen [3]. The transformer is shown in figure 2.6.

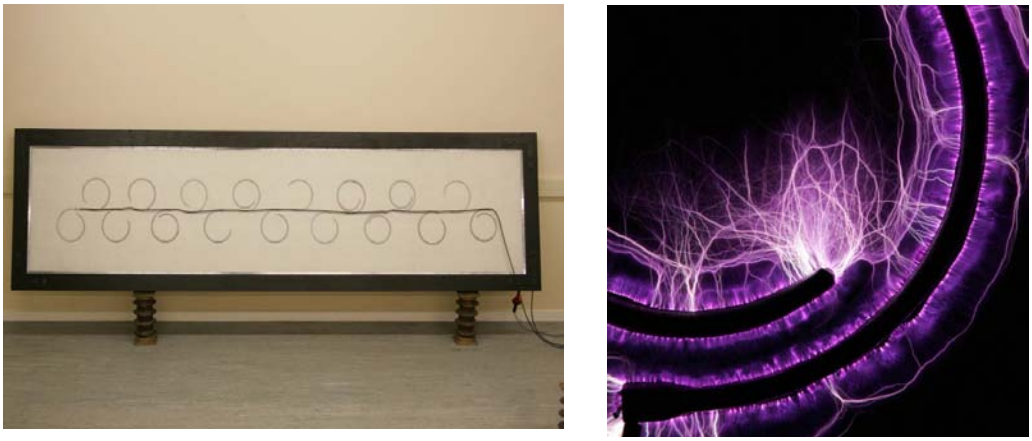
Figure 2.6: A prototype of a partial core high temperature superconducting transformer

2.2.4 Energization of high voltage arc-signs

A collaborative study between the Departments' of Electrical and Computer Engineering and Fine Arts at the University of Canterbury has developed lightning arc drawings or "arc signs". These arc-signs require a high voltage to obtain their arcing effect. Figure 2.7(a), shows the basic arrangement of an arc-sign [12].

The configuration consists of a top electrode which forms the design, a sheet of insulating film (NMN 5-10-5), and a thin sheet of conductor which forms the bottom electrode. The arc sign is a parallel plate capacitor of very small value.

At rated voltage, power arcs appear on the surface of the sign. The power supply gets short circuited, although when the power arcs are being formed on the sign's surface, very little real power is dissipated.



(a) De-energized **(b) Energized (close-up)**

Figure 2.7: The arc sign showing the top electrode and insulation layer

The partial core transformer designed for this purpose consists of two separate LV windings wound onto the outside of the HV winding. The two windings are connected in series by an external link to give the very high turns ratio required for an output voltage of 80 kV from a 230 V supply. The completed transformer along with the core weighs 69 kg. Figure 2.8 shows a photo of the transformer and its mounting arrangement.

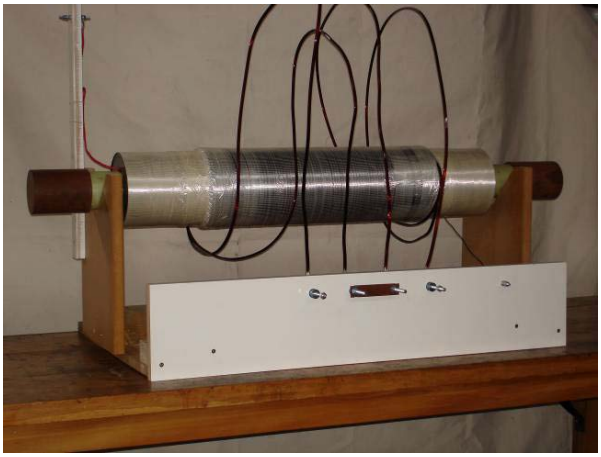


Figure 2.8: 80 kV Transformer

Figure 2.7(b), shows one of the arc signs loaded by the transformer. The arc sign has a de-energized capacitance of 7 nF, corresponding to 450 Ω of capacitive load reactance, or 3.32 Ω when referred to the primary winding of the transformer.

The transformer can also be employed for flashing sphere gaps used for high voltage testing protection.

2.3 Summary

A partial core transformer is a compromise between a full core and coreless transformer. It is superior to its full core counterpart as far as cost, weight and ease of manufacturing and transportation are concerned. A number of partial core inductors and transformers have been designed, developed and built. The lower magnetising reactance of a partial core transformer, with a capability of adjusting its magnitude, makes the partial core transformer a perfect fit for applications where loads are capacitive, such as a.c. power frequency high voltage testing of generator insulation. The generator stator insulation capacitance is resonated with the transformer magnetising reactance by adjusting the position of transformer's central core. This effectively eliminates the reactive power demand from the main power supply. Only the real power losses of the transformer, and any mismatch between the magnetisation current and the stator capacitance, are provided from the supply. A number of hydro-generators in New Zealand have been tested successfully with the partial core high voltage testing kit.

A high current partial core transformer was designed which can be used for testing current transformers. It can provide a continuous current of 4000 A.

The performance of a partial core high temperature superconducting transformer immersed in liquid nitrogen was evaluated. The superconducting transformer shows a very high magnetic flux coupling between the windings and a reduced percentage of leakage flux. This supports the possibility of real power transfer using partial core technology.

For displaying power arc-signs, a single phase, 80 kV partial core transformer was designed and built. This transformer operates near to an open circuit condition. It can be used to flash spheres for HV testing protection.

Chapter 3

A thyristor controlled three winding transformer as a static VAr compensator

3.1 Overview

In chapter 2, a number of partial core transformers and their applications were discussed. This chapter describes a thyristor controlled three winding partial core transformer for controlling the amount of reactive power in the supply winding.

3.2 Thyristor-Controlled Reactor (TCR)

A basic single-phase thyristor-controlled reactor (TCR) is shown in Figure 3.1. It consists of a bi-directional thyristor valve and a fixed inductance L of reactance X_L. The fine tuning is achieved by varying the TCR firing delay angle (α). The controllable range of α extends from 90^o to 180^o. A firing angle of 90^o results in full thyristor conduction with a continuous sinusoidal current (i_{TCR}) flowing through the TCR. As the firing angle is varied towards 180^o, the current flows through the reactor (X_L) in the form of discontinuous pulses symmetrically located in the positive and negative half cycles [13].

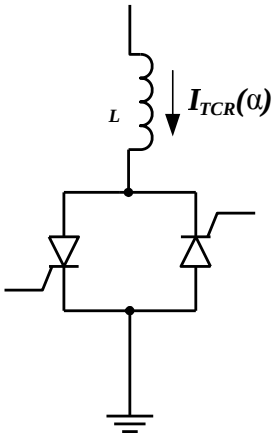


Figure 3.1: Thyristor controlled reactor

The firing angle is derived from the conduction angle equation in [14]. A relationship between the firing delay angle and the TCR reactance (X_{TCR}) is given in equation 3.1.

$$X_{TCR} = \left(\frac{2[(\pi - \alpha)] + sin2\alpha}{\pi\omega L}\right)^{-1} \quad (3.1)$$

Equation 3.2, gives the range of reactance values which can be obtained from the TCR.

$$X_L \leq X_{TCR} \leq \infty \quad (3.2)$$

3.3 Parameters of a single phase three winding transformer

An available partial core, three winding transformer was chosen on which to perform experiments, and simulations using the PSCAD/EMTDC software package. The transformer has ratings of 2.52 kVA, 90/345/90 V, and 50 Hz. In order to determine its parameters, short circuit and open circuit tests were performed on all the three windings. These parameters are presented in Table 3.1. Mathematical modelling of a three winding transformer can be found in [15].

Table 3.1 Electrical characteristics of the chosen partial core three winding transformer

Parameter	Value	Unit
Rated winding currents	28/7.30/28	A
Short circuit impedances (All values are referred to the primary/supply winding)	Z_{ps} = 0.296 + 0.308 j	Ω
	Z_{st} = 0.317 + 0.271 j	Ω
	Z_{pt} = 0.508 + 0.024 j	Ω
Magnetising reactance (X_m)	16.2	mH
No load loss component	73	Ω

Where, p, s and t denote the primary (supply), secondary (high voltage), and tertiary (control) windings respectively.

- Z_{ps} is the winding resistance and leakage inductance measured in the primary winding when the secondary winding is short circuited and the tertiary winding is kept open.
- Z_{st} is the winding resistance and leakage inductance measured in the secondary winding when the tertiary winding is short circuited and the primary winding is kept open.
- Z_{pt} is the winding resistance and leakage inductance measured in the tertiary winding when the primary winding is short circuited and the secondary winding is kept open.

3.4 Concept of thyristor controlled three winding transformer

As shown in Figure. 3.2, the tertiary winding of the three winding transformer is closed through an anti-parallel connected pair of thyristor valves. If the leakage reactance ($X_{leakage}$) of this transformer is not high enough, an additional current limiting reactor (X_L) in the tertiary winding is essential. In Fig. 3.2, X_{TCR} represents ($X_{leakage} + X_L$)*.

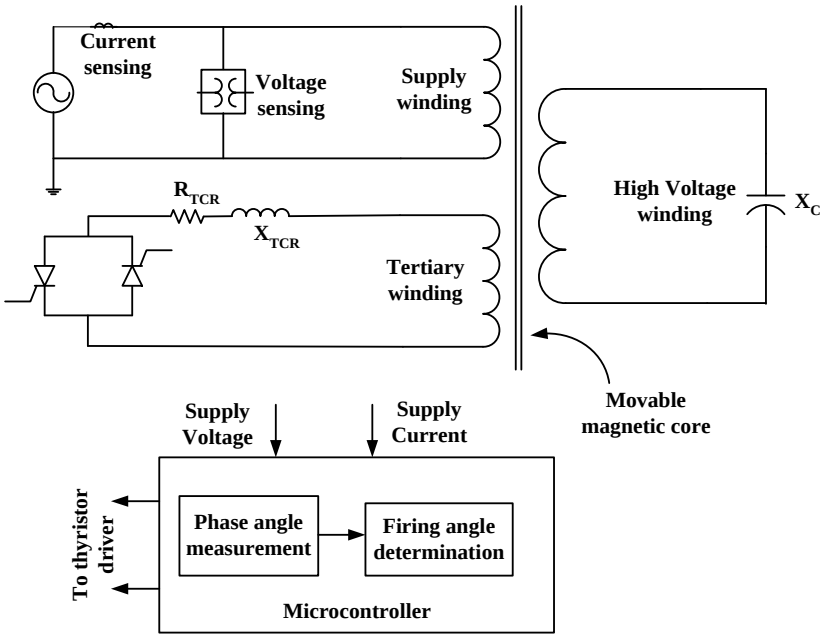


Figure 3.2: Proposed thyristor controlled scheme for partial core three winding resonant transformer

* In actual case, the value of $X_{leakage}$ in the tertiary winding was very low as stated in equation 3.6.

X_L is also essential for reducing the magnitude of harmonics that are not only detrimental to the test object and the transformer itself, but also an a.c. high potential test with polluted supply, may not be accepted as per standards.

Firing angle control of these thyristor valves provides a continuous variation of reactive power. R_{TCR} represents the internal resistance of the TCR when one of the thyristors is conducting. X_C denotes a capacitive load, e.g. generator insulation capacitance.

Automatic control of the TCR controlled three winding transformer can be achieved by using a compatible micro-controller [16]. Inputs to the micro-controller are the supply voltage and current waveforms.

3.5 Design value for series reactor (X_L)

The current rating of the tertiary winding is 28 A, while the voltage rating, *V,* is 90 V. The value of the series reactor, X_L, is calculated using equation 3.3 as 3.2 Ω. It was decided to operate the TCR at 85% of the full load current. This corresponds to an inductance value, *L,* of 12 mH.

$$X_L = -j\frac{V}{I_{TCR}} \tag{3.3}$$

3.6 Modelling in PSCAD/EMTDC

A basic model of a thyristor controlled three winding transformer as a SVC is shown in Figure 3.3. It implemented in PSCAD/EMTDC software. Equations for determining the values of the winding resistance and leakage reactance of the individual windings are derived in [15]. These equations are given as,

$$Z_p = \frac{1}{2}\left[Z_{ps} + Z_{pt} - Z_{st}\right] = \left(0.245 + 0.0305i\right)\Omega \tag{3.4}$$

$$Z_s = \frac{1}{2}\left[Z_{ps} + Z_{st} - Z_{pt}\right] = \left(0.7721 + 0.277i\right)\Omega^{\dagger} \tag{3.5}$$

$$Z_t = \frac{1}{2}\left[Z_{pt} + Z_{st} - Z_{ps}\right] = \left(0.265 - 0.00628i\right)\Omega \tag{3.6}$$

It can be observed that the tertiary winding short circuit reactance has a negative value. This characteristic is discussed in [17]. The three winding transformer model block set available in the PSCAD/EMTDC library, is treated as an ideal one with no saturation.

Values of resistance and self inductance for each winding can be calculated by using equations 3.4 to 3.6. Both open and short circuit parameters are connected externally to the terminals of the ideal three winding transformer model as shown in Figure 3.3.

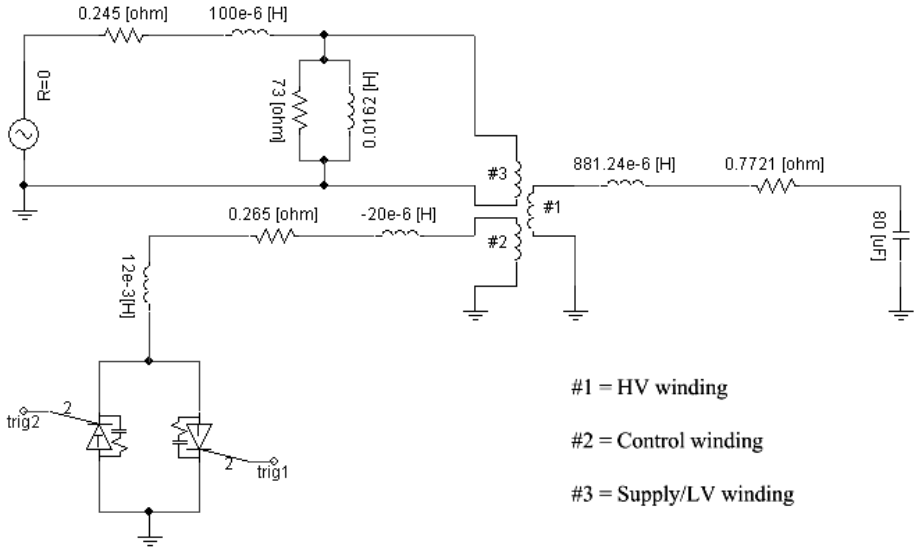


Figure 3.3: A model of the thyristor controlled three winding transformer in PSCAD/EMTDC

In order to identify the main characteristics of the TCR controlled three winding transformer, at first the amount of reactive power in the tertiary winding as a function of α is determined, as shown in Figure 3.4. The firing signals for the thyristor valves are derived from a voltage controlled oscillator (VCO). It generates a 0 to 360 degree ramp function waveform, repeating at a frequency of

† Calculated corresponding to the high voltage winding

50 Hz. This waveform is used as a reference for determining the firing delay angle, α. At α = 180^o, the tertiary winding behaves like an open circuit.

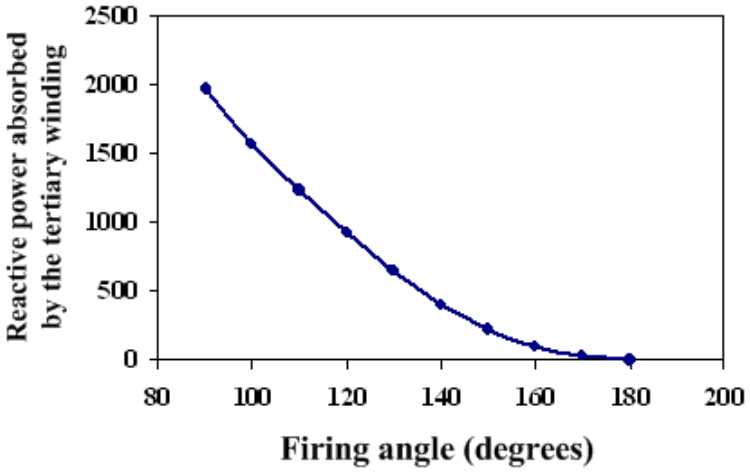


Figure 3.4: Behaviour of reactive power (in VAr) in the tertiary winding with respect to firing angle, α

As α is reduced gradually, more and more inductive reactive power is absorbed by the tertiary winding. When α = 90°, i.e. the thyristor valves are completely closed, the reactive power absorbed by the tertiary winding is 1968 VAr. The core supplies 1590 VArs (lagging) at 90 V. This indicates that theoretically the system in total is capable of absorbing 3558 VAr without drawing any VArs from the supply side.

3.7 Automatic control

The actual application requires the TCR to be controlled in a closed loop fashion. As shown in Figure 3.5, the reactive power is measured in the LV winding and is compared with the reference. The error signal is then processed by a PI controller that generates the appropriate firing angle levels. Before firing signals are sent to the interpolated signal generators, the output of the PI controller is converted to angle units and properly conditioned to keep the angle within the limits, i.e. 90^o ≤ α ≤ 180^o. These angle units are then compared against the saw tooth waveforms generated by the VCO and firing signals to be fed to the thyristor valves are generated.

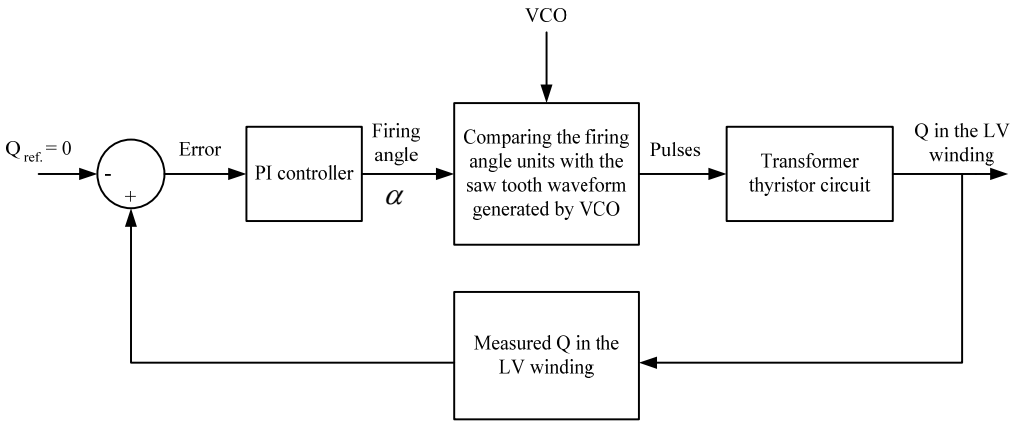


Figure 3.5: Automatic control strategy implemented in PSCAD/EMTDC

3.7.1 Behaviour of reactive power in all the three windings

A capacitive load of 2470 VAr is connected to the terminals of the high voltage winding. The transformer is supplied with a rated voltage i.e. 90 V. In order to demonstrate the effectiveness and accuracy offered by the proposed system, initially, the circuit breaker in the tertiary winding is kept open and the total reactive power required by a capacitive load on the high voltage side is supplied by the core and the supply. At 1 sec, the circuit breaker is closed and the TCR starts operating. The initial value of the firing angle is 180^{o}.

The TCR firing angle starts reducing and increasing its conductivity. Initially, 952 VArs are drawn from the supply while remaining VArs are supplied by the core. As more and more reactive power is absorbed by the tertiary winding, the requirement of reactive power from the supply gets dropped. At a steady state condition at which $\alpha = 113.6°$, negligible reactive power is drawn from the supply. Figure 3.6 demonstrates the behaviour of reactive power in the three windings.

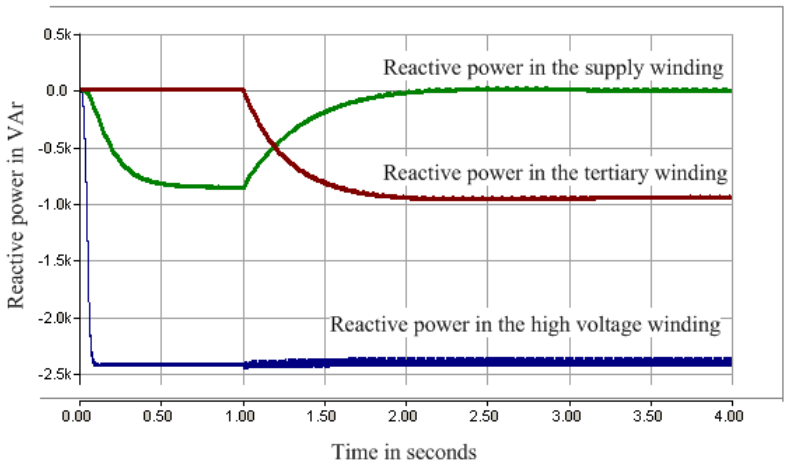


Figure 3.6: Behaviour of reactive power in all the three windings

3.7.2 Behaviour of currents in the three windings

After application of the TCR, the current in the supply winding dropped from 9.8 A to 4.3 A, of which the fundamental component accounts for 2.54 A. Total reactive current is provided by the tertiary winding. As shown in Figure 3.7, in addition to fundamental components, the TCR generates harmonics. The total harmonic distortion is dominant in the middle range of firing angle. As positive and negative current cycles are identical, only odd ordered harmonics are generated. As shown in equation 3.7, the amplitudes of these harmonics are a function of firing angle, α.

$$I_{TCR}(\alpha) = \frac{4}{\pi}\frac{V}{\omega L}\left\{\frac{sin\alpha\cos(n\alpha) - ncos\alpha\sin(n\alpha)}{n(n^2-1)}\right\} \qquad (3.7)$$

where, $n = 2k+1,\ k = 1,\ 2,\ 3,\ ...$

As the supply winding is magnetically coupled with the TCR controlled tertiary winding, the supply current also gets injected with harmonics. Total harmonic distortion (THD) in the currents in the supply, tertiary and high voltage windings is 138 %, 32% and 4% respectively. The current in the high voltage winding remains considerably unaffected by harmonics due to its higher inherent self inductance. Unlike three phase systems where harmonics can be reduced by

circuit arrangements, harmonics in the single phase system must be reduced by employing filters [18].

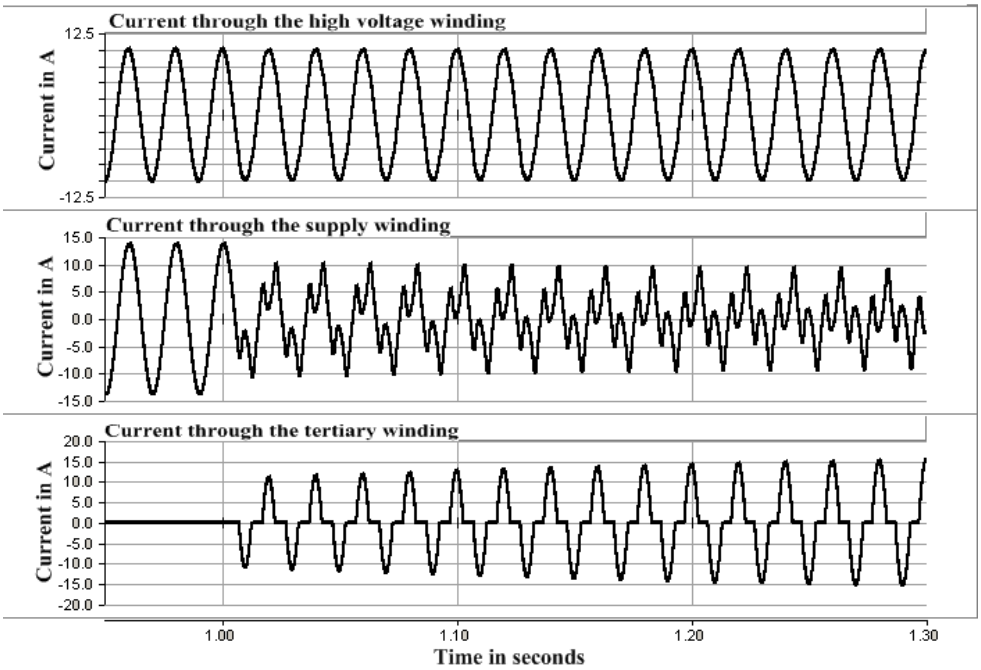


Figure 3.7: Current waveforms in all the three windings

3.7.3 Behaviour of voltage in all three windings

Figure 3.8, shows the voltage waveforms across the terminals of all windings and series reactor X_L at $\alpha = 113.6°$. Considering the voltage supply is an ideal one, the higher value of series reactor in the tertiary winding prevents pollution of voltage waveforms in the remaining two windings.

3.7.4 VA gain

After application of the TCR, VA gain from the supply to load is 2.27. As the load increases, TCR branch absorbs more and more reactive power and hence VA gain increases. VA gains for other capacitive loads with respect to the firing angle, α, are demonstrated in Figure 3.9.

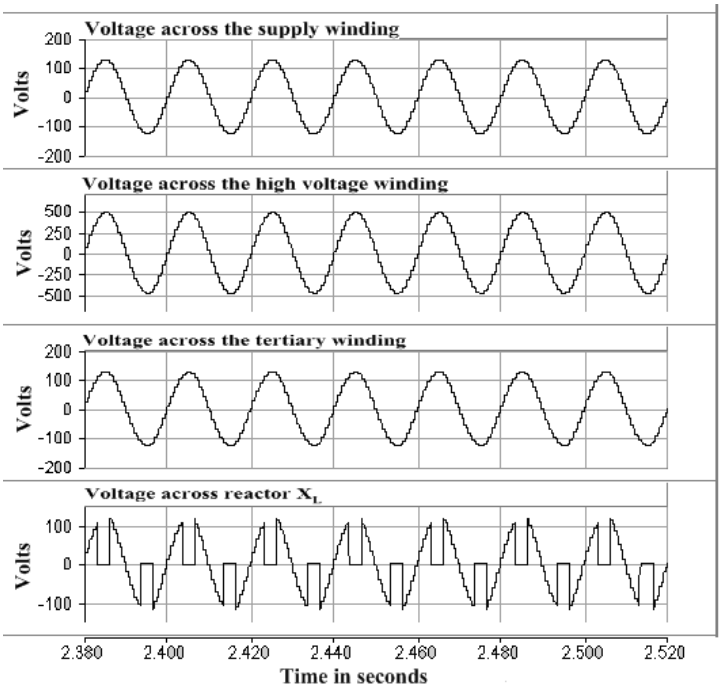


Figure 3.8: Voltage waveforms in all the three windings

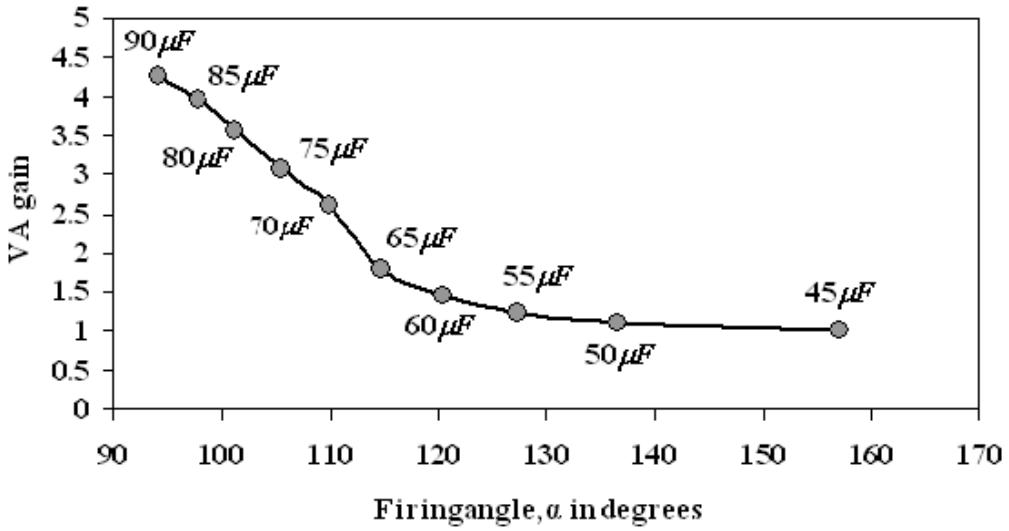


Figure 3.9: VA gain from the supply to load with respect to firing angle, α

3.7.5 Real power

There is an increase in amount of real power losses from 170 W to 215 W due to the resistance in the tertiary winding and the TCR branch. Harmonics generated by the TCR branch also cause significant real power losses. For other capacitive

loads, as show in Figure 3.10, after application of the TCR, the system draws more real power from the supply side.

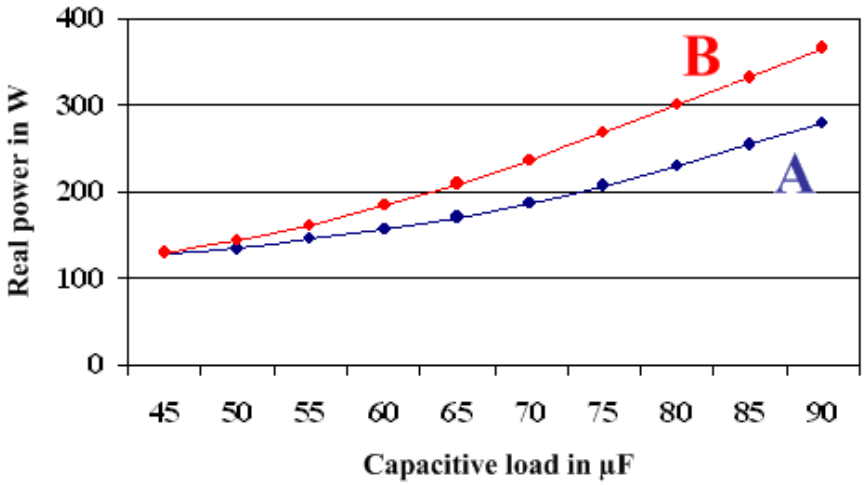


Figure 3.10: Real power losses at various capacitive loads, before (curve A) and after (curve B) application of the TCR

Simulation results for other sizes of capacitive loads are given in table 3.2.

3.8 Limitations of TCR application

1. This method is only applicable for the capacitive loads which generate VArs more than the minimum that the partial core transformer can absorb, in this case, $1591 \leq X_C \leq 3330 \mu F$, otherwise the system would either under or overcompensate.

2. In order to operate such a system in a more inductive environment, i.e. $X_C \leq 1591$, another branch with either a fixed or variable capacitance value is needed, which would add cost and complexity to the system.

3. The major problem with this kind of system is that the TCR injects lower order harmonics. They are especially dominant when the value of the firing angle, α, approaches 125°. In a single phase system, it is difficult to eliminate these harmonics without a proper filter. A filter would add additional cost and complexity to the system. Filters for eliminating lower

order harmonics become bulky and expensive. Increasing the value of series reactance can reduce the total harmonic distortion but it also de-rates the system.

One of the solutions to overcome the above limitations, fully or partially, is to consider a voltage source converter (VSC) based STATCOM. The theory, modelling and analysis of the VSC based STATCOM is discussed in Chapter 4.

Table 3.2: Summary of the performance of the thyristor controlled three winding transformer as a static VAr compensator.

Load (μF)	VAr (leading)	α [3] (degrees)	VA			Real power		Supply current in A	
			A	B	Gain	A	B	A	B
45	1647	157.0	153	150	1.02	130	130	1.71	1.67
50	1832	136.5	300	267	1.12	134.5	144	3.33	2.9
55	2019	127.3	476	330	1.23	144.5	162	5.29	3.68
60	2212	120.4	657.5	366.5	1.44	156.4	185	7.32	4.1
65	2397	114.7	844	385	1.79	171	210	9.37	4.34
70	2583	109.8	1029	392	2.62	187.5	236.5	11.44	4.37
75	2772	105.3	1216	394	3.08	207.0	268	13.51	4.4
80	2961	101.2	1403	395	3.56	229.0	300	15.6	4.4
85	3150	97.8	1591	400	3.97	254	332.6	17.68	4.404
90	3340	94.0	1780	416	4.27	280	367	19.77	4.64

[3] Firing angle, α at which only the real power is drawn from the supply.
A: without application of the TCR.
B: with application of the TCR.

3.9 Summary

Partial core transformers are used to perform high voltage testing of generator insulation (a capacitive load) at a.c. power frequencies. Manual position adjustment of the transformer's central core imposes challenges such as involvement of higher magnetic forces, proximity of the operator to high voltage and the possibility of under or over compensation.

In this chapter, a concept of a thyristor controlled three winding transformer is proposed. The theory, modelling and simulations have revealed the performance of the proposed scheme. Application of the TCR to a three winding transformer offers continuous variation of the reactive power. When the system is compensated, there is no reactive power demand from the main power supply. This makes it possible to use a supply of a lower VA rating. Performance of the TCR controlled three winding transformer is demonstrated for the range of load conditions in table 3.2

After application of the TCR, real power losses are increased. The TCR also injects harmonics in the currents in the three windings. This adds more real power losses and reduces the VA gain of the system. The higher self inductance of the high voltage winding reduces the current harmonic distortion in that winding.

Chapter 4

Modelling, analysis and design of a single phase voltage source converter (VSC) based STATCOM

4.1 Overview

In chapter 3, the TCR controlled three winding partial core transformer is modelled, analysed and simulated using the PSCAD/EMTDC software. In order to compensate the system, continuous variation of reactive power is achieved by adjusting the shunt impedance of the TCR. Though the application of the TCR is simple, this technique has limitations as discussed in section 8. The amount of reactive power absorbed is directly dependent on the rating of the energy storage devices. For certain applications, the system may become bulky and complicated.

This chapter discusses a STATCOM controlled partial core transformer. A detailed mathematical design of the voltage source converter (VSC) based STATCOM along with its transfer function is demonstrated. A proportional – integral (PI) controller is designed using MATLAB. Stability of the designed control system is evaluated for *capacitive* and *inductive* loads. The proposed system is modelled in PSCAD/EMTDC software. The model verifies the capability of the system to offer a continuous reactive power control in the partial core transformer, and to limit the supply current magnitude to its real component.

4.2 Introduction

In 1976 Gyugyi disclosed switching power converters that generate controllable reactive power directly, without the use of a.c. capacitors or reactors. For multiphase systems, the ability to generate or absorb reactive power without the presence of large reactive energy storage elements makes them very useful in power applications. In a three phase STATCOM this is accomplished by making

the currents circulate through the phases of the a.c. system with the aid of power switching devices [19]. From the point of view of reactive power generation, their operation mirrors an ideal synchronous machine that uses excitation for controlling the reactive power output. They are also capable of exchanging real power with the a.c. system, if they are provided with a d.c. energy source at the d.c. terminals of the converter. Because of these similarities, they are also called Static Synchronous Generators (SSGs). When a SSG is used as a shunt connected reactive compensator with no energy source, it is termed a Static Synchronous Compensator or STATCOM. Although current source converters are possible, voltage sourced converters are preferred. Justification for this is well documented in [18]. Unlike the TCR, the VSC based STATCOM generates an a.c. output waveform using a sinusoidal pulse width modulation (SPWM) technique; this significantly reduces lower order harmonics without the need of any additional filters.

4.3 Modelling and analysis of a single phase VSI based STATCOM

Figure 4.1 shows a simplified circuit diagram of a single phase VSI based STATCOM. In this circuit, V_s signifies the supply voltage, and the series inductance L_s represents the leakage inductance of the transformer. R_s accounts for the conduction losses of the converter.

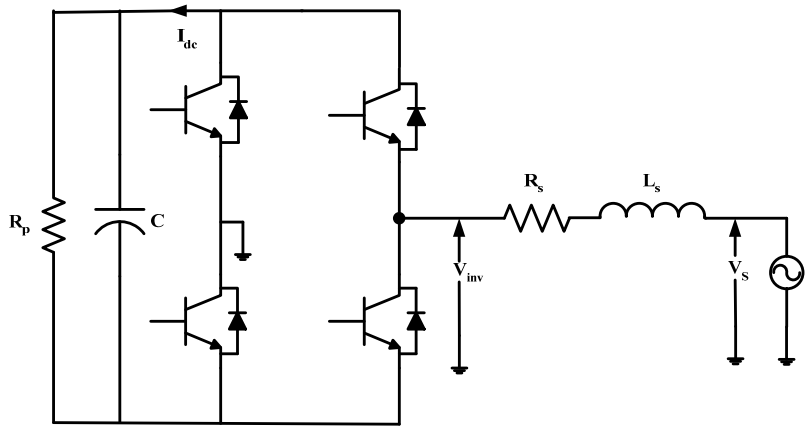


Figure 4.1: A single phase voltage source converter based STATCOM

The charged capacitor, C acts as a d. c. voltage source for the converter. The converter consists of four IGBTs in a single phase 'H' bridge configuration

which produces a controllable single-phase SPWM output voltage, V_{inv}, with a frequency of that of the a.c. power system. The output voltage waveform of the converter is never a pure sine wave. It contains a fluctuating (ripple) component of instantaneous output power (VA). The voltage will fluctuate at low frequency as the converter is required to store the 'reactive energy'. R_p represents the switching losses in the converter.

The d.c. storage capacitor is required for maintaining the net instantaneous power at the d.c. input terminals (ignoring the switching losses of the semiconductor devices) equal to the net instantaneous power at the a.c. output terminals. Thus, the d.c. capacitor maintains a balance between the input and output during the dynamic change in the VAr output [18]. This can require a significant capacitance.

In a practical situation, semiconductor switches incur active power losses. These internal losses are supplied by the a.c. supply, and the voltage level drops down lower than expected. In order to prevent this, the switching losses are supplied by the a.c. system by making the converter a.c. output voltage lag behind the a.c. system voltage by a small angle, δ. Equation 4.1 gives the relationship between the real power, *P* absorbed by the STATCOM and the phase angle δ. X_L accounts for the reactance between V_s and V_{inv}. R_s is neglected.

$$P = \frac{V_{inv} V_s}{X_L} \sin \delta \tag{4.1}$$

The phase angle can be used to control the capacitor voltage and hence the converter output voltage, V_{inv}. As shown in equation 4.2, the magnitude and nature (inductive or capacitive) of reactive power, Q, exchanged between the STATCOM and the system, can be adjusted by controlling the voltage drop across the equivalent series impedance, X_L, between the a.c. side of the STATCOM and the system voltage.

$$Q = \frac{V_{inv} - V_s}{X_L} V_s \tag{4.2}$$

If Q is positive, the STATCOM delivers reactive power to the system. Otherwise the STATCOM absorbs reactive power from the system [20]. The voltage, V_{inv}, can be controlled either by adjusting the modulation index, m, of the PWM waveform, or by changing the phase angle, δ, between V_{inv} and V_s which charges or discharges the capacitor d.c. voltage. Both systems are explained in detail in [18]. Work carried out for this research employs the latter scheme.

4.4 Concept of STATCOM controlled partial core transformer

In the case of a partial core transformer, the lack of a closed core reduces the magnetising reactance (X_m) significantly and increases the reactive power requirement. Thus it draws a higher magnitude of lagging current from the supply as compared to its full core counterpart. If this demand is supplied by a compensator which can eliminate the reactive power demand on the main supply, the partial core transformer can be used like a full core transformer [4]. Its applications can be found where weight, size and ease of transportation are the major priorities, e.g. relocatable compensating systems [21].

As shown in figure 4.2, a single phase, VSI-based STATCOM is connected to the tertiary winding of a partial core three winding transformer. In order to minimise the total harmonic distortion and ripple content in the supply current, the a.c. terminals of the converter are connected to the mains supply through an external inductor, L_s.

The magnitude of the supply current is sensed by measuring a voltage drop across a low value resistance, R_{sense}. The phase angle, θ, the angle between the supply voltage and current, is measured by detecting the time difference between the zero crossings of the supply voltage and current waveforms.

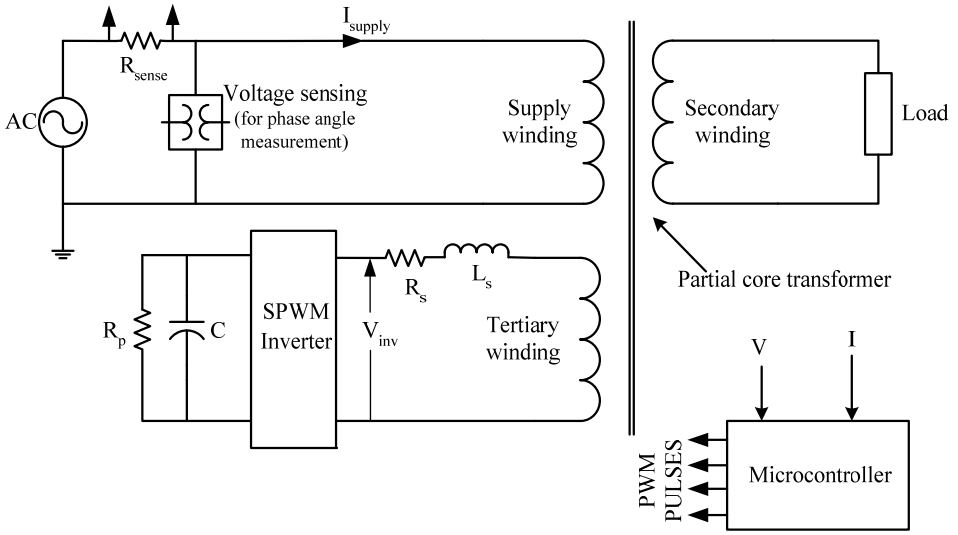


Figure 4.2: Proposed STATCOM controlled scheme for a partial core transformer

An 8 bit micro-controller is used to generate SPWM waveforms as well as to accomplish automatic control of the STATCOM. The actual hardware developed is described in chapter 5.

4.5. Design of the STATCOM

The STATCOM design is considered for compensating the reactive power required by the lower X_m of the partial core transformer. As a prototype, the proposed STATCOM is designed for ± 1 kVAr.

4.5.1 Current rating of the STATCOM

The current rating of the STATCOM is related to the total reactive power delivered to the load and partial core transformer for compensating X_m.

$$Q_{total} = V_s \times I_s \tag{4.3}$$

where V_s is the a.c. mains voltage (i.e. 90 V r.m.s.) and I_s is the STATCOM line current. After substituting the values of V_s and Q_{total} (i.e. 1 kVAr), the current rating of the STATCOM is 11.11 A. [22].

4.5.2 Determination of series inductance (L_s)

The equation for determining the series inductance, L_s for a single phase STATCOM is derived from [23],

$$L_s = \frac{V_{dc} \times m}{4 \times f_s \times I_{ripple(p-p)}} \tag{4.4}$$

where V_{dc} is the DC voltage across the electrolytic capacitor. The modulation index, m is considered as 1. The switching frequency, f_s, of the PWM synthesised, is chosen as 1350 Hz. $I_{ripple(p-p)}$ is the peak-peak ripple current, which is designed to be 8% of the total current. Thus the peak-peak ripple current is given by,

$$I_{ripple(peak-peak)} = 2\sqrt{2} \times 0.08 \times 11.11 = \ 2.5 \ \text{A} \tag{4.5}$$

For calculating L_s, the maximum magnitude of $V_{dc}\left(> \sqrt{2}\ V_{inv}^{max}\right)$ is taken into account. From equation 4.2, it can be seen that the magnitude of the STATCOM output voltage controls the reactive power exchange between the STATCOM and the system, assuming that the system voltage and the series impedance are kept constant. Re-writing equation 4.2 for the maximum rated reactive power, Q_{max}, the STATCOM can deliver

$$Q_{\max} = \left(\frac{\frac{V_{dc}}{\sqrt{2}} - V_s^{\max}}{\omega L_s} \right) \times V_s^{\max} \tag{4.6}$$

In this case, Q_{max} is 1000 VAr and maximum system voltage, V_s^{max}, is 90 V. Substituting these values into equation 4.6 yeilds

$$1000 = \left(\frac{\frac{V_{dc}}{\sqrt{2}} - 90}{\omega L_s} \right) \times 90 \tag{4.7}$$

Substituting the value of $I_{ripple(peak-peak)}$ in equation 4.4 and simultaneously solving the equations 4.4 and 4.7, magnitudes of V_{dc} = 200 V and L_s = 14.8 mH are obtained. The approximate voltage drop across the pair of power switches is

assumed to be 6 V and is added to V_{dc}. Hence V_{dc} becomes 206 V. The resistance in series, R_s, representing the active losses, is assumed to be 0.5 Ω.

4.5.3 Choosing the value of d.c. capacitor (C)

The equations for proper sizing of the d.c. capacitor for one converter system are detailed in [20]. The d.c. capacitor peak to peak voltage ripple is given by,

$$\Delta V_c = \frac{m\, I}{2\omega C} \tag{4.8}$$

The selected value of d.c. voltage ripple is 4 V, which is 2% of the selected V_{dc} (= 206 V). From equation 4.8, the value of C can be derived as

$$C = \frac{m\, I}{2\omega \Delta V_c} \tag{4.9}$$

After substituting the required values in equation 4.9, the magnitude of the d.c. capacitor is found to be 4,420 μF. The nearest available value was 4700 μF, and hence was selected.

4.6 Transfer function for a single phase STATCOM

Figure 4.3 shows the equivalent circuit of a single phase VSC based STATCOM. All notations represent their usual meanings as defined in the previous sections.

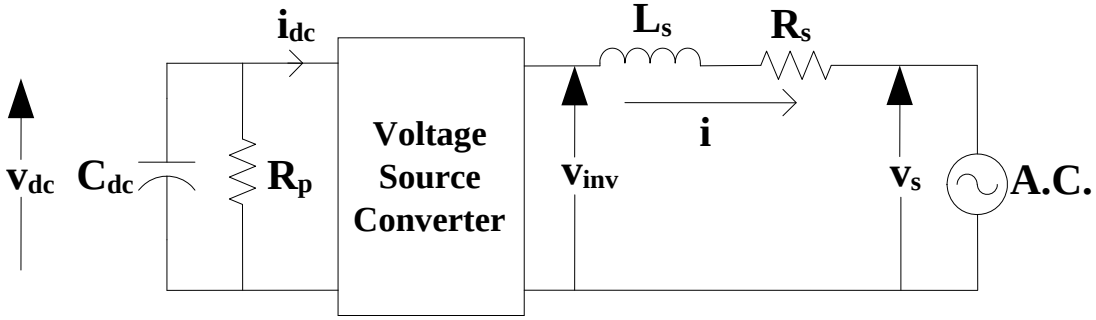


Figure 4.3: Equivalent circuit of a single phase STATCOM

Fig. 4.4 illustrates the vectors of the a.c. side of the circuit in the synchronous reference frame. When i_q is positive, the VSC draws inductive VArs from the a.c. supply. For negative values of i_q, VSC draws capacitive VArs.

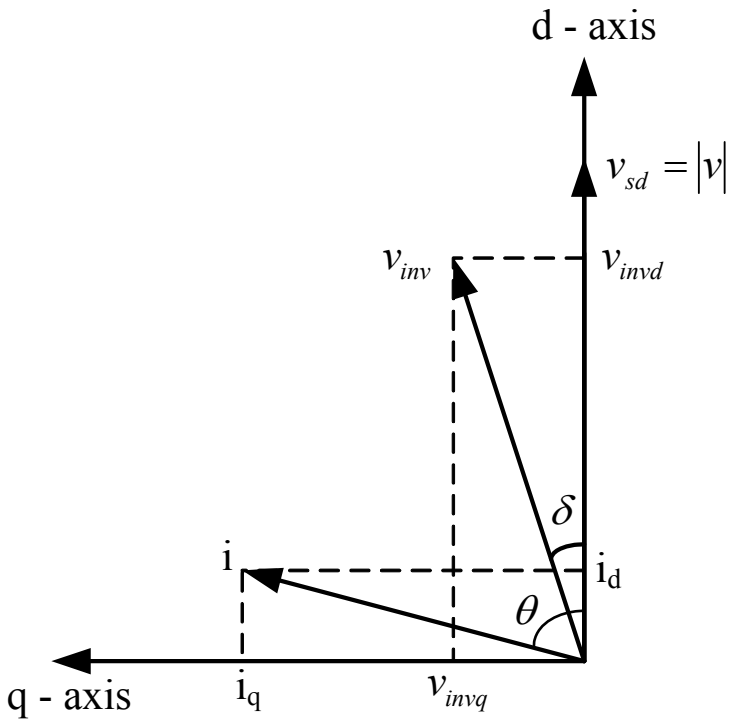


Figure 4.4: Vectors for the VSC based STATCOM in the synchronous reference frame

Referring to Figs. 4.3 and 4.4, the relationship between the voltage and the current in the inductor, L_s is given by,

$$L_s \frac{di}{dt} = v_{inv} - v_s \tag{4.10}$$

The d-q transforms of equation 4.10 gives,

$$\frac{d}{dt}\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} -\frac{R_s}{L_s} & \omega \\ -\omega & -\frac{R_s}{L_s} \end{bmatrix}\begin{bmatrix} i_d \\ i_q \end{bmatrix} + \frac{1}{L_s}\begin{bmatrix} v_{invd-|v|} \\ v_{invq} \end{bmatrix} \tag{4.11}$$

where, angular frequency $\omega = \frac{d\theta}{dt}$. By neglecting voltage harmonics produced by the inverter, a pair of equations for v_{invd} and v_{invq} can be written as,

$$v_{invd} = mV_{dc}\cos(\delta) \tag{4.12}$$

$$v_{invq} = mV_{dc}\sin(\delta) \tag{4.13}$$

For the purpose of designing the control system, *m* is kept constant, and the delay angle, δ, of the inverter voltage vector is used as the controlling parameter. For this type of controller, it is essential to include inverter and d.c. side equations for the model. The power balance equation for the single phase inverter is given by,

$$v_{dc}i_{dc} = \left(v_{invd}i_d + v_{invq}i_q\right) \tag{4.14}$$

The d.c. side circuit equation is,

$$\frac{dv_{dc}}{dt} = -\frac{1}{C_{dc}}\left(i_{dc} + \frac{v_{dc}}{R_p}\right) \tag{4.15}$$

$$\rho\begin{bmatrix} i_d \\ i_q \\ v_{dc} \end{bmatrix} = \begin{bmatrix} -\frac{R_s}{L_s} & \omega & \frac{m}{L_s}\cos(\delta) \\ -\omega & -\frac{R_s}{L_s} & \frac{m}{L_s}\sin(\delta) \\ -\frac{m}{C_{dc}}\cos(\delta) & -\frac{m}{C_{dc}}\sin(\delta) & -\frac{1}{R_pC_{dc}} \end{bmatrix}\begin{bmatrix} i_d \\ i_q \\ v_{dc} \end{bmatrix} - \begin{bmatrix} \frac{|v|}{L_s} \\ 0 \\ 0 \end{bmatrix} \tag{4.16}$$

where, $\frac{d}{dt} = \rho$.

The proposed system is modelled and simulated using PSCAD/EMTDC software for obtaining steady state parameter values for equation 4.16. As shown in Fig. 4.5, the typical system parameters such as i_{d0}, i_{q0}, v_{dc0} (all in p. u.) are plotted versus the delay angle, δ_0. The sub-script 0 indicates a steady state parameter.

It can be noted from Fig. 4.5 that i_{q0} varies almost linearly with respect to δ_0. If δ is considered as an input variable; the STATCOM state equations given in section 4.16 are non-linear. These equations can be linearised with small deviations around a selected steady state equilibrium point. The perturbation equation 4.17 gives result for the linearisation process [24-25].

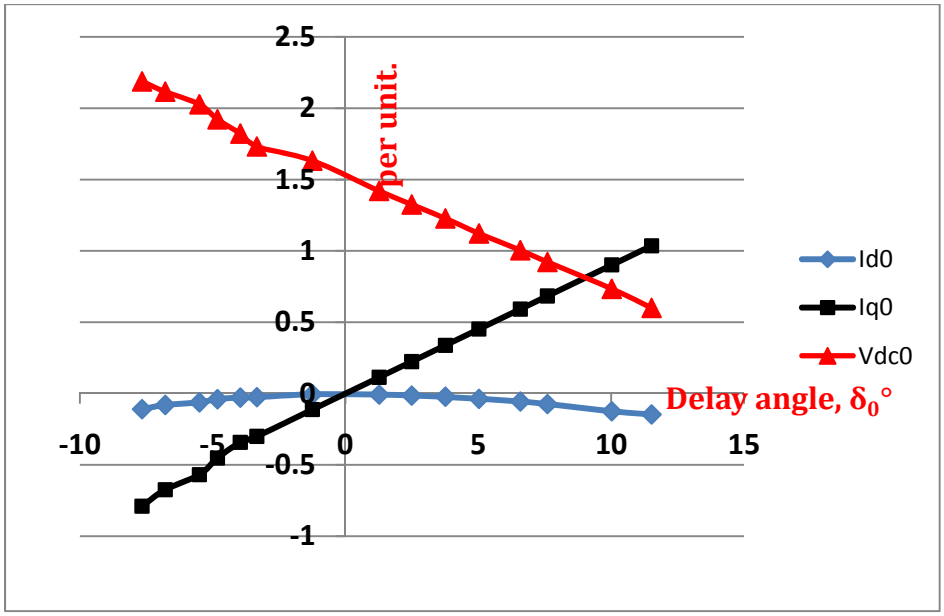


Figure 4.5: Variation of state variables of the considered system (in p. u.)[1] with respect to the delay angle[2], δ_0 °

$$\rho \begin{bmatrix} \Delta i_d \\ \Delta i_q \\ \Delta v_{dc} \end{bmatrix} = [A_\Delta] \begin{bmatrix} \Delta i_d \\ \Delta i_q \\ \Delta v_{dc} \end{bmatrix} + [B_\Delta] \begin{bmatrix} \Delta v \\ \Delta \delta \end{bmatrix}$$

$$[A_\Delta] = \begin{bmatrix} -\frac{R_s}{L_s} & \omega & \frac{m}{L_s}\cos(\delta_0) \\ -\omega & -\frac{R_s}{L_s} & \frac{m}{L_s}\sin(\delta_0) \\ -\frac{m}{C_{dc}}\cos(\delta_0) & -\frac{m}{C_{dc}}\sin(\delta_0) & -\frac{1}{R_p C_{dc}} \end{bmatrix}$$

$$[B_\Delta] = \begin{bmatrix} -\frac{1}{L_s} & -\frac{m v_{dc0}\sin(\delta_0)}{L_s} \\ 0 & \frac{m v_{dc0}\cos(\delta_0)}{L_s} \\ 0 & \frac{m}{C_{dc}}\left(i_{d0}\sin(\delta_0) - i_{q0}\cos(\delta_0)\right) \end{bmatrix} \qquad (4.17)$$

[1] Base voltage = 90 V, base current = 11.11 A

[2] Non-linearity of curves in the inductive region is because of presence of harmonics in the supply current

Equation 4.17 can be simplified by neglecting the system power losses i.e. $R_s = 0$, $R_p = \infty$. The corresponding transfer function relating Δi_q and $\Delta\delta$ can be written as,

$$G(s) = \frac{\Delta i_q(s)}{\Delta\delta(s)} = \frac{\frac{m}{L_s}\left[s^2 + \frac{m^2}{L_s C_{dc}}\right] v_{dc0} + \left[\frac{m^2\omega}{L_s C_{dc}}\right] i_{q0}}{s\left[s^2 + \omega^2 + \frac{m^2}{L_s C_{dc}}\right]} \qquad (4.18)$$

4.7 Determining parameters for a PI controller

The PI transfer function is given by,

$$F_{PI}(s) = K\left(1 + \frac{1}{T_i s}\right) \qquad (4.19)$$

where K serves as a proportional constant (K_p), T_i is a time constant while, $\frac{K}{T_i}$ gives the value for an integral constant (K_i). The closed loop transfer function of the proposed STATCOM is,

$$[F_{PI}G](s) = \frac{F_{PI}G}{1 + F_{PI}G} \qquad (4.20)$$

4.7.1 Case 1: A full capacitive load

In the PSCAD/EMTDC model, a capacitive load of 58 μF (2631 VAr) is connected across the H.V. winding terminals of the partial core transformer. Then the load seen by the STATCOM is capacitive. A rated voltage, i.e. 90 V, is applied to the supply winding. To solve equation 4.17, initial steady state values for i_{d0}, i_{q0}, v_{dc0} and δ_0 are required. These values are obtained from the PSCAD/EMTDC simulations as given below,

i_{d0} = -1.63 A	i_{q0} = -11.52 A	v_{dc0} = 54 V	δ_0 = -11°

The transfer function is given by,

$$\frac{\Delta i_q(s)}{\Delta \delta(s)} = \frac{3599\, s^2 - 107500\, s + 5.182e7}{s^3 + 68.24\, s^2 + 114400\, s + 513500} \tag{4.21}$$

To predict the closed loop performance of the system, open loop Root locus and Bode plots are obtained using MATLAB. These plots are shown in Fig. 4.6. The system seems to be unstable as it has a high gain and the closed loop complex poles are very near to the imaginary axis.

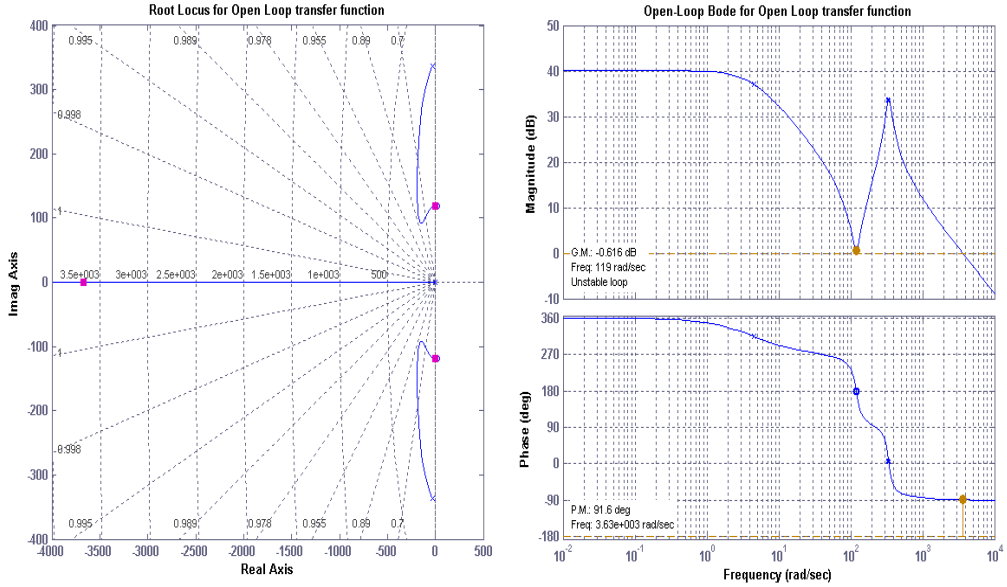


Figure 4.6: Root locus (left) and Bode plot (right) of the transfer function given in equation 4.21

MATLAB is used to design the PI controller such that the PI controller:

- Eliminates the steady state error
- Limits the percentage overshoot < 120%
- Maintains the minimum damping ratio around 0.5 to 0.6

The open loop block diagram PI controller together with the system transfer function is shown in Fig. 4.7.

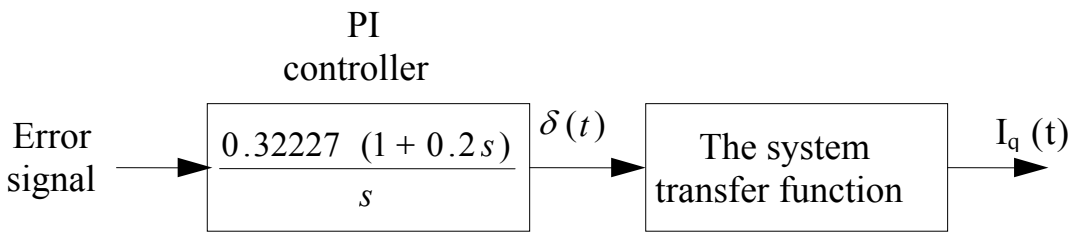


Figure 4.7: Transfer function of the PI controller

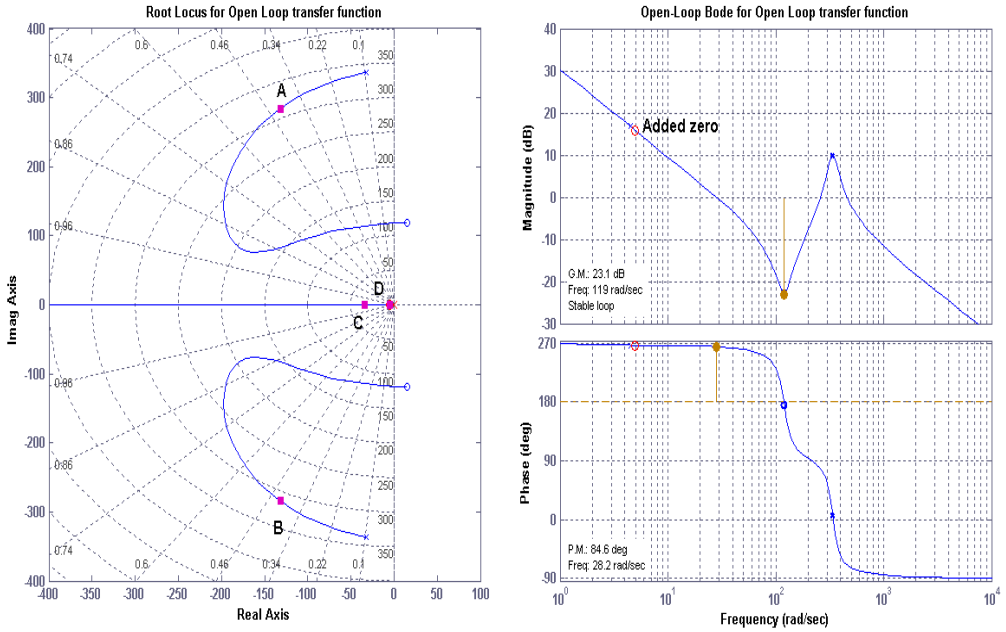


Figure 4.8: The modified Root locus (left) and open loop Bode plot after adding the PI controller

Root locus and Bode plots after adding the PI controller are shown in Fig. 4.8. In the Root Locus curve, points A, B, C and D represent the closed loop poles of the system. Zeros of the system determines the nature of the system response. A step response illustrated in Fig. 4.9 verifies that the designed system is stable and meets the predefined requirements.

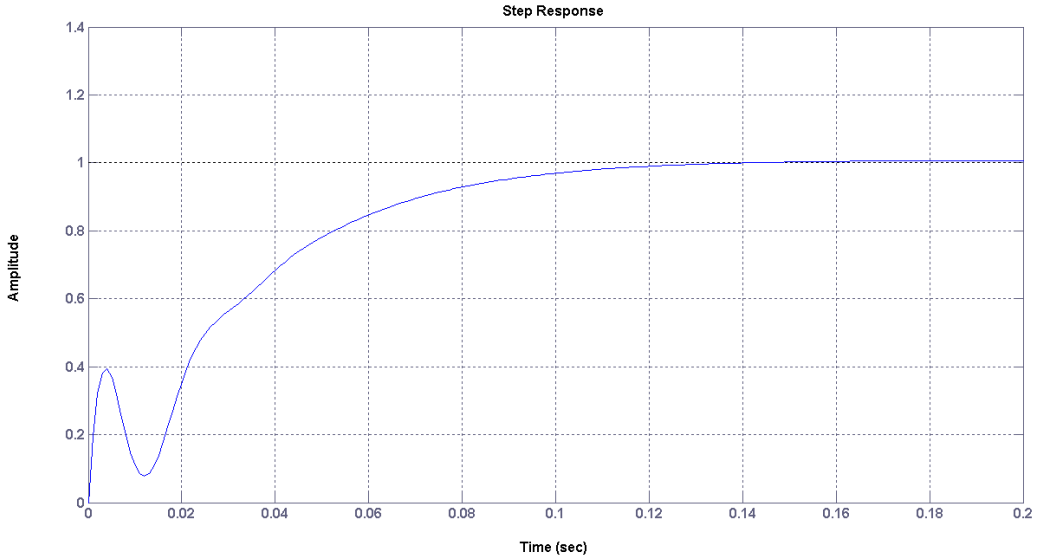


Figure 4.9: Step response of the system for a full capacitive load

4.7.2 Case 2: Full inductive load

A reduced capacitive load of 15 μF is connected across the H.V. winding terminals of the partial core transformer. In this case, the resultant load is dominated by the magnetizing reactance (X_m) of the partial core transformer. Thus the STATCOM sees this as an inductive load. For this case, the steady state initial values of i_{d0}, i_{q0}, v_{dc0} and δ_0 are obtained using PSCAD/EMTDC simulations as given below,

i_{d0} = - 1.56 A	i_{q0} = 10 A	v_{dc0} = 207 V	δ_0 = 8.08°

Then the transfer function for this case can be estimated as,

$$\frac{\Delta i_q(s)}{\Delta \delta(s)} = \frac{13940\ s^2 + 1.099e6 + 2.022e8}{s^3 + 68.24\ s^2 + 114400\ s + 513500} \qquad (4.22)$$

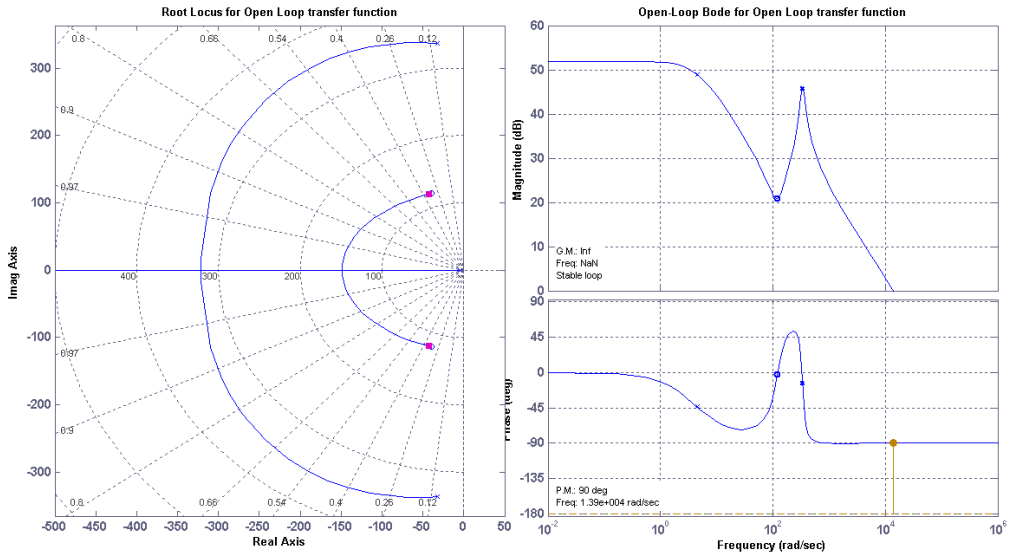


Figure 4.10: Root locus (left) and Bode plot (right) of the transfer function given in equation 4.22

Fig. 4.10 shows the Root locus and open loop Bode plots obtained using MATLAB. As all three poles of the system are located on the left hand side of the imaginary axis, the system is stable. The performance of the designed PI controller is evaluated also for this inductive case.

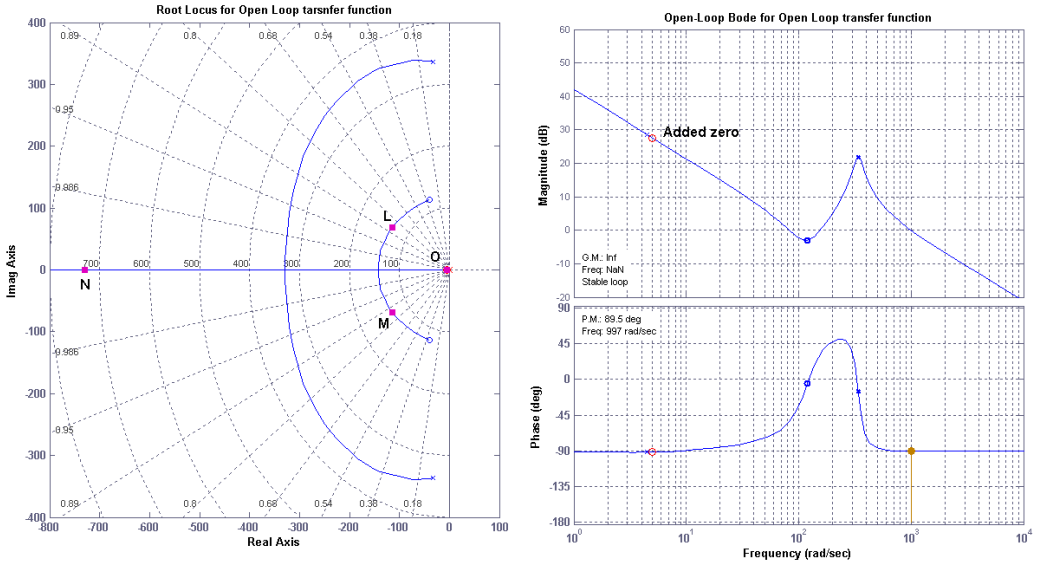


Figure 4.11: Root locus (left) and open loop Bode plot after adding the PI controller

Fig. 4.11 shows that all closed loop poles of the system such as L, M, N and O are located on the left hand side of the imaginary axis i.e. the system is stable. Unlike in the capacitive case, zeros in the inductive case are also located on the left hand side of the imaginary axis. This indicates that for the same control system the nature of the system response (e.g. shape of a step curve) depends on the type of the load. Fig. 4.12 shows that the system is also stable for inductive loads.

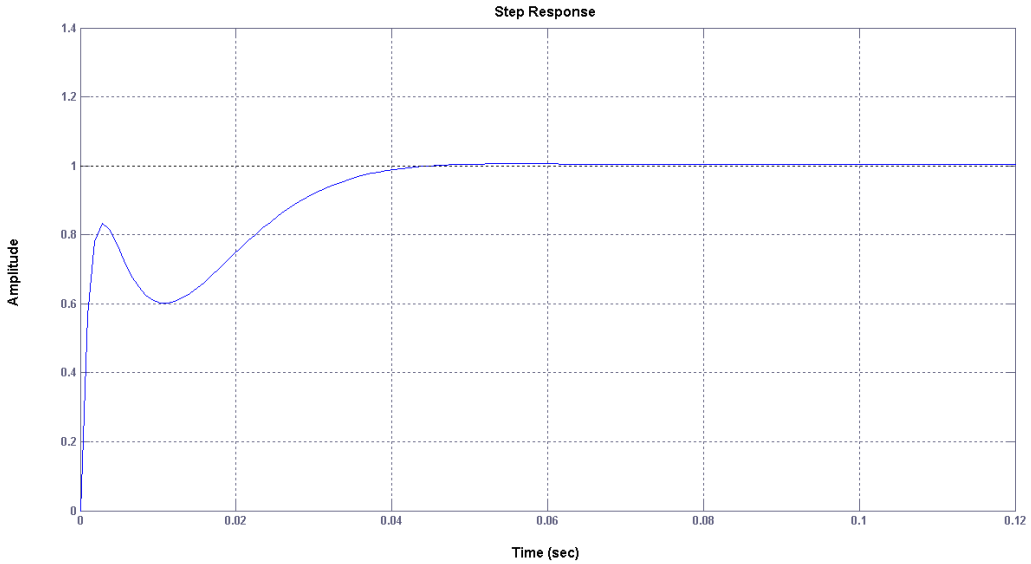


Figure 4.12: Step response of the system for full inductive load

4.8 Control system structure

The control system derived is simple, with an indirect approach of a dc capacitor voltage control as shown in figure 4.13. This can be implemented on a compatible micro-controller or a digital signal processing (DSP) chip. The voltage V_s and the current, I_s, are measured from the supply side. I_s is measured by sensing the voltage drop across the current sensing resistor, R_{sense}, (0.02 Ω). In order to obtain the reactive component of the supply current, the phase angle between I_s and V_s is measured by the zero crossing detection technique. False or multiple zero-crossing detections are avoided by filtering the current and voltage signals.

The supply current, I_s, is decomposed into real and reactive components. The reactive component, I_{sq}, of the supply current is then compared with the reference

(Ref I_q). The error signal obtained is processed by a PI controller that generates the appropriate phase angle, δ, which determines a phase shift between the output of the converter and the mains voltage.

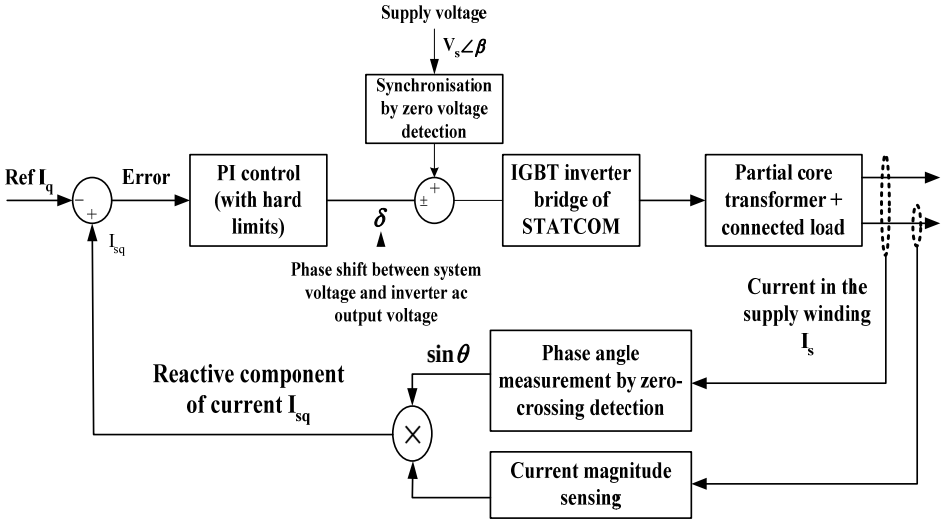


Figure 4.13: Automatic control system implemented for the STATCOM controlled partial core transformer

Depending on whether the load seen by the STATCOM is inductive or capacitive, the angle δ is added or subtracted from the synchronised supply voltage angle, θ, respectively. This controls the real power exchange between the STATCOM and the system, and thus the DC capacitor voltage is regulated [18, 21]. The scheme also should work for a 3-phase transformer.

4.9 Dynamic performance of the VSC based STATCOM

Fig. 4.14 shows the basic model in PSCAD/EMTDC of the proposed VSC based STATCOM controlling the three winding transformer. The implemented control system is detailed in section 4.8. To evaluate dynamic as well as steady state performance of the model, a scenario is created as shown in Fig. 4.15.

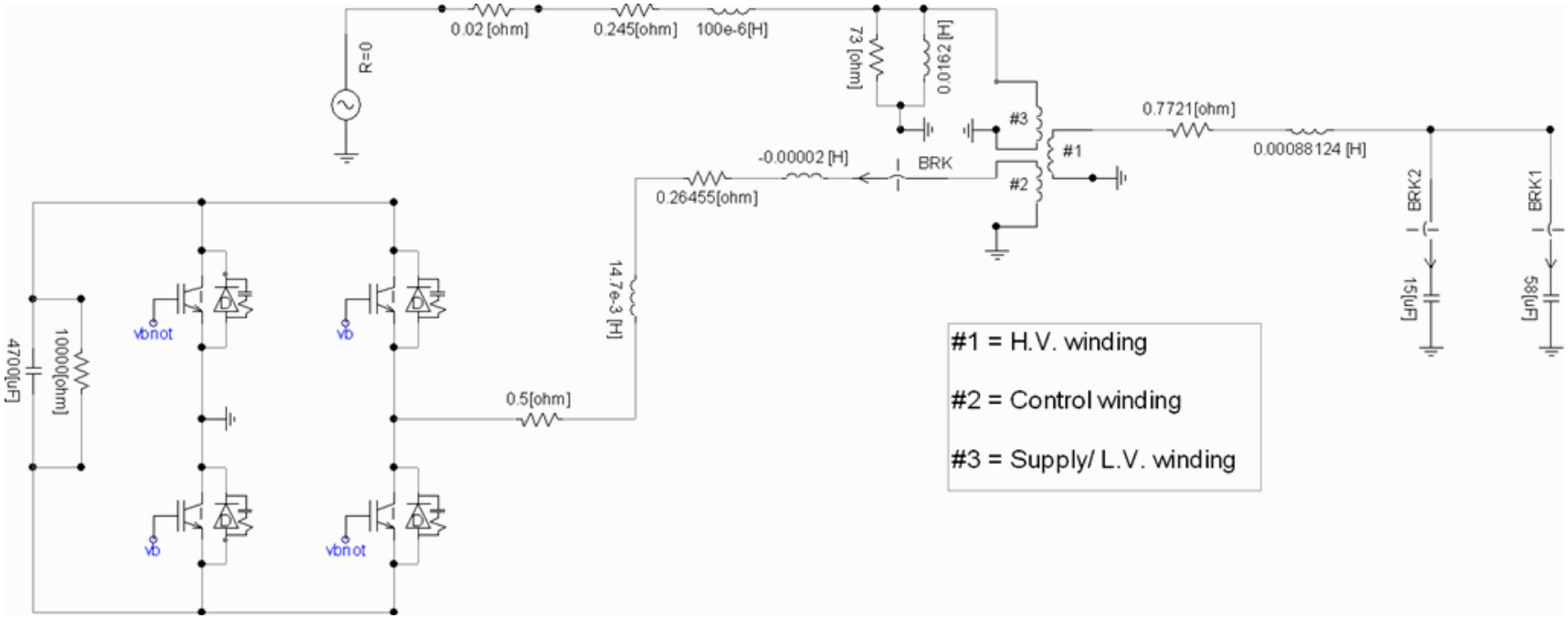


Figure 4.14: PSCAD/EMTDC model of the STATCOM controlled three winding transformer

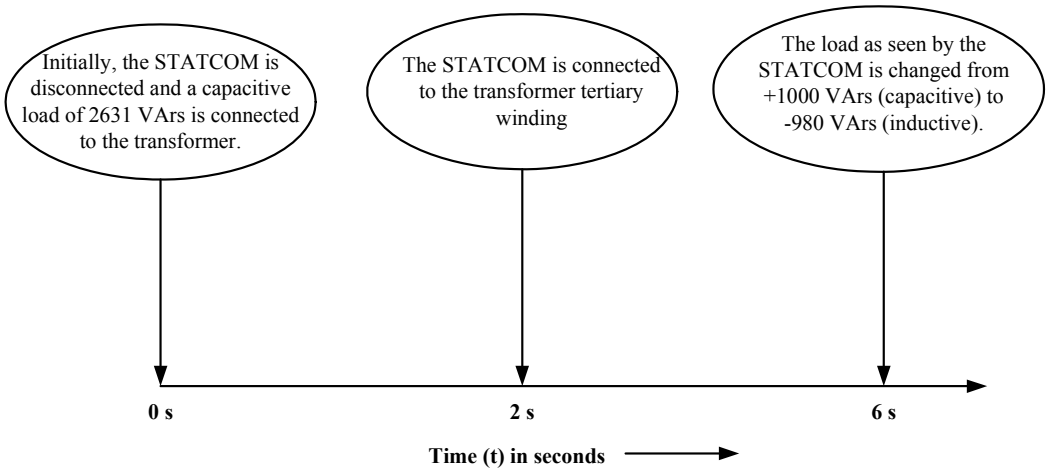


Figure 4.15: The scenario created for evaluating performance of the proposed system

The various time periods of the considered scenario are described below.

From t = 0 s to t = 2 s

Initially, a capacitive load of 58 μF (2631 VArs) is connected to the transformer H.V. terminals. The supply winding is excited with 90 V. The tertiary winding is kept open, i.e. the STATCOM is not connected. The magnetising reactance, X_m, of the partial core absorbs 1590 VArs, and the remaining capacitive VArs are drawn from the supply. Before connecting the STATCOM, the current drawn from the supply is 11.8 A.

From t = 2 s to t = 6 s

When t = 2s, the breaker, BRK, of the tertiary winding is closed, i.e. the STATCOM is connected to the magnetically coupled tertiary winding of the transformer and begins to absorb additional capacitive VArs. Although connection of the STATCOM reduces the reactive burden on the supply winding, it draws additional real power from the supply to provide the losses that occur in the STATCOM and the tertiary winding.

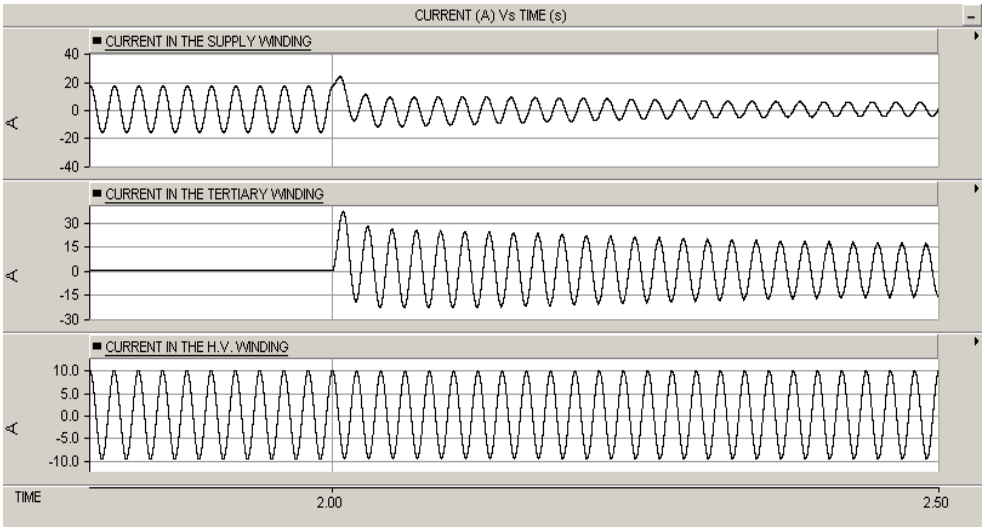


Figure 4.16: Behaviour of the currents in the three windings

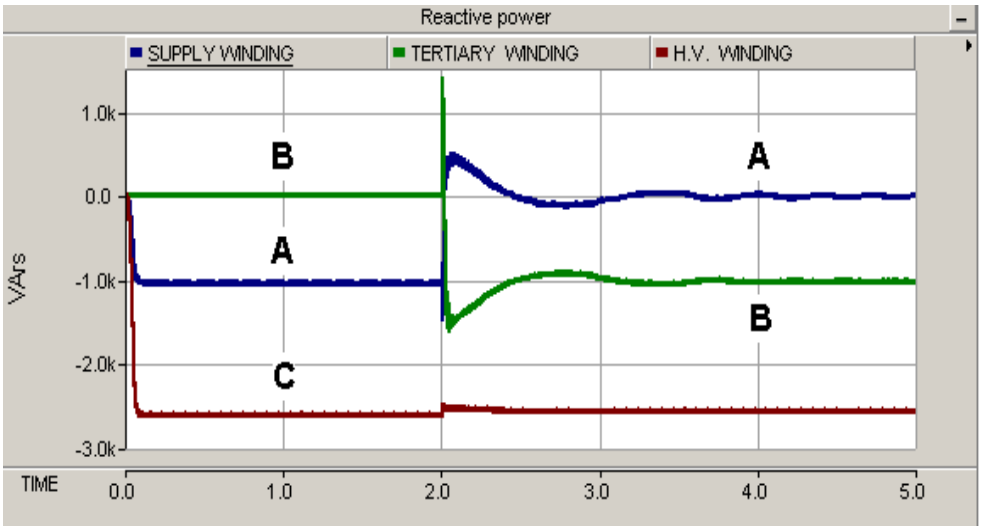


Figure 4.17: Behaviour of reactive power in the supply winding (A), the tertiary winding (B), and the H. V. winding (C)

Fig. 4.16 shows the behaviour of the currents in the three windings, and the dynamics of the reactive power exchange is illustrated in Fig. 4.17. When the steady state condition is reached the supply current is limited to 3.4 A. After connecting the STATCOM, VA gain is 3.4.

From t = 6 s

When t = 6 s, the capacitive load is reduced from 58 µF (2631 VArs) to 15 µF (680 VArs). Now, the resultant load is formed by the transformer magnetising

reactance, X_m, and the reduced capacitive load, becomes inductive. The overall load as seen from the STATCOM changes from + 1040 VArs (capacitive) to – 980 VArs (inductive).

Fig. 4.18 shows dynamic and steady state behaviour of currents in the three windings for t > 6 s. When the system reaches the steady state condition, the supply current remains 2.81 A. Fig. 4.19 demonstrates reactive power exchange in the three windings.

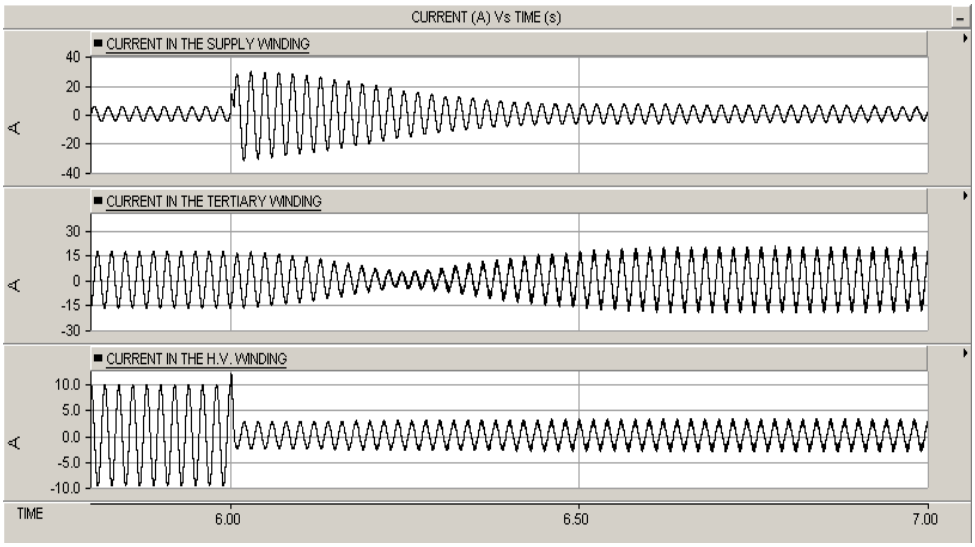


Figure 4.18: Behaviour of currents in the three windings before and after the load changes from full capacitive to full inductive.

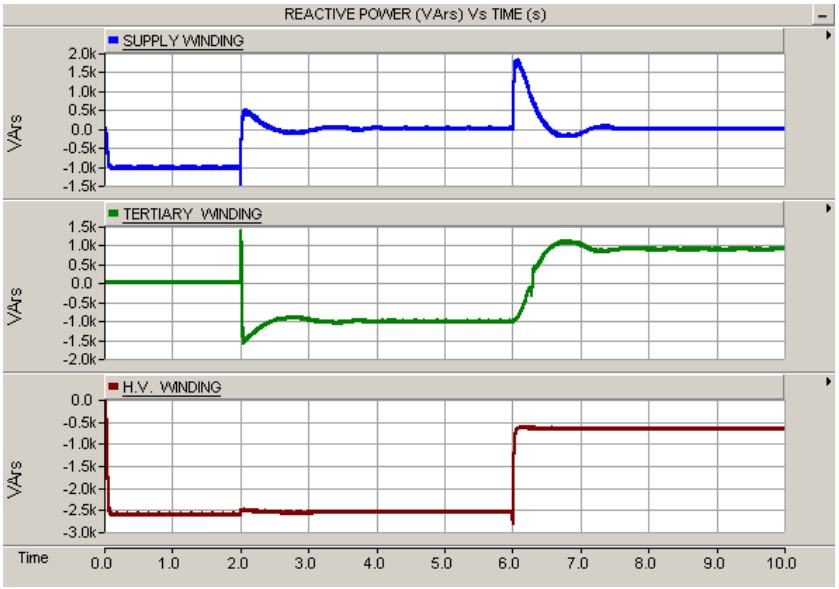


Figure 4.19: Dynamic behaviour of reactive power in the three windings

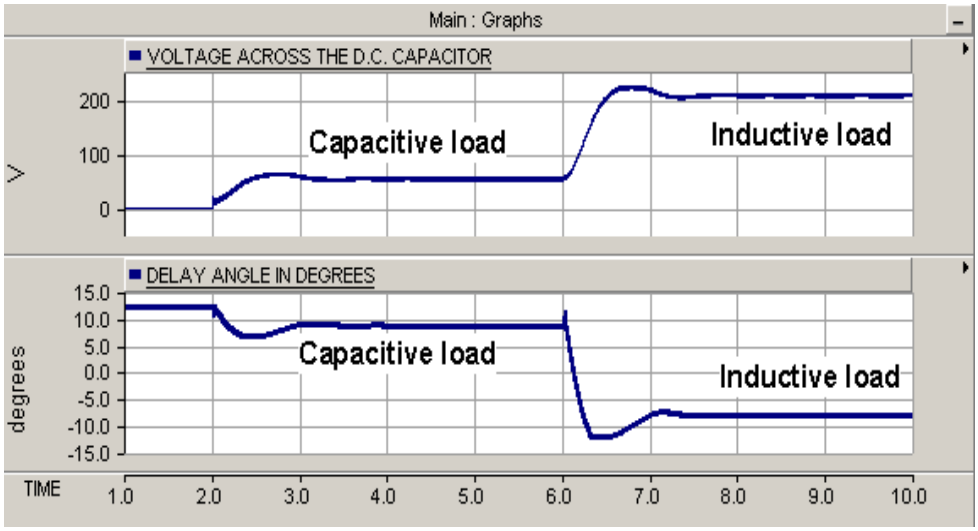


Figure 4.20: Dynamic behaviour of voltage across the d.c. capacitor, V_{dc}, and the delay angle, δ

Behaviour of other parameters of the STATCOM such as voltage across the d.c. capacitor, V_{dc}, delay angle, δ, for the considered scenario is demonstrated in Fig. 4.20.

4.9.1 Voltage quality

The PSCAD model assumes an ideal supply. In this case, the voltage quality across the three windings remains unchanged during switchings. However, in practice, a voltage source may have high impedance. In such cases, voltage quality of the system may deteriorate during system disturbances.

4.10 Summary

This chapter covers the theory, modelling and analysis of a single phase VSC based STATCOM. The concept of a STATCOM controlled three winding partial core transfer is mathematically explained in detail.

In order to determine the control parameters, the transfer function is derived for the considered system. Analysis of the system using Root locus and Bode plots in MATLAB shows that the system is stable for the full capacitive and inductive loads. The PSCAD/EMTDC model demonstrates that the designed system is dynamically stable and capable of handling system disturbances. This verifies that the system is capable of offering a continuous reactive power control.

Chapter 5

Development of controller board for the proposed single phase VSC based STATCOM

5.1 Overview

In chapter 4, the theory, modelling, analysis and design of a single phase VSC based STATCOM is covered in detail. A prototype of the proposed single phase STATCOM for controlling the amount of reactive power in the partial core transformer was built for experimental verification. Although the power devices are rated for a higher VA rating, experiments in a laboratory were carried out at lower power, i.e. 600 VA.

This chapter covers the conceptual design and development of the hardware part of the control system while chapter 6 details the design and development of the power circuit of the proposed VSC based STATCOM. The main function of the hardware part of the control circuit is to measure and control the reactive component of the supply current, I_q.

Figure 5.1 shows a schematic diagram of the controller board, while the prototype can be seen in figure 5.2. The controller board consists of a regulated power supply, various sensor circuits, a dual channel electronic active filter, a micro-controller, PWM driver ICs and a LCD display.

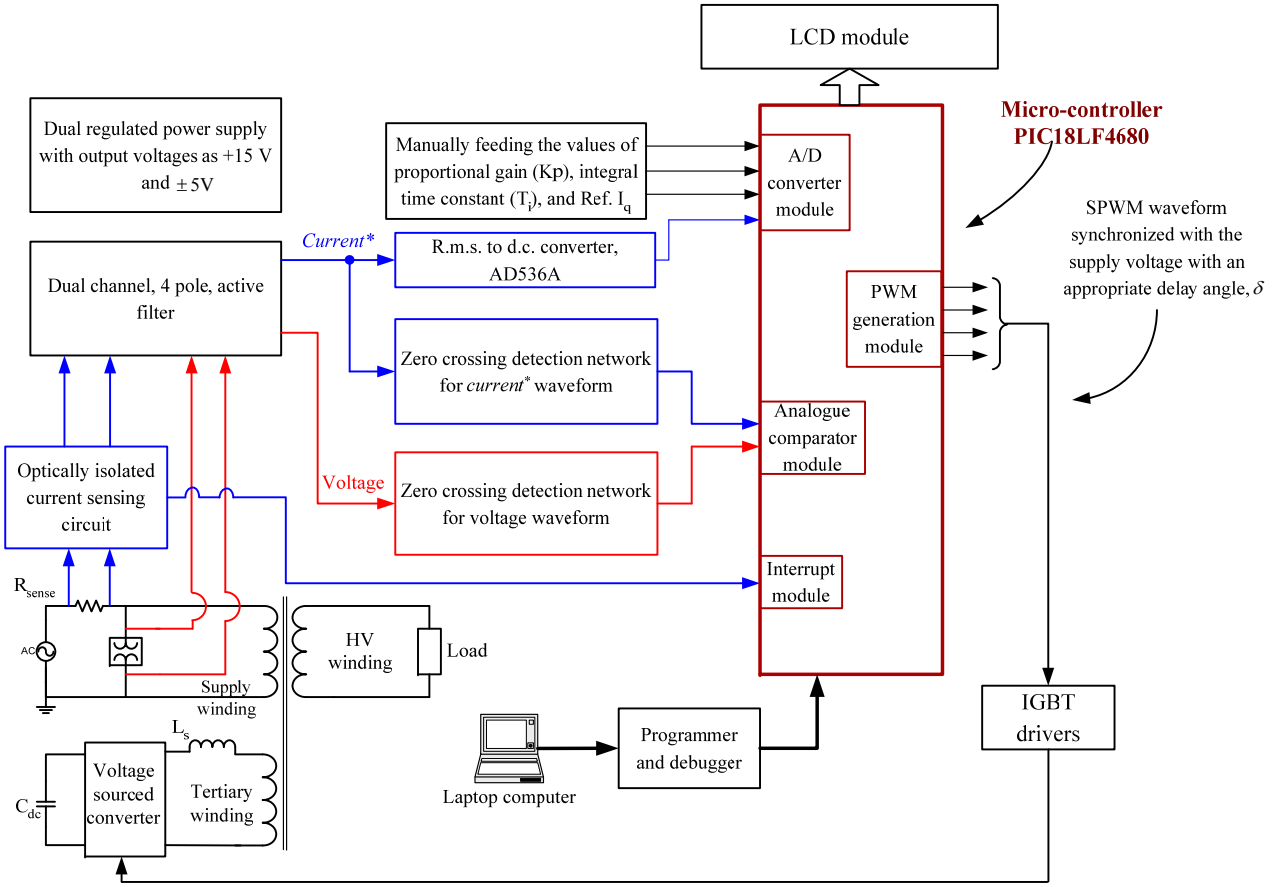


Figure 5.1: Schematic diagram of the controller board

*Current** is a voltage waveform proportional to the actual supply current.

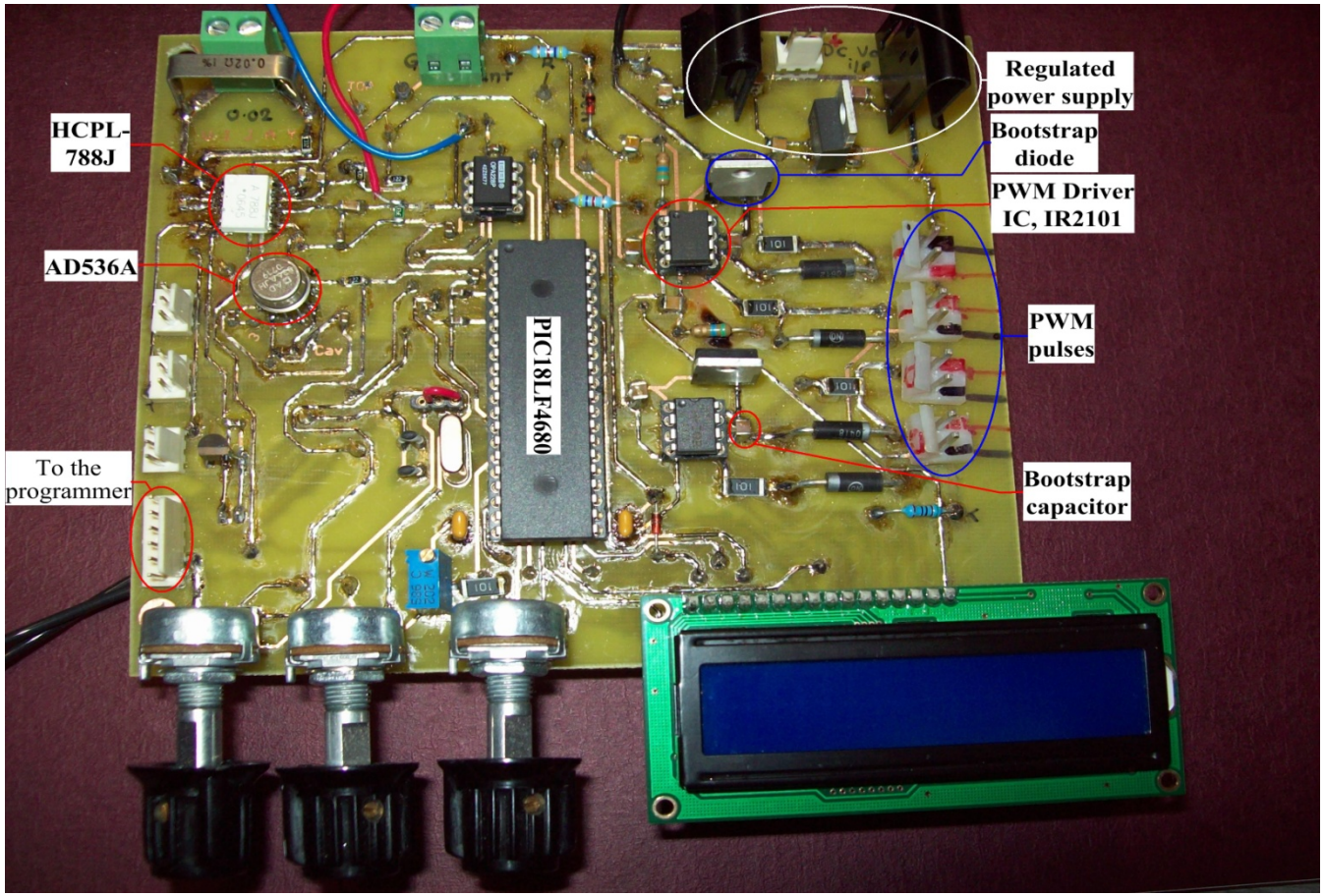


Figure 5.2: Controller board built for proposed single phase VSC based STATCOM

5.2. Regulated dual power supply

For proper controller board operation, the external supply should be rated for at least 17 V. Even if the voltage magnitude of the external power supply varies from 17 to 40 V, the controller board is equipped with a regulated power supply block as shown in figure 5.3. The regulator block guarantees a stable, reliable and noise free supply of power with the rated voltages required by all circuits/ICs mounted on the controller board. The circuits mounted on the controller board demand either +15 V or +5 V or ±5 V supply for their operation.

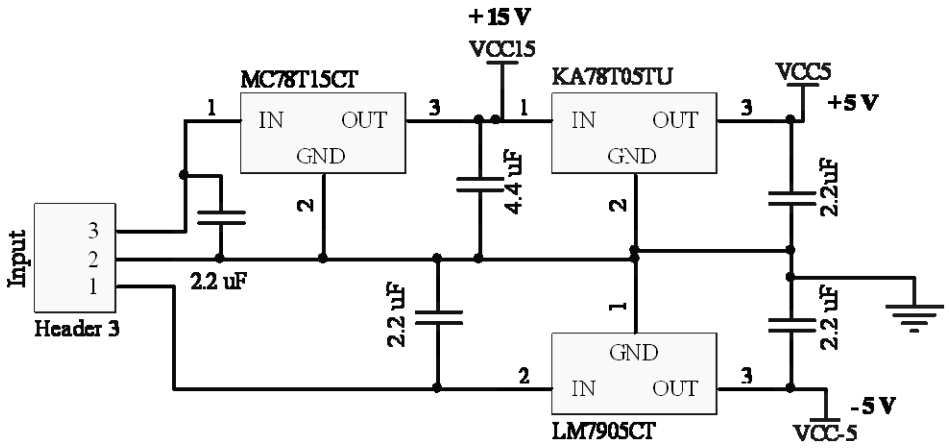


Figure 5.3: The dual supply regulator mounted on the controller board

The regulated power supply block consists of voltage regulator ICs as described in table 5.1,

Table 5.1: Regulator ICs used to build the dual supply regulator and their ratings

Regulator IC	Fixed output rating
MC78T15CT	15 V, 3 A
KA78T05TU	+5 V, 3 A
LM7905CT	-5 V, 1 A

Voltage regulator IC MC78T15CT derives a fixed 15 V supply from the external power supply. This fixed 15 V supply is used to derive a ± 5 V dual supply by

employing KA78T05TU (+ 5 V) and LM7905CT (-5 V) regulator ICs, with higher current ratings that make the supply very robust and reliable.

5.3 Micro-controller PIC18LF4680

An 8 bit fixed point micro-controller PIC18LF4680, manufactured by Microchip, is chosen as the main controller and used to execute the control algorithm. Its power consumption while in operation is as low as a few nanoWatts and can be operated from power supplies ranging from 2 to 5.5 V.

The PIC18LF4680 has a program memory of up to 64k bytes and a data memory of up to 1024 bytes. It is a 40-pin IC of which most pins are multiplexed with peripherals. These pins either can be used to perform specialised tasks such as A/D conversion, PWM generation, interrupt generation, etc., or can be assigned as input/output (I/O) ports. The detailed information about PIC18LF4680 along with the allocation of the micro-controller pins for accomplishing various applications is given in [26]. A description of various peripherals used to develop the control system for the proposed application is given in table 5.2.

The micro-controller employs a flexible oscillator structure. The frequency of the micro-controller oscillator can be varied from 31 kHz to 40 MHz. For building the prototype, the chosen frequency was 8 MHz. Too low a frequency can incur errors while running timers and/or counters. On the other hand, if the frequency of the operation is too high, timer and/or counter registers may overflow and run out of capacity.

Table 5.2: The list of peripherals of PIC18LF4680 used to develop an automatic control of a VSC based STATCOM.

Name of the peripheral	Application of the peripheral in the proposed system	Description/ remarks.
Analogue to digital conversion module	• Sensing the magnitude of the supply current, I_s. • Sensing the values corresponding to the proportional (K_p), integral time constant (T_i), reference I_q for the control system.	• Converts an analogue input signal to a corresponding 10 bit digital number. • Speed of conversion up to 100 ksps. • Auto acquisition capability.
Enhanced capture/compare/ PWM (ECCP) module	Generation of precisely controlled PWM signals for a 'H' bridge single phase converter.	• Up to 4 PWM outputs with selectable polarity. • Programmable precise dead time control. • In case of fault, auto shut down and auto-restart.
Analogue comparators	• Zero crossing detection of the voltage is used to synchronize the supply voltage with the converter output waveform. • Zero crossing detection of the supply voltage and current waveforms. This helps in the measurement of the phase angle, θ.	Dual channel with the capability of internal voltage reference configuration.
External interrupts	Input signal to an external interrupt forces the control program to take corrective measures, in case of odd situations like short circuits or overload current	3 individual programmable interrupts with selectable different priority levels.
Timers	• TIMER0 is used to measure the phase angle, θ. • TIMER2 is used to synthesize PWM waveform. Precise period and duty cycles are timed by TIMER2. • TIMER1 and TMER3 are used to shift the converter output PWM waveform with respect to the supply voltage.	• TIMER0 configured as an 8 bit counter. • TIMER2 is interfaced with the ECCP module and used as a 16 bit timer. • TIMER1 and TIMER3 are configured as 16 bit timers.

5.4 Sensing the control system parameters

System parameters are manually entered using a potentiometer as a voltage divider circuit. Figure 5.4 shows a voltage divider, commonly known as a 'pot'. The voltage magnitude (V_{pot}) across the pointer can be varied from 0 to 5 V with respect to ground by adjusting its position. The V_{pot} value is fed to the A/D converter of the micro-controller. The micro-controller samples the value of V_{pot}, and stores it as a 10 bit binary number. The control algorithm then re-calculates the actual value of the parameter by multiplying the number with an appropriate factor.

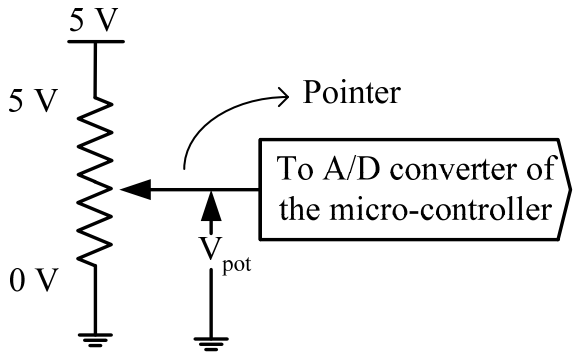


Figure 5.4: Application of a potentiometer for manually feeding analogue voltage values to the digital system

Control system parameters like proportional gain constant (K_p), integral time constant (T_i), reference I_q (Ref. I_q) are manually adjusted by adjusting the positions of the corresponding potentiometers mounted on the controller board. The schematic diagram is shown in figure 5.5.

A 0.1 μF capacitor with respect to ground eliminates any noise or transients in the d.c. voltage magnitude to be fed to the A/D converter of the micro-controller.

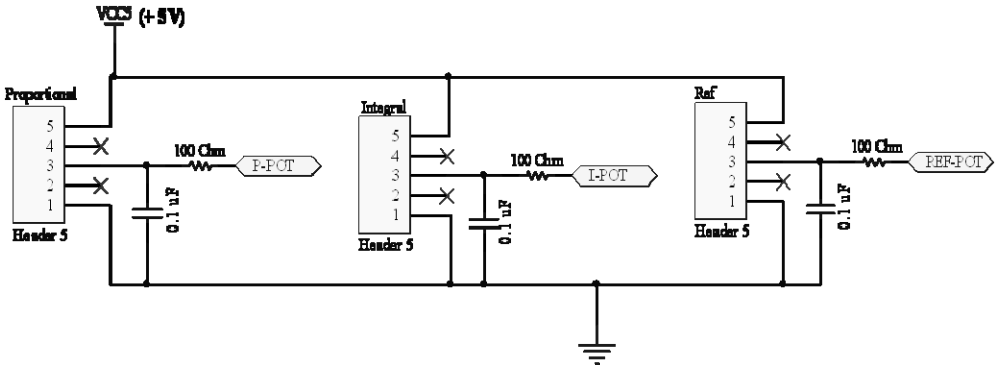


Figure 5.5: Potentiometers used for manually entering the analogue values for the control system to the digital system

The resistance value of 100 Ω in series with the A/D converter acts as a current limiter when V_{pot} approaches 5 V.

5.5 Sensing reactive component of the supply current

The control system proposed for the single phase STATCOM was discussed in section 8 of chapter 4. The input parameter for the control system is the magnitude of reactive current, I_q. This section explains the hardware built for measuring I_q. The explanation can be divided in following steps,

- Measurement of the magnitude of the supply current, I_s
- Measurement of the phase angle between the supply voltage and current, θ. This also includes determining whether it is leading, lagging or zero (unity power factor situation).
- Once the phase angle, θ, is available, the micro-controller computes $sin\theta$ up to 4 digit accuracy using the sine table programmed in its memory.
- The calculation, $I_s \times sin\theta$, is performed by the control program and the reactive component of the supply current, I_q, is obtained.

5.5.1 Measurement of the supply current, I_s

An isolation amplifier IC, HCPL-788J as shown in figure 5.6, is used to measure the supply current. It is designed for sensing current in electronic motor drives and its design enables ignoring very high voltage common mode transient slew rates (10 kV/µs). IC HCPL-788J also has features such as,

- Fast (3 µs) short circuit detection with transient fault rejection
- Absolute value signal output for overload detection
- Output compatible with digital circuits such as A/D converters or micro-controllers.
- The isolation capability between the input supply system and the output of the IC is up to 891 V_{PEAK}
- Better linearity, offset vs. temperature and common mode rejection (CMR) performance than most Hall-effect sensors.
- Can be operated within temperatures ranging from -40°C to +85°C.

These features make it a perfect fit for the proposed application.

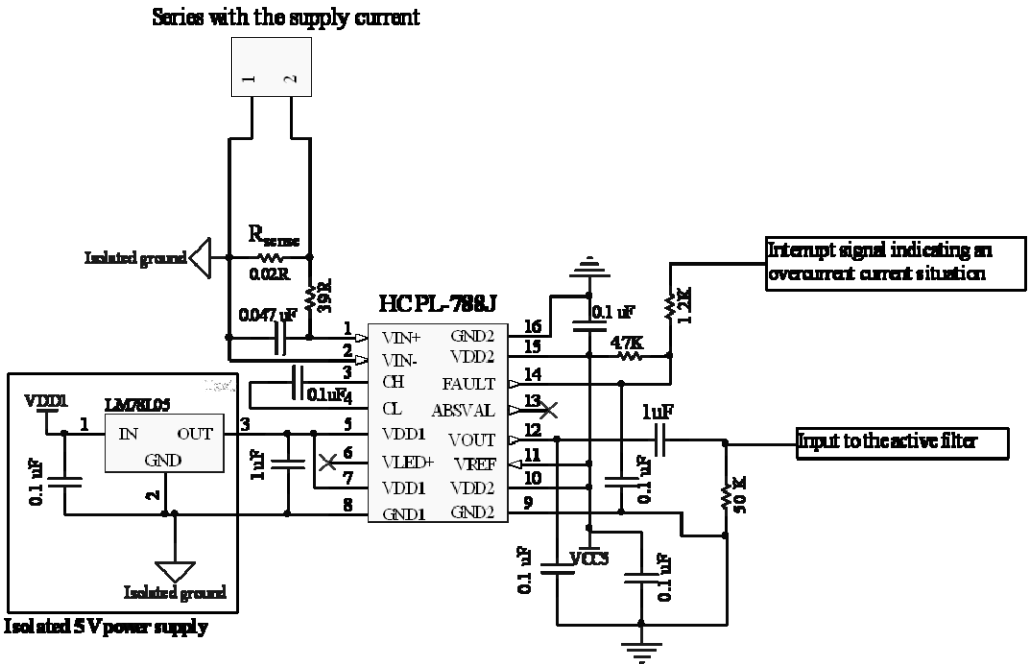


Figure 5.6: Schematic diagram of the optically isolated current sensing circuit using IC, HCPL-788J

A resistance of small value, R_{sense}, is inserted in series with the supply winding of the partial core transformer. The voltage drop across R_{sense} (in mV) is sensed by HCPL-788J. A larger analogue voltage (≈ 10 times the voltage drop across R_{sense}) is produced on the output side of the HCPL-788J's optical isolator barrier [27]. This output voltage at the V_{OUT} pin is proportional to the supply current. The d.c. component in the output waveform is eliminated by connecting a capacitor in series with the V_{OUT} pin.

The input and output sides of the HCPL788J are totally isolated from each other. The input side has its own dedicated 5 V power supply. The isolated 5 V supply is derived from a 5 V regulator connected to a 9 V battery on its input side.

5.5.1.1 Selecting a value for R_{sense}

In order to minimise the power losses, the value of R_{sense} is kept as low as possible. Selecting a proper value of R_{sense} is a compromise between minimising the power losses and maximising the accuracy. The value of R_{sense} is chosen in such a way that it minimises the power losses, has low inductance which minimises di/dt induced voltage spikes, and utilises the full input range of the HCPL-788J [27].

Currently the maximum rms current at which the system is designed is 10 A. Assuming a maximum input voltage of 250 mV, then the maximum value of R_{sense} is,

$$R_{sense} = \frac{250\ \text{mV}}{10\sqrt{2}} = 17.7\ \text{m}\Omega$$

The nearest available and chosen value for R_{sense} is 20 mΩ. This limits the supply current up to 8.8 A.

5.5.2 Nature of harmonic distortion problem

The supply current contains harmonics due to PWM switching. As discussed previously, pin number 12, i.e. the V_{OUT} pin of the HCPL-788J, produces an amplified waveform of the voltage drop sensed across the input side of the HCPL-788J. The voltage waveform obtained at the V_{OUT} pin also contains harmonics.

Since the distorted waveform may contain multiple zero crossings, the zero crossing detection circuit employed for measuring the phase angle, θ, would be vulnerable to false and multiple zero crossing detentions. The presence of harmonics in the control signal may affect accurate measurement of the supply current, I_s.

The voltage supply is not an ideal one but has a finite value of input impedance; high frequency switching spikes are observed in it. These spikes may confuse the zero crossing detection circuit as discussed above.

Zero crossing detection for the voltage waveform is not only important from the phase angle measurement point of view, but the total process of synchronism between the supply voltage waveform and the converter output waveform is solely dependent on it. It is absolutely essential to design a robust filter which rejects all higher order harmonics and high frequency spikes.

5.5.3. Dual channel active filter design

A dual channel, 4 pole Butterworth active filter was designed using the FilterPro^{TM} computer aided design program, and added externally to the main control board [28].

A Butterworth filter has advantages such as,

- Excellent flat magnitude response in the pass-band
- Good all around performance
- Pulse response better than Chebyshev

- Rate of attenuation better than Bessel

The filter is designed for a 50 Hz cut-off frequency using the FilterPro™ software. Figure 5.7 demonstrates the performance of the filter by gain, phase and group delay traces. The blue line indicates the 50 Hz frequency mark. The circuit diagram for the active filter is shown in figure 5.8.

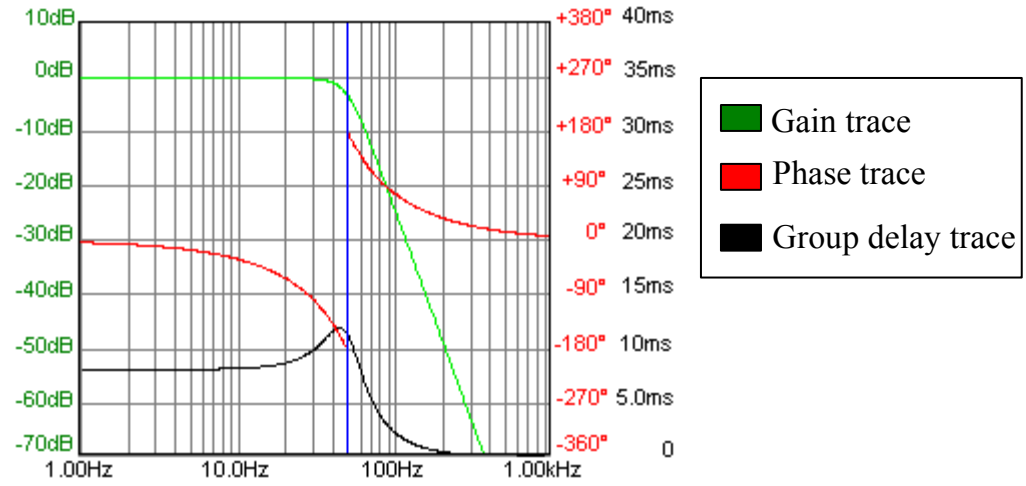


Figure 5.7: Performance of the 4 pole, Butterworth active filter

As shown in figure 5.9, two universal active filter ICs, UAF42, are used to build the proposed dual channel active filter. It is a monolithic IC that contains the operational amplifiers, matched resistors and precision capacitors needed for the state-variable filter pole pair. The state variable topology has low sensitivity of filter parameters to external components. The two filters built with UAF42 are time-continuous, free from the switching noise and aliasing problems of the switched capacitor filters [29].

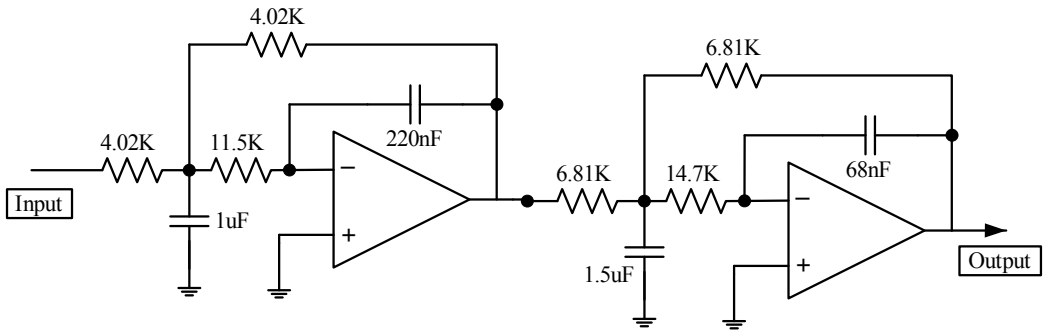


Figure 5.8: Four pole, low pass Butterworth filter

Although the designed filter shifts the actual waveform by 180.7° the correction is done by using an uncommitted precision operational amplifier available in the IC itself as an inverter. In total phase shift of 360.7° is added to the actual waveform. The filter totally eliminated problem of multiple false zero crossings and sinusoidal waveforms are obtained. Figure 5.9 shows the photo of the dual channel filter.

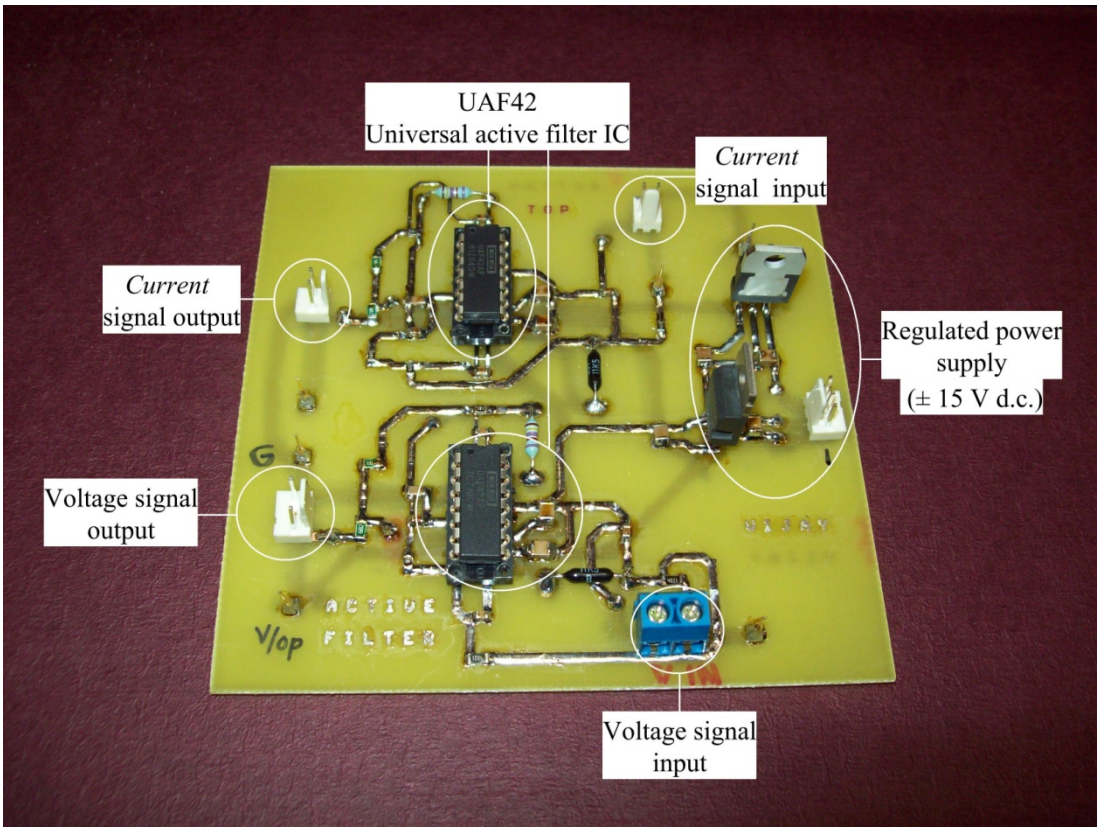


Figure 5.9: Dual channel, 4 pole Butterworth active filter built using IC, UAF42

5.5.4 True rms to DC converter, AD536A

The output waveform of one of the channels of the active filter that corresponds to the supply current, is directly fed to the input of the true rms to d.c. converter, AD536A. The IC calculates the true rms value of the a.c. input waveform and gives an equivalent d.c. value as an output. The ripple content in the d.c. waveform is dependent on the value of an averaging capacitor, $C_{AV,}$ which should be connected externally. The higher the value of C_{AV}, the lower is the

ripple content in the output of AD536A, but this means the averaging time increases.

For selecting a value of C_{av}, the datasheet of the AD536A gives tips and logarithmic curves. After performing some experiments in the laboratory, the value of C_{AV} was selected as 4.3 μF, which corresponds to a 107.5 ms averaging time (time constant = 25 ms per μF). The output of the AD536A is connected to the A/D pin of the micro-controller. The A/D converter samples the waveform and the exact value of the supply current, I_s, is calculated in the control program. A schematic diagram of IC AD536A is shown in figure 5.10.

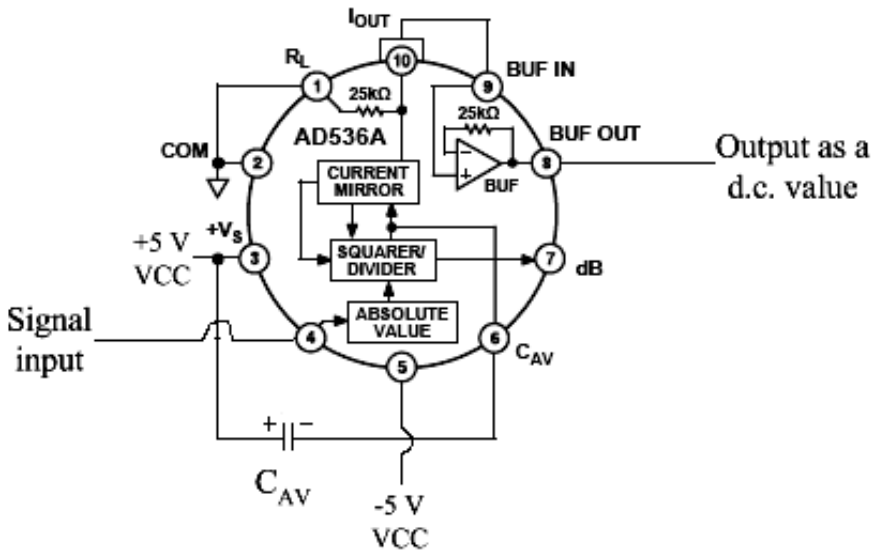


Figure 5.10: Pin diagram and internal structure of a r.m.s. to d.c. converter IC, AD536A [30]

5.5.5 Determination of the phase angle, θ

The filtered a.c. waveforms (corresponding to the supply voltage and current) from the active filter are rectified and clipped using two 4.7 V, 60 mW Zener diode networks, one each for the supply voltage and current as shown in figure 5.11. Rectification is necessary because waveforms fed to the micro-controller should be non-negative.

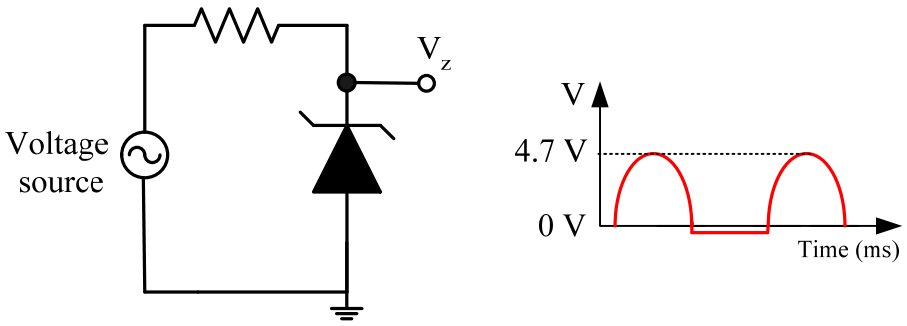


Figure 5.11: A Zener diode network and the voltage waveform across the point V_z

Voltage waveform across the Zener diode corresponding to the supply voltage is fed to the comparator, C_1 while waveform across the Zener diode corresponding to the supply current is fed to the comparator, C_2. Both comparators are embodied within the micro-controller. Figure 5.12 shows an example of an analogue comparator and the output voltage, V_{comp}.

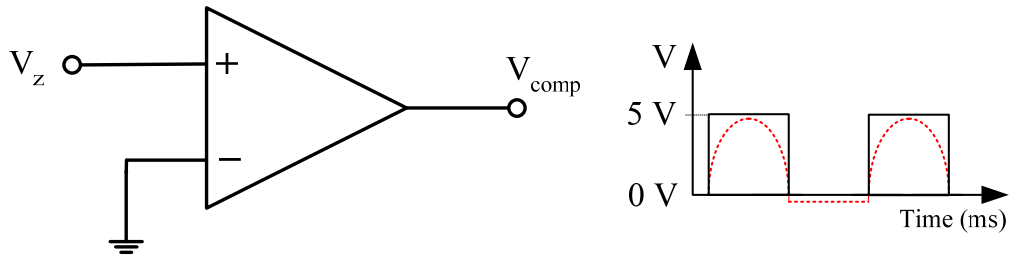


Figure 5.12: An analogue comparator and output voltage, V_{comp}

5.5.5.1 Detection and measurement of a phase angle when it is lagging

Comparator C_1 of the microcontroller detects the positive voltage level of the supply voltage waveform and changes its status from 0 to 1. At this point of detection, the micro-controller is programmed to check the status of the comparator, C_2. If the status of the comparator, C_2 is 0 as shown in figure 5.13, i.e. C_1=1 and C_2=0. It indicates that, the current is lagging behind the voltage; hence the variable in the control program stores this case as 'lagging'.

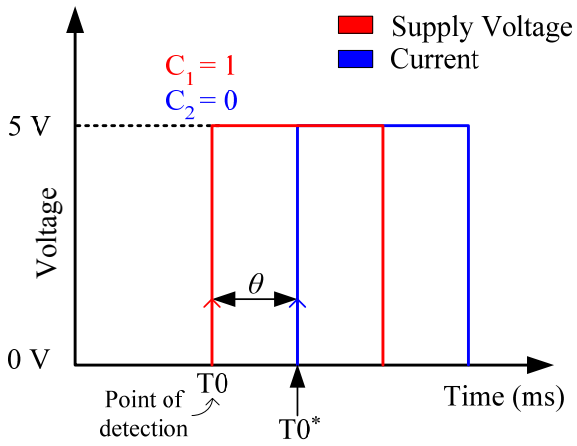


Figure 5.13: Lagging phase angle situation as seen by micro-controller

The control algorithm commands the measurement of the phase angle, θ, to be carried out every 120 ms. It is achieved by using an 8 bit timer, Timer0. This timer is configured as a counter. Timer0 starts to count at the point of detection, T0, and stops at $T0^*$. In case of lagging phase angle situations, $T0^*$ is the point at which the status of comparator C_2 changes from 0 to 1. The number of counts is stored in the register, TIMR0L, and is directly proportional to the phase angle, θ. The control program calculates the actual value of θ by dividing the number of counts stored in TMR0L register by an appropriate factor.

5.5.5.2 Detection and measurement of a phase angle, θ when it is leading

As shown in figure 5.14, at the point of detection, if the status of both the comparators C_1 and C2 are observed is 1, it indicates that the system has a leading phase angle.

If the nature of the phase angle θ is detected in the 'n^{th}' positive cycle, then its measurement is carried out in the negative half of the same cycle. The control program keeps a track of the time interval.

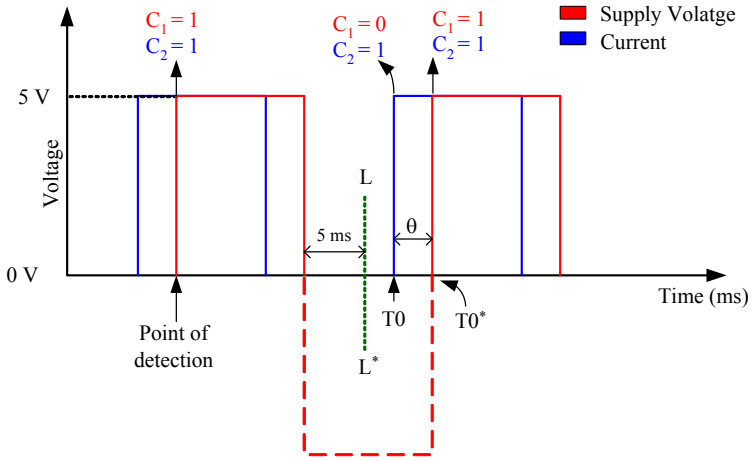


Figure 5.14: Leading phase angle situation as seen by micro-controller

The line L-L* indicates 270° in a typical sine wave. Before this line, the level of the current waveform is 0 V, and the status of comparator, C_2, is also 0. After crossing the line L-L*, comparator C_2 constantly checks the level of the current waveform.

At T0, comparator C_2 changes its status from 0 to 1 while the status of comparator, C_1 is 0. At this point, Timer0 starts to count the time and stops at T0* where the supply voltage changes its level from 0 to 5 V, i.e. comparator C_1 changes its status from 0 to 1. The number of counts stored in register TMR0L is directly proportional to the phase angle θ, and its actual value is calculated in the control program.

5.5.5.3 Unity power factor situation

As shown in figure 5.15, when the supply voltage and current waveforms coincide, the phase angle, θ, is zero. The system power factor is unity.

Measurement of unity power factor is accomplished by the same technique described as for the leading phase angle condition. At the point of detection, the control program concludes that the system has a '*leading*' power factor.

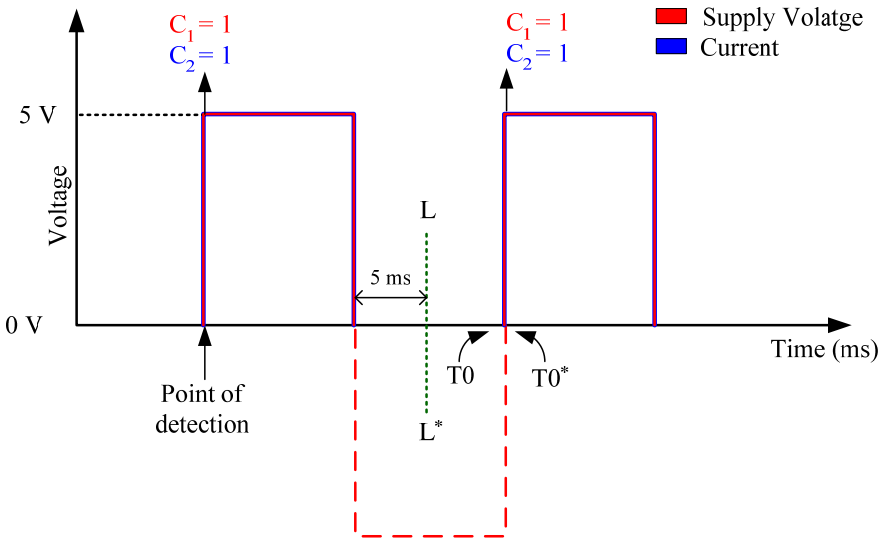


Figure 5.15: Unity power factor situation as seen by the micro-controller

Comparator, C_2 detects the positive level of the current waveform and changes its status from 0 to 1. Exactly at this point, comparator C_1 also changes its status from 0 to 1. Due to the higher oscillator frequency of the micro-controller, the TIMR0L register may have a number of counts more than zero, as the control program also takes 4 clock cycles to execute each command (checking the status of comparator, C_1) but the actual value of the corresponding phase angle, θ is less than 1°. A phase angle, θ less than 1° is approximated to 0°.

5.5.6 Computing the magnitude of I_q

The steps involved in measuring the magnitude of the supply current, I_s are described in sections 5.1 to 5.5. Section 5.6 deals with detecting the nature and magnitude of the phase angle, θ. A look up table consisting of '*sine*' values corresponding to angles ranging from 0° to 90° is stored in the memory of the micro-controller.

From the measured phase angle, θ, the control program computes its '*sine'* value and then the product of I_s and $sin\theta$ to obtain the magnitude of I_q. If the phase angle is lagging, I_q is assigned –ve. On the other hand, if the phase angle is leading, Iq is assigned +ve.

5.6 Driving a liquid crystal display (LCD)

A LCD plays important roles in providing an interface for the user, and debugging an application. The LCD controller used in this application is the Hitachi 44780. The LCD display module has 2 lines each with 16 characters. In the proposed application, speed of data transfer from the micro-controller to the LCD display is a critical factor; hence parallel data transfer in an eight bit mode was the best option. The LCD displays the following parameters from the system,

- Magnitude and nature (lagging or leading) of the phase angle, θ. Phase angle, θ is expressed in degrees and its sine value is also displayed.
- Magnitude of the proportional constant (K_p)
- Magnitude of the integral constant (K_i)
- Magnitude of the reference reactive component of current, Ref. I_q.
- Reactive component of current, I_q
- Phase angle δ, the angle between the supply voltage and converter output voltage.

Each parameter is displayed for 5 seconds and updated every 30 seconds.

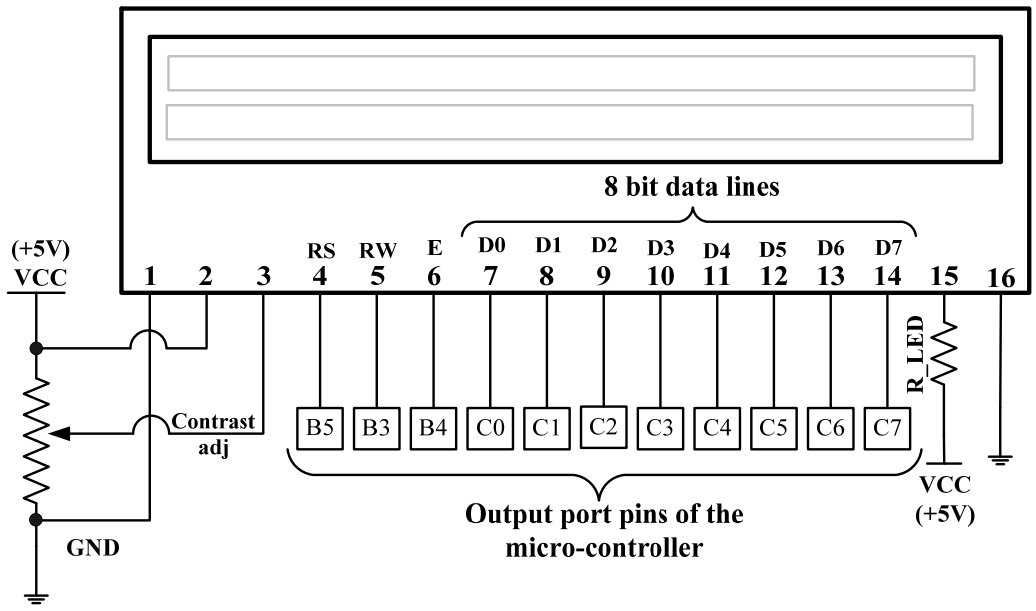


Figure 5.16: A LCD interfaced with the micro-controller in parallel 8 bit data transfer mode

Figure 5.16 demonstrates the interfacing of the LCD with the micro-controller. The supply voltage, VCC, required for correct operation of the LCD is +5 V. The magnitude of the voltage at pin no. 3 determines the contrast (or darkness) of the characters on the LCD screen. This voltage is varied using a potential divider circuit.

For the proposed application, only one way communication is essential, i.e. the micro-controller transfers data to be displayed to the LCD and not the other way round. The RS bit (4^{th} pin of the LCD) is used to select whether data or an instruction is being transferred from the micro-controller to the LCD. If the bit is set, then *8 bit data* at the current cursor position of the LCD can be written. On the other hand, if the bit is reset, an *instruction* is sent to the LCD [31].

When the R/W bit (5^{th} pin of the LCD) is set, the data is read from the LCD. If the R/W bit is reset, the data is written to the LCD. A dedicated library built for LCDs in 'MikroC' software program deals with this bit. The software program gives enough time to transfer data from the micro-controller to the LCD before transmitting the next data or instruction. This minimises the complexity of the program.

Data bits from D0 to D7 are used for transferring the 8 bit data from the micro-controller to the LCD. The clock pulse at E bit (6^{th} pin of the LCD) is used to initiate the data transfer within the LCD.

In order to see the displayed characters clearly, LCD has its own light emitting diode, LED. The supply (+5 V) to the LED is given by pins 15 and 16. Resistance, R_LED, not only limits the current passing through the LED but also controls the brightness of the LED.

5.7 Summary

The chapter has presented the design and development of the hardware part of the control system built for the automatic control of the VSC based STATCOM.

Major components of the system such as the regulated power supply, micro-controller, optically isolated current sensing circuit, and dual channel active filter zero crossing circuits, are explained in detail with schematic diagrams and/or photos. The process of measuring the magnitude of reactive component of the supply current, I_q is elaborated step by step. Section 5.6 described the programming of a LCD in 8 bit parallel transfer mode.

Chapter 6

Development of power circuit for the VSC based STATCOM

6.1 Overview

In Chapter 5, design and development of the hardware circuit used to implement the closed loop control system was discussed. This chapter describes the design and development of the power circuit.

The control circuit and the power circuit are electrically isolated from each other. The input parameters required for the control system such as the supply current and voltage waveforms are sensed in the supply winding, while the power circuit is connected to the tertiary winding of the partial core transformer. This completely eliminates the problems involved in accidental ground loops and protects the control circuit from the high voltages in the power circuit.

Since incidents such as over currents, over voltages, transients, faults etc. were expected while performing experiments on this prototype STATCOM (especially during the initial stages), the ratings of the components used are of much higher rating than those shown by the actual calculations.

6.2 Power circuit components

The concept of the VSC based STATCOM controlled partial core transformer along with its detailed schematic diagram is described in Section 4.4 of Chapter 4. Figure 6.1 shows the detailed diagram of the power circuit in the tertiary winding of the partial core transformer.

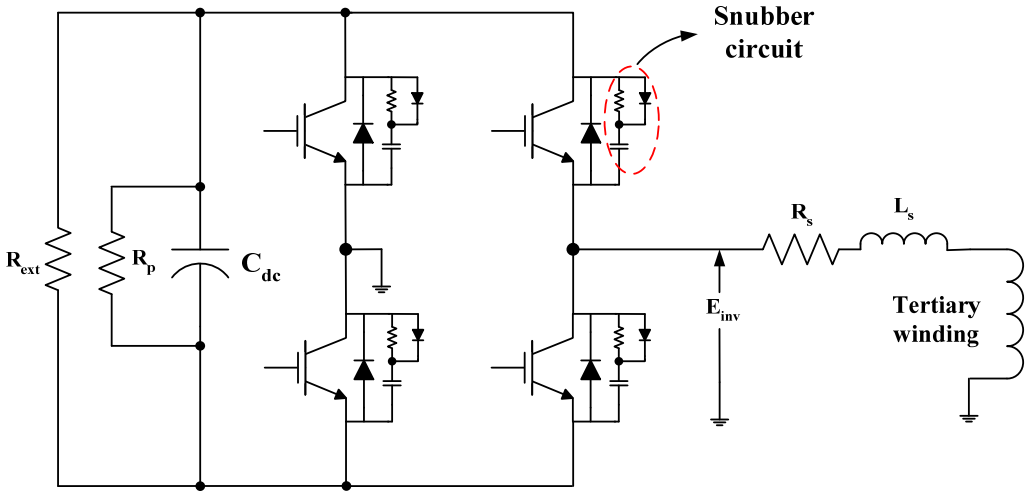


Figure 6.1: Power circuit in the tertiary winding

It consists of the following components,

- IGBTs in 'H' bridge configuration and the IGBT driver circuit (shown in figure 6.5),
- Snubber circuit to protect IGBTs from switching stresses.
- Current limiting reactor, L_s
- D.C. capacitor for energy storage, C_{dc}
- Series resistance, R_s, represents the total active losses in the tertiary winding and the inverter.
- Parallel resistance across the d.c. capacitor, R_p, represents the losses in the capacitor.
- A charged high voltage capacitor may prove a fatal hazard. Safety of the system is improved by connecting an external resistance, R_{ext} of 10 kΩ value across the terminals of the d.c. capacitor. This resistance serves the purpose of discharging the d.c. capacitor when the circuit is de-energised.

6.2.1 Selection of IGBTs for the 'H' bridge inverter

IGBTs are becoming increasingly popular for inverter circuits used in power electronics applications. They are superior to MOSFETs in many high voltage, hard switching applications as they have lower conduction losses and smaller die area for the same output power. The smaller die size means lower cost and less

input capacitance. Switching losses in the IGBTs are low for frequencies up to 20 kHz [32]. Detailed information about IGBTs can be obtained from [27].

A 600 V, 20 A, 3 phase IGBT module (BSM 20 GD 60 DN2) manufactured by EUPEC, Germany was already available in the Electrical Engineering Department and it was suitable for the proposed application. A photo of the IGBT module is shown in figure 6.2.

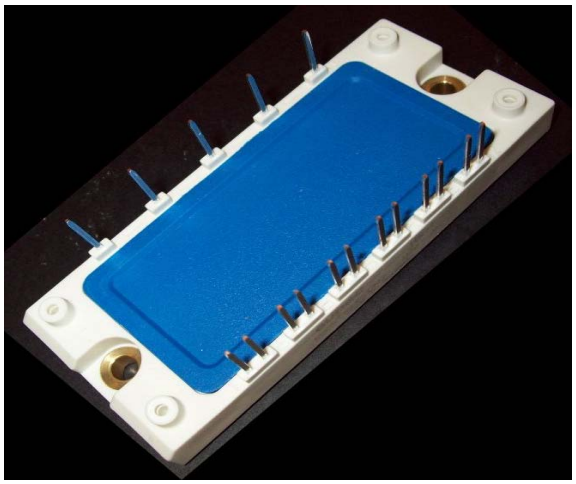


Figure 6.2: A photo of the IGBT module, BSM 20 GD 60 DN2

Internal structure of the IGBT module is shown in figure 6.3. It consists of three legs, each with two IGBTs. Each IGBT has its own free wheeling diode across it. For a single phase application, four IGBTs out of six were used.

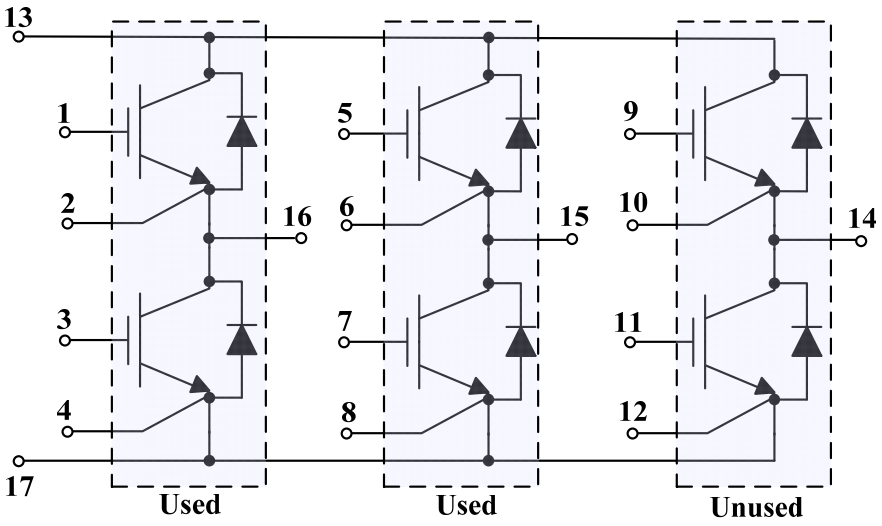


Figure 6.3: Internal structure of the IGBT module [33]

6.2.2 Driver requirements for the high and low side IGBTs

As described previously, the converter comprises of two individual legs, each consists of a high side IGBT and a low side IGBT. One of the legs is shown in figure 6.4.

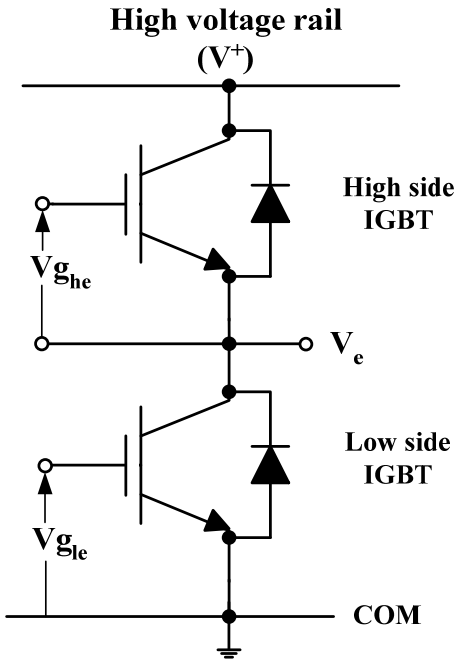


Figure 6.4: IGBTs in the high side and low side configuration

Collector of the high side IGBT is connected to the high voltage rail. In this case, the gate voltage, Vg_{he} must be 10 V to 20 V higher than the voltage, V_e, at the emitter of the high side IGBT. In most cases, Vg_{he} is the highest voltage available in the system.

The micro-controller logic which produces the gate voltages is normally referenced to ground. Thus, the control signals have to be level shifted to the emitter voltage, V_e, of the high side IGBT. The gate voltage at the high side IGBT swings between V_e and Vg_{he}. The gate voltage, Vg_{le} must be between 10 V to 20 V with respect to ground (COM) for turning on the low side IGBT [34].

6.2.3 Selection of the IGBT driver IC

International Rectifier's MOS-gate drivers (MGDs) integrate most of the functions required to drive one high and one low side power MOSFET or IGBT in a compact, high performance package. They operate on the bootstrap principle with a floating power supply. With the addition of few components, they can operate in most applications from frequencies in the tens of Hz to hundreds of kHz with low power dissipation.

The most important parameter required for the correct power dimensioning of the IGBT driver is the gate charge, Q_G. For a given IGBT, its value can be found out using equation,

$$Q_G = C_{IN} \times \Delta V_{GE} \tag{6.1}$$

where, C_{IN} is the input capacitance of the IGBT and ΔV_{GE} is the total voltage rise at the gate i.e. the driving voltage from 0 to +15 V.

The value given in the datasheet of the IGBT for defining the input capacitance, C_{iss}, does not represent its *actual* input capacitance, C_{IN}. As a rule of thumb, experience with IGBTs manufactured by SIEMENS and EUPEC has shown that the following conversion for the input capacitance yields sufficient accuracy [35, 36].

$$C_{IN} \cong 5 \times C_{iss} = 5 \times 1100\ pF = 5500\ pF \tag{6.2}$$

The value of the gate charge, Q_G is obtained by putting the values of C_{IN} and ΔV_{GE} in equation 6.3,

$$Q_G = 5500 pF \times 15 = 82.5\ nC \tag{6.3}$$

Power dissipated in the two channel IGBT driver is given by,

$$P_G = 2 \times f \times C_{IN} \times \Delta V_{GE}^2 = 2 \times 1350 \times 5500 \times 10^{-12} \times 15^2 = 3.34\ mW \tag{6.4}$$

International Rectifier's power MOSFET/IGBT driving IC, IR2101 was selected. The 8 pin PDIP package of this IC is rated for 1 W. The maximum short circuit pulsed current rating when the output of the IC goes high (i.e. logic 1) is 210 mA [37].

6.2.4 Determining parameters for the bootstrap circuit

As shown in figure 6.5, basic components of the bootstrap circuit consists of a bootstrap capacitor, C_B, bootstrap diode, bootstrap resistor, R_{boot}, a capacitor between VCC to COM, C_{COM}, which supports both the low side output buffer and bootstrap recharge. Detailed information about the bootstrap technique can be found in [34].

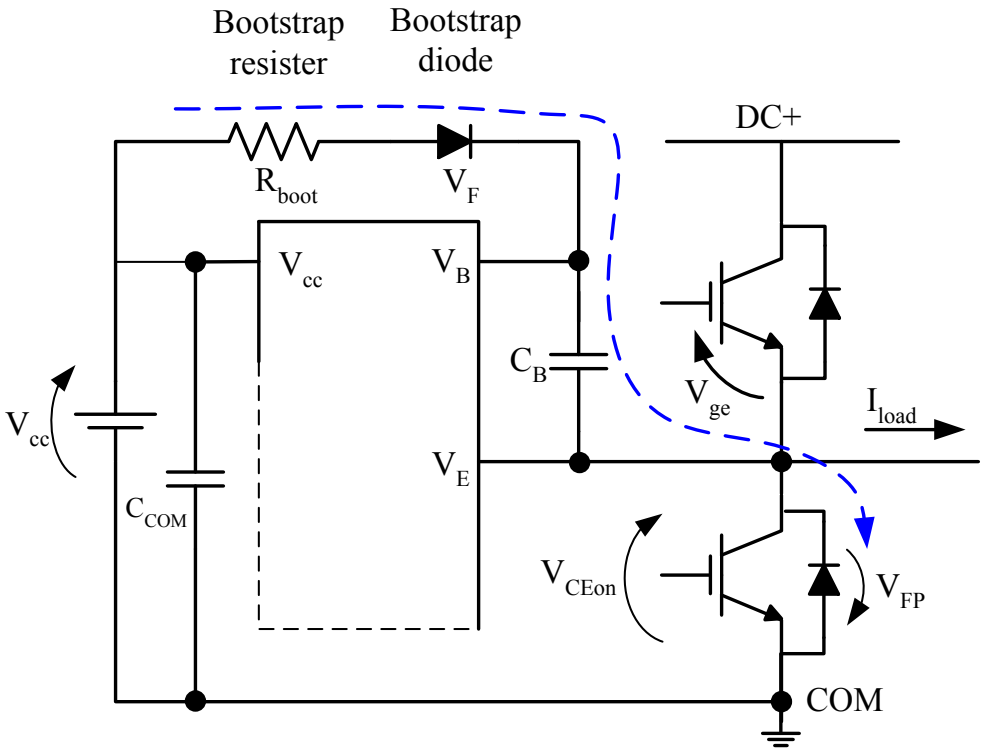


Figure 6.5: Schematic diagram of a bootstrap circuit

6.2.4.1 Selecting a bootstrap diode

The bootstrap diode must be able to block the full voltage, i.e. the voltage across the power rail. It should also have an ultra-fast recovery (t_{rr} < 100 ns) to reduce the amount of charge that is fed back from the bootstrap capacitor, C_B into the supply. Time required for charging the bootstrap capacitor, C_B can be reduced by using a bootstrap diode with higher current rating.

Considering the above requirements, MUR8100E ultra-fast diode was chosen. It is rated for 800 V, 8 A. Voltage rating of the bootstrap diode is chosen to be much higher than the required value because of its critical role in the bootstrap circuit.

6.2.4.2 Selecting a bootstrap capacitor, C_B

The minimum size of the bootstrap capacitor, C_B required for proper functioning of the bootstrap circuit depends on various constrains mentioned in table 6.1.

Table 6.1: Parameters of the components required for designing the bootstrap circuit.

Description	Symbol	Value	Unit	Reference (datasheet)
Emitter-collector voltage of a low side IGBT	V_{CEon}	2.8	V	BSM20GD60DN2
Minimum gate-emitter voltage	V_{GEmin}	10	V	
IGBT turn on required gate charge	Q_G	65	nC	
IGBT gate-source leakage current	I_{LK_GE}	100	nA	
Supply voltage for IC	V_{CC}	15	V	IR2101
Floating section quiescent current	I_{QBS}	55	µA	
Floating section leakage current	I_{LK}	50	µA	
Bootstrap diode forward voltage	V_F	1.8	V	MUR8100E
Bootstrap diode leakage current	I_{LK_DIODE}	25	µA	
Charge required by the internal level shifters	Q_{LS}	5	nC	[34]
High side turn on time	T_{HON}	740	µs	

To select a suitable size for the bootstrap capacitor, C_B, the first step is to establish the minimum voltage drop (ΔV_{BE}) that has to be guaranteed when the high side IGBT is on. The value of ΔV_{BE} is calculated using equation 6.5

$$\Delta V_{BE} \leq V_{cc} - V_F - V_{GE\min} - V_{CEon} \tag{6.5}$$

Using the values from table 6.1, $\Delta V_{BE} = 0.4$

The total charge, Q_{TOT} can be calculated using equation,

$$Q_{TOT} = Q_{GE} + Q_{LS} + \left(I_{LK\_GE} + I_{QBS} + I_{LK} + I_{LK\_DIODE}\right) \times T_{HON} \tag{6.6}$$

Putting the appropriate values from table 6.1, in equation 6.6, the calculated value of Q_{TOT} is 166.4 nC. The minimum value of bootstrap capacitor is given by,

$$C_B \geq \frac{166.4\ nC}{0.4\,V} = 416\ nF \tag{6.7}$$

Other factors which influence the value of C_B are;

- Higher value of C_B improves the quality of local decoupling and reduces the risk of overcharging from severe V_E overshoot.

- This type of bootstrap capacitor sizing approach considers only the amount of charge that is needed when the high voltage side of the driver is floating and the IGBT gate is driven once. It does not take into account both the duty cycle of the PWM and the fundamental frequency of the current.

- The type of PWM waveform, i.e. six step, 12-step, SPWM also should be considered with their own peculiarity to achieve the best bootstrap circuit sizing [30].

Considering the above mentioned constraints, and performing independent experiments in the laboratory C_B is chosen to be substantially oversized, at 2.2 µF, 25 V (ceramic type).

6.2.4.3 Selecting the size of the capacitor, C_{COM}, from V_{CC} to COM

- Since the capacitor, C_{COM}, supports both the low side output buffer and recharges the bootstrap capacitor, the value for this capacitor should be *at least* ten times higher than C_B [34].

- A 22 µF i.e. ($10\times C_B$), 16 V, ceramic type capacitor was selected as C_{COM}.

6.2.4.4 Boot strap resistor

As shown in figure 6.5, the resistor, R_{boot}, is inserted in series with the bootstrap diode for limiting the current, I_{boot}, through the bootstrap diode, when the bootstrap capacitor is initially charged. Its value is calculated using equation 6.8

$$R_{boot} = \frac{V_{CC}}{I_{boot}} = \frac{15}{8} = 1.87\,\Omega \text{ (minimum)} \tag{6.8}$$

The choice of bootstrap resistor, R_{boot}, is also related to the V_{BE} time constant. The actual value of R_{boot}, chosen is 3.3 Ω. The bootstrap circuit RC time constant, $\tau_{bootstrap}$, is given by,

$$\tau_{bootstrap} = R_{boot} \times C_B = 3.3 \times 2.2\,\mu s = 7.26\,\mu s \tag{6.9}$$

Since $\tau_{bootstrap}$ is much less ($\cong 10\ times$) than the period of the SPWM waveform, the bootstrap circuit should work without any trouble.

6.2.5 Gate resistance, R_G

The value of the gate resistor, R_G has a significant impact on the dynamic performance of the IGBT. A smaller gate resistor will charge/discharge the gate capacitance faster, reducing the switching times and losses. On the other hand the use of smaller gate resistances is not recommended due to following reasons,

- During turn off of the free wheeling diode across an IGBT or under short circuit conditions, the dv/dt applied to the IGBT and its collector to gate capacitance can cause a current to flow in the gate circuit. If this current is large enough the voltage developed across the gate resistor can cause the IGBT to turn on.

- They provide reduced margin for noise and can lead to oscillation problems in conjunction with the gate-emitter capacitance and any parasitic inductance in the gate drive wiring.

- Smaller gate resistors allow faster turn-on di/dt of the IGBT. This may cause high dv/dt and increased surge voltage at free wheeling diode recovery [27].

Considering the above constraints, the recommended values of R_G in the IGBT datasheet and the output current rating of the IGBT driver IC, IR2101, the gate current, I_G, is limited to 150 mA (peak). The gate resistance to be inserted in series is given by,

$$R_G = \frac{\Delta V_{GE}}{I_G} = \frac{15\,V}{150\,mA} = 100\,\Omega \tag{6.10}$$

6.2.6 Snubber circuit considerations for the IGBT inverter

Reliable operation of an IGBT demands that its specified ratings are not exceeded. A snubber circuit reduces the switching stresses to safe levels and shape the load line to keep it within the safe operating area (SOA) by,

- Limiting voltages applied to devices during turn-off transients.
- Limiting rate of rise (dv/dt) of voltages across devices device turn off or during reapplied forward blocking voltages
- Reducing total losses during switching
- Transferring power dissipation from the switch to a resistor

Although there are many topologies for designing snubber circuits the most common ones are the resistor-capacitor (RC) and resistor-capacitor-diode (RCD) networks. These are discussed in [24, 32].

6.2.6.1 Choosing snubber component values

RC snubbers are very effective for low and medium power applications up to a few hundred watts. When power levels increase, losses in the snubber can be excessive and this issue requires considering other types of snubbers. The chosen RCD snubber as shown in figure 6.6 has several benefits over the RC snubber:

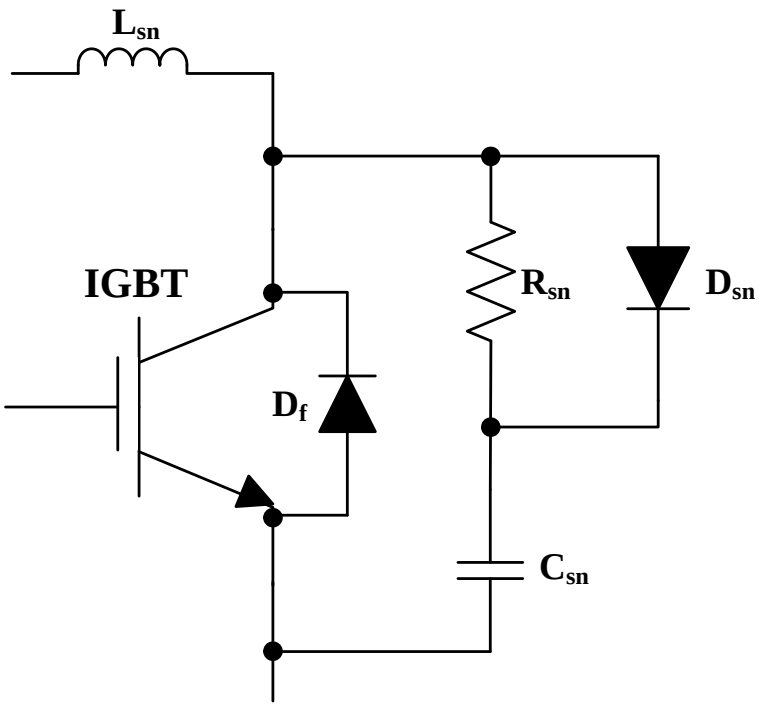


Figure 6.6: RCD snubber circuit for an IGBT

- Apart from peak voltage limiting, the circuit can reduce switching as well as snubber losses.
- The total losses will be less for a given value of C_{sn}.
- Better load lines can be obtained which allows the loss line to remain well within the SOA

It suffers from major disadvantage that is the effective value of R_{sn}, during the charging of C_{sn}, becomes zero due to presence of the diode across R_{sn}. This is not the optimum value and voltage across the capacitor, C_{sn} will be higher than it would be in an optimised RC snubber network.

6.2.6.2 Design of the snubber circuit

- Value of C_{sn} is given by equation [32],

$$C_{sn} = \frac{I_0 t_s}{2E_0} \tag{6.11}$$

where, I_0 is the rated current for the IGBT module i.e. 20 A, t_s is fall time of the switch current. The value of t_s was taken as 1.50 µs (3 times the value given in the datasheet of the IGBT). E_0 = 300 V, the maximum expected voltage across the d.c. rail. Putting these values in equation 6.11, the value of C_{sn} is obtained as 50 nF. The actual value of the capacitor, C_{sn} employed to implement the snubber circuit is 47 nF.

- The value of R_{sn} is chosen to allow the voltage on C_{sn} to decay to a small value during the minimum switch on time ($t_{on,min}$). The capacitor voltage decay is a RC exponential and in two time constants ($\tau = R_{sn} \times C_{sn}$)will be down to 0.14 E_0. The selected value of R_{sn} is 20 Ω.

6.2.7 D.C. link

The D.C. link which makes the connection between the d.c. capacitor terminals and the converter d.c. side terminals is made up of two parallel plates, with each polarity on the either side of the printed circuit board (PCB). This significantly minimises d.c. loop inductance, and hence the need of snubber circuit is not a critical issue. A photo of the PCB is shown in figure 6.7.

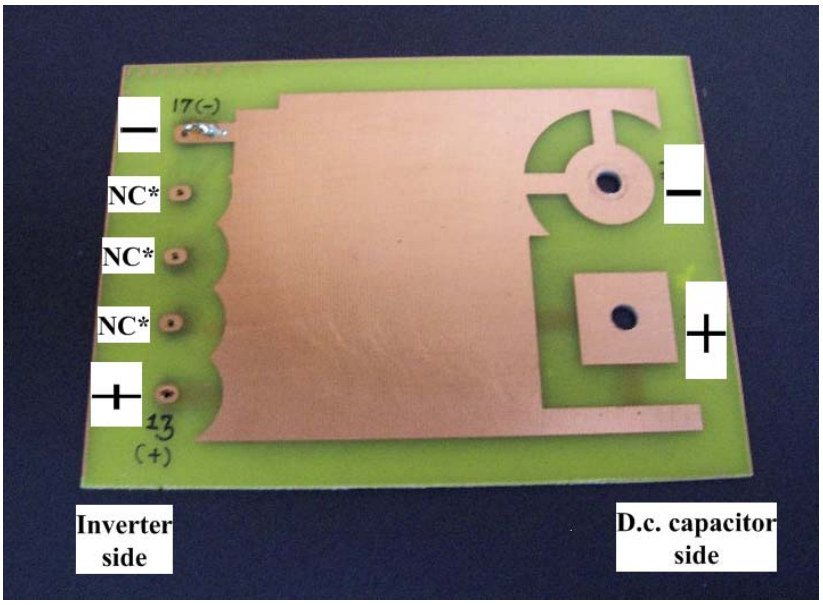


Figure 6.7: PCB with two parallel plates, one on each side

6.2.8 Verification of the Snubber design

A detailed diagram of the parallel plate is shown in Fig. 6.8, in which '*d1'* and '*d2'* represent thickness and length of the PCB respectively. The width of the metallic circuit is indicated by 'w'. Assume that d.c. current, i_{dc}, in the metallic top layer flows from the d.c. capacitor to the inverter d.c. side. According to Faraday's right hand rule, it can be concluded that the magnetic field produced by i_{dc} comes out in the 'm' direction and penetrates into the PCB cross section which is formed by the 'd1' and 'd2' sides. The magnetic field distributed in air is ignored since it is too weak to consider for the calculations.

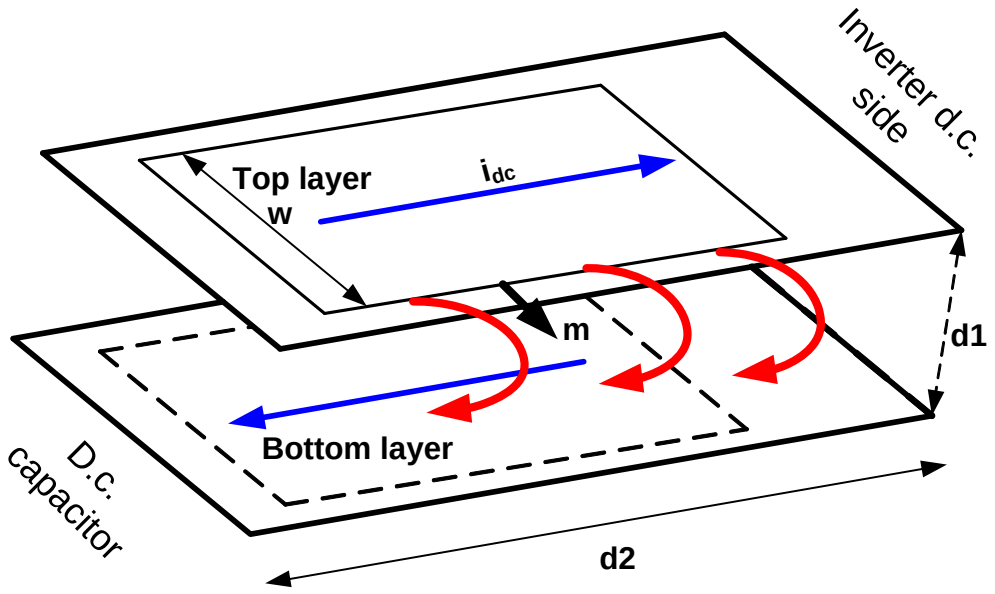


Figure 6.8: Detailed diagram of the parallel plate

The area of the PCB cross section, A, is given by,

$$A = d1 \times d2 = 134.5 \times 1.5 = 201.75\, mm^2 \quad (6.12)$$

The reluctance, R, of the magnetic circuit is given by,

$$R = \frac{w}{\mu_0 \mu_r A} = \frac{80 \times 10^{-3}}{4\pi \times 10^{-7} \times 1 \times 201.75 \times 10^{-6}} = 315.5 \times 10^6\, AT/Wb \quad (6.13)$$

where,

w = Length of the circuit (80 mm), which is perpendicular to the direction of i_{dc}.

μ_0= Permeability of free space ($4\pi \times 10^{-7}\, N/A^2$)

μ_r = Relative permeability of the PCB material is assumed as 1.

Equation 6.14, gives inductance of the top layer circuit, L_{sn}.

$$L_{sn} = \frac{N^2}{R} = \frac{1}{315.5 \times 10^6} = 0.0032\, \mu H \quad (6.14)$$

Energy stored in the inductive circuit,

$$E = \frac{1}{2} L_{sn} i_{dc}^2 = \frac{1}{2} \times 0.0032 \times 10^{-6} \times (20)^2 = 0.64\ \mu J \qquad (6.15)$$

As shown in Fig. 6.6, at turn off, when the load current free wheels through D_f, the energy stored in the snubber inductance gets transferred to the snubber capacitance, C_{sn}, through the diode D_{sn}. The overvoltage ΔV_{CE} across the IGBT is given by,

$$\frac{C_{sn} \Delta V_{CEmax}^2}{2} = \frac{L_{sn} i_{dc}^2}{2} \qquad (6.16)$$

where,

$\Delta V_{CE,max}$ = Maximum voltage across collector to emitter terminals of an IGBT

= Maximum d.c. rail voltage

= 300 V

Putting appropriate values in equation 6.16, the minimum value for C_{sn} is calculated as 15 pF. Equation 6.16 also shows that a larger value of C_{sn} minimises the over voltage, $\Delta V_{CE,\ max}$. As discussed in the section 6.2.6.2, the actual value of C_{sn} that has been used in the circuit is 47 nF. This limits ΔV_{CE} to about 5.2 V during the IGBT turn off.

6.2.9 Current limiting reactor, L_s

The design of the proposed STATCOM requires 14.7 mH of inductance in series with the tertiary winding. A single phase, variable reactor with adequate current carrying capacity was used as a series reactor.

6.2.10 Capacitor on the d.c. side

The size of the capacitor on the d.c. side of the converter is chosen as 4700 µF and is rated for 350 V (d.c.). Its design calculations are given in section 4.5.

6.3 Summary

This chapter covers the detailed design of the power circuit of the proposed VSC based STATCOM. The power circuit which is connected to the tertiary winding electrically isolates both the windings, and also the control system.

Components of the power circuit such as the 'H' bridge inverter, the compact IGBT driver circuit for driving the high side and low side IGBTs with over and under voltage protection, gate resistance (R_G), snubber circuit, D.C. link are designed for desirable operation of the system.

The calculations show the minimum values that should be used for obtaining the optimum performance from the system, however for designing the prototype, components which are rated for much higher values are used. This minimized the risk of component damage when unexpected over currents, over voltages, occurred while carrying out experiments. Photo of the completely built model of the STATCOM is shown in figure 6.9, while figure 6.10, shows a photo of the single phase, three winding, partial core transformer for which the STATCOM is built.

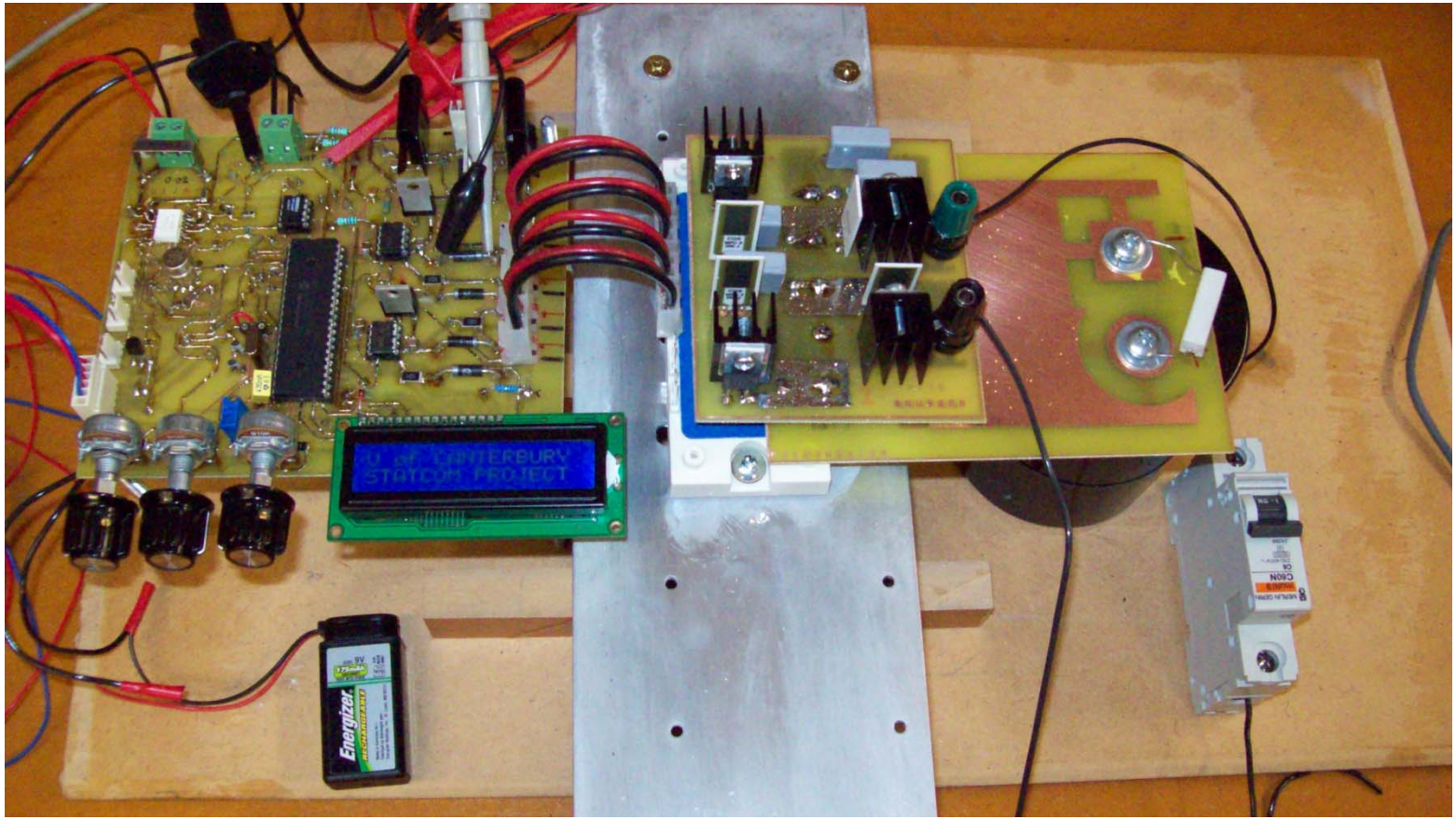


Figure 6.9: A photo of the controller board and power circuit of the single phase, VSC based STATCOM

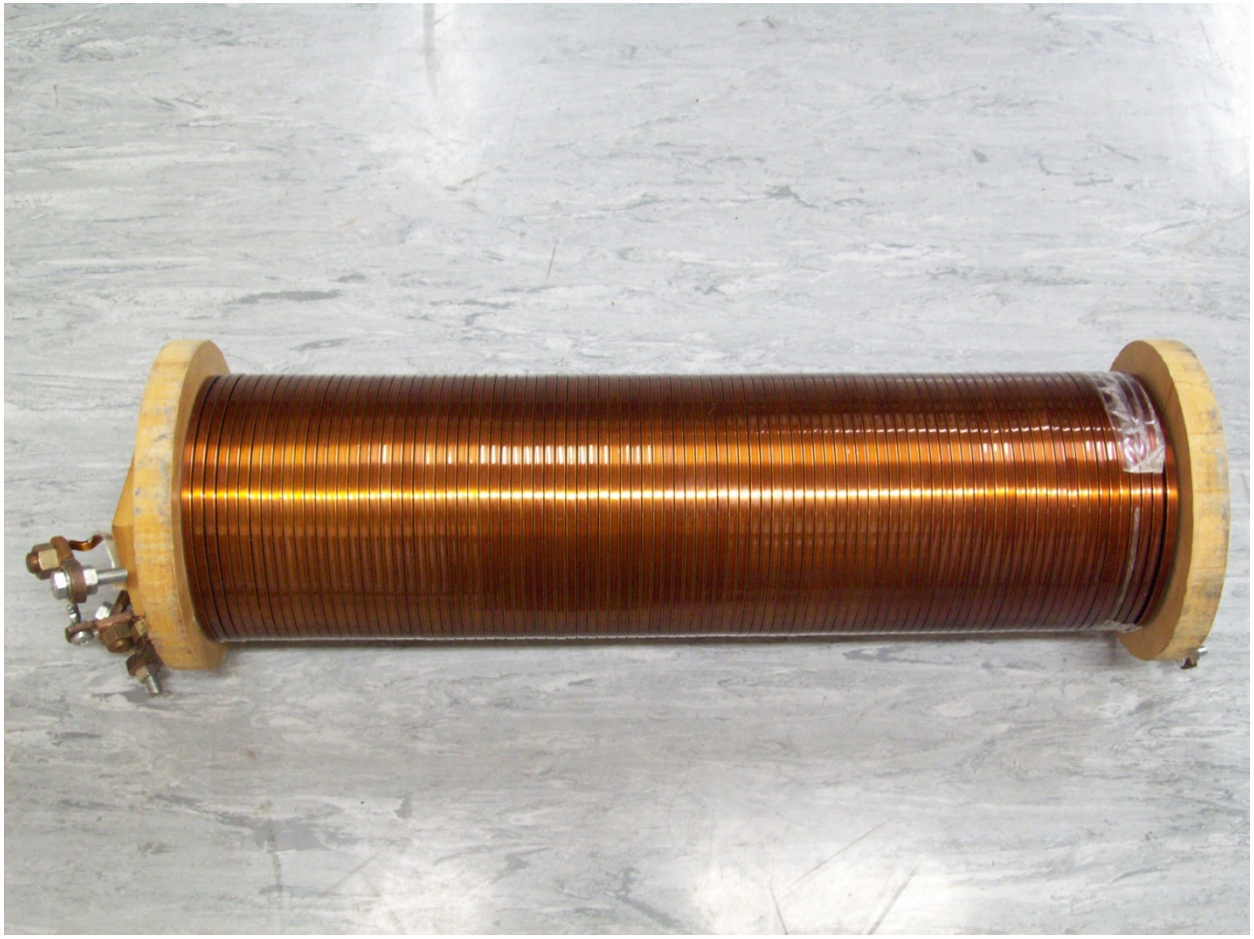


Figure 6.10: A photo of the single phase, three winding partial core transformer

Chapter 7

Control program software

7.1 Overview

In Chapter 5, the conceptual design of the control circuit for the proposed VSC based STATCOM was explained while Chapter 6 explained the power circuit of the controller board. In this chapter, the control algorithm developed for the digital control of the VSC based STATCOM using the micro-controller IC, PIC18LF4680 is explained.

7.2 Structure of the control program

The explanation of the control program is divided into the following steps,

- Initialization process before the STATCOM output voltage is synchronised with the supply voltage waveform.

- Synthesis of SPWM using PSCAD/EMTDC to obtain the values of periods and duty cycles of all PWM pulses in one cycle of 20 ms.

- Structure of the enhanced PWM module embedded in the micro-controller, PIC18LF4686.

- Generation of the SPWM waveform digitally, using the micro-controller.

- Implementation of the proposed control system by performing the required tasks such as data-acquisition, A/D conversion, various mathematical operations, and shifting the SPWM waveform 'earlier' or 'later' with respect to the supply voltage waveform by a delay angle, δ.

7.2.1 Development board for PIC micro-controllers, MikroICD

The control program is implemented in C language. It allows for ease of debugging and programming. The development board MikroICD, shown in figure 7.1, is used for real time debugging and downloading the control program. It allows execution of the program on a PIC micro-controller and viewing variable values, special function registers (SFR) and EPROM on a computer screen while the program is running. The development board and its well documented user's manual played a very important role in learning the micro-controller and all its peripherals especially during the developmental phase of the project. The program titled MikroC is used to compile the program and generate an output '.hex' file of the C program.

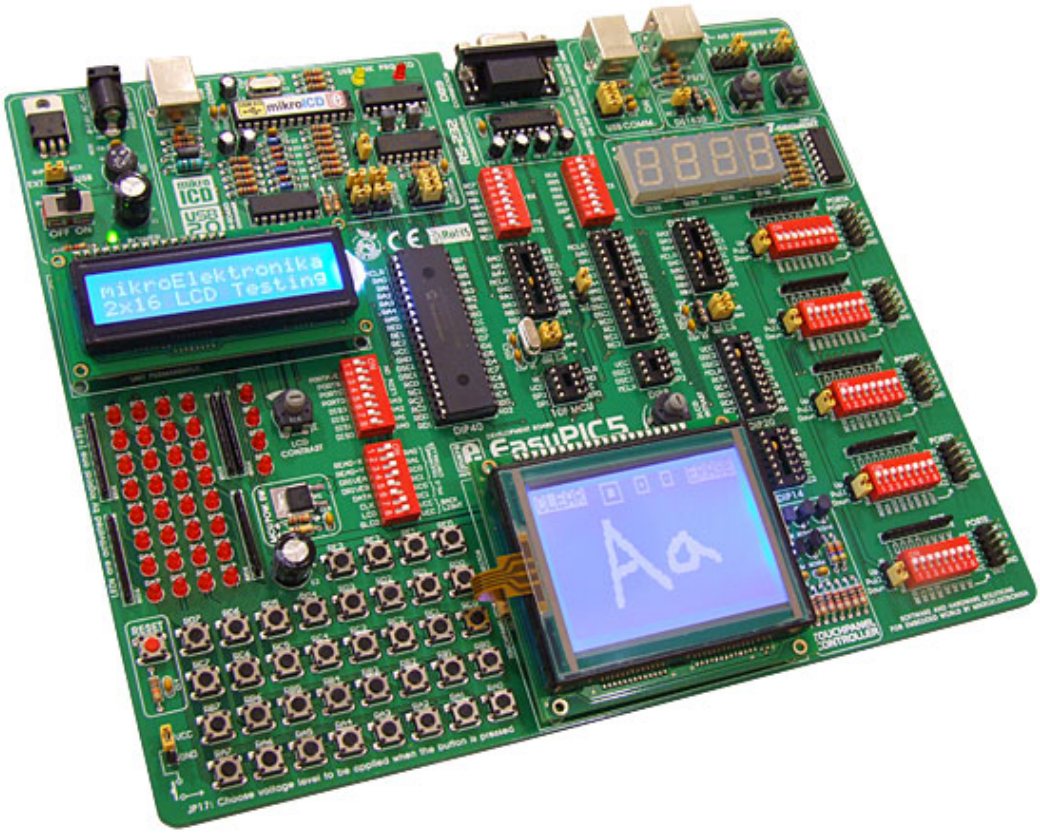


Figure 7.1: Development board, MikroICD board for learning, programming and debugging PIC micro-controllers [32]

7.2.2 Initialisation process

In the beginning of the control program, during the initialisation process, the variables interrupt vectors, and control registers used in the program are initialised. Various peripherals incorporated into the micro-controller such as an oscillator module, timers (TIMER0, TIMER1, TIMER2, and TIMER3), A/D converter module, analogue comparators and PWM generation module are configured.

The STATCOM may be turned ON at any instant (b1, b2, b3 or b4) as shown in figure 7.2, but the PWM waveform is not generated until the supply voltage zero crossing instant is detected at its rising edge. The analogue comparator, C1, is responsible for detecting the supply voltage zero crossing. The reliability and robustness of the zero crossing detection network is enhanced by testing the zero crossings for 'three' levels that should occur in the exact sequence (C1 = 0, C1 = 1, C1 = 0) before the initiating TIMER3, which is programmed to count 20 ms. TIMER3 counts 20 ms and sets the interrupt flag, TMR3IF. At this point, the comparator, C1, checks the status of the supply voltage waveform. If C1 is 1, then the PWM module is activated. This initialisation process has never failed to detect the exact 'rising edge zero crossing' instant. TIMER3 counting loop is important from the program logic point of view and forms a bridge between the initialisation process and the main program. The flow chart of the initialisation process is shown in figure 7.3.

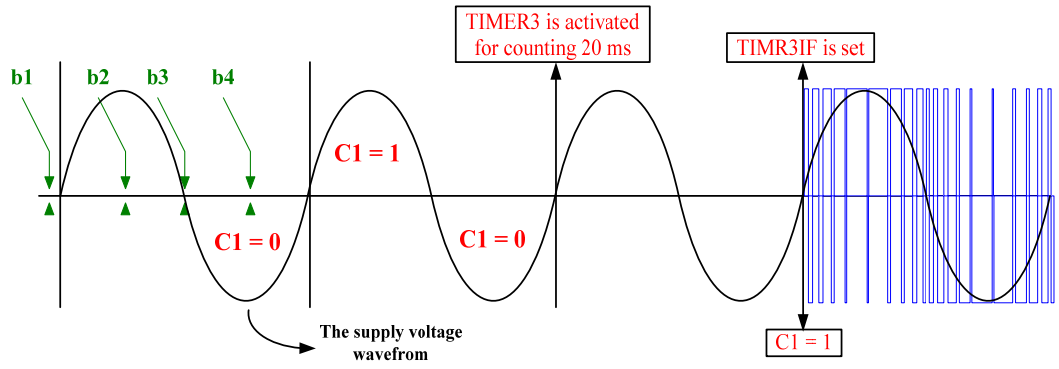


Figure 7.2: Initialization process for the proposed VSC based STATCOM

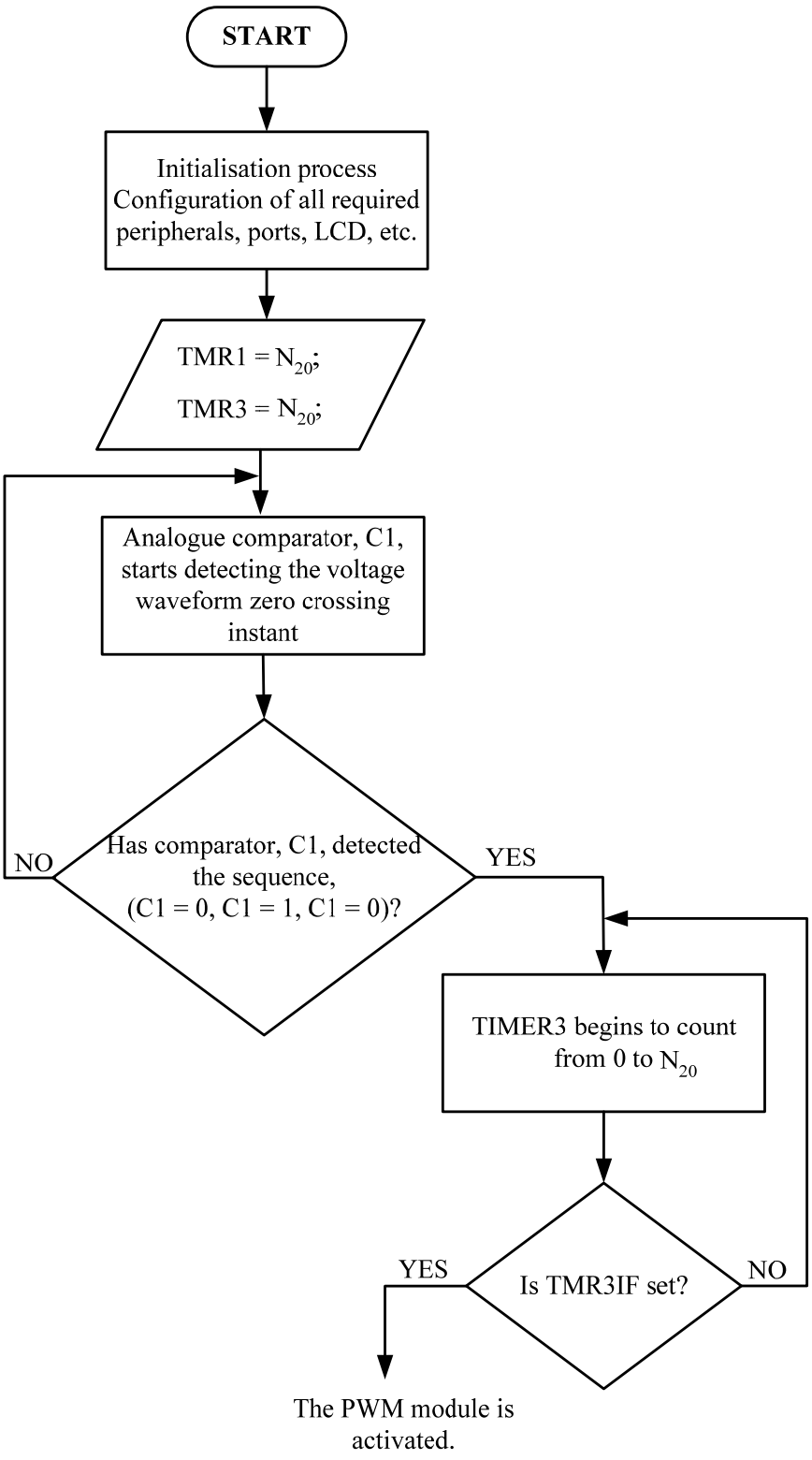


Figure 7.3: Flow chart of the initialization process before the PWM module is activated

7.2.3 Synthesis of SPWM in PSCAD/EMTDC

Before synthesising the mono-polar SPWM waveform digitally, PSCAD/EMTDC software was used to synthesize it. The selected switching frequency was 27 times the supply frequency. A sinusoidal reference waveform of 50 Hz frequency was compared with the triangular carrier waveform corresponding to 1350 Hz. In this case, the zero of the triangular wave coincides with zero of the reference sinusoid. The number of pulses, N, per complete cycle is given by,

$$N = \left(\frac{f_c}{f} \right) \tag{7.1}$$

where, f_c is the frequency of the triangular waveform and f is the frequency of the sinusoidal waveform. Substituting the value of f_c = 1350 Hz and f = 50 Hz in equation 7.1, the number of pulses per cycle is calculated as 27.

The resultant SPWM waveform obtained from PSCAD/EMTDC simulations is demonstrated in figure 7.4. SPWM waveforms generated at the channel 'A' and channel 'B' are complementary with each other. The modulation index, m, which controls the output voltage, is chosen as 1.

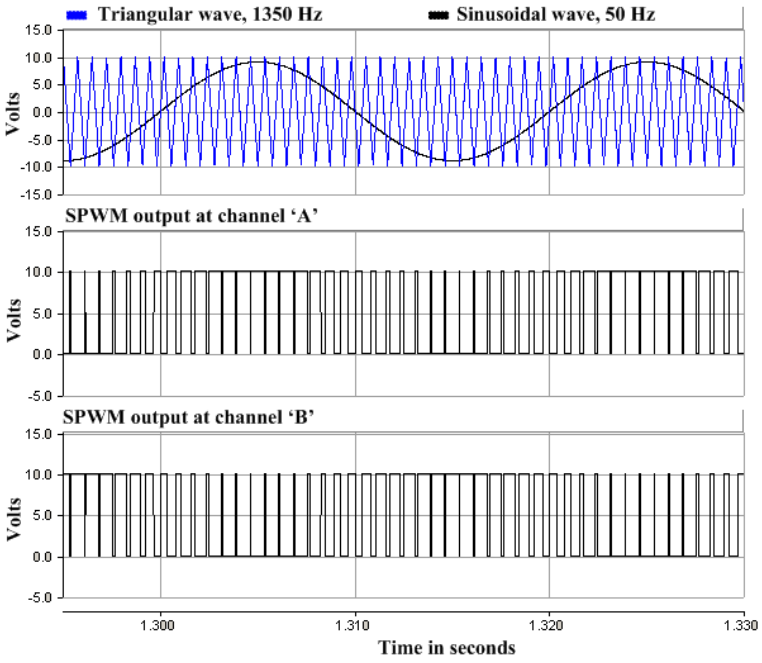


Figure7.4: Generation of a mono-polar, 1350 Hz SPWM waveform using PSCAD/EMTDC

7.2.4 Structure of the enhanced PWM module embedded inside the micro-controller

Precise SPWM waveform of switching frequency 1350 Hz, is generated using the enhanced PWM module incorporated in the micro-controller. The detailed schematic diagram of the enhanced PWM module is shown in figure 7.5. The control register bits, ECCP1CON<1:0>* and ECCP1CON<3:0> are used to configure the PWM module in the half bridge mode. Two PWM output channels P1A and P1B are multiplexed with the PORTD <4> and PORTD <5> data latches respectively. In the half bridge mode, PWM signal outputs on pins P1A and P1B are modulated and are complementary with respect to each other.

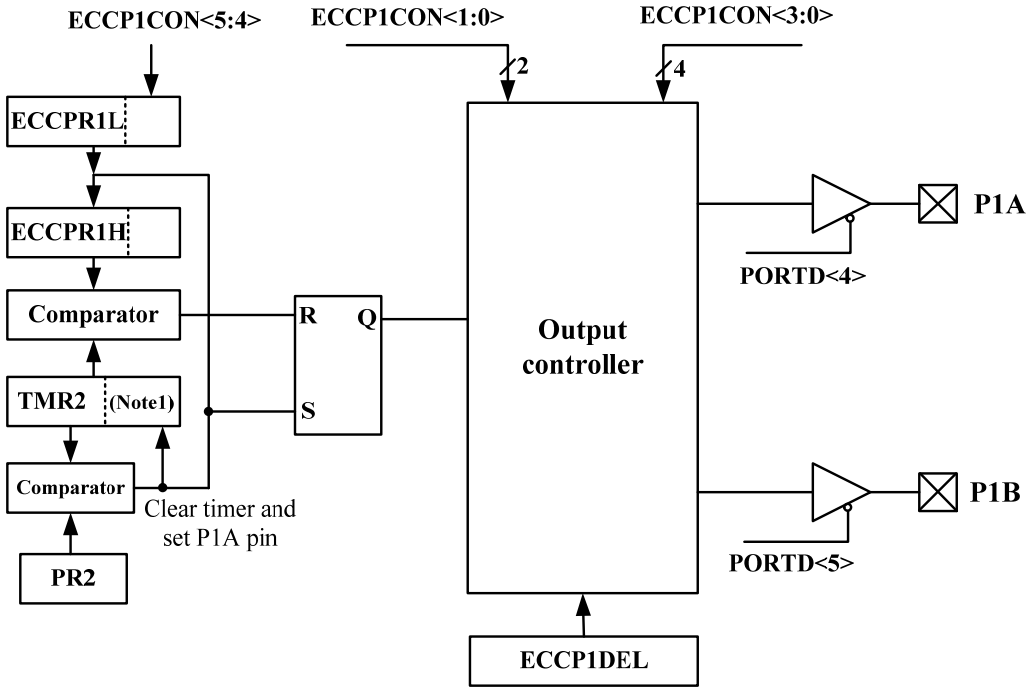


Figure 7.5: Schematic diagram of the enhanced PWM module embedded inside PIC18LF4680 [26]

* <x:y> indicates the bit numbers from 'x' to 'y'.

Note 1: The 8-bit TMR2 register is concatenated with the 2-bit internal Q clock, or 2 bits of the prescaler, to create the 10-bit time base.

7.2.4.1 Specifying PWM period

For generating a PWM waveform, a 16 bit timer, TIMER2, is configured as a counter. Values corresponding to the periods and duty cycles of all 27 PWM pulses are obtained from PSCAD/EMTDC simulations. The number corresponding to the period of each PWM pulse in a complete cycle (of 20 ms) is stored in an 8 bit register, PR2, and is calculated using equation 7.2 [26],

$$PR2 = \left(\frac{PWM\ \ period}{4 \times T_{osc} \times prescale\ value\ \ for\ TIMER2} \right) \tag{7.2}$$

where, the value of the 'PWM period' is in seconds and T_{osc} is the period of oscillations of the micro-controller oscillator, i.e. 0.125×10^{-6} s. For preventing TIMER2 from overflow, a pre-scale value of 16 is used. The number of counts of timer TIMER2 is stored in the TMR2 register.

7.2.4.2 Specifying ON time for each pulse

As shown in figure 7.5, the PWM ON time is specified by writing it to the ECCPR1L register and to the ECCP1CON <5:4> bits. ECCP1RL contains the eight MSbs while the ECCP1CON <5:4> contains the two LSbs. The 10 bit value is represented by ECCPR1L:ECCP1CON<5:4>. The number, T_{ON}, to be entered is calculated using equation 7.3 [26],

$$T_{ON} = \left(\frac{PWM\ \ duty\ cycle}{T_{osc} \times prescale\ value\ \ for\ TIMER2} \right) \tag{7.3}$$

In order to prevent any glitches in the output, all control registers are double buffered and loaded at the beginning of a new PWM cycle. Because of the buffering, the module waits until the assigned timer, TIMER2, resets, instead of starting immediately. This means that the generated PWM waveforms do not exactly match the standard PWM waveforms but are instead offset by 2 μs (one complete instruction cycle, $4 \times T_{osc}$).

7.2.4.3 Setting dead band delay time

The turn OFF time for the IGBT is 225 ns [33]. A dead band delay of 2 µs (10× turn OFF time) is programmed by writing the corresponding value to an 8 bit register, ECCP1DEL. The dead band delay prevents any cross-conduction between the power devices which belong to the same leg of the inverter bridge.

7.2.5 SPWM generation by the micro-controller

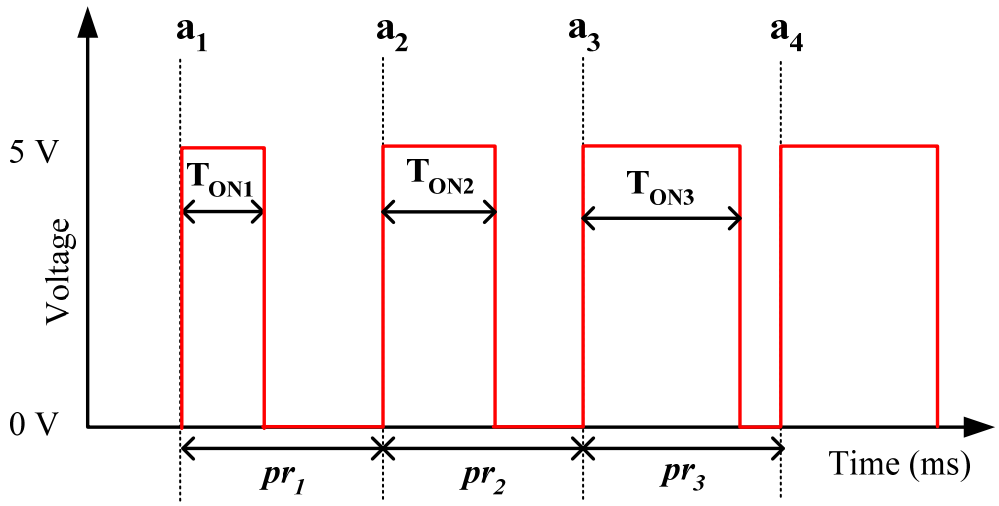


Figure 7.6: Generation of PWM waveform using PIC18LF4680

- The value corresponding to the period of the n^{th} PWM pulse, pr_n, can be written to register PR2, while the PWM ON time, T_{ONn}, corresponding to the n^{th} PWM pulse can be written to ECCPR1L and ECCP1CON<5:4> anytime before instant a_n.

- Because of the double buffering mechanism, T_{ONn} is not copied into the buffered register, ECCPR1H, until the previous PWM period, $pr_{(n-1)}$, is completed.

- At instant a_n, the previous PWM period, $pr_{(n-1)}$, is completed as the number of counts stored in TMR2 register matches with the number, $pr_{(n-1)}$, stored

in the register PR2. When TMR2 is equal to PR2, the following three events occur on the next increment cycle,

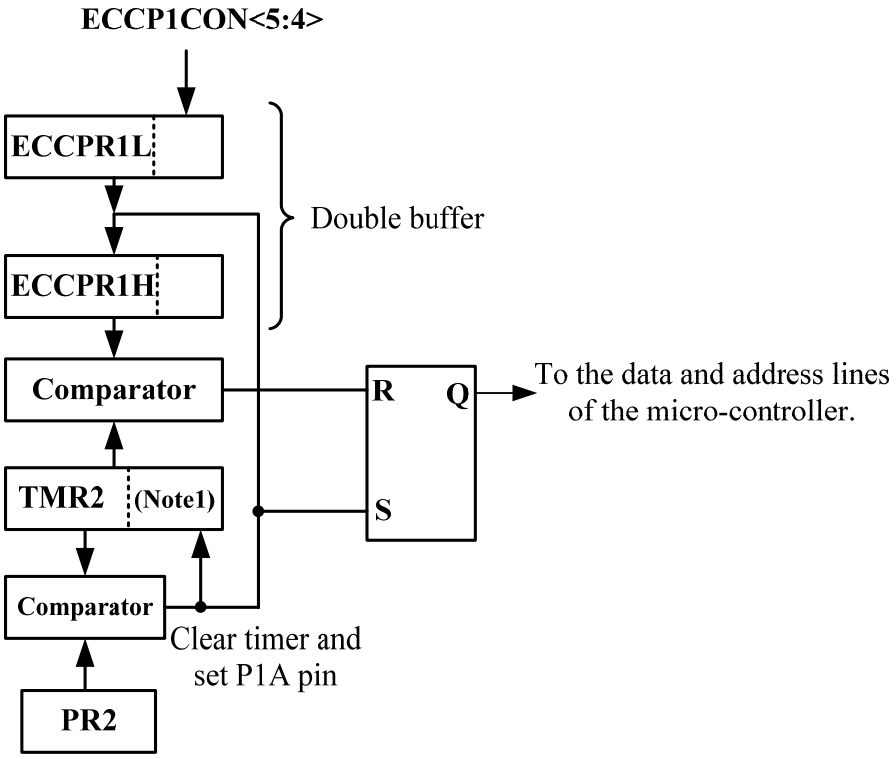


Figure 7.7: Register structure of the enhanced PWM module in PIC18LF4680†

- The TMR2 register is cleared.

- The ON time value, T_{ONn}, for the n^{th} PWM pulse is copied from ECCPR1L to ECCP1H and the ON time value for the next PWM cycle, $T_{ON(n+1)}$, is copied from the look up table to the ECCPR1L:ECCP1CON <5:4> registers.

- The P1A pin is set (P1A = 1) and as TIMER2 starts to count, the number of counts stored in TMR2 starts incrementing. When TMR2 is equal to T_{ONn}, P1A is reset (P1A = 0) and TIMER2 keeps on counting until the number of counts stored in TMR2 equals pr_n.

†Note1: The 8 bit TMR2 register is concatenated with the 2-bit internal Q clock, or 2 bits of the pre-scalar, to create the 10 bit time base.

- When TMR2 = pr_n, a new PWM period, $pr_{(n+1)}$, begins. All 27 PWM pulses are generated in 20 ms with precise accuracy and are repeated in a continuous manner. The generated SPWM in this way is then synchronised with the main supply by the zero crossing detection circuit. Initially, the zero of the supply voltage coincides with zero of the SPWM, i.e. the delay angle, δ, is zero. The complete process of generation of the SPWM is given by the flow chart in figure 7.8.

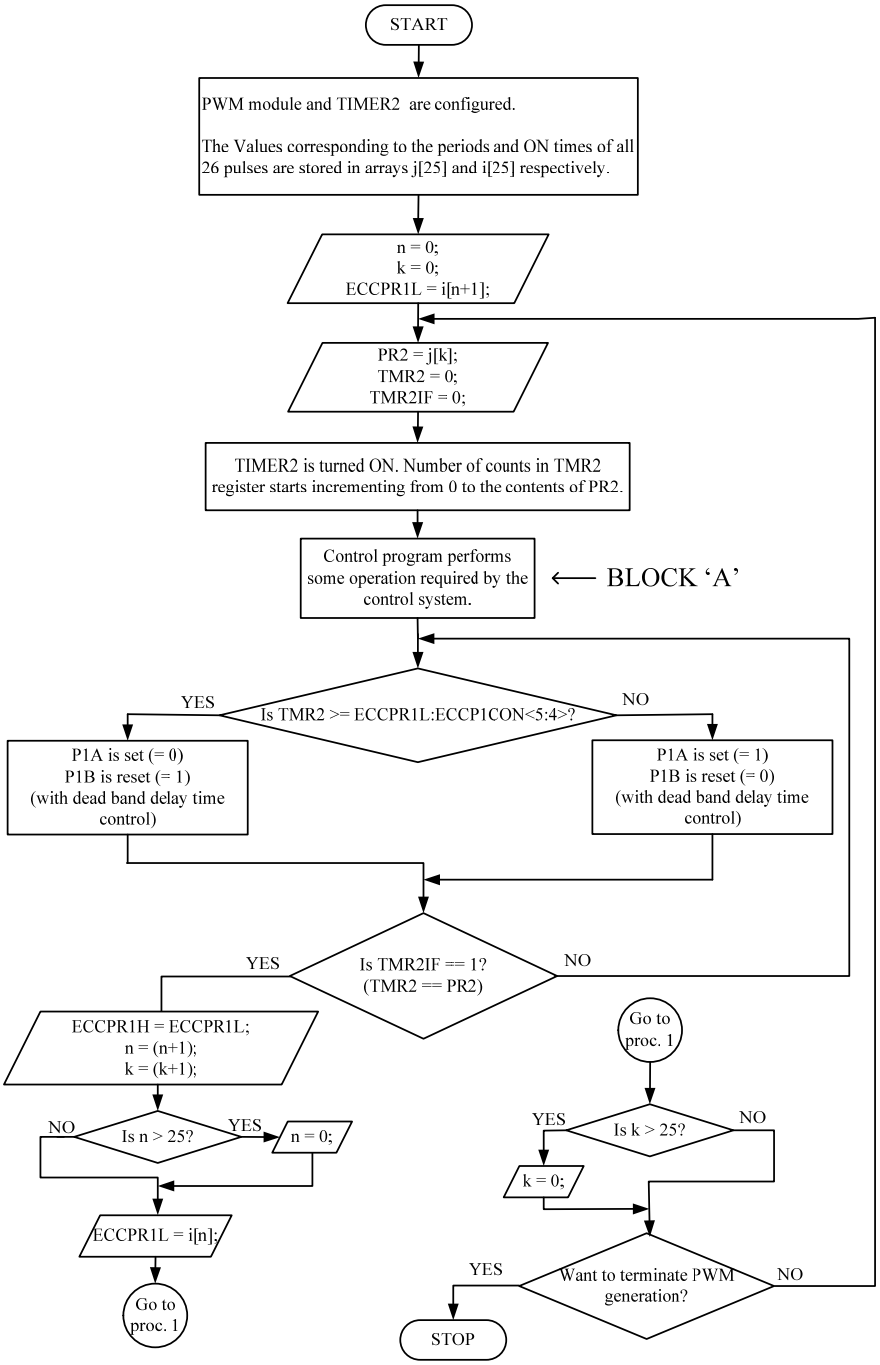


Figure 7.8: Flow chart for the generation of SPWM waveform using PIC18LF4680

7.2.6 Mathematical calculations and implementing the control system

From the beginning to the end of the period, the PWM generation module, along with TIMER2, runs without causing any interference to the main program. The main program is interrupted only at the beginning of each new period (at every a_n in figure 7.6). This indicates that the time corresponding to each period, pr_n, (time difference between instants a_n and $a_{(n+1)}$) can be utilised for sensing other parameters and mathematical calculations. In figure 7.8, this time is represented by 'BLOCK A'.

The time required for processing each step, e.g. A/D conversion, multiplying two float numbers, etc., is observed with the help of a digital storage oscilloscope. Depending on the time required for each step, one or more steps are combined in such a way that the total time required for executing all steps in one block should be less than the PWM period in which these steps are going to be carried out. Otherwise, the PWM generation would fail.

As discussed in section 5.5.4 from Chapter 5, the averaging time for the AD536, the IC which converts rms current waveform to its equivalent d.c. value, is 107 ms. The time required to complete each mains sinusoidal cycle is 20 ms. The larger value nearest to 107 and an integer multiple of 20 is 120. Hence 120 ms (6 cycles) is selected as a time constant for the system. This means that at every 120^{th} ms or at the beginning of every 6^{th} cycle, the system updates the delay angle, δ.

7.2.6.1 Operations performed during first of six cycles (0 to 20 ms)

- During the first cycle, the values corresponding to the proportional gain (K_p), the integral time constant (T_i), and the reference I_q, are sensed by the A/D converter.

- The integral time constant is calculated using equation,

$$K_i = \frac{K_p}{T_i} \tag{7.4}$$

The reason behind not sensing the value of K_i directly and keeping it dependent on the value of K_p, is the type of PI control equation used and is explained in section 7.2.6.4.

- In order to display a number on the LCD, the value of the quantity to be displayed should be an integer. The decimal point is used as a character and it is added at the required position during LCD programming. For this reason, the values of K_p, K_i and ref. I_q are converted into integers, and stored in variables lcd_kp, lcd_ki, and lcd_ref_iq respectively.

7.2.6.2 Operations performed during second cycle (20 ms to 40 ms)

- At the beginning of every cycle, the control program detects the nature of the phase angle, θ (lagging or leading). In the unity power factor situation, the program detects the case as 'leading' but while counting the magnitude of θ, the result comes out as zero. The topic of the phase angle measurement is covered in the Section 5.5.5 of Chapter 5.

- If the nature of the phase angle, θ is '*leading*', then its magnitude in terms of time difference is measured in the second of the six cycles.

7.2.6.3 Operations performed during third cycle (40 ms to 60 ms)

- If the nature of θ is detected as '*lagging*', then its magnitude in terms of time difference is measured during this cycle.

- The sine value of the measured phase angle is computed up to a 4 digit accuracy, by using the look up table. The computed sine value is stored in the variable, *sinq*.

7.2.6.4 Operations performed during fourth cycle (60 ms to 80 ms)

- The A/D module acquires the 25 samples of the supply current, I_s.

- The average of the acquired samples is calculated and assigned to the variable, *lvcurrent*.

- The reactive component of the supply current, I_q, $(lvcurrent \times sinq)$, is calculated and stored in the *i_sinq* variable.

- **Implementation of PI controller**

  Figure 7.9 shows a PI control system which is used to model the proposed VSC based STATCOM. The desired set point Ref. $I_q(t)$ of this system is achieved when the reactive component of the supply current, I_q = Ref. $I_q(t)$. Any magnitude of I_q other than the set reference Ref. $I_q(t)$ is an error or Ref. $I_q(t) - I_q(t) = E(t)$. Iq is the reactive component of the supply current.

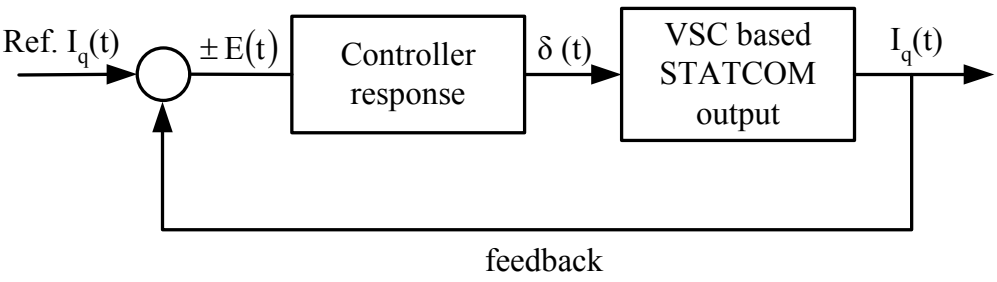


Figure 7.9: A typical PI control system model

For implementing the PI controller, two terms are obtained from,

$$Proportional\ \ term = K_p \times E(t) \tag{7.5}$$

$$Integral\ term = K_i \int_0^t E(t)dt \tag{7.6}$$

Then, the equation for the delay angle, δ(t), as an output, is given by,

$$\delta(t) = K_p \times E(t) + K_i \int_0^t E(t)dt \tag{7.7}$$

The sign of the delay angle, δ(t), determines the direction of the generated SPWM waveform (later or earlier) with respect to the supply voltage waveform.

PI controller in digital system

In order to implement the PI controller digitally, the error, E(t) is integrated using the equation,

$$\int_0^t E(t) \approx T_s \sum_0^N E(n) \tag{7.8}$$

where E(n) is the current error and T_s is the sampling time. With this approximation, an equation for δ(t) can be rewritten as,

$$\delta(n) = K\left[E(n) + \left(\frac{1}{T_i} \right) \sum_0^N E(n) \right] \tag{7.9}$$

where $K_p = K$ and $\frac{K}{T_i}$ is nothing but the integral gain constant K_i. The main advantage of using this type of equation is that the pole response of the controller will not be affected by changing the proportional constant [38].

7.2.6.5 Operations performed during fifth cycle (80 ms to 100 ms)

- Depending on the situation, the newly calculated delay angle, δ, is added to or subtracted from the previous delay angle shift. The resultant delay angle is prevented from exceeding the maximum limits. The SPWM waveform can be shifted forwards up to 22.92° while it can be shifted backwards up to 27.67°. The delay angle is designed to shift more

backwards than forwards with respect to the supply voltage as the system has to compensate for more inductive loads. The angle shift is converted into the number of counts for which the timers, TIMER1 and TIMER3 can set.

7.2.6.6 Operations performed during sixth cycle (100 ms to 120 ms)

- From this cycle, the SPWM waveform actually gets shifted to the newly updated delay angle, δ, with respect to the supply voltage waveform.

7.3 Shifting SPWM waveform with respect to the supply voltage waveform

At each positive zero crossing instant of the supply voltage waveform, the micro-controller begins to execute the SPWM loop consisting of 27 PWM pulses. In such a situation, single set of a PWM waveform can be synchronised and/or delayed by angle, δ with respect to the supply voltage waveform but it is not possible to generate the SPWM waveform before the positive zero crossing instant is reached. In order to accommodate the later feature in the control program, two sets of sine wave functions, SPWM1 and SPWM2 which are exactly the same in all aspects but are applied alternatively as shown in Figure 7.10.

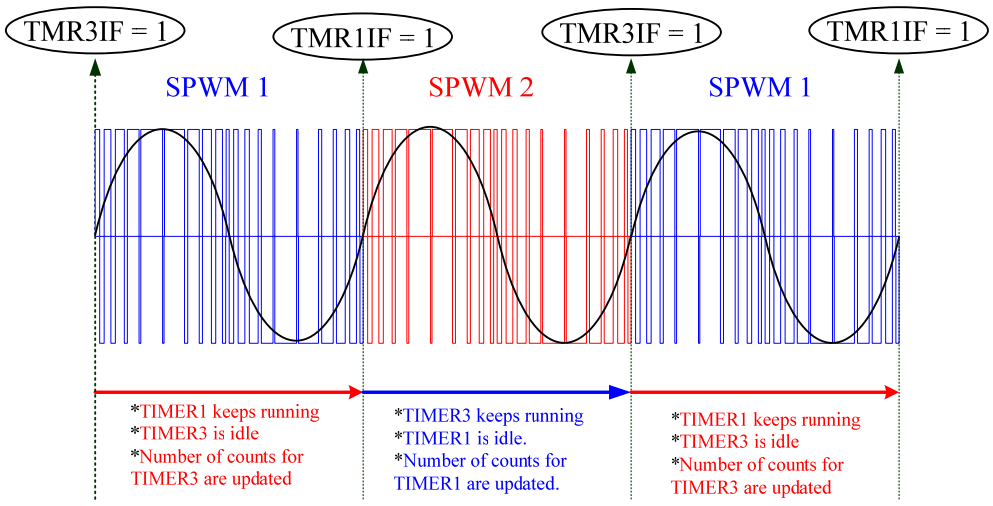


Figure 7.10: The timer controlled SPWM1 and SPWM2 waveforms with respect to the supply voltage

The instant of initialization of the SPWM1 waveform depends on the number of counts of TIMER3 stored in the 16 bit register, TMR3. When TIMER3 resets, i.e. the interrupt flag TMR3IF is set (=1) and SPWM1 is initialized. In a similar fashion, the SPWM2 waveform is dependent on TIMER1 for its initialization.

When the control program executes the SPWM1 waveform, the number of counts is updated for TMR3. Similarly, while executing the SPWM2 waveform, the number of counts is updated for TMR1.

As shown in Figure 7.11, each SPWM waveform has its own 'front side' and 'tail side.' PWM pulses in these zones are used to detect the supply voltage zero crossing instants and initiate the timers, TIMER1 and TIMER3. This feature allows shifting of the SPWM waveform *'earlier'* or *'later'* with respect to the supply voltage waveform. The magnitude and direction of the angle shift depends on the result of the PI controller given by equation 7.9. The number of counts is updated before their respective waveforms reach the tail side.

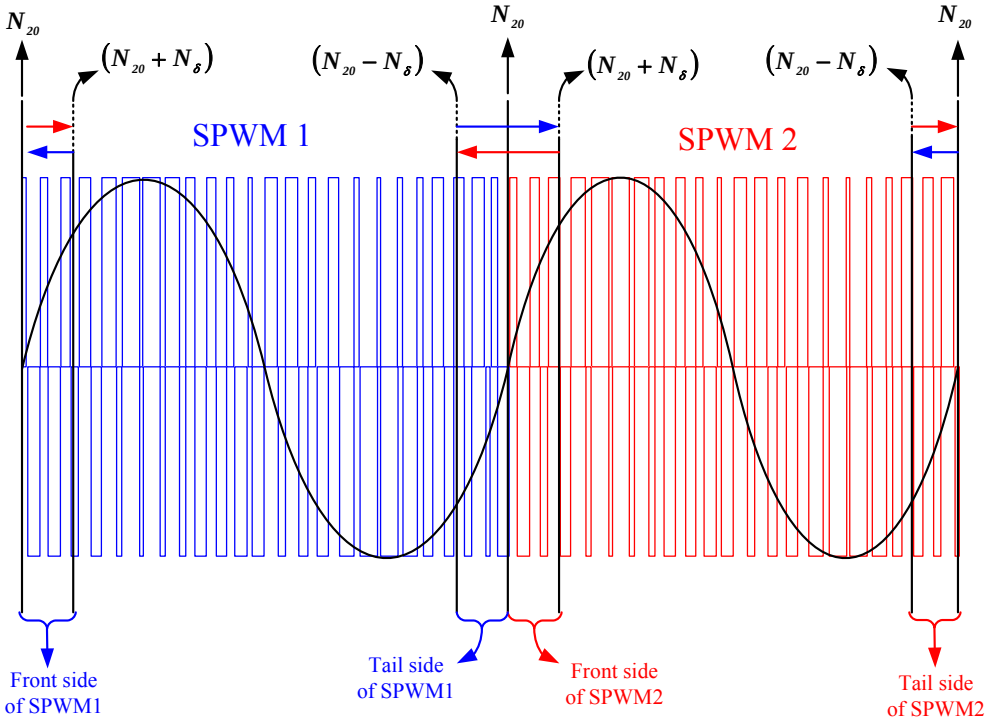


Figure 7.11: The SPWM1 and SPWM2 waveforms with their front and tail sides

If the number of counts corresponding to 20 ms is N_{20}, and those for delay angle, δ, is N_{δ}, then the total number of counts stored in both the timer registers is given by

$$TMR1 = TMR3 = (N_{20} \pm N_{\delta}) \quad (7.10)$$

Depending on the value and sign of N_{δ}, three cases are possible, namely

- $N_{\delta} = 0$ The SPWM waveform is synchronized with the zero crossing instants of the supply voltage.
- $N_{\delta} > 0$ The waveform is shifted backwards with respect to the supply voltage by the delay angle, δ.
- $N_{\delta} < 0$ The waveform is shifted forwards with respect to the supply voltage by the delay angle, δ.

The logic behind shifting the SPWM waveform with respect to the supply voltage can be better understood by the following principles,

- For the timers (TIMER1 or TIMER3) to start counting, the supply voltage zero crossing detection is necessary.

- Initialization of SPWM1 or SPWM2 is dependent on the setting of timer flag TMR3IF or TMR1IF respectively.

7.3.1 Waveform is shifted later with respect to the supply voltage by the delay angle, δ.

As shown in Figure 7.12, Z1 and Z2 represent the supply voltage zero crossing instants, while S1 and S2 are the instants at which the timer interrupts, TMR3IF and TMR1IF, are set respectively.

For a 50 Hz waveform, the time difference between the two consecutive rising edge zero crossings is 20 ms. As $N_{\delta} > 0$, the timers have to count time more than

20 ms from the zero crossing instants to initiate the next consecutive SPWM loop, and hence the SPWM waveform lags behind the supply voltage waveform.

The supply voltage zero crossing is detected at the instant Z1 and TIMER1 starts to count from 0 to (N_{20} + N_{δ}). At the S1 instant, the TIMER3 interrupt, TMR3IF is set and the SPWM1 loop is initialized. TIMER3, is stopped, while TIMER1 keeps running.

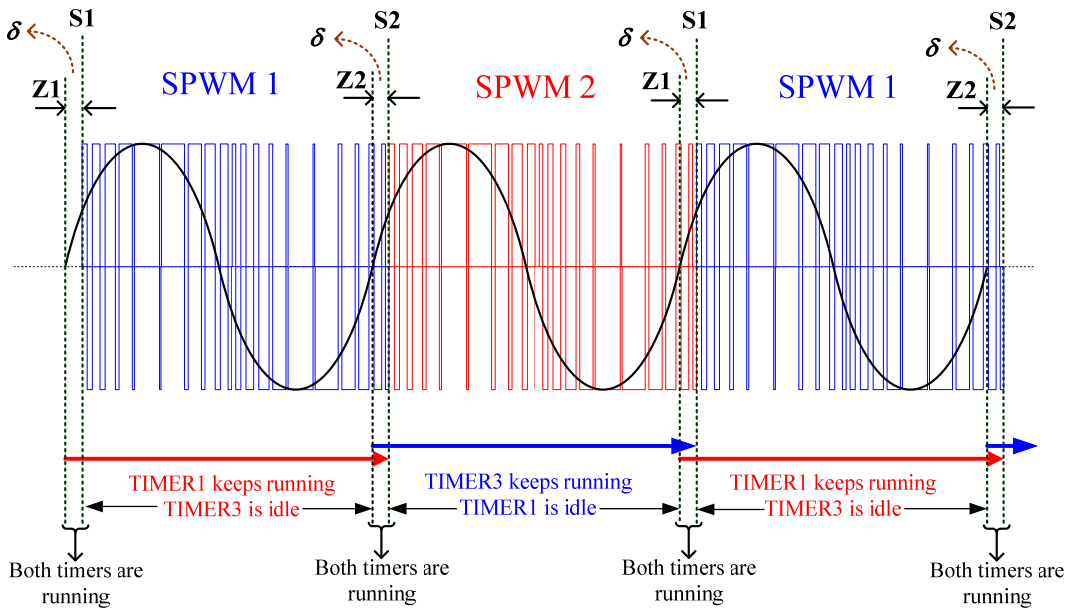


Figure 7.12: Shifting the SPWM waveform later with respect to the supply voltage waveform

At 20 ms, the consecutive zero crossing instant, Z2 is detected and TIMER3 is initialized. Between time period, Z1-S1 and Z2-S2, both the timers keep running. The time difference between Z1-S1 and Z1-S2 represent the delay angle, δ and can be measured using a suitable digital storage oscilloscope.

At the instant, S2, TIMER1 completes counting (N_{20} + N_{δ}) and the interrupt, TMR1IF, is set. At this instant the SPWM2 loop begins to execute.

7.3.2 The SPWM waveform is synchronized with the zero crossing of the supply voltage.

When the delay angle, δ is zero, the timers have to count 20 ms. As shown in Figure 7.13, under this situation, the supply voltage zero crossing instants Z1 and Z2 coincide with the timers' interrupt setting instants, S1 and S2, respectively.

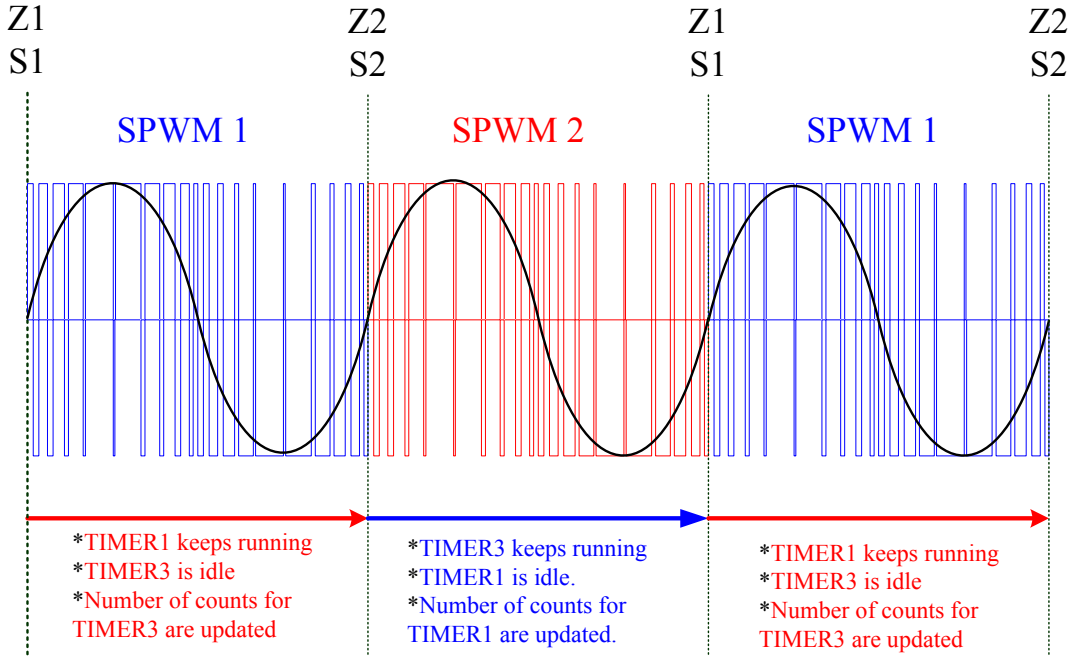


Figure 7.13: The SPWM waveform is synchronized with the supply voltage waveform with the delay angle, δ = 0

When the supply voltage zero crossing is detected at the point Z1 or S1.

- The TIMER3 flag, TIMER3IF, is set (=1)
- The control program begins to execute the SPWM1 loop
- TIMER1 starts to count from 0 to N_{20}.
- When the control program executes SPWM1 loop, TIMER3 remains idle.

The point Z2 or S2 is said to have been reached when the zero crossing detection circuit detects the next consecutive voltage zero crossing. Since the delay angle, δ is zero, TIMER1 counts 20 ms and sets the flag, TIMER1IF. At this point,

- The control program begins to execute the SPWM2 loop

- TIMER3 starts to count from 0 to N_{20}
- When the control program executes the SPWM2 loop, TIMER1 remains idle.

7.3.3 Waveform is shifted earlier with respect to the supply voltage by the delay angle, δ.

If the result of the PI controller mentioned in equation 7.9, is a negative number, then the corresponding number of counts, N_δ, is assigned with negative sign. According to equation 7.10, the timers have to count less than 20 ms from the supply voltage zero crossing instants to initiate the next consecutive SPWM waveform. Due to this, the SPWM waveform leads the supply voltage by the delay angle, δ.

As demonstrated in Figure 7.14, the supply voltage zero crossing is detected at the instant Z1 and TIMER1 begins to count from 0 to (N_{20}-N_δ). At the instant, S2, TIMER1 completes counting the number (N_{20}-N_δ) and the interrupt flag, TMR1IF, is set. The SPWM2 loop is initiated, although the next consecutive rising edge zero crossing is not yet detected.

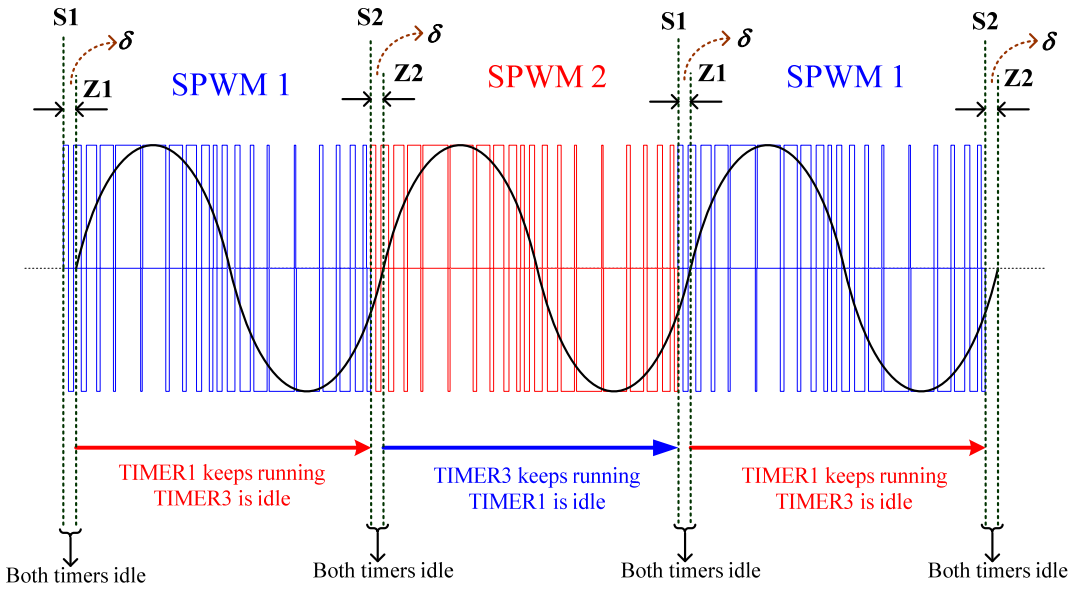


Figure 7.14: Shifting the SPWM waveform earlier with respect to the supply voltage waveform.

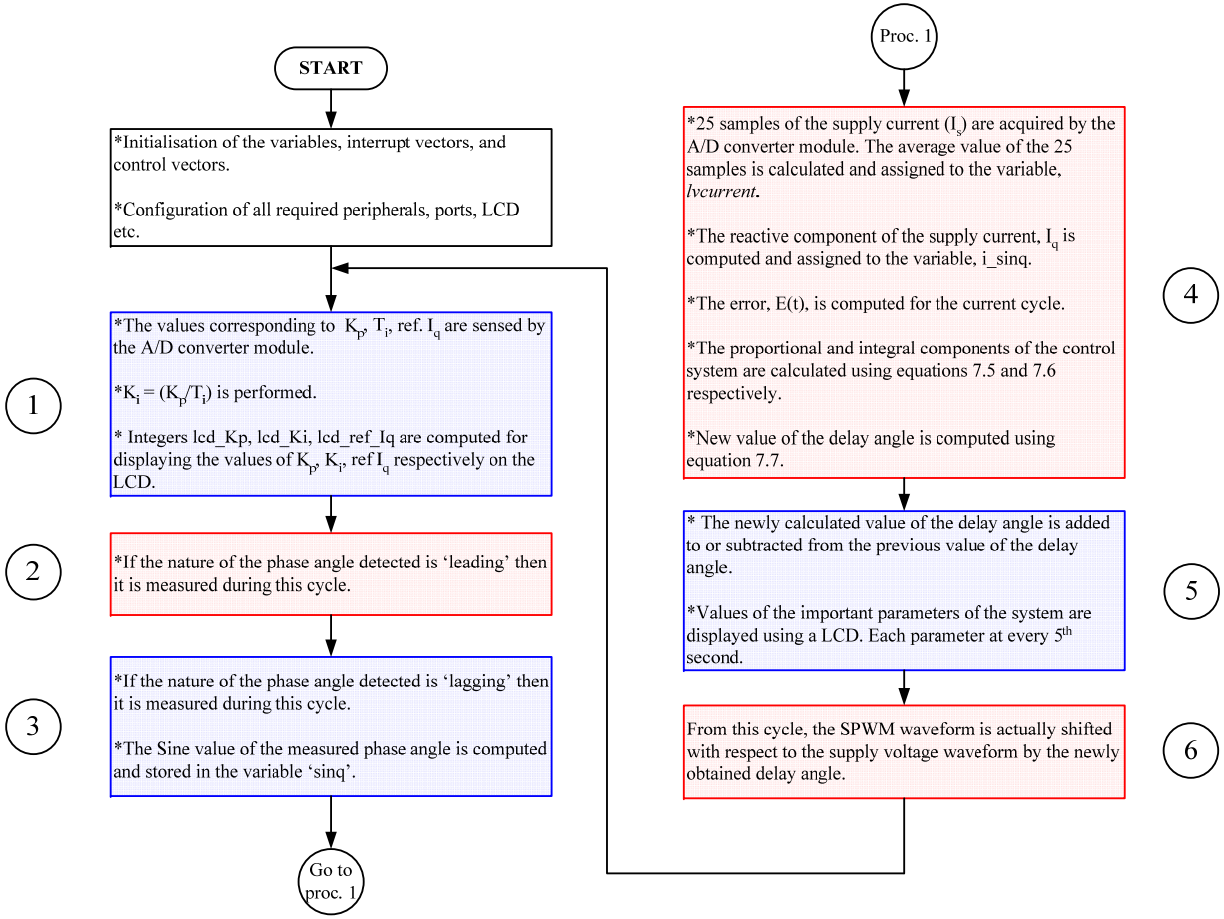


Figure 7.15: An algorithm for the implementation of the proposed control system

SPWM1 SPWM2 The number inside a circle displays the number of cycle.

Between the time instants, S1-Z1 and S2-Z2, both the timers, TIMER1 and TIMER3, remain in the idle mode. At the next consecutive supply voltage zero crossing instant, Z2, TIMER3 begins to count from 0 to (N_{20}-N_{δ}). The TIMER3 interrupt, TMR3IF is set at the instant S1 and the SPWM1 loop continues.

The flow chart developed for the implementation of the control system is shown in Figure 7.15.

7.4. Summary

The chapter is focused on the implementation of the digital control system using the micro-controller, PIC18LF4680, for development of the proposed VSC based STATCOM.

MikroElectronica development tools and its user friendly manuals were used to learn the micro-controller, program and debug the source code in 'C' language.

In the beginning, the variables, control registers, peripherals embedded inside the micro-controller were initialized. The SPWM waveform was generated precisely using PIC18LF4680; simultaneously the digital closed loop control system for the proposed STATCOM was implemented. The complete control system is implemented in the 6 cycles of the supply voltage waveform, and the delay angle, δ is updated after every 120^{th} ms. The system parameters such as the phase angle, the magnitude of the supply, I_s, and the reactive current, I_q, the error, E(t) generated, the delay angle, δ are displayed using LCD.

Chapter 8

Results and discussions

8.1 Overview

A VSC based STATCOM was built and connected to the tertiary winding of the partial core transformer for the purpose of evaluating of the overall performance of the system. This chapter discusses results and findings.

Based on laboratory experimental results, an analysis was carried out of various important electric parameters of the partial core transformer before and after application of the STATCOM, taking a range of capacitive loads into account. The electric parameters taken into consideration were:

- Currents in the three windings
- VA gain in the supply winding
- Real power losses in the supply and the tertiary windings
- Behaviour of real power losses in the supply and the tertiary windings with respect to the delay angle, δ
- % total harmonic distortion of currents in the three windings
- % total harmonic distortion of voltages across the terminals of the three windings

8.2 Experimental set up

For safety purposes, the system is operated at 45 V using a single-phase autotransformer rated at 230 V, 50 Hz and 10 A. As stated in Section 2.3, the transformer turns ratio between the supply, the high voltage and the tertiary windings is 1**:**3.83**:**1 respectively. The high voltage winding of the partial core

transformer is connected to a variable capacitor bank. The value of the capacitive load is increased from 0 µF to 70 µF (653† VAr) in the steps of 10 µF (93 VAr). The transformer core is kept exactly at the centre and its position is unchanged while performing experiments.

When the value of the capacitive load, X_c is around 38 µF, it resonates with the magnetising reactance, X_m of the transformer. Under this situation, the least current (only the real component) is drawn from the supply i.e. loads connected to the high voltage winding less than 38 µF result in an inductive supply current, while loads higher than 38 µF result in a capacitive supply current. This is illustrated in Fig. 8.1.

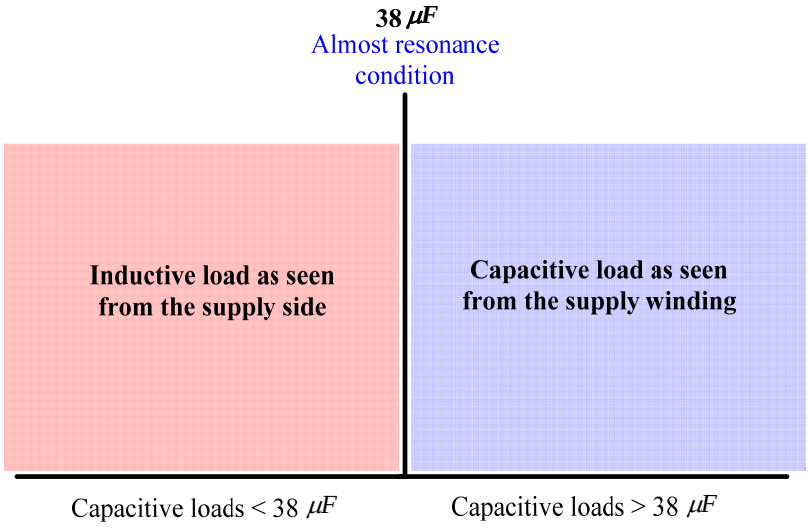


Figure 8.1: Nature of loads as seen from the supply side

8.3 Electric parameters of the system

8.3.1 Supply current

The main objective of this project is to reduce the magnitude of the supply current to its real component. As shown in Fig. 8.2, curve B shows the amount of current drawn from the supply for a range of capacitive loads before connecting the STATCOM across the transformer tertiary winding.

† Calculated at 172.3 V i.e. 45×3.83

After connecting the STATCOM across the tertiary winding, most of the reactive burden from the supply side was taken by the STATCOM controlled tertiary winding (curve C), and a significant drop in the magnitude of the supply current was observed as shown by curve A.

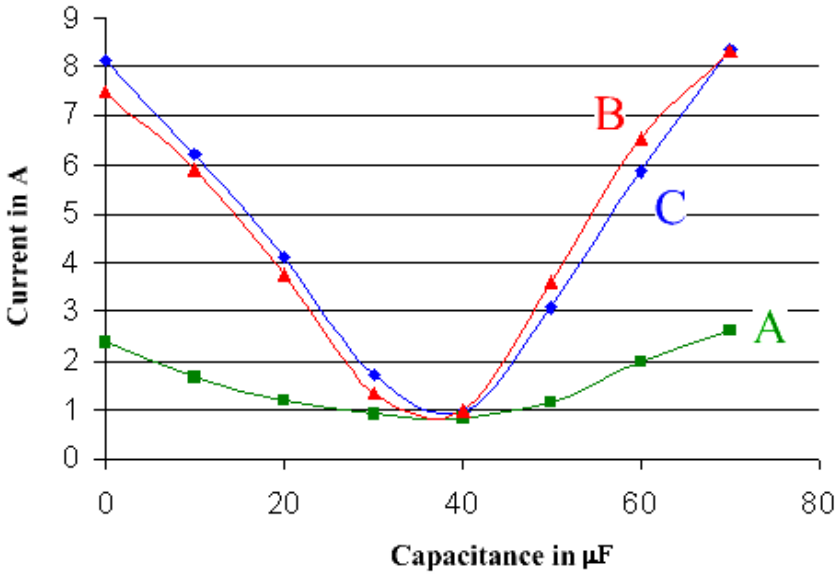


Figure 8.2: Current in the supply winding before (curve B) and after (curve A) application of the STATCOM, while the curve C represents the magnitude of the tertiary winding current

8.3.1.1 When the load seen from the supply side is inductive

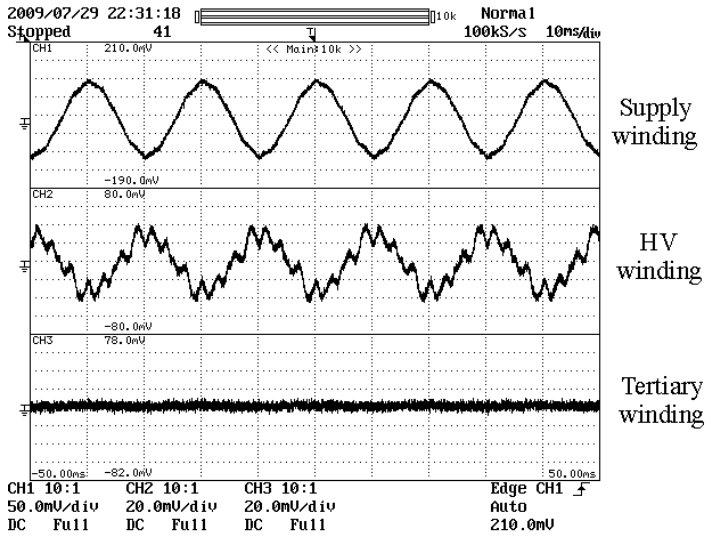


Figure 8.3 (a): Current waveforms, before application of the STATCOM, with a capacitive load of 5 µF connected across the HV winding

Figure 8.3(a) shows waveforms of the currents flowing through the three windings when a capacitive load of 5 μF was connected across the HV winding, and the tertiary winding was kept open.

Magnitudes of the currents flowing through the supply and the HV windings were 7.2 A (8% THD) and 0.27 A (THD > 35 %) respectively. From Figure 8.3 (a), it can be seen that 7^{th} order harmonic component is dominant due to the resonance effect.

The connection of the STATCOM to the tertiary winding reduces the supply current to 2 A (35% THD), while magnitude of the tertiary winding current measured is 6.8 A (10% THD). The HV winding current remains the same. The total harmonic distortion issue is discussed in Section 8.3.2.

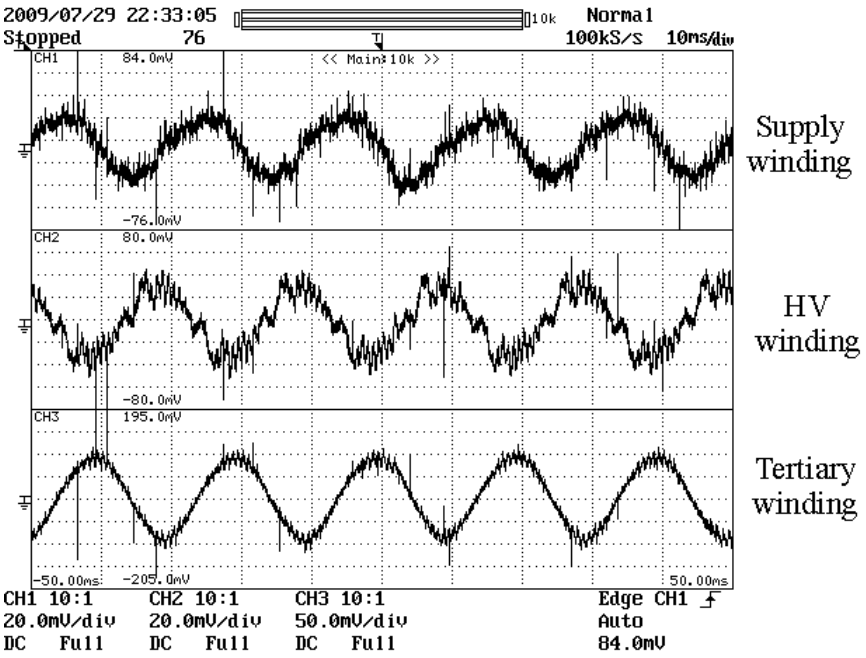


Figure 8.3 (b): Current waveforms, after application of the STATCOM, with a capacitive load of 5 μF connected across the HV winding terminals

8.3.1.2 When the load seen from the supply side is capacitive

As the load connected to the terminals of the HV winding becomes more and more capacitive, the total harmonic distortion reduces significantly. Figure 8.4 (a) shows the current waveforms in the three windings, when a capacitive load of 60 μF was connected across the HV winding terminals, before connecting the

STATCOM. Magnitudes of the supply and HV winding currents were 5.85 A (1.32 % THD) and 3.77 A (5.6 % THD) respectively.

As shown in Figure 8.4(b), after connecting of the STATCOM, the supply current reduces to 2 A (33.5 % THD), and the current flowing in the tertiary winding increases to 6.56 A (1.8 % THD).

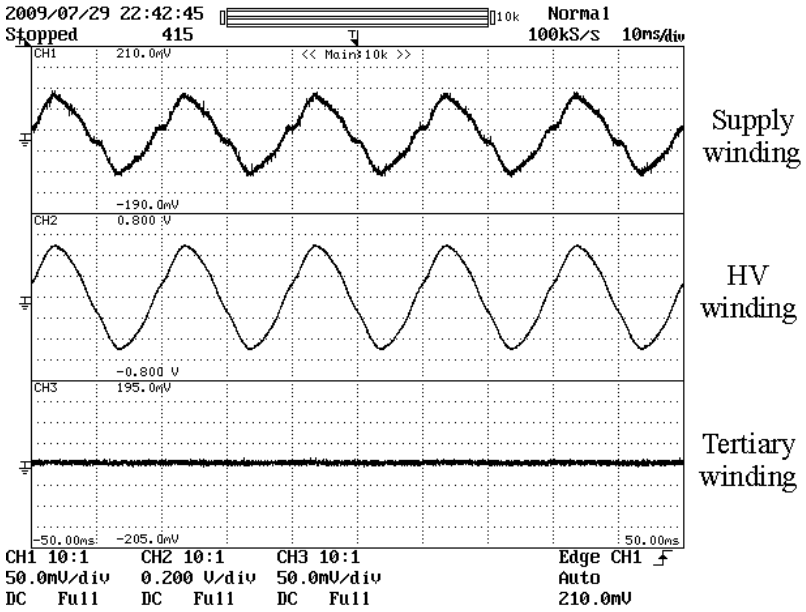


Figure 8.4(a): Current waveforms, before application of the STATCOM, with a capacitive load of 60 μF connected across the HV winding terminals

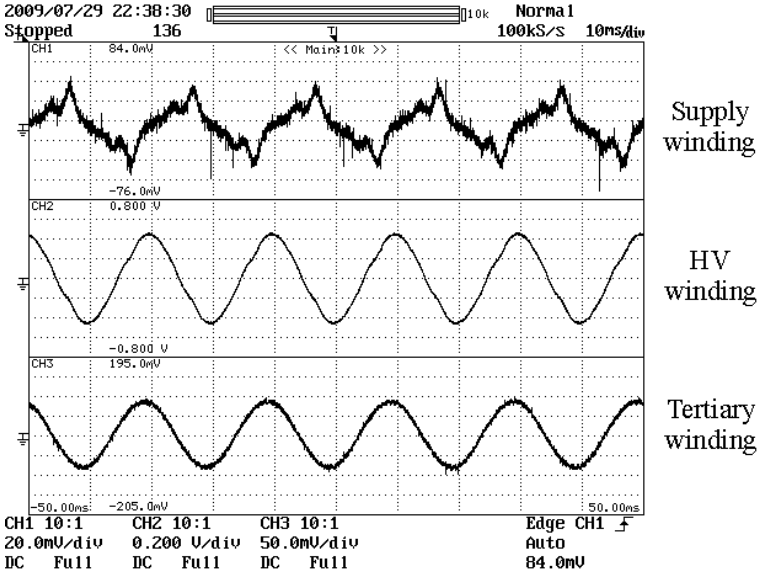


Figure 8.4(b): Current waveforms, after application of the STATCOM, with a capacitive load of 60 μF connected across the HV winding terminals

8.3.2 Total harmonic distortion of currents flowing through the three windings

As shown by curve B in Figure 8.5, before applying the STATCOM to the tertiary winding, the total harmonic distortion, I_{S_THD}, corresponding to the current in the supply winding, I_s, increases with the capacitance until the resonance condition is reached.

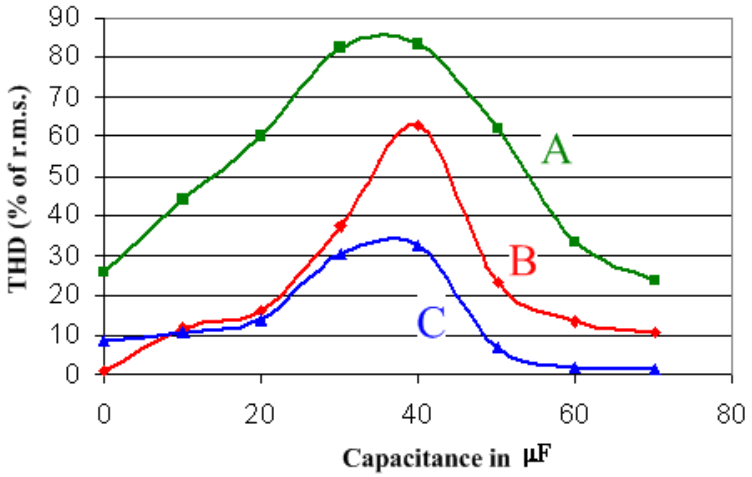


Figure 8.5: THD (% of r.m.s. value) in the supply current before (curve B) and after (curve A) application of the STATCOM, where curve C represents the % THD in the tertiary winding current

At the resonance condition the supply current THD is at its highest, and then reduces as the capacitive load increases further (i.e. $X_c > X_m$). Near resonance condition, the magnitude of the fundamental component of the total current is at the minimum and hence the harmonic components become dominant.

After application of the STATCOM, a considerable level of current harmonic distortion was observed in the tertiary winding as shown by curve C. As the tertiary winding is magnetically coupled with the supply winding, a significant increase in I_{S_THD} was observed as shown by curve A.

As demonstrated in Fig. 8.6, the total harmonic distortion corresponding to the HV winding current after connecting the STATCOM remains similar to that before (curve B) connecting the STATCOM.

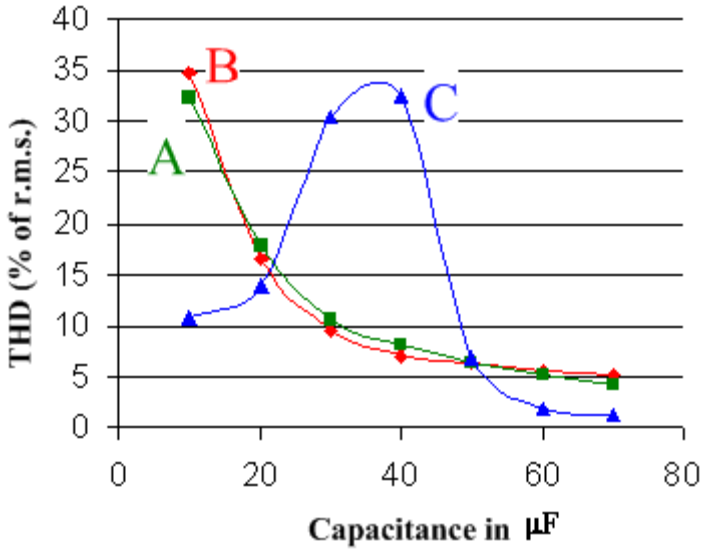


Figure 8.6: THD (% of r.m.s value) in the HV winding current before (curve B) and after (curve A) connecting of the STATCOM, where the % THD in the tertiary winding current is shown by curve C

8.3.3 VA gain of the supply winding

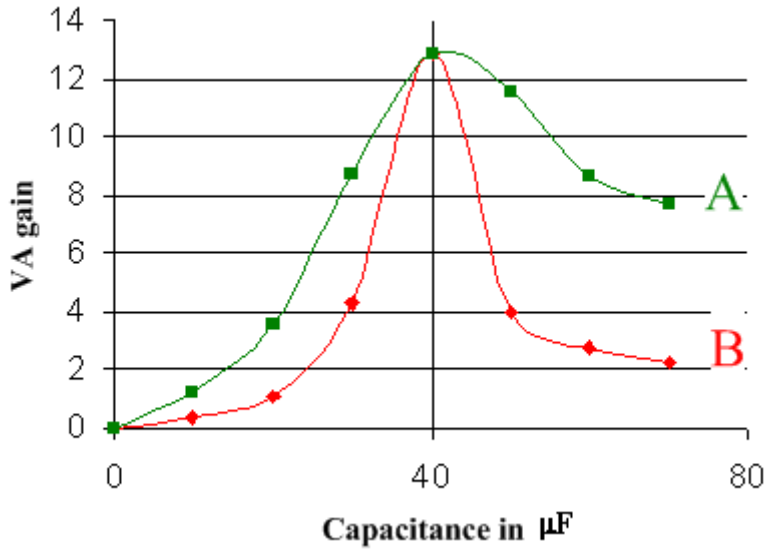


Figure 8.7: VA gain of the supply winding before (curve B) and after (curve A) connecting the STATCOM

Before connecting the STATCOM, as shown in Figure 8.7, the supply voltage winding attains higher VA gains with respect to the HV winding at/near resonance conditions. The STATCOM connection changes the VA gain curve of the supply winding and higher VA gains are achieved than without its connection.

8.3.4 Real power losses

The real power losses that occur in the converter, tertiary winding and d.c. capacitor are drawn from the supply side. As illustrated in Fig. 8.8, there is a significant increase in the real power losses after connection of the STATCOM (curve 'A') as compared to before its application (curve 'B').

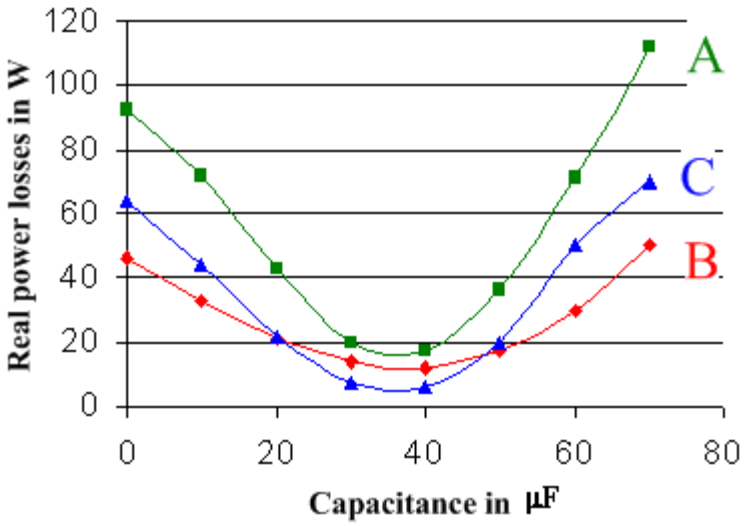


Figure 8.8: Real power losses in the supply winding before (curve B) and after (curve A) connecting the STATCOM, and curve C represents the real power losses in the tertiary winding

Except near the resonance point, the real power losses with the STATCOM are almost twice as large as without the STATCOM. This is because of the additional real power consumed by the STATCOM. Curve C shows the real power loss in the tertiary winding and the VSC.

As given by equation 4.1, the real power exchange between the supply side and the STATCOM varies in a form of a sine function with the delay angle, δ. In Fig. 8.9, curves S and T show the variation of the real power loss in the supply and the tertiary windings respectively with the delay angle, δ.

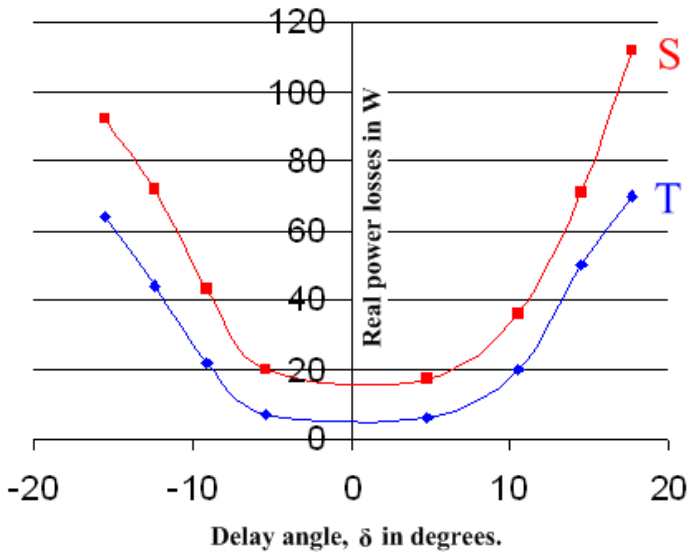


Figure 8.9: Variation of real power losses in the supply (curve S) and the tertiary (T') windings with respect to the delay angle, δ

8.3.5 Voltage waveforms across the terminals of the three windings under different loading conditions

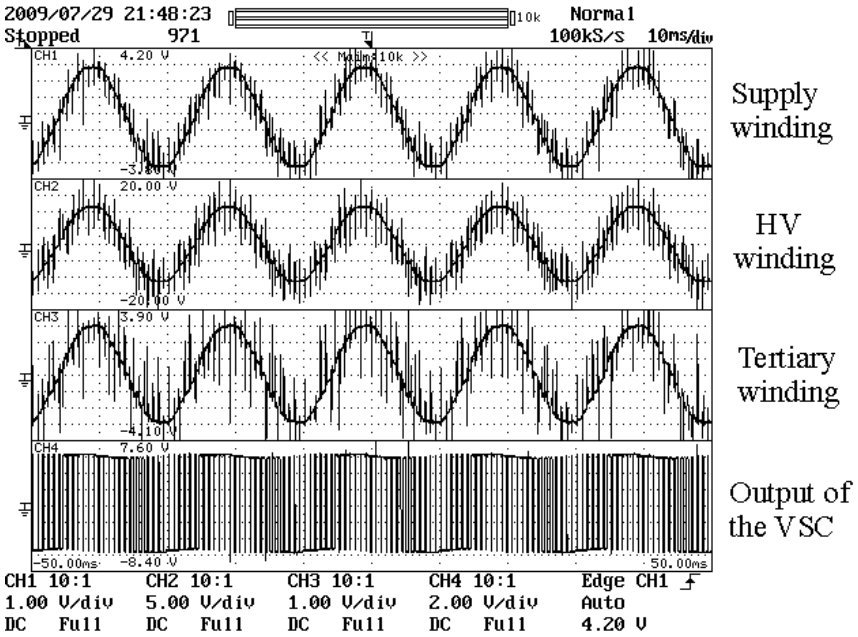


Figure 8.10: Voltage waveforms across the different parts of the system under 'no load' situation after application of the STATCOM

Switching of IGBTs of the STATCOM injects harmonics into the system. This results in harmonics not only in the tertiary winding but also in the windings magnetically coupled with it, i.e. the supply and the HV windings. This is illustrated in Fig. 8.10.

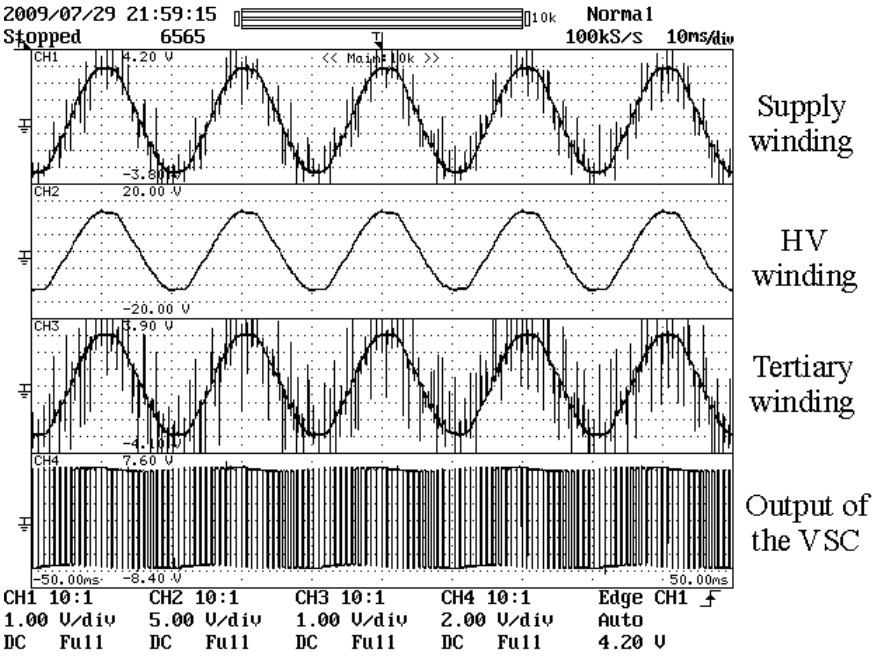


Figure 8.11: Voltage waveforms across the different parts of the system, when a capacitive load of 5 μF was connected across the HV winding terminals

When a capacitive load of 5 μF is connected across the HV winding, harmonics in the voltage waveform of that winding are filtered out completely. This capacitor also reduces the harmonics in the supply voltage. These are shown in Fig. 8.11.

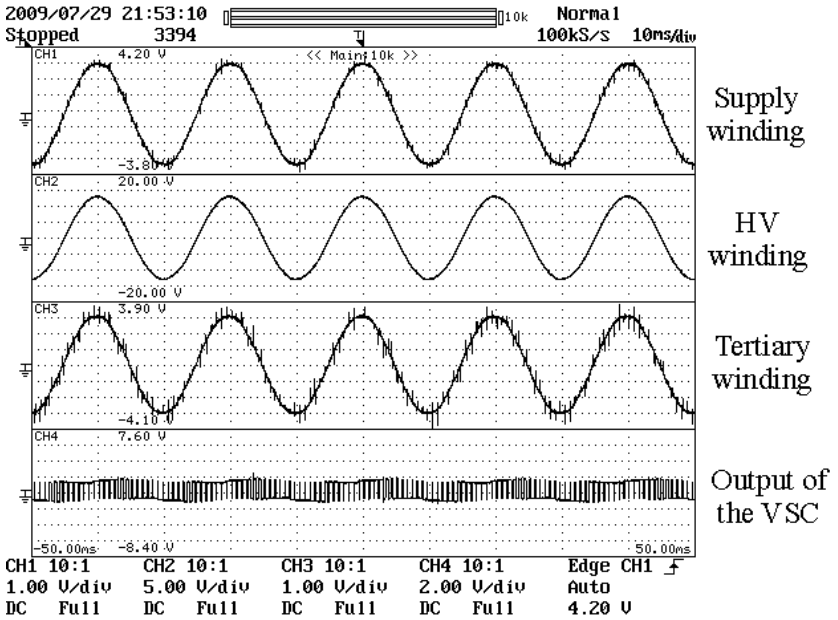


Figure 8.12: Voltage waveforms across the different parts of the system, when a capacitive load of 60 μF was connected across the HV winding terminals

As the size of the capacitive load connected across the HV winding terminals increases, harmonics injected by the STATCOM reduce. Figure 8.12 shows the voltage waveforms across the three windings and SPWM waveform across the a.c. terminals of the VSC when a capacitive load of 60 μF is applied across the HV winding.

8.4 Summary

The performance of the prototype VSC based STATCOM is demonstrated in this chapter. The main aim of reducing the amount of the supply current to its real component is achieved.

It is observed that the application of the STATCOM to the tertiary winding not only injects harmonics into that winding but also into the windings magnetically coupled with it. Application of the STATCOM changes the characteristics of the system such as VA gain of the supply winding, real power loss etc.

Chapter 9

Conclusions and recommendations for future work

9.1 Introduction

The University of Canterbury has designed and built partial core inductors and transformers. The low magnetising reactance of a partial core transformer, with the ability to adjust its magnitude, makes the transformer a perfect fit for applications where loads are capacitive e.g. a.c. power frequency high voltage testing of generator insulation. The purpose of this research was to develop a scheme to automatically control the amount of reactive power in the supply winding of a partial core transformer. This will reduce the magnitude of the total supply current to its real component.

9.2 Applying a thyristor controlled static VAr compensator to a partial core transformer

Application of a thyristor controlled static VAr compensator to the tertiary winding was proposed. The scheme was modelled and analysed using PSCAD/EMTDC software. From the results obtained, it can be concluded that the TCR application to the three winding transformer enables a continuous variation of reactive power.

9.2.1 Limitations of the TCR application

Depending on the value of the firing angle, α, the TCR switching injects harmonics into the transformer windings.

The TCR consumes active power, which is drawn from the supply.

9.2.2 Suggestions for overcoming the limitations

The magnitude of harmonics can be reduced by designing a partial core transformer with a tertiary having a high leakage reactance.

Instead of implementing only the TCR control, a combined control could be considered, i.e. adjusting the position of the core of the partial core transformer such that most of reactive power can be supplied by the transformer magnetising reactance of the transformer. The TCR can be considered for only for fine tuning such that over or under compensation in the supply winding is avoided.

9.3 Applying a voltage source converter (VSC) to the third winding of a partial core transformer

9.3.1 Software part of the project

A single phase VSC based STATCOM was designed, modelled and analysed. Analysis of the system using Root locus and Bode plots in MATLAB shows that the system is stable for the full capacitive and inductive loads.

The PSCAD/EMTDC model demonstrates that the designed system is dynamically stable and capable of handling system disturbances. This confirms that the system is capable of offering a continuous reactive power control.

9.3.2 Hardware part of the project

Automatic closed loop control was achieved by implementing a PI based digital control system.

A controller board for sensing the control parameters in the supply winding was built. A 4 - pole Butterworth active filter was designed to filter noise, transients and harmonics in voltage and current waveforms to be fed to the control circuit. The controller board is capable of measuring the reactive component of the supply current. A zero crossing detection technique for the measurement of the phase angle θ, and synchronising the SPWM waveform with the supply voltage waveform was successfully implemented.

The power circuit consisting an IGBT based H - inverter, driver circuits, snubber circuits was designed, developed and built. Ratings of the components used to build the power circuit are of much higher values, which avoided failures while performing the experiments.

The control program was implemented in an 8 bit micro-controller, PIC18LF4680. The micro-controller was not only programmed to generate the SPWM waveform in a continuous manner but also simultaneously execute the PI based digital control system to achieve the required VAr compensation in the supply winding without losing stability.

Experiments were performed on the prototype for a range of load conditions. Results of the experiments are presented and discussed in Chapter 8. VAr compensation in the transformer supply circuit was achieved.

9.4 Recommendations for future work

9.4.1 Implementing the TCR control in partial core transformers

A prototype of the proposed TCR controlled three winding partial core transformer could be built.

9.4.2 Implementing the VSC based STATCOM in partial core transformers

- The switching frequency of the current system is 1350 Hz. However, it could be increased further to reduce harmonics in the system.
- The system could be designed and built for higher power ratings.
- The number of sensors could be reduced by implementing a better data acquisition system within the micro-controller.
- Instead of using a micro-controller, higher technology such as Digital Signal Processors could be used to enhance the performance and speed of the system.

- Robust, reliable and fast protection system could be designed to protect the STATCOM from any damage.

- The feasibility of using a partial core transformer/ VSC combination to replace a full core transformer could be studied and implemented.

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