Three-Phase Phase-Locked Loop Control of a New Generation Power Converter

W. Phipps[1] M.J. Harrison[2] and R. M. Duke[1]

[1] Department of Electrical and Computer Engineering,
University of Canterbury,
Christchurch, New Zealand.
Email: williamsphipps@eaton.com

[2]Eaton Powerware Ltd
Christchurch, New Zealand

Abstract

This paper describes the development of a new generation of power converter, used to power telecommunications equipment. A telecommunications converter must comply with the psophometric noise standard CCIF-1951 and the IEC1000-3-2 harmonic standard. While the IEC1000-3-2 standard is easily met with active power factor correction techniques, a high degree of effort is usually required to meet with the psophometric standard. Therefore, a control methodology utilising a three-phase phase-locked loop is introduced as a method of complying with the psophometric standard under distorted mains conditions. Simulations show that combining this with a novel feedback controller, results in an improved load step response over using a traditional proportional integral type controller.

1 Introduction

Traditional converters, used as dc power supplies in the telecommunications industry are typically a single-phase two-stage design. The reason for a two-stage design is that there are industry specific standards that the converters have to comply with. The major two being the CCIF-1951 and the IEC1000-3-2 standard [1]. The CCIF-1951, commonly known as the psophometric noise standard was originally introduced to regulate audible noise on telephone networks. The source of this noise was due to the use, at that time, of full bridge SCR rectifiers.

These rectifiers typically had no output filtering and as a result had considerable noise on the output (600Hz ripple). The telephone networks were initially analogue and because of the output ripple, audible noise was produced on the phone lines. Nowadays, with digital exchanges the telephone systems have become more immune to dc power supply noise. The psophometric standard is still used however as the defining standard for the interface between telecommunication switching equipment and telecommunication dc power equipment, hence dc power manufacturers have to comply with this standard in order to market their products.

The IEC1000-3-2 standard was introduced to regulate harmonic currents drawn from the mains supply. These harmonic currents reduce the efficiency of the power drawn from the mains and can excite resonances, as well as overloading the circuit wiring. Having to comply with these standards has dictated the way in which telecommunications manufacturers have had to design their systems. A typical telecommunications power converter is a single-phase two-stage topology as shown in Figure 1. The first stage of the converter is usually a boost stage, used to provide power factor correction (PFC) and hence regulate the maximum allowable input harmonic current content defined by the IEC1000-3-2 standard [1]. The boost regulator is a popular choice for PFC. Some of the reasons are, a simple topology, a high efficiency, and due to the input inductor being in series with the ac power the input current is continuous, resulting in less EMI and therefore reduced input filtering requirements [2]. A boost converter however, has an inherent weakness in that it cannot provide effective protection from output short-circuit failure.

The dc-dc converter second stage is required to provide fast regulation of the output voltage to reject the psophometric noise, as well as providing isolation and voltage transformation. The isolation is both a functional and a safety requirement of the telecommunications industry; the voltage transformation is needed as telecommunication systems typically operate off a -48V supply.

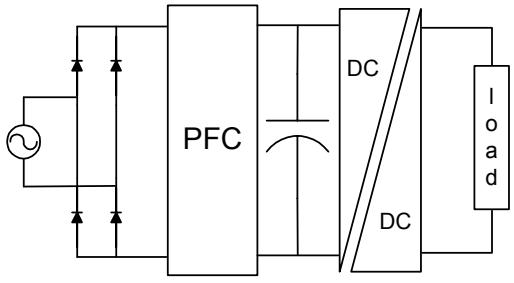

Figure 1: Traditional Converter

The traditional single-phase converter has at the output of the PFC stage 100Hz ripple content due to the discontinuity at the mains zero crossing. As a consequence of this a large storage capacitor is required.

0-7803-9514-X/06/$20.00 ©2006 IEEE ICIEA 2006

Having a two-stage design results in the output power being processed twice, this cascade effect results in a reduction in the overall efficiency. Typical two-stage designs have efficiencies of around 90%. In addition, a two-stage design requires two independent controllers, one for each stage.

A new three-phase single-stage converter has been proposed in [3]. The design allows a constant power flow from supply to load by implementation of a squaring transfer function on the input voltage. This allows the load to be ripple free as well as maintaining a unity power factor, thus satisfying all the necessary standards. The IEC1000-3-2 standard needs only to be met under ideal conditions, whereas the psophometric standard needs to be constantly maintained.

The performance of this three-phase single-stage converter was previously investigated under conditions of a mains phase voltage imbalance [3], it was found that in order to theoretically maintain zero output voltage ripple, and maintain compliance with the psophometric standard, a three-phase phase-locked loop (PLL) control technique was needed.

2 Phase Locked Loop

The PLL was originally described in 1923 and 1932 [4] and has been used as a common way of recovering and utilising phase and frequency information in electrical systems. In the area of power electronics, the PLL technique has been adopted in the speed control of electric motors, as well as synchronising of utility voltages and the control of currents or voltages in utility interface operations [5]. A commonly used three-phase PLL structure is illustrated in Fig. 2. In this design the phase voltages V_a,V_b,V_c are obtained from the line voltages, these stationary reference frames are transformed via the Clark-Park transformation into a reference frame synchronised to the utility frequency. The angle θ used in these transformations is obtained by integrating a frequency command ω^*. If the frequency command is identical to the frequency of the utility ω_{ref} the voltages V_d and V_q appear as dc values depending on the angle θ. Setting the direct axis reference voltage (V_d^*) to zero results in the extinguishing of the error between V_d^* and V_d as a result of the feedback. This locks the PLL output with the utility voltage. In order to generate three-phase outputs (u,v,w), θ needs to undergo an inverse Park and inverse Clark transformation.

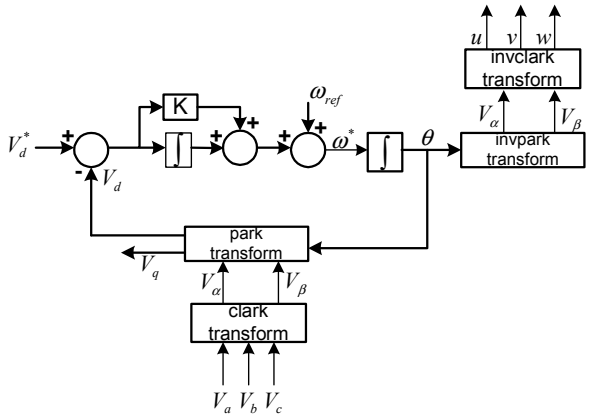

Figure 2: Traditional PLL Structure

2.1 New Three-Phase PLL Design

A new three-phase PLL design is proposed by the authors and is shown in Fig. 3. Unlike the traditional design the new PLL operation does not involve any coordinate system transformations, resulting in a more simple PLL solution.

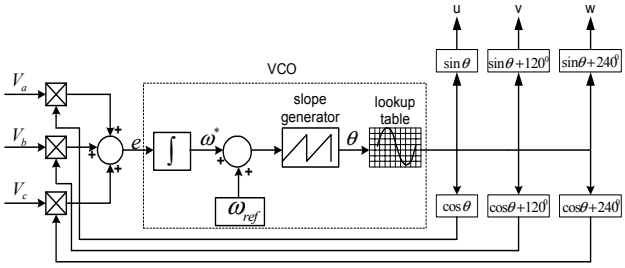

Figure 3: New Proposed PLL Structure

The PLL consists of the input three phase voltages V_a,V_b,V_c being fed into multipliers; these multipliers serve as phase detectors. In any PLL system under conditions of a phase lock the two input signals into the multiplier are phase shifted by 90°. The principle of phase detection is shown in the following mathematical analysis; where S_1 and S_2 are two sinusoidal signals phase shifted by 90°and S_3 is their product.

$$S_3(t) = S_1(t)S_2(t)$$

where $S_1(t) = A_1 \sin[\omega t + \theta_1(t)]$

and $S_2(t) = A_2 \cos[\omega t + \theta_2(t)]$

The output of the multiplier is

$$S_3(t) = A_1 A_2 \sin[\omega t + \theta_1(t)]\cos[\omega t + \theta_2(t)]$$

This expression can be rewritten as

$$S_3(t) = \frac{A_1 A_2}{2}\sin[\theta_1(t) - \theta_2(t)] + \frac{A_1 A_2}{2}\sin[2\omega t + \theta_1(t) + \theta_2(t)] \quad (1)$$

In this form it can be seen that the multiplier signal consists of two parts, the first being a function of the phase difference only, whilst the second term is at a frequency that is twice the signal frequency plus the sum of the two phases. In other words the multiplier output consists of a dc signal, since the phase difference is not a function of frequency, and a signal at twice the fundamental frequency. The first term is called the error signal $S_e(t)$.

$$S_e(t) = \frac{A_1 A_2}{2} \sin[\theta_1(t) - \theta_2(t)]$$

If the phase difference is zero degrees, then the error signal is zero, which represents the locked state of the PLL. Any state other than the locked state will result in a non-zero error signal. In single-phase PLL systems it is necessary to remove the second harmonic term by using a low pass filter since it contains no useful information.

In the proposed three-phase PLL, this second harmonic term does not naturally occur and therefore reduces the filtering requirement of the system. If the output signal of each multiplier shown in Fig. 3 is represented by equation (1), but phase shifted by 120˚, then the following mathematical analysis applies.

Let $\frac{A_1 A_2}{2}$=G and $[2\omega t + \theta_1(t) + \theta_2(t)] = \phi$

The second harmonic term can now be simply written as $G\sin\varphi$. In the proposed PLL the outputs of the phase detectors are summed together under conditions of a phase lock, the error signal or dc term will be zero. What remains are the three second harmonic terms which sum to zero.

$$\begin{aligned} &G\sin\varphi + G\sin(\varphi + 120^o) + G\sin(\varphi + 240^o) \\ &= G\sin\varphi - \frac{1}{2}G\sin\varphi + \frac{\sqrt{3}}{2}\cos\varphi - \frac{1}{2}\sin\varphi - \frac{\sqrt{3}}{2}G\cos\varphi \\ &= 0 \end{aligned}$$

Hence, under ideal mains conditions there is theoretically no second harmonic component present. This result reduces the filtering effort required for implementation. Similarly, any common noise at the three-phase inputs will also be removed. The resultant error signal $S_{ERR}(t)$ in the proposed three-phase PLL is given as

$$S_{ERR}(t) = \frac{3A_1 A_2}{2} \sin[\theta_1(t) - \theta_2(t)] \qquad (2)$$

Summing together the three phase detector outputs, results in a dc error signal. A zero error signal is achieved by changing the phase of the feedback signals to match the phase of the input voltages V_a,V_b,V_c. The voltage-controlled oscillator (VCO) depicted in Fig. 3 performs this task. If the error signal is zero the VCO produces a 50Hz quiescent frequency ω_{ref}, but if the error signal is something other than zero, then it responds by changing its operating frequency. In general the VCO (Fig. 3) has a constant K_0 representing the change in the instantaneous frequency of the VCO as a function of the error signal (e) such that

$$K_0 = \frac{d\omega}{de}$$

The feedback signal out of the VCO for each phase is given by

$$S_2(t) = A_2 \cos[\omega_{ref} + \theta_2(t)]$$

As the error signal e(t) changes with time, the VCO will produce a change in the output signal frequency ω_{out} given by the following relationship

$$\omega_{out} = \omega_{ref} + K_0 e(t)$$

where ω_{ref} is the usual operating frequency (50Hz). The phase $\theta_2(t)$ is the integral of the time varying error signal.

$$\begin{aligned} \theta_2(t) &= 2\pi K_0 \int_0^t e(t)dt \qquad (3) \\ &= 2\pi K_0 et \end{aligned}$$

So as long as the error signal has a non-zero value, the phase of the VCO signal will keep on increasing until such time as it equals $\theta_1(t)$ and the error decreases to zero. Substituting equation (3) into (2) $S_{ERR}(t)$ can now be represented as

$$S_{ERR}(t) = \frac{3A_1 A_2}{2} \sin[\theta_1(t) - 2\pi K_0 et] \qquad (4)$$

For small angles $\sin(\theta) \approx \theta$ and equation 4 can now be rewritten as

$$S_{ERR}(t) = \frac{3A_1 A_2}{2} [\theta_1(t) - 2\pi K_0 et]$$

It can now be seen that at time t, the frequency of the signal produced by the VCO increases by $K_o e$. As long as the error signal is present, the phase keeps changing linearly. However, as the phase of the signal out of the VCO changes, the new difference in phase decreases and the error signal amplitude decreases as a consequence. This decreases the phase change further until the error signal amplitude has reached zero. In the event of a negative error signal the VCO will simply

decrease its frequency by $K_o e(t)$ giving the effective frequency range as

$$\omega_{out} = \omega_{ref} \pm K_0 e(t)$$

3 PLL Simulation

Fig. 4 shows a simulation model of the proposed PLL, which is carried out using a software package called PSIM. The simulation is performed with the input voltages at unity magnitude, 50Hz frequency and with an initial 30˚ phase shift relative to the output. From Fig. 5 the results show the input phase voltage R and output phase voltage Vr achieving synchronism within three mains cycles. The same is the case for the yellow and blue phase voltages.

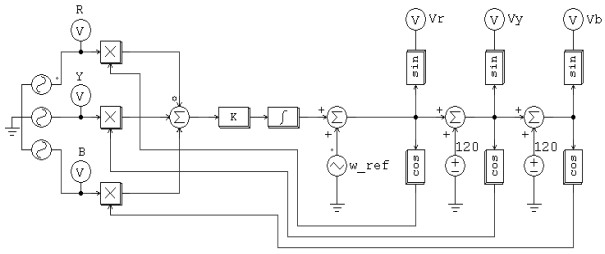

Figure 4: PLL Simulation Model

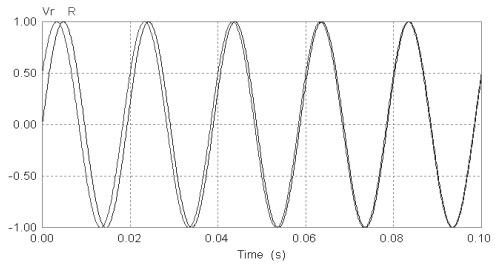

Figure 5: PLL Synchronisation

3.1 PLL Under Mains Distortion

The PLL is now simulated with a mains input phase voltage imbalance; this is done by attenuating the red phase voltage R by 20% at t=40ms as well as having an intial 30˚ phase shift. Harmonic distortion is introduced as well representing extreme mains conditions. The waveform as seen in Fig. 6 shows that even under these conditions the PLL is able to obtain and maintain phase lock within three mains cycles producing a clean output sinewave Vr. The noise immunity of the PLL is very good, due the good filtering characteristic achieved by the summing of the three phases and by the integrator in the feedforward path (Fig. 4).

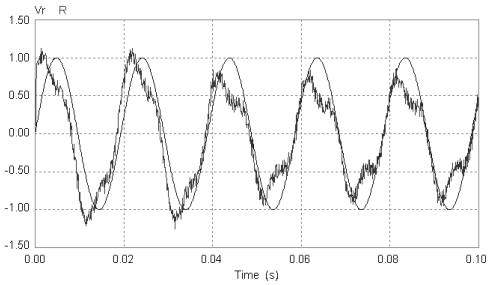

Figure 6: PLL Synchronisation Under Mains Distortion

4 Converter Control

During mains phase voltage imbalance there is a deterioration of the power factor and the occurrence of output voltage ripple in the converter proposed in [3]. Since the psophometric standard needs to be maintained there can be no output voltage ripple permitted. A control technique involving the three-phase PLL is introduced to the converter controller to compensate for mains phase imbalance. Fig. 7 shows the model of the converter with PLL feedforward control.

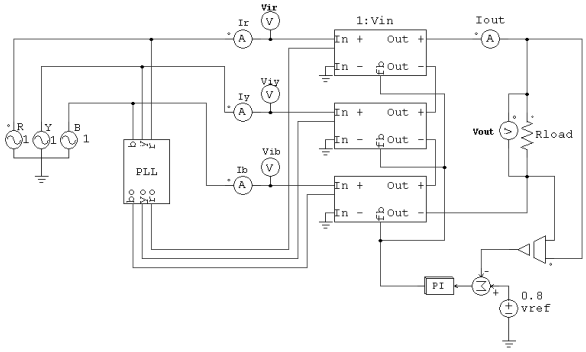

Figure 7: Converter with PLL Control

The converter controller is able to compensate for mains phase imbalance due to the fact that the PLL is placed in the feedforward path. Since the inputs to the PLL are the mains voltages, and as already shown in sections 3 and 3.1 the outputs of the PLL represent pure sine waves despite any mains distortion that may be present. These clean three-phase output signals, all having equal magnitude, are an ideal representation of the mains voltages. Any discrepancies then show up as an error signal and the converter controller generates the appropriate compensation signals to maintain a constant power flow to the load, preventing any voltage ripple, due to mains variations from occurring.

Assuming the PLL is initially in a locked state, by applying a distorted mains phase voltage undergoing a 20% attenuation at t=40ms one can see from Fig. 8 the output voltage V_{out} as seen across the load has no ripple present, thereby showing that the PLL control used as a feedforward compensation component allows the converter to successfully prevent any output voltage ripple from occurring under the conditions of a mains

phase voltage imbalance, as well as providing immunity from input harmonic phase distortions.

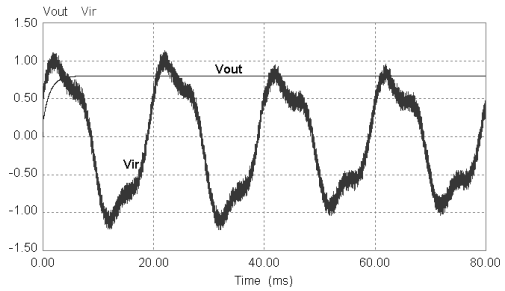

Figure 8: Output voltage under PLL Control

5 Converter Load Step Response

The performance of the converter is further investigated under conditions of a load step response and its ability to react to a change in the load. The simulated converter undergoes a 10% load step change at time t=40ms and the output voltage can be seen in Fig. 9. During the load step change there exists an amount of overshoot occurring when using a traditional PI controller. An improved control technique is required to compensate for the output voltage variations brought about by a load step change.

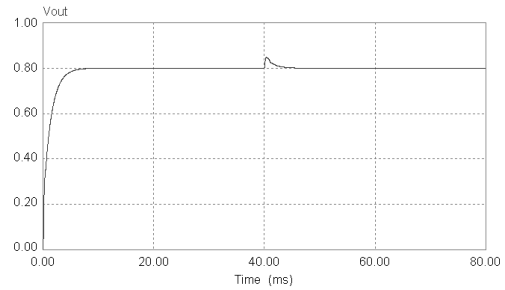

Figure 9: Output Voltage With Load Step Change

6 PDF Control

A control strategy is proposed to compensate for any load step changes. This involves incorporating a pseudo derivative feedback (PDF) control technique, which has been used successfully in the area of motion control and offers a high degree of disturbance rejection capability [6] [7].
Fig. 10 shows that under the same load step change described previously in Section 5, there is no overshoot taking place.

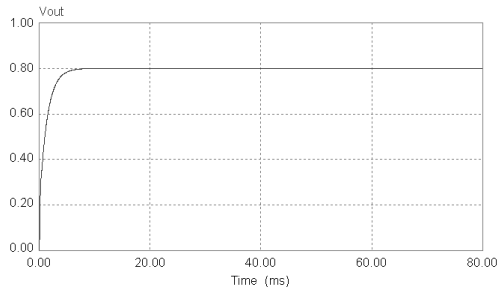

Figure 10: Load Step Response Under PDF Control

7 Conclusion

A new three-phase PLL has been introduced and shown to have a benefit over the traditional three-phase PLL by virtue of the fact that no coordinate transformations are required. The transformations associated with the traditional PLL amount to processing overhead, which in turn lead to delays in the overall control process.

Simulations have shown that the new PLL is able to synchronise with the mains voltages even when there is a high degree of harmonic distortion and phase imbalance. This allows the implementation of a control method of compensating for these non-ideal mains conditions. This controller uses the new PLL as part of a feedforward loop that enables the converter to compensate for mains non-linearity's while still maintaining zero output voltage ripple, thus complying with the psophometric standard.

Under the conditions of a load step change it was shown that output voltage consistency couldn't be sustained using the conventional PI type feedback control loop. A new PDF feedback control technique was introduced as a solution, with simulations showing no output voltage overshoot being theoretically achievable.

It can be concluded with confidence that the results of the simulations using the new three-phase PLL controller with PDF control allows the realisation of a new generation power converter that meets the required industry standards and offers improved performance over conventional designs.

8 Acknowledgements

I would like to thank Eaton Powerware Ltd for their continued support for the converter project as well as the Tertiary Education Commission.

References

[1] A. Pietkiewitz, D. Tollik, "Single-Stage Power Factor Corrected Rectifier Topology", Telecommunications Energy Conference, INTELEC 21st International, 6pp., 6-9 June 1999.

[2] Z. Yang and P.C. Sen, "Recent Developments in High Power Factor Switch-mode Converters", IEEE Canadian Conference on Electrical and Computer Engineering, Vol 2, pp. 477-480, 24-28 May 1998.

[3] W. Phipps, M.J. Harrison and R. Duke, "New Generation Power Converters", paper no. 110, accepted for presentation at the Australasian Universities Power Engineering Conference AUPEC 05, Sept. 2005.

[4] H. Awad, J. Svensson, and M.J. Bollen, "Tuning Software Phase-locked Loop for Series-Connected Converters", IEEE Transactions on Power Delivery, Vol. 20, No. 1, pp. 300-308, Jan. 2005.

[5] S. Chung, "A Phase Tracking System for Three Phase Utility Interface Inverters", IEEE Transactions on Power Electronics, Vol. 15, No. 3, pp. 431-438, May 2000.

[6] D.Y. Ohm, "Analysis of PID and PDF Compensators For Motion Control Systems", IEEE Industry Applications Society Annual Meeting, Vol. 3, pp. 1923-1929, Oct. 1994.

[7] J.K. Kang, J.T. Lee, Y.M. Kim, B.H. Kwon, K.S. Choi, "Speed Controller Design For Induction Motor Drives Using a PDF Control and Load Disturbance Observer", International Conference on Industrial Electronics, Control and Instrumentation, IECON'91, Vol. 1, pp. 799-803, Oct. 1991.