SCALED-DOWN MODELLING AND MICROPROCESSOR FACILITIES FOR THE
SIMULATION AND ASSESSMENT OF HVDC CONVERTOR DISTURBANCES

A thesis

submitted for the degree of

Doctor of Philosophy in Electrical Engineering

in the

University of Canterbury

by

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Department of Electrical and Electronic Engineering,

University of Canterbury,

Christchurch, New Zealand

1983
Please kindly correct the following errors rectified recently.

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<th>Page</th>
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Title:

SCALED-DOWN MODELLING AND MICROPROCESSOR FACILITIES FOR THE SIMULATION AND ASSESSMENT OF HVDC CONVERTOR DISTURBANCES

Ph.D. Thesis submitted on the 29th of March, 1983

Yours Sincerely,

[Signature]
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Units and Abbreviations
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The majority of symbols are defined as they appear in the text, and a comprehensive system of scripting is used for clarity. For convenience the principal symbols are redefined below.

<table>
<thead>
<tr>
<th>Symbols</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>Variable Gain of Error Signal Generator</td>
</tr>
<tr>
<td>$A_i$</td>
<td>Anode of Convertor Valve $V_i$</td>
</tr>
<tr>
<td>$A_i, ADR_i$</td>
<td>Address Bus Bit $i$ ($i = 0$ to $15$)</td>
</tr>
<tr>
<td>$AB_i$</td>
<td>Arcback (Backfire) of Convertor Valve $V_i$</td>
</tr>
<tr>
<td>$BLK_i$</td>
<td>&quot;Low&quot; to Block $FP_i$</td>
</tr>
<tr>
<td>C</td>
<td>Capacitance</td>
</tr>
<tr>
<td>$C_i$</td>
<td>Capacitor $i$</td>
</tr>
<tr>
<td>$C_{i+1}$</td>
<td>Commutating-voltage-zero Crossing Instant ($i = 1$ to $6$) (in the Figures $C_i$)</td>
</tr>
<tr>
<td>$Ck$</td>
<td>Clock Pulse</td>
</tr>
<tr>
<td>$CP_i, i+2$</td>
<td>Commutation Failure, i.e. Failure to Commutate Current from Valve $V_i$ to Valve $V_{i+2}$</td>
</tr>
<tr>
<td>$CLR_i$</td>
<td>&quot;Low&quot; to Clear $FP_i$</td>
</tr>
<tr>
<td>$CS_i$</td>
<td>Chip-Select Signal of Integrated Circuit $i$ (Active-Low)</td>
</tr>
<tr>
<td>$Di$</td>
<td>Diode $i$</td>
</tr>
<tr>
<td>$D_i, DAT_i$</td>
<td>Data Bus Bit $i$ ($i = 0$ to $7$)</td>
</tr>
<tr>
<td>E</td>
<td>Root-mean-square (r.m.s.) Value of Commutating Voltage</td>
</tr>
<tr>
<td>$E_m$</td>
<td>Crest Value of Line-to-Neutral Voltage of an AC System, Normally $\sqrt{3} E_m = \sqrt{2}E$</td>
</tr>
<tr>
<td>$EA_i, \delta_i$</td>
<td>Extinction Angle of Convertor Valve $V_i$ ($i = 1$ to $6$)</td>
</tr>
<tr>
<td>$EDDC$</td>
<td>&quot;Low&quot; to Enable Direct Digital Control</td>
</tr>
<tr>
<td>$FP_i$</td>
<td>Firing Pulses to Valve Gates $G_1$ to $G_8$ (Normally about 120 degrees of Duration for Valve $V_{i}$ to $V_6$)</td>
</tr>
<tr>
<td>$PT_i$</td>
<td>Firethrough of Convertor Valve $V_i$</td>
</tr>
<tr>
<td>G</td>
<td>Ground Potential</td>
</tr>
<tr>
<td>$G_i$</td>
<td>Gate (or Grid) of Convertor Valve $V_i$</td>
</tr>
<tr>
<td>$I_d$</td>
<td>Direct Current of Convertor (Direct Line Current)</td>
</tr>
<tr>
<td>$I_{dn}$</td>
<td>Nominal Direct Current of Convertor</td>
</tr>
<tr>
<td>Symbol</td>
<td>Description</td>
</tr>
<tr>
<td>--------</td>
<td>-------------</td>
</tr>
<tr>
<td>$I_{ds}$</td>
<td>Constant Current Control Setting (Direct Current Reference)</td>
</tr>
<tr>
<td>$\Delta I_{ds}$</td>
<td>Direct Current Margin</td>
</tr>
<tr>
<td>$I_{Ci}$</td>
<td>Integrated Circuit $i$</td>
</tr>
<tr>
<td>$I$-INT$n$</td>
<td>Interrupt Service Routine Level $n$ of Interactive Controller</td>
</tr>
<tr>
<td>$K_i$</td>
<td>Convertor Control-System Constant</td>
</tr>
<tr>
<td>$K_{li}$</td>
<td>Cathode of Convertor Valve $V_i$</td>
</tr>
<tr>
<td>$L$</td>
<td>Inductance in General</td>
</tr>
<tr>
<td>$L_L$</td>
<td>Leakage Inductance (Commutating Reactance $\omega L$) per Phase of Convertor Transformer</td>
</tr>
<tr>
<td>$L_b$</td>
<td>DC Blocking Reactor</td>
</tr>
<tr>
<td>$I_d$</td>
<td>DC Smoothing Reactor or its Inductance</td>
</tr>
<tr>
<td>LED$i$</td>
<td>Light Emitting Diode $i$</td>
</tr>
<tr>
<td>MF$_i$</td>
<td>Misfire of Convertor Valve $V_i$</td>
</tr>
<tr>
<td>$N$</td>
<td>AC-System Neutral</td>
</tr>
<tr>
<td>ON$_i$</td>
<td>ON/OFF (Conducting or Non-Conducting) State of Convertor Valve $V_i$</td>
</tr>
<tr>
<td>$P_{i}$</td>
<td>Instant of Start of Conduction of Convertor Valve $V_i$</td>
</tr>
<tr>
<td>$\Delta P_{i}$</td>
<td>Firing Instant Correction</td>
</tr>
<tr>
<td>P-INT$n$</td>
<td>Interrupt Service Routine Level $n$ of Process Controller</td>
</tr>
<tr>
<td>$P_{RI}$</td>
<td>Normally, &quot;Low&quot; to Fire Convertor Valve $V_i$</td>
</tr>
<tr>
<td>$Q$</td>
<td>Quality Factor of Filter</td>
</tr>
<tr>
<td>$Q$</td>
<td>Logic Output State &quot;High&quot; or &quot;Low&quot;</td>
</tr>
<tr>
<td>$R$</td>
<td>&quot;High&quot; to Reset Flip-Flop</td>
</tr>
<tr>
<td>$R$</td>
<td>Resistance</td>
</tr>
<tr>
<td>$R_{i}$</td>
<td>Resistor $i$</td>
</tr>
<tr>
<td>$R$, $Y$, $B$</td>
<td>Red, Yellow and Blue Phases of an AC System (Equivalent to a, b, and c Phases)</td>
</tr>
<tr>
<td>$RD$</td>
<td>Generalized Memory/Port Read Strobe (Active-Low)</td>
</tr>
<tr>
<td>RST$n$</td>
<td>Interrupt Request Level $n$</td>
</tr>
<tr>
<td>$S_i$</td>
<td>Instant of End of Conduction of Convertor Valve $V_i$</td>
</tr>
<tr>
<td>$\Sigma_i$</td>
<td>Combined CC and CEA Output for Valve $V_i$, Firing in Predictive Controller</td>
</tr>
<tr>
<td>SW$i$</td>
<td>Switch $i$</td>
</tr>
<tr>
<td>$T$</td>
<td>Period of AC-System Frequency</td>
</tr>
</tbody>
</table>
Initiation of Conduction of Convertor Valve \( V_i \) (i = 1 to 6, Timing Pulses of Short Duration)

Thyristor Valves Numbered from 1 to 6 Referring to Firing Sequence; also By-pass and Auxiliary Valves TH\(_7\) and TH\(_8\) in the Convertor Model, Respectively

Transistor i

Trigger Pulse Output to Fault Recording Instrument(s)

Control Voltage of Analogue-type HVDC Control System

Direct Line Voltage of Convertor

Direct Line Voltage of Inverter

Nominal Direct Line Voltage of Convertor

Ideal No-Load Direct Line Voltage of Convertor

Direct Line Voltage of Rectifier

6-pulse Bridge Valves Numbered from 1 to 6 Referring to Firing Sequence (Mercury-arc or Thyristor Valves)

By-pass Valve (Mercury-arc Valve)

Variable Resistor or Potentiometer i

Generalized Memory/Port Write Strobe (Active-Low)

Reactance

Impedance

Zener Diode i

Convertor Firing Delay Angle

Preset Minimum Delay Angle on MDA Control

Firing Delay Angle of Convertor Valve \( V_i \)

Preset Constant Extinction Angle on CEA Control

Extinction Angle of Convertor Valve \( V_i \), i.e. Angle between the End of Commutation (Si), and Respective Commutating-voltage-zero Crossing \( C_{i-1} \)

Minimum Extinction Angle \( \delta \) per Cycle \( j \) prior to Valve \( V_i \) Firing

Preset Optimum Extinction Angle \( \delta \) on MEA Control

Rate of Change of Direct Current \( I_d \)

Current Error Signal, i.e. \( A(I_d - I_{ds}) \)
\( e_a, e_b, e_c \) : Instantaneous AC-System Voltages to Neutral (Phases a, b, and c)

\( e_{ac}, e_{ba}, e_{cb} \) : Commutating AC-System Voltages (Phase a to Phase c, etc.)

\( f \) : Frequency in General or AC-System Frequency

\( f_0 \) : Nominal AC-System Frequency, 50 (or 60) Hz

\( \phi \) : Impedance Angle of an AC-System

\( i_a, i_b, i_c \) : Instantaneous AC-Line Currents (Phases a, b, and c)

\( i_c \) : Commutating Current

\( i_i \) : Instantaneous Current of Valve \( V_i \)

\( j \) : \( j^2 = -1 \)

\( \pi \) : 3.14159 or equivalent to 180 electric degrees

\( r \) : Resistance of Windings

\( t \) : Time

\( u \) : Convertor Overlap Angle

\( v_a, v_b, v_c \) : Commutating Convertor Voltages to Neutral (Phases a, b, and c)

\( v_d \) : Direct Bridge Voltage of Convertor

\( v_i \) : Instantaneous Anode-to-Cathode Voltage of Convertor Valve \( V_i \)

\( v_n \) : Negative Direct Voltage with respect to Convertor Transformer Neutral N

\( v_p \) : Positive Direct Voltage with respect to Convertor Transformer Neutral

\( \omega \) : AC-System Angular Frequency, i.e. \( 2\pi f \)

\( \omega_0 \) : Nominal AC-System Angular Frequency, i.e. \( 2\pi f_0 \)

\( \sqrt{\ } \) : Square Root

\( \int \) : Integration

\( a > b \) : "a" greater than "b"

\( a < b \) : "a" less than "b"

\( \alpha \) : Angle "\( \alpha \)" in electric degrees

\% : per cent

Units and Abbreviations

A : ampere

AC, a.c. : Alternating Current

A/D, D/A : Analogue-to-Digital, Digital-to-Analogue (Conversion)
ASCII : American Standard Code for Information Interchange
ASEA : Allmanna Svenska Electriska Aktiebolaget, Ludvika, Sweden
ASM : Assembly Language
BCD : Binary-Coded Decimal
Byte : Unit of 8 Binary Digits (Bits)
CB : Circuit Breaker
CC : Constant Current of Convertor as CC Control
CEA : Constant Extinction Angle of Convertor as CEA Control
CIGRÉ : International Conference on Large High-Voltage Electrical Systems, Paris, France
CPU : Central Processing Unit
CT : Current Transformer(s)
D.C., d.c. : Direct Current
DCT : Differentiating Current Transformer
DDC : Direct Digital Control
EA : Extinction Angle of Convertor as EA Control
EPROM : Erasable Programmable Read-Only Memory
F : Filter(s)
FS : Fault Simulation
GEC : General Electric Company, Stafford, England
German-Swiss HVDC Group : Group Organized by AEG-Telefunken, Siemens, and Brown, Boveri & Cie., West Germany and Switzerland
H : henry
Hi : Logic State "High"
HP : High-Pass (Filter)
HVDC : High Voltage Direct Current
Hz : hertz
IC : Integrated Circuit
IEEE : Institute of Electrical and Electronic Engineers, New York, U.S.A.
INT : Interrupt or Interrupt Service Routine
Inv : Inverter
I/O, IO : Input/Output
IOC : Inverter Optimum Control
ISC : Inverter Safety Control
K : \(2^{10} = 1024\), Unit of Memory
Lo : Logic State "Low"
LSB : Least Significant Bit or Byte (8 Bits)
<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>MDA</td>
<td>Minimum Delay Angle of Convertor as MDA Control</td>
</tr>
<tr>
<td>MEA</td>
<td>Minimum Extinction Angle of Convertor as MEA Control</td>
</tr>
<tr>
<td>MSB</td>
<td>Most Significant Bit or Byte (8 Bits)</td>
</tr>
<tr>
<td>MW</td>
<td>megawatt (10^6) watt</td>
</tr>
<tr>
<td>N.Z.</td>
<td>New Zealand</td>
</tr>
<tr>
<td>(\Omega)</td>
<td>ohm</td>
</tr>
<tr>
<td>P-A, Pre-Amp</td>
<td>Pre-Amplifier</td>
</tr>
<tr>
<td>PIC</td>
<td>Programmable Interrupt Controller</td>
</tr>
<tr>
<td>PIT</td>
<td>Programmable Interval Timer</td>
</tr>
<tr>
<td>PL/M, PLM</td>
<td>High-Level Programming Language Similar to PL/1 Modified for Intel's Microprocessors</td>
</tr>
<tr>
<td>PPI</td>
<td>Programmable Peripheral Interface</td>
</tr>
<tr>
<td>PT</td>
<td>Potential Transformer(s)</td>
</tr>
<tr>
<td>RAM</td>
<td>Random-Access (Read-Write) Memory</td>
</tr>
<tr>
<td>Rec</td>
<td>Rectifier</td>
</tr>
<tr>
<td>ROM</td>
<td>Read-Only Memory</td>
</tr>
<tr>
<td>SCR</td>
<td>Short Circuit Ratio</td>
</tr>
<tr>
<td>TTL</td>
<td>Transistor-Transistor Logic</td>
</tr>
<tr>
<td>UMIST</td>
<td>University of Manchester Institute of Science and Technology, England</td>
</tr>
<tr>
<td>USART</td>
<td>Universal Synchronous/Asynchronous Receiver/Transmitter</td>
</tr>
<tr>
<td>V</td>
<td>volt</td>
</tr>
<tr>
<td>VDU</td>
<td>Visual Display Unit</td>
</tr>
<tr>
<td>W</td>
<td>watt</td>
</tr>
<tr>
<td>11111111B</td>
<td>8-bit Binary Number, Equivalent to 255</td>
</tr>
<tr>
<td>00H to FFH</td>
<td>8-bit Hexadecimal Numbers, Equivalent to 0 to 255</td>
</tr>
<tr>
<td>cos</td>
<td>cosine</td>
</tr>
<tr>
<td>dB</td>
<td>decibel ((10^{-1}) bel.)</td>
</tr>
<tr>
<td>h</td>
<td>hour</td>
</tr>
<tr>
<td>i</td>
<td>Inverter (Subscript)</td>
</tr>
<tr>
<td>kVA</td>
<td>kilovolt-ampere ((10^3) volt-ampere)</td>
</tr>
<tr>
<td>mm</td>
<td>millimetre ((10^{-3}) metre)</td>
</tr>
<tr>
<td>ms</td>
<td>millisecond</td>
</tr>
<tr>
<td>n</td>
<td>Nominal (Subscript)</td>
</tr>
<tr>
<td>nF</td>
<td>nanofarad ((10^{-9}) farad)</td>
</tr>
<tr>
<td>ns</td>
<td>nanosecond</td>
</tr>
</tbody>
</table>
pF : picofarad \(10^{-12} \text{ farad}\)
r : Rectifier (Subscript)
r.m.s., rms : Root Mean Square
s : second
sin : sine
tan : tangent
\(\mu\)F : microfarad \(10^{-6} \text{ farad}\)
\(\mu\)s : microsecond

**Graphic Symbols**

- Source of Electromotive Force
- Earth
- Three-phase Star (or Wye, Y) Transformer Connection
- Three-phase Delta \(\Delta\) Transformer Connection
- Three-phase Two-winding Convertor Transformer with Tap Changer for 6-pulse Operation
- AC Harmonic Filters Bank(s)
- Convertor Valve in General or Conducting Valve
- Non-Conducting Valve
- Incoming Valve (being fired)
- Outgoing Valve (to be extinguished)
- 6-pulse Graetz Bridge
- Circuit Breaker
Isolator or Disconnector (Switch)
Transistor (NPN)
Diode
Zener Diode
Resistor
Capacitor
Inductor
Direct Voltage Source
Ground Potential
Operational Amplifier (Op.-Amp.)
Positive AND Gate
Positive (Inclusive) OR Gate
Inverter Gate
Integrated Circuit (IC) with Specified Function
1 mm or 2 mm Socket
Fuse
ABSTRACT

Aimed at the eventual implementation of direct digital control and protection in a.c./d.c. power systems, this thesis describes the design of a thyristor converter model and an interrupt-driven multiple microprocessor system capable of simulating various faults encountered in real systems, and of monitoring the normal and abnormal converter operating states in real time.

Recent developments of HVDC converter control and operation are first reviewed, and a fast and reliable method of deriving converter-valve ON/OFF states is practically implemented in the model and assessed for other applications.

A comprehensive set of normal and abnormal converter waveforms is derived and used as a basis for the software-based fault simulation and fault-data acquisition scheme. The proposed scheme takes full advantage of the versatile and cost-effective general-purpose microprocessor to provide sophisticated converter operating-state monitoring, fault data recording and immediate display on the inter-connected VDU terminal.

In conjunction with the fault simulation scheme, the conditions for fast shut-down of the converter upon the occurrence of certain disturbances are investigated.
ACKNOWLEDGEMENTS

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I also acknowledge the value of the many stimulating discussions with and generous assistance from my Power Systems colleagues, in particular M. B. Dewe, C. P. Arnold, C. B. Lake, M. I. Parr, B. J. Harker, K. S. Turner, M. D. Heffernan, and J. C. Graham. My wholehearted gratitude goes to the technical staff who provided the precious skills such as mimic engraving and transformer winding.

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CHAPTER 1

INTRODUCTION

The number and sophistication of a.c./d.c. simulators have increased dramatically in recent years. Their development is costing millions of dollars and their use and maintenance require experienced engineers.\(^{(1-5)}\)

In the author's opinion such expensive facilities do not provide the complete answer to the modelling problem.

The Power Systems group at the University of Canterbury has been investigating the behaviour of a.c./d.c. power systems for the past several years. The main emphasis has been on computer models rather than simulators on the basis that sooner or later computer software will replace the hardware models as it did in the case of the network analyzer in the previous two decades. A large measure of success has already been achieved in this respect.\(^{(6-8)}\)

However, it is recognised that there are certain areas where the use of computer modelling is very limited, e.g. control stability, real-time control and protection, and in such cases there is a need for a restricted purpose scaled-down model. For the specific complementary purposes indicated, i.e. investigations on high voltage direct current (HVDC) control and protection, the model should be flexible to accommodate alternative schemes based on conventional and new ideas as well as permitting their implementation using new technologies such as microprocessors.

Recent developments of HVDC convertor control and operation are briefly reviewed in Chapter 2, and basic considerations are made towards the prospective application of direct digital control and protection.
A scaled-down model is indispensable to demonstrate qualitatively the behaviour of HVDC links. In this respect it is important to provide sufficient monitoring points and switches to show the effect of each plant component. The design of the basic convertor for transmission line models is discussed in Chapter 3.

Considering the high level of information available at the convertor plant, the eventual implementation of direct digital control and protection philosophies such as proposed by Arrillaga and Galanos, \(^{(9-11)}\) is a definite possibility. It is realised that such developments are largely restricted by the unavailability of sufficiently accurate and fast transducers and Chapter 4 concentrates in this area with particular emphasis on the development of valve ON/OFF information.

Chapter 5 deals with fault simulation and data acquisition facilities. A comprehensive fault simulation scheme is needed capable of subjecting the a.c./d.c. system to the various faults encountered in practice with point-on-wave control of the instant of fault application, valves involved and their duration, etc. In order to provide exact diagnosis of convertor behaviour, the model should be provided with a fast data acquisition scheme capable of storing sequential valve ON/OFF information, direct current and voltage, control angles, etc. A versatile graphic display facility is also indispensable to present the recorded data for analysis.

Based on the fault simulation scheme described in Chapter 5, some examples are demonstrated in Chapter 6 to illustrate the potential application of the microprocessor-based system to the detection and protection of HVDC convertor faults.

Finally, general conclusions are given in Chapter 7.
CHAPTER 2

GENERAL REVIEW OF HVDC CONVERTOR CONTROLS AND OPERATIONS

2.1 TRENDS IN HVDC APPLICATIONS

Ever since high voltage direct current (HVDC) transmission of electric power first became a commercial reality with static convertors in 1954, HVDC systems have been progressively applied to various transmission schemes for a variety of reasons — where long transmission distances from generation to load centres exist (e.g. Volgograd-Donbass, U.S.S.R. 1962, and Nelson River, Canada 1975); where asynchronous ties are required or preferred (e.g. Sakuma Frequency Changer, Japan 1965, and Cross-Channel, England-France 1961); where underground or underwater cables of considerable length are necessary (e.g. Kingsnorth, England 1975, and New Zealand 1965, respectively). Over the last two decades, the unique characteristics of HVDC schemes have proved technologically desirable over existing alternatives, and/or economically competitive with conventional extra high voltage a.c. (EHVAC) transmission.

Until the early 1970's all HVDC schemes utilized mercury-arc valves in the a.c./d.c. conversion process. However, following the commercial appearance of silicon-controlled rectifiers (SCR) or thyristors in 1957, an intensive development of the high-voltage and high-current thyristor for HVDC applications took place in the late 1960's. The first commercial application of thyristor valves (Gotland, Sweden 1970) and thyristor convertor stations (Eel River, Canada 1972) were successfully achieved. Technological developments of thyristors and in particular the blocking capabilities against reverse voltage have not only superseded the mercury-arc valves, but also provided higher reliability and wider ranges of voltage and current ratings to HVDC.
designers. The practical voltage and current ratings for a specific
HVDC power scheme can only be determined by an optimal study involving
the convertors and other related technology, e.g. convertor transformers,
transmission cables, etc.

In the last decade bipolar HVDC schemes with power capacities
between 1,000 MW and 2,000 MW have been constructed, and the bipolar
power capability of 2,500 to 4,000 MW (±600 kV, and 2,100 to 3,300 A) is
currently available with thyristor valves.\(^{(16)}\) In addition to the
upgrading of thyristor valves and hence the practical power ratings of
HVDC schemes, the size and relative cost of convertor stations have
dropped in general, due to innovations in design concepts.\(^{(17,18)}\)

The reliable operation of HVDC convertors is of prime importance
under various a.c./d.c.-system conditions, especially as the amount of
electric power transmitted by HVDC is becoming relatively larger and the
a.c. systems becoming "weaker". Various disturbances in the a.c./d.c.
 system can lead to maloperation of HVDC convertors, e.g. commutation
failures of the inverter.

Due to the interaction which exists between HVDC control and
protection, fast diagnosis of HVDC convertor disturbances is of great
importance for rapid adjustment of control, and correct measure of
overall protection.\(^{(11)}\) The growing acceptability of HVDC transmission
has been enhanced by its ability to increase system reliability,\(^{(19)}\) to
improve a.c. system stability\(^{(20)}\) and/or damp oscillations\(^{(21)}\) by rapid
control of active power flow. Such applications demand a high level of
sophistication in HVDC control and protection system.
2.2 BASIC CONVERTOR-STATION CONFIGURATIONS

2.2.1 Introduction

The three phase convertor which has found universal acceptance in HVDC schemes is the 6-pulse Graetz bridge and early schemes permitted individual bridge operation during a period of emergency transmission at half a rated power, where two 6-pulse bridges are normally connected in series on the d.c. side to provide 12-pulse operation (double-series 6-pulse convertors to be described in Section 2.2.2.2). In recent HVDC schemes with thyristor valves, two 6-pulse bridges form a 12-pulse convertor unit which simplifies a.c./d.c. main circuits and eliminates the requirement of 5th and 7th harmonic filters on the a.c. side of the convertor.

The operation of these convertors and two-terminal systems is well documented in literature by Adamson and Hingorani 1960, Cory ed. 1965, Kimbark 1971, and Uhlmann 1975. A concise report about the present state of the art in the control of two-terminal HVDC systems is presented by CIGRÉ's Study Committee No. 14 (DC Links) 1978. The performance of existing HVDC schemes are regularly surveyed, and these demonstrate the present level of technical achievements associated with the use of the HVDC attributes to meet the particular system requirements.
2.2.2 Convertor-Station Configurations

2.2.2.1 Single 6-pulse Convertor. Fig. 2.1 schematically illustrates a typical 6-pulse convertor which consists of a 6-pulse bridge, a d.c. smoothing reactor, a three-phase two-winding convertor transformer, an a.c. circuit breaker, and a.c. harmonic filters as the main components. In order to provide safe maintenance work a.c./d.c. isolating switches are used to disconnect the valve group, as shown in Fig. 2.1a. Various earthing switches (not shown in Fig. 2.1) are also provided to ground these main components.

In most HVDC schemes commissioned before early 1970's mercury-arc valves are used. These are prone to stochastic arcbacks (i.e. abnormal reverse conduction of a valve) due to rise of direct current or valve temperature, and/or overvoltages. In order primarily to protect the main valves from the overcurrent caused by the arcback in the rectifier, a seventh valve or by-pass valve $V_7$ is provided as shown in Fig. 2.1a, which takes over the bridge current when the main valves are blocked. In association with the by-pass valve is the by-pass switch. This is closed when longer or permanent bridge-blocking is required, or it is opened when the convertor bridge takes over the direct current via the by-pass valve.

With automatic selection of the by-pass pair formed by the main valves $V_1-V_4'$, $V_3-V_6'$, or $V_5-V_2'$, however, it has been proposed that the by-pass valve can be eliminated under normal and abnormal convertor conditions. Because thyristor valves do not have the arcback phenomenon, the by-pass valve is not required in recent HVDC convertors, where thyristor valves are installed. In such cases, one of the three by-pass pairs is automatically selected for blocking/deblocking the bridge.

The d.c. smoothing reactor $L_d$, usually having a large inductance of 0.4 to 1.5 H, is connected in series with each pole of the d.c.
Convertor Busbars

6-pulse Bridge

AC Isolating Switches

DC Isolating Switches

(a)

By-pass Switch

RYB

5th, 7th, 11th, 13th Harmonic and High-pass (HP) Filters per Phase

(b)

Fig. 2.1 Single 6-pulse Convertor:
(a) Main AC/DC Circuit,
(b) Simplified Single-line AC/DC Circuit.
Its main purposes are to ensure a continuity of the direct current with reduced current ripples, and to limit the rate of increase of direct current during commutation in one bridge when the direct voltage of another inverter bridge collapses due to commutation failures. The crest current in the rectifier due to a short circuit on the d.c. line is also limited by the reactor.

As shown in Fig. 2.1 a circuit breaker is required for clearing faults in the transformer or flashover faults in the bridge, or for taking the whole d.c. link out of service.

2.2.2.2 Double-Series 6-pulse Convertors. Most of HVDC convertors normally perform 12-pulse operation. A simple configuration which realizes such 12-pulse operation consists of two single 6-pulse convertors connected in series on the d.c. side, but in parallel on the a.c. side of the convertor transformers, as illustrated in Fig. 2.2.

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**Fig. 2.2** Double-Series 6-pulse Convertors: 12-pulse Convertor which can be Developed at Stages.
During a testing period before commercial commissioning, with a minor modification of switching arrangement on the d.c. side, back-to-back connected convertors are formed by the 6-pulse convertors, viz., one convertor rectifies the alternating power and the other inverts the rectified direct power back to the same a.c. system and the direct current flows through the smoothing reactor $L_d$. This is one of the standard testing configurations of HVDC convertors before the d.c. lines and other convertor stations are involved for further tests.

2.2.2.3 Unit 12-pulse Convertor. The unit concept of 12-pulse operation, as illustrated in Fig. 2.3, is becoming standard for large HVDC applications. In this configuration the convertor station is greatly simplified by the absence of by-pass and d.c. isolating switches which are required for 6-pulse operation. The a.c. circuit breaker is common to the two bridges and the 5th and 7th harmonic filters are eliminated.

![Diagram of 12-pulse Convertor](image)

Fig. 2.3 Unit 12-pulse Convertor:
12-pulse Convertor which is Regarded as a Unit.
Referring to Fig. 2.3, the d.c. smoothing reactor $L_d$ is transferred to the ground side of bridge 2, so that overcurrents of conducting valves due to ground (flashover) faults in the bridges or at the d.c. terminals can be reduced.\(^{(48,57)}\) This arrangement also allows the insulation requirement on the reactor to be reduced, however, an additional small d.c. blocking reactor $L_b$ is still required to protect the valves from steep overvoltages which are caused by travelling waves from the d.c. line and switching operations in the d.c. switchyard. The inductance of $L_b$ is normally about 5 to 10 mH\(^{(48)}\) and practically, an air-cored reactor may be installed near the d.c.-line terminal of bridge 1 as shown in Fig. 2.3.\(^{(57)}\) A similar arrangement of the reactors is also applicable to the previous configuration shown in Fig. 2.2, but a blocking reactor $L_b$ must be provided for each valve group.

2.2.2.4 Multibridge Convertors. From an HVDC system-designer's point of view, the use of single 12-pulse convertor per pole (Figs. 2.2 and 2.3) for the required full transmission capacity is the easiest solution since the switchyards, on both the a.c. and d.c. sides, will be therefore greatly simplified. Thyristor convertors with 12-pulse ratings of 480 MW (Cabora Bassa-Apollo, South Africa 1977), 560 MW (Inga-Shaba, Zaire 1977) and 500 MW (Nelson River Bipole-two, Canada 1978) are already operating and there is a demand for ratings of 1000 MW to 1500 MW per 12-pulse convertor.\(^{(16)}\) However, as convertor ratings increase, transportation limitations for convertor transformers, i.e. their weight and size, will often determine convertor station configurations. One method to cope with the transportation limitations may be to install three single-phase three-winding transformers or even six single-phase two-winding transformers instead of the two three-phase two-winding transformers of Figs. 2.2 and 2.3.\(^{(16)}\)

In practice, considerations on higher availability of transmitted power have led to a choice of two 12-pulse convertors connected in either
series or parallel on the d.c. side at reduced ratings per 12-pulse convertor, as illustrated in Fig. 2.4. These configurations also enable staged developments of HVDC schemes which are sometimes desirable, for example, when large-scale hydroelectric generators are continually developed over years. Referring to Fig. 2.4a, double-series unit 12-pulse convertors can be developed in stages such as the Nelson River Bipole-two scheme except with conventional installation of smoothing reactors on the d.c.-line side.\(^{(58)}\) In this case conventional control operation is applicable. Double-series 6-pulse convertors (Fig. 2.2) can be also developed in stages to form multibridge configurations (quadruple-series 6-pulse convertors), e.g. Cabora Bassa-Apollo scheme.\(^{(3)}\)

For mercury-arc valves where the practical maximum voltage ratings are 133 kV to 150 kV,\(^{(59)}\) triple-series 6-pulse convertors per pole are not uncommon. High transmission voltages of ±400 kV for the Pacific Intertie, U.S.A. 1970, and ±450 kV for the Nelson River Bipole-one, Canada 1972, can thus be achieved.

The relative merits of the series and parallel configurations of unit 12-pulse convertors depend on the particular HVDC application.\(^{(5)}\) In the parallel configuration of Fig. 2.4b, the smoothing reactor is required for each 12-pulse convertor and a current-balancing control is necessary for both rectifiers and inverters mutually connected in parallel.\(^{(5)}\) When HVDC schemes are developed in several stages over years and long overhead transmission lines are only used in rural areas where both convertor stations are normally provided with earth as shown in Fig. 2.4b and electrolytic corrosion of buried or immersed metallic structures due to ground currents can be made negligible,\(^{(47)}\) the parallel configuration provides less line losses during the period when full line currents are not established, e.g. Inga-Shaba scheme in Zaire.\(^{(5)}\) In this scheme, ohmic (resistive) line losses have been found more significant than corona line losses at the full line voltages ultimately
Fig. 2.4 Double Unit 12-pulse Convertors:
(a) Double-Series Unit 12-pulse Convertors,
(b) Double-Parallel Unit 12-pulse Convertors.
scheduled.

Following permanent d.c. line faults, bipolar overhead line schemes can be so arranged that two d.c.-line terminals (station poles) are automatically paralleled to operate in monopolar mode, where the unfaulty line is provided with ground return, e.g. Cabora Bassa-Apollo\(^{(3)}\) and Nelson River\(^{(58)}\) schemes. In this case the requirements for parallel operation\(^{(5)}\) should be fulfilled during the temporary period. The transmission line should be also able to carry the excess direct current for a desired time. (When the current is doubled, the ohmic line loss becomes four times bigger.)

2.2.2.5 Some Design Aspects to Unit 12-pole Convertor. In spite of the economic considerations made for higher direct voltage and current ratings\(^{(16,19,48)}\) and the higher availability of transmitted power, the limitations of present HVDC technology such as d.c. cables ratings up to 500 kV \((1,000 \text{ A})\) or 600 kV \((850 \text{ A})\)\(^{(60-65)}\) and environmental impacts\(^{(17-19,66)}\) may also introduce some restrictions on convertor-station configurations. For instance, a proposed new 2,000 MW Cross-Channel HVDC Link (England-France, December 1984 for commissioning) employs two links of the bipolar unit 12-pulse convertors which are similar to Fig. 2.3 except with conventional installation of smoothing reactors on the d.c.-line side, rather than the multibridge configuration described in Section 2.2.2.4. Eight d.c. cables rated at 270 kV and 2,000 A will be buried in four trenches dug into the sea bed, since experience with the existing 160 MW link is that the principal cause of faults has been due to damage to the submarine cables caused by fishing trawls and ships' anchors.\(^{(55,66)}\)
According to the unit concept of 12-pulse convertors, fresh consideration has been given to exclusively apply high-pass (damped) a.c. filters for the proposed Cross-Channel HVDC Link. (67) These provide a simpler design and maintenance requirements.

A concise review of the d.c. harmonic filters (damper circuits) provided on various HVDC schemes is given by a CIGRE report. (68) With respect to the unit concept of 12-pulse convertors, smaller smoothing reactors and simpler d.c. filters may be expected in future HVDC schemes.

Back-to-back connected convertors and 12-pulse operation are normally applied to frequency changer, e.g. Shin-Shinano Frequency Changer, Japan 1977, (69) and to asynchronous interties between different power authorities, e.g. the USSR-Finland HVDC Intertie, where three pairs of unit 12-pulse convertors are to be connected back-to-back between the two a.c. systems. (70)

2.3 BASIC CONTROLS

2.3.1 Introduction

The operating characteristics of the control system of HVDC schemes are different for each particular application. However, two basic controls are normally used, i.e. constant direct current and commutation margin or extinction angle control. (22) The extinction angle of the inverter is normally maintained at its lowest practical value so that the requirement of reactive power compensation in the a.c. system can be minimized, whilst the normal commutation process can be maintained on the occurrence of a.c./d.c.-system disturbances.
In order to achieve reliable operation of HVDC convertors, maximum and minimum direct current and voltage limits are normally incorporated with the basic controls, and during the disturbances protection-related firing-angle controls are transiently incorporated for both rectifier and inverter operations of HVDC convertors.

A weak a.c. system with very light damping is a very severe system condition and controllability of the extinction angle of inverter is of prime importance, since inverters are the most susceptible to transient disturbances in the a.c./d.c. system.

There are two different basic methods for the extinction angle control, i.e. predictive firing to achieve the desired extinction angle, and closed-loop control of the extinction angle actually measured. Moreover, the advantage of symmetrical or equidistant firing-angle control techniques over the basic predictive (individual phase) control for HVDC convertors are by now well established. In particular, a considerable reduction of the abnormal harmonic content of the a.c. system (orders other than 5th, 7th, 11th, 13th, etc. for a 6-pulse three-phase convertor) can be obtained, which results in more stable operation.

Sections 2.3.2 and 2.3.3 briefly describe the present state of art of the basic controls and their potential influence to requirements of direct digital control described in Section 2.3.4, and interacting protection.
2.3.2 Individual Phase Control

2.3.2.1 Predictive Control. For basic predictive control the individual firing angles are calculated using the converter commutating voltages and currents up to the instant of firing of each valve. The control is directly phase-locked to the a.c. system voltages in both magnitude and frequency, and under steady state conditions with balanced a.c. sinusoidal voltage-waveforms, the resultant extinction angle is constant for each valve. The relationship governing the commutation process relies on the fact that the time integral of the commutating voltage, i.e. voltage integral, is equal to the overall voltage change produced by the commutating current $i_c$. With reference to Fig. 2.5, the relationship can be expressed as:

$$\int_{\alpha}^{\pi/2} E \sin(\omega t) \, dt = 2(\omega L) \int_0^{I_d} \, di_c,$$

where $\alpha$ is the firing delay angle,
$\delta_c$ is the preset constant extinction angle (CEA),
$E$ is the r.m.s. value of the commutating voltage,
$\omega$ is the a.c. system angular frequency,
$L$ is the leakage inductance per phase of the converter transformer (assumed constant),
$I_d$ is the direct line current.

Thus the equation for the predictive constant extinction angle (CEA) control is:

$$\sqrt{2} E \cos \alpha + \sqrt{2} E \cos \delta_c = 2 \omega L I_d.$$

With respect to the overlap angle $\psi$, which corresponds to the time for the commutating current to transfer from one valve to the next, the equation signifies that the voltage integral shown as the hatched area
Fig. 2.5 Typical 6-pulse Inverter under Predictive Constant Extinction Angle (CEA) Control:

(a) Positive and Negative Direct Voltages with respect to the Transformer Neutral,
(b) Voltage across Valve 1, and Commutating Voltages,
(c) Valve Current \( i_1 \), \( i_3 \), and \( i_5 \),
(d) Valve Current \( i_2 \), \( i_4 \), and \( i_6 \).
in Fig. 2.5 is directly proportional to the direct current $I_d$. In relation to the variables $E$, $\omega$, and $I_d$ in equation 2.2, the firing delay angle $\alpha$ can be computed so that the desired constant extinction angle can be maintained. Since the frequency deviation of an a.c. system is normally small, the commutation reactance $\omega L$ is practically constant. However, equation 2.2 provides the phase-locking characteristic even with a.c.-system frequency variations.

With regard to the direct current $I_d$ rising during the commutation process due to a.c./d.c.-system disturbances, the current at the end of commutation will be larger than that anticipated by the predictive CEA controller. Hence, compensation must be made for the rate of rise of direct current, i.e. $\frac{dI_d}{dt}$, so that the firing occurs at a correspondingly earlier instant. Assuming a steady increase of current during the commutating period, equation 2.2 becomes:

$$\sqrt{2} E \cos \alpha + \sqrt{2} E \cos \delta_c = 2 \omega L (I_d + u \frac{dI_d}{dt}).$$

(2.3)

In practice there is a normal maximum value of $u$ as used in equation 2.3. A transducer for the rate of change of direct current can provide a fast signal in response by measuring the voltage induced across the smoothing reactor or the d.c. transductor coupled with d.c. busbar.

With respect to previous Fig. 2.5, however, it should be noted that the commutating voltage actually governing the extinction angle of outgoing valve is that of the previous valve; e.g. the commutating voltage $e_{ac}$ (RB) is used to compute equation 2.2 for the valve $V_1$, and its extinction angle is determined by the commutating voltage $e_{ab}$ (RY) which is directly related to equation 2.2 for the previous valve $V_6$ and incoming valve $V_3$ as well. (Three commutating voltages are relatively independent, and any disturbance on single phase a.c. voltage influences the phase and magnitude of two of the three commutating voltages, i.e.
four extinction angles in 6-pulse bridge.)

Although the convertor firings are independently computed for the fast response to system change, non-symmetrical firings are caused by unbalanced and distorted a.c. voltages, a common phenomena with weak a.c. systems. This is because the accuracy and predictive ability of the control is closely related to the validity of the assumptions made in the development of the mathematical expression of the commutation process. Moreover, any inaccuracy in the firing instants of the valves generates uncharacteristic harmonic currents in the a.c. system, which can lead to the harmonic waveform-distortion instability of the HVDC system. Any secondary d.c. components of convertor transformer caused by firing-angle unbalance will cause additional zero-sequence primary-current components which contain higher harmonics owing to transformer-saturation effects. Installation of a.c. main harmonic and/or control system filters can reduce this problem, but not remove it.

By measurement of the direct current and the integration (i.e. 90° phase shift) of the appropriate valve-commutating voltages, the correct firing angle for the predictive CEA control can be achieved. From the first commercial application of HVDC transmission, i.e. Gotland scheme in 1954, until early 1970's, all the HVDC schemes commissioned were based on the principle of predictive CEA control.

Chapter 3 describes a practical design of the control which combines the constant current (CC) control and minimum delay angle (MDA) control. For the CC control, a so-called inverse-cosine control is implemented, and a constant delay angle can be set manually.

2.3.2.2 Closed-loop CEA Control. In order to prevent commutation failures in an inverter, an early closed-loop control of extinction angle was based on a direct comparison of the measured extinction angle and a set value. In this reference the measurement of extinction angle is achieved from the negative-going instant of anode-to-cathode
voltage per valve and the respective commutating-voltage-zero crossing. In order to derive the control signal, i.e. extinction-angle error, each extinction angle measured at about 60° intervals is successively converted to a voltage level by an integrator, and its output compared with the direct voltage representative of the CEA setting.

During a transient period of a.c.-system voltage reduction, the detection-correction circuit is assigned to increase the CEA setting so that the probability of commutation failure can be reduced. However, because of the analogue circuitry applied and the smoothing time-constant lags either in the feedback loops or control system filters, the proposed CEA control is unrealistically slow in response, e.g. a new extinction angle can not be achieved until about 0.5 second after the correction of CEA setting.

According to a similar principle, a refined closed-loop CEA control has been independently proposed by the German-Swiss HVDC Group, and its dynamic behaviour has been tested on an HVDC model plant. In this scheme two integrators are separately applied to convert the extinction angles measured on both sides of a 6-pulse bridge, and at about 60° intervals the greater value of either previous or present deviation from the CEA setting is selected and held to obtain the error signal. Triple gains are introduced to scale the angular adjustment, so that the smaller the measured extinction angle is, the larger will be the reduction of firing delay angle. In order also to achieve a faster closed-loop CEA control, a rate of rise of direct current \( \frac{dI_d}{dt} \), is incorporated into the closed-loop. With strong and balanced a.c. systems, the proposed control is fast enough to follow after a gradual increase of direct current which normally occurs after an increment of current setting. Under a severe a.c. single-phase fault, the recovery of the inverter after initial commutation failures is significantly improved over the previously mentioned proposal; however, the loop gain
is still limited by smoothing time-constant lags.

Since then the same German-Swiss HVDC Group has proposed a closed-loop extinction-angle-pair control.\(^{(32,33)}\) In this proposal, three relatively independent extinction-angle-pairs (i.e. \(\delta_1\) and \(\delta_4\), \(\delta_2\) and \(\delta_6, \delta_5\) and \(\delta_2\)) are separately controlled. (Three control loops refer to the common CEA setting.) This modified closed-loop CEA control can in the steady state provide better characteristic of harmonic stability over the previous closed-loop CEA control; however, during and after a.c.-system disturbances, considerable amounts of normal and abnormal harmonic-current contents in the a.c. system are observed. This is because d.c. components superimposed on the a.c. voltage cause asymmetry of the positive and negative half-cycles of the a.c.-system voltages which are in the steady state assumed nearly symmetrical. With increased reduction of single-phase a.c.-system voltage, considerable magnitudes of 3rd and 9th harmonic currents are observed in the a.c. system, which is highly undesirable especially when the a.c. system has a resonant frequency close to these harmonic frequencies, e.g. Cross-Channel and New Zealand HVDC schemes.\(^{(12,23)}\)

Although the direct measurement of extinction angle and its implementation to the control loop is technically valid, the closed-loop CEA control alone will be only applicable to relatively strong a.c. systems. This is primarily due to the nature of individual or asymmetrical phase control as mentioned in Section 2.3.2.1.

However, for the sake of minimum reactive power consumption in the a.c. system in the steady states,\(^{(6,34)}\) a closed-loop CEA control should not be overlooked, since an individual discrimination and phase correction of corresponding extinction angle can be achieved by digital processors with extensive memory capabilities and desired accuracy of firing angle. Thus, depending on the strength and resonant conditions of a.c. systems, the control mode may be selected, i.e. adaptive control,
without altering the hardware devised. In this case the digital closed-loop CEA control mode may have to contain a detective-corrective iterative process per extinction angle, such as the one to be described in Section 2.3.4.3. Moreover, a predictive adjustment of firing delay angle should be also incorporated, so that commutation failures in an inverter may be prevented or at least the recovery made as quickly as possible.

2.3.3. Equidistant Control

2.3.3.1. Ainsworth's Phase-locked Oscillator Control System.

Equidistant control features equally spaced firing pulses in steady state, i.e., each valve receives a firing pulse $60^\circ$ after the previous firing. The first practical application to the Kingsnorth and Nelson River Bipole-one HVDC schemes (GEC, England 1975) utilized a voltage controlled oscillator (VCO) and a ring counter as the main components for equidistant control.\(^{(35)}\) Fig. 2.6 shows the principle of Ainsworth's phase-locked oscillator control system which implements constant current (CC) and minimum extinction angle (MEA) controls.

The output of the oscillator is a train of short pulses at a pulse repetition frequency $f_1$, such that $f_1 = k V_c$, where $k$ is the oscillator constant and $V_c$ is the oscillator control voltage. The 6-stage ring counter changes by one step per input pulse, each transition sequentially producing the firing pulse to a valve gate or grid. In the steady state condition, $V_c$ is such that $f_1 = 6f$, where $f$ is the a.c.-system frequency. Thus each valve receives a firing pulse $60^\circ$ after the previous firing. In practice the independent oscillator described would drift in frequency and phase relative to the a.c. system. Hence, the control voltage $V_c$ is derived from a negative feedback control loop for the control of the convertor parameters, e.g. direct current and extinction angle, so that the oscillator is phase-
Fig. 2.6 Principle of Ainsworth's Phase-locked Oscillator Control System:

Equidistant Firing Angle Control System Implementing Minimum Extinction Angle (MEA) and Constant Current (CC) Controls.
locked to the a.c.-system voltages.

For the closed-loop CC control, as shown in Fig. 2.6, \( V_{c2} \) is assumed to be zero and therefore \( V_c = V_{cl} \). Voltage \( V_{cl'} \), produced by the control amplifier, is the amplified difference between the current setting \( I_d \) and the measured direct current \( I_d \), i.e. current error. In the steady state condition the oscillator will adjust its output frequency to \( 6f \), and its phase, which corresponds to the firing delay angle, retains its value so that the direct current will be very nearly equal to the current setting. It must, however, always be in error so that following a change of direct current due to a change of d.c. load resistance (i.e. the required new value of firing delay angle has been reached), the control voltage \( V_c \) can remain at \( V_{cl} \) to maintain the oscillator frequency at \( 6f \). The error is therefore a function of the control amplifier gain and a.c.-system frequency, i.e., the whole control system can follow moderately wide, but slow a.c.-system frequency-variations.

For the closed-loop MEA control of an inverter, as shown in Fig. 2.6, \( V_{cl} \) is blocked by the diode (i.e. \( V_{cl} \) is zero) and therefore \( V_c = V_{c2} \). Voltage \( V_{c2} \), produced by the "extinction-angle measuring-circuit" per valve, where each value of extinction angle is measured in period and then it is converted to a voltage ramp by an integrator, is sampled at the respective commutating-voltage-zero crossing. Its output direct-voltage \( EA_1 \) is in this case inversely proportional to the time duration of extinction angle. Thus only the most negative voltage is passed to produce \( V_{c2} \) because of the six diodes, corresponding to the smallest value of extinction angles per previous cycle. At full inversion in the steady state condition, voltage \( V_{c2} \) controls the oscillator frequency holding the smallest value of extinction angle at the set minimum value. In practice one particular extinction angle is normally involved in the MEA control per cycle. (The values of six
extinction angles will only be equal if the a.c.-system voltages are perfectly symmetrical.)

In addition to the basic MEA control mentioned above, in transient conditions when extinction angles become smaller than the set minimum value, an additional finite impulse (not shown in Fig. 2.6) is delivered to the oscillator which jumps back suddenly in phase (i.e. firing delay angle) by an integral-proportional amount for about $60^\circ$ in duration so that the following commutation process of inverter can be safely maintained. A fast response of the extinction-angle control can therefore reinforce the recovery of inverter after initial commutation failure. In this scheme a new value of minimum extinction angle can be set within about a cycle of a.c.-system frequency.

However, it can be concluded that, whereas predictive extinction-angle controls may take action to prevent commutation failures, this type of iterative closed-loop MEA control can only detect the condition after it has occurred.

2.3.3.2 ASEA's Refined HVDC Control System. Based on a very similar principle to that described in the previous section, ASEA introduced a refined equidistant control system which implements an additional control parameter into CC control loop and utilizes a predictive MEA control in an inverter by approximation and correction of a commutating-voltage integral. The refinement is directed toward HVDC applications on weak a.c. systems or on generator stations with large frequency variations. For these system conditions a minimization of the probability of commutation failures is considered for the inverter control.

For the closed-loop CC control a bias voltage proportional to one sixth of the period of the a.c.-system frequency $\left(\frac{T}{6}\right)$ has been superimposed on the current error signal $V_{cl}$ in Fig. 2.6), which may provide a fast phase-locking characteristic to large a.c.-system
frequency-variations. Moreover, a linearization of the dynamic response over the whole CC control mode is approximately obtained by dividing the control voltage $V_c$ by the respective commutating voltage. However, in transient conditions with a non-zero a.c.-system impedance, and with the rectifier operating into a non-resistance load, the linearization will not be possible due to the changing a.c. busbar voltages \(^{(37,38)}\).

A predictive element is incorporated in the equidistant control system of MEA control. The operation of this circuit is based on the triangular approximation of the remaining voltage integral after commutation, e.g., a predictor calculates the hatched area shown in Fig. 2.7, which will be available at the end of commutation ($S_6$), and is used to determine firing instant $P_3$ for valve $V_3$. In order to compute the approximated voltage integral the predicted time $t^*$ remaining to the next commutating-voltage-zero crossing $C_6$ is calculated, which is represented as the voltage difference between the output voltage $\frac{T}{2}$ from the half-a-period measuring circuit and the saw-toothed voltage at the instant of the end of commutation $S_6$, as illustrated in Fig. 2.8. The saw-toothed voltage is derived from a constant-slope ramp-function generator which starts at the previous commutating-voltage-zero crossing $C_3$. In order to improve the operation on weak a.c. systems a feedback loop is introduced to update the prediction model, i.e., the predicted time is compared with the actual time measured, and is then used to correct the predictor one cycle later.

This however gives individual phase control (i.e., predictive CEA control) rather than equidistant firing. At this point a firing-angle selector which implements equidistant firing is introduced. Namely, when one valve fires on the minimum extinction-angle condition, the following five valves are fired at regular 60° intervals. Thus, when the a.c.-system voltages are not balanced, only the most critical (i.e. smallest) value of extinction angle is selected and controlled.
Fig. 2.7 Typical 6-pulse Inverter under Equidistant Firing Angle Control with Predictive Triangular Approximation of a Commutating-Voltage Integral:

(a) Positive and Negative Direct Voltages with respect to the Transformer Neutral,
(b) Voltage across Valve 1, and Commutating Voltages,
(c) Valve Current $i_1$, $i_3$, and $i_5$,
(d) Valve Current $i_2$, $i_4$, and $i_6$. 
Fig. 2.8 Derivation of Predicted Remaining Time $t^*$ — ASEA's Predictive Triangular Approximation Method of a Commutating-Voltage Integral:

(a) Positive and Negative Direct Voltages with respect to the Transformer Neutral,
(b) Voltage across Valve 1, Commutating Voltages, and Saw-toothed Voltage for the Prediction,
(c),(d) Valve Currents $i_1$ to $i_6$. 
However, because of the approximations involved in the predictor, the predictive MEA control alone will not be a sufficient safeguard against initial and/or successive commutation failures following a sudden reduction of the inverter alternating voltages and increase of the direct current. (Note that a variation of direct current has a minor influence to the deionization time of mercury-arc and thyristor valves.) In other words extinction-angle control can only be maintained by the negative feedback loop.\(^{(35,38)}\) With the advent of microprocessors, however, a new approach to a commutating-voltage integral for firing prediction may theoretically reduce the probability of initial inverter commutation-failures, and provide a fast recovery after such initial commutation-failures, if any. It may also provide a predictive angular-scaling technique for closed-loop MEA or CEA control. The proposed technique is discussed in Section 6.2.

2.3.3.3 Modified HVDC Control Systems. Both references 35 and 36 agree in that the phase-locked oscillator control system provides sufficient harmonic-waveform stability when controlling HVDC links. However, these pulse-frequency control systems\(^{(32)}\) have common drawbacks as follows:

- A voltage controlled oscillator (VCO) has an inherent integral characteristic, i.e., with a constant value of control voltage \(V_c\), the firing instant shifts with constant rate of change in relation to the commutating-voltage-zero crossings.
- Without auxiliary devices, it is not possible to set a constant firing delay angle \(\alpha\).
- Linearizing the CC control characteristic, i.e. a rate of change of direct voltage \(V_d\) directly proportional to the control voltage \(V_c\), is not possible to achieve by simple means, if this is desired.
With respect to these drawbacks, a modified analogue-based pulse-phase control system is proposed by the German-Swiss HVDC Group.\(^{(32,33)}\) The system employs a voltage controlled constant current source which charges a capacitor in proportion to a control parameter derived from an auxiliary control loop. The auxiliary loop provides information of the mean deviation of firing delay angle and a.c.-system frequency measured, thus the synchronism with the a.c.-system voltages is assured. A voltage comparator generates firing pulses at an appropriate level of control voltage \(V_c\) which is representative of either direct current \(I_d\), minimum extinction angle (MEA), or constant firing delay angle \(\alpha\) externally set, so that a change in the control voltage \(V_c\) causes a proportional change in the firing delay angle \(\alpha\), i.e. firing-phase modification which follows the error of the control parameter. (For this reason the term "pulse-phase control" is used.) In the steady state a ring counter distributes equidistant firing pulses to corresponding convertor valves.

For the closed-loop CC control, the dynamic response is linearized by calculating the inverse cosine value of the current error. By taking the smallest firing delay angle, therefore, a transfer of control modes between CC and MEA can be achieved by an analogue selector.

For the closed-loop MEA control, triple gains are applied for scaling the angular adjustment. In order to prevent commutation failures, rate of rise of direct current \(\frac{dI_d}{dt}\) and rate of decrease of commutation voltages are incorporated. For the latter the rectified three-phase a.c. voltages are used, and half-a-cycle change of the rate is sampled at about 60° intervals to evaluate a magnitude of disturbances, so that the following delay angle can be advanced. Moreover, during severe a.c./d.c.-system disturbances, the inverter can be driven at the minimum firing delay angle of about 110° to 120°. (Rectifier operation of inverter is normally prevented.) After the disturbance is
cleared, the firing delay angle retards very slowly to its nominal MEA.

Based on the functional requirements of equidistant CC and MEA controls, (35) an analogue and hardwired-logic based convertor control has been proposed. (39,40) In this later proposal, a phase-locked frequency multiplier is used to provide reference (clock) pulses directly from the a.c. system, and closed-loop control of parameters is based on the modification of the counting of the reference pulses. The proposal has a common feature with the pulse-phase control described above. (32)

Recently, a microprocessor-based scheme has been developed, (41) which is exactly based on the proposal. (39,40)

In view of the previous applications of the voltage controlled oscillator to equidistant HVDC control, an analogue circuitry of modified pulse-timing oscillator has been proposed in principle. (42) Although the practicability of this proposal is doubtful, the provision of separate control of phase and frequency with respect to a.c.-system voltages is valid in concept, especially with regard to the advantages of pulse-phase control described above and an eventual application of direct digital control (DDC) to new HVDC schemes.

2.3.4 Direct Digital Control

2.3.4.1 Introduction. The speed and accuracy of existing control and protection schemes which use analogue techniques does not utilize the inherent advantages of HVDC links sufficiently, viz., convertor operation which is based on discrete gate (or grid) control pulses can theoretically achieve instantaneous control by using direct digital control including fast protective action. (7,43) Based on the development of equidistant firing control in HVDC transmission, (35,36) more recently, proposals have been made to implement the equidistant control by digital techniques, (9,10,38,44) where independent feedback loops of digital information provide the theoretical basis of each loop as well as its
performance and relation to the other loops.

A valve is switched to the conducting state "ON" when there is adequate anode-to-cathode voltage and a firing pulse has been applied to the grid (or gate). The next valve $V_i$ to fire is then set by a ring counter (or equivalent software) sequence and its firing instant $P_i$ is directly related to the firing instant $(P_{i-1})$ of the previous valve $V_{i-1}$ by the following cyclic equation:

$$P_i = P_{i-1} + 60^\circ + \Delta P_i,$$

(2.4)

where $i$ changes in a cyclic manner (1 to 6), and $\Delta P_i$ is the angle-termed firing correction produced by the controllers, which in the steady state will be zero, i.e. equidistant control. This correction (referred to as the relative "phase of firing") is proportional to the deviation of the control parameter (e.g. direct current, extinction angle) from its nominal value, dependent on the particular controller. The periodic time reference (clock pulse) is derived from the a.c.-system voltages by the phase-locked frequency multiplier (pulse generator) which provides a synchronized multiple of the a.c.-system frequency.

2.3.4.2 Digital CC Control. For rectifier operation in the CC control mode, the following equation is applied:

$$\Delta P_i = K1 (I_d - I_{ds}) + K2 \frac{dI_d}{dt},$$

(2.5)

where $K1$ and $K2$ are correction factors for the current error and rate of change of current, respectively. CC setting $I_{ds}$ normally differs according to either rectifier or inverter operation; current control at the inverter normally has the setting less than that at the rectifier by some 10 to 15%. The difference $\Delta I_{ds}$ is referred to as the "current margin".

Under steady state conditions the convertor valves are fired at regular intervals of $60^\circ$, and in general, firing according to equation
2.4 will result in six different firing angles \(\alpha_i\) per cycle. Upon disturbances, a common variation of the firing angles is generated, which is proportional to the variation of direct current. In order to accelerate CC convergence to the new steady state, rate of change of direct current \(\frac{dI}{dt}\) is incorporated as expressed in equation 2.5, although it can introduce transient variations of firing angles. In order to optimize the CC convergence (stability), a relatively long time constant of the control loop should be considered for a particular HVDC scheme, where the time constant is mainly determined by such factors as inductance of the d.c. smoothing reactors, resistance of the HVDC transmission lines, and strength of the a.c. systems.

2.3.4.3 Digital MEA Control. For inverter operation in the MEA control mode, two mutually exclusive closed-loop controls, i.e. inverter safety control (ISC) and inverter optimum control (IOC), are introduced. Unlike conventional analogue methods, this control mode is performed by a detective-corrective iterative process. The realization of the digital MEA control mode has similar features with the Ainsworth's phase-locked oscillator control system, however, the one-way correction by ISC followed by one-way iterative optimization of MEA by IOC, provide unique characteristics which are better suited to direct digital implementation.

ISC is performed immediately after the previous valve \(V_{i-1}\) is detected to have an extinction angle \(\delta_{i-1}\) less than the preset optimum extinction angle \(\delta_o\) (MEA setting, typically 15° to 18°), by the following action:

\[
\Delta P_i = K3 (\delta_i - \delta_{i-1}) < 0, \text{ only if } \delta_{i-1} < \delta_o',
\]

where the extinction angle \(\delta_i\) of valve \(V_i\) is defined as the period \((S_i - C_{i-1})\) and \(S_i\) is the instant of end of conduction of valve \(V_i\) and \(C_{i-1}\) is the respective commutating-voltage-zero crossing. This provides an emergency-type of delay-angle reduction under minor disturbances in
a.c./d.c. systems, and also prevents excessive encroachment on a correction of extinction angle. Note that in this case inverter safety constant K3 (dimensionless) may be equal to or greater than unity to ensure safe operation. (As the a.c. system becomes weaker, however, the constant K3 has to be reduced.\(^{44}\)) The control action of ISC for safe operation can take place at every firing, i.e. six times per cycle. After the condition \(\delta_i > \delta_o\) has been established, the ISC remains passive to the following new conditions (e.g. \(\delta_{i+1} > \delta_o\), etc.), therefore the optimization of the extinction angle is a function of the IOC, as described below.

In order to maintain or restore the steady-state operation of the inverter MEA control mode, prior to a valve \(V_i\) firing about a cycle after the latest ISC action in the cycle \(j\), the IOC compares the smallest of the six most recent extinction angles \((\delta_{\min}^{j+1})\) in the previous cycle \(j+1\) with preset \(\delta_o\), and applies a common correction \(\Delta P_i\) for the following cycle \(j+2\) according to:

\[
(\Delta P_i)_{j+2} = K4(\delta_{\min}^{j+1} - \delta_o) > 0, \text{ only if } (\delta_{\min}^{j+1}) > \delta_o, \quad (2.7)
\]

where inverter optimization constant K4 (dimensionless) must be less than unity since overlap angle \(\theta\) will increase with retardation of \(P_i\). The IOC is only activated when the safety of the inverter has been established during the previous cycle, i.e. within the MEA control mode, the IOC has second priority with respect to the ISC. (The control action of IOC for optimum operation can take place only once every cycle.) In this scheme \(^{9}\) the optimization cycle IOC is initiated at the particular commutating-voltage-zero crossing \(C_i\) after the latest ISC action which occurred between one and two cycles previously, therefore asymmetry normally occurs in \(360^\circ\) intervals until the optimization process completed (Fig. 7 in reference 9).
2.3.4.4 Ceiling Limits. Normally either the minimum delay angle per cycle is under CC control or extinction angle per cycle is under MEA control. The tendency of the current to reduce can only be compensated up to a limit when $\alpha = 0^\circ$. However, when a valve consists of multiple serial and possibly parallel units, this is limited to a larger value (e.g. $5^\circ$ to $7^\circ$) to ensure correct valve turn-on and equal current sharing between the multiple parallel units. Therefore, in this scheme, the minimum delay angle per cycle is the ceiling limit permissible for the firing delay angle for the rectifier. (This requires measurement of the delay angle $\alpha_{\text{f}}$.) Moreover, a valve is triggered prematurely if maximum delay angle per cycle reaches the maximum limit permissible (e.g. $120^\circ$ to $135^\circ$) for the firing angle for the rectifier, to avoid commutation failures during severe transients. An example of this is when the rectifier is suddenly driven into inversion to reduce d.c. overcurrents as a result of a d.c. line fault. Under this circumstance the whole pulse train is advanced by the same amount.

Similarly a ceiling limit is imposed on the inverter controls to prevent the inverter operating in the rectifier region. Thus, a valve is normally triggered prematurely if minimum delay angle per cycle reaches the minimum limit (e.g. $100^\circ$ to $120^\circ$). Since the MEA control provides a maximum limit of firing delay angle for the inverter controls, there is no need for this.

Unlike most of analogue techniques implementing equidistant control, in the steady state, constant or even individual delay angle can be set without replacing major control loops by special devices.

2.3.4.5 Minicomputer Application. A comprehensive minicomputer (single processor) application to the digital convertor control described in previous Sections 2.3.4.1 to 2.3.4.4 has been recently reported. This minicomputer application involving software includes a method for the measurement of the a.c. period and also a dual-gain CC control.
implemented for inverter operation over $120^\circ$ of firing delay angle before the closed-loop MEA control mode. In order to prevent commutation failures at the inverter, the values of direct current and appropriate commutating-voltage are both sampled at regular $10^\circ$ intervals and used to temporarily reduce the firing delay angle in case of a.c./d.c. disturbances.

2.4 CONVERTOR-STATION OPERATIONS

Operation of convertor stations generally differs from scheme to scheme according to specific requirements, however, the basic controls and ceiling limits are as described in Section 2.3.

2.4.1 Two-Terminal Systems

A basic monopolar HVDC transmission system (link) is illustrated in Fig. 2.9a. Although bipolar schemes are widely used in practice, each pole is normally controlled as an independent unit. The direction of power transmission can be altered by simultaneously reversing the voltage polarities of the convertors at both ends of the transmission lines. The direct voltage of the rectifier ($V_{dr}$) is always greater in absolute value than that of the inverter ($V_{di}$), because of the ohmic (resistive) line losses and specified control characteristics as described below.

In relation to the basic controls, theoretical convertor control characteristics of the direct voltage $V_d$ versus direct current $I_d$ are shown in Fig. 2.9b. Assuming balanced a.c. sinusoidal voltage-waveforms on the a.c. side and infinite inductance $L_d$ on the d.c. side, a number of basic convertor equations can be derived from convertor principles,\(^{(22,46,47)}\) to interrelate convertor variables and constants,
Fig. 2.9 Principal HVDC Transmission System and its Basic Control Characteristics:

(a) Two-Terminal HVDC System with Voltage Polarities Shown,
(b) Theoretical Convertor Control Characteristics of Direct Voltage $V_d$ versus Direct Current $I_d$. 

Formulas:

- MDA Control: $V_d = V_{do} \cos a_c - \frac{3wL}{\pi} I_d$
- CC Control: $V_d = V_{do} \cos a - \frac{3wL}{\pi} I_d$
- EA Control: $V_d = -V_{do} \cos \delta + \frac{3wL}{\pi} I_d$
and control parameters. For rectifier operation in the minimum delay angle (MDA) control mode A-B-J in Fig. 2.9b, i.e. $\alpha = \alpha_c$, the following equation is given:

$$V_d = V_{do} \cos \alpha - \frac{3wL}{\pi} I_d,$$

(2.8)

where

$$V_{do} = \frac{3\sqrt{2}}{\pi} E,$$

(2.9)

which is the ideal no-load direct voltage of the converter when $\alpha = 0$.

(If $\alpha_c = 0$ in equation 2.8, the MDA control mode is then referred to as the "natural voltage" characteristic.)

The second term of the right-hand side of equation 2.8, $-\frac{3wL}{\pi} I_d$, corresponds to the voltage reduction due to the current commutation which takes place at $60^\circ$ intervals.

Similarly the following equation is applied to the constant current (CC) control mode B-E in Fig. 2.9b:

$$V_d = V_{do} \cos \alpha - \frac{3wL}{\pi} I_d.$$

(2.10)

Optimum capability of direct current regulation, i.e. control gain which is represented by a slope of the CC control characteristic B-E, is normally determined by the time-constant lags in the control system applied, e.g. 2.5 kΩ with predictive control in New Zealand scheme.

Since the extinction angle of inverter ($\delta$) is normally under control, the following equation is given for inverter operation H-E-G in Fig. 2.9b:

$$V_d = -V_{do} \cos \delta + \frac{3wL}{\pi} I_d.$$

(2.11)

Having the assumptions made above, minimum extinction angle (MEA) control results in constant extinction angle (CEA) control in the steady state condition. For this reason the normal inverter characteristic is simply referred to as "extinction angle (EA) control".

If high accuracy is required in the above calculations, the effect
of transformer windings' resistance and the forward ON-state voltage of convertor valves (typically 1.5 to 2.5 V per thyristor) can be further included in equations 2.8, 2.10 and 2.11.\(^{(47)}\)

At the operating point both control characteristics intersect as shown in Fig. 2.10 (point C), where the rectifier controls the direct current \(I_d\) and the inverter determines the direct voltage.

In order to maintain the normal operation, the direct voltages measured at both ends of the transmission lines can be either increased or decreased further by changing on-load taps on the convertor transformers. Specifically, the rectifier tap changer is automatically controlled so as to maintain the firing delay angle \(\alpha\) at about 15° and within the range between 10° and 20°.\(^{(46)}\) For example in the Pacific Intertie scheme\(^{(71)}\) which implements predictive control as described in Section 2.3.2.1, the firing angle range is 12.5° to 17°. In order to avoid unnecessary wear on contact elements due to hunting of the tap changer, it is only activated if the delay angle \(\alpha\) exceeds the specified range over a long period, e.g. 1 s.\(^{(71)}\) This arrangement represents a technical compromise between keeping the power factor high (which requires small \(\alpha\)) and having a margin for fast increases in rectifier voltage (which requires large values of \(\alpha\)).\(^{(47,72)}\)

The inverter tap changer is controlled so that the direct voltage \(V_d\), at some specific point of the transmission lines, preferably the sending end, is close to its nominal value by an amount not exceeding, e.g. 5%. The voltage reduction in the transmission lines can be computed, given the value of the direct current \(I_d\) with known value of the transmission lines' resistance, and is used for operating the inverter tap changer.\(^{(47,49)}\) If two different power authorities are responsible for operating an HVDC transmission link, the mid-point voltage of the lines is used as the specific point because each authority shares half the line losses, e.g. Cross-Channel Link between England and France.\(^{(46)}\)
Fig. 2.10 Combined Control Characteristics of HVDC Transmission System.

N.B. C denotes a normal operating point.
The tap changers usually have a tap step of between \( \frac{1}{2} \) and 2% of the nominal a.c. voltage, within a certain maximum and minimum operational range, e.g. \( +16\frac{2}{3}\% \) to \( -13\frac{1}{3}\% \) in \( \frac{2}{3}\% \) steps, and \( +19\frac{1}{2}\% \) to \( -7\frac{1}{2}\% \) in \( \frac{1}{2}\% \) steps.

The inverter is also provided with CC control mode B'-E' as shown in Fig. 2.10. The inverter normally has the current setting less than that of the rectifier by some \( 10 \) to \( 15\% \) (current margin \( \Delta I_{ds} \)), so that CC control is only invoked under transient or abnormal conditions. This may occur when the two convertors' currents are different due to d.c. line faults, or when the rectifier is unable to increase the direct current \( I_{d} \) beyond the inverter's setting \( (I_{ds} - \Delta I_{ds}) \) due to a reduction in rectifier alternating voltages or a blocking of one or more of series-connected bridges in a rectifier. In practice, the current settings are determined from HVDC power transmission requirements or auxiliary control functions such as a.c.-system frequency modulation and/or damping of a.c.-system oscillations.

Fast telecommunications channels are provided for the exchange of information such as the current settings, blocking and deblocking state of convertors, power reversal, etc. Power line carrier telecommunications are widely used and overall communication delays including propagation delays, modem delays and coding/decoding time have been practically reduced in recent schemes, e.g. 100 ms Sardinia-Italian Mainland 1967, 90 ms New Zealand 1965, 30 ms Nelson River Bipole-one 1975, and 25 ms Kingsnorth 1975. For power flow control with damping capability of a.c.-system oscillations, one 1,200 baud (bits/s) channel per HVDC pole, which gives a communication delay and a sampling (relaying) interval of about 20 ms with a resolution of 0.05% of maximum CC setting (maximum rated power), is regarded adequate in most practical two-terminal schemes. This is because substantial damping can be achieved with a small amount of direct power modulation at a
relatively fast speed to an a.c.-system oscillations and/or frequency variations.\(^{(21,49,66)}\)

Although more expensive to install, microwave telecommunications can provide very fast and reliable alternative method of exchange of information. For example, at the capacity of 42,000 baud (bits/s), microwave telecommunications have been effectively achieved within 5 to 10 ms for the fast exchange of required information such as the power reversal and severe convertor faults.\(^{(74,79)}\)

Control instability, which is referred to as relaxation oscillation\(^{(49)}\) due to multiple operating points, can occur in cases where the inverter commutating reactance \(\omega L_i\) is greater than the rectifier commutating reactance \(\omega L_r\), and the rectifier alternating voltages are transiently reduced.\(^{(80)}\) Since slow acting tap changers can not normally cope with control instability, a modification of the inverter CC control mode, i.e. dual-gain CC control,\(^{(5,36)}\) has normally been provided in recent HVDC schemes when a firing delay angle \(\alpha\) is larger than a certain value (e.g. \(120^\circ\) to \(140^\circ\)) and before the extinction angle (EA) control mode is established.\(^{(49)}\) An example is shown in Fig. 2.11 as part D'-F'.

A low-voltage-dependent current limit P-Q for rectifier operation is also commonly applied as shown in Fig. 2.11. Such a limit is required to avoid voltage instability on starting transmission when the direct voltage is being raised slowly.\(^{(47)}\) A similar limit can be implemented so as to reduce the rectifier current on occurrences of a.c./d.c. line faults\(^{(81)}\) or sustained commutation failure of the inverter due to very severe faults in the receiving a.c. system.\(^{(49)}\) Similarly the inverter is normally limited with a minimum delay angle setting of more than \(90^\circ\) (e.g. \(100^\circ\) to \(120^\circ\)) for CC control such as part P'-Q', to prevent it from reversing the voltage polarity, i.e. to prevent it operating as a rectifier. (Part S'-T' may be further imposed for this purpose.)
Fig. 2.11 General Control Characteristics of HVDC Transmission System:
Dual-Gain Modification of CC Control, and an Example of Low-Voltage/Low-Current Characteristics are Shown.
provision of the low-voltage-dependent current limit and CC control for inverter operation also enables fast control of power (voltage) reversal in conventional two-terminal systems, \(^{(81)}\) if it is required.\(^ {(55)}\)

In Fig. 2.11, branches Q-R and Q'-R' represent maximum current limits at low voltage.\(^ {(49)}\) Besides this, a minimum current limit \(M\) is usually provided to prevent operation with discontinuous current, e.g. 5 to 10\% of the nominal current \(I_{dn}\).\(^ {(47,82)}\) With presently installed mercury-arc valves, the minimum current is typically 80 A.\(^ {\text{(46,83)}}\)

Moreover, HVDC transmission systems normally have short-to-long time overload capabilities, viz., depending on ambient temperatures or cable-conductor's cooling conditions maximum operating current (and thus power) can be set about 10 to 20\% more than the nominal current \(I_{dn}\).\(^ {\text{(47)}}\) e.g. 11\% for most days of a year in Nelson River Bipole-two scheme,\(^ {\text{(58)}}\) and 25\% for several seconds when one pole is rejected due to the d.c. line faults in Cabora Bassa-Apollo bipolar scheme.\(^ {\text{(84)}}\)

As mentioned before, the direction of power transmission is reversed by the reversal of direct voltage. If power reversal is required in two-terminal systems, this can be effectively achieved by transferring the current margin \(\Delta I_{ds}\) to the station that becomes the inverter station.

Based on the digital implementation of basic controls described in Section 2.3.4, a direct digital control of power and fast power reversal has been proposed with point-on-wave control and adjustable speed characteristics.\(^ {\text{(78,85)}}\) The required logic sequence for digital processing also includes tap-changer operation, manual or automatic starting with predetermined power and time-step intervals, and selection of a current or power setting before and during convertor operation with predetermined power and time steps.\(^ {\text{(85)}}\)

2.4.2 Multiterminal Systems

Control and protection schemes for multiterminal operation have been proposed and developed since the early stage of commercial HVDC
applications with static convertors.

One of the basic schemes is a constant-voltage operation with all convertors connected in parallel. In this scheme a current margin is given to one of parallel-connected convertors, which controls the direct voltage in EA control mode. Other convertors operate in CC control mode at appropriate current settings.

An alternative scheme uses constant-current operation with all convertors connected in series. The voltage is controlled by a combined operation of CC control characteristics, tap changers, and blocking/deblocking of 6-pulse bridges connected in series. Moreover, adjacent two-terminal schemes, which at present exist as separate schemes, could be converted into a multiterminal scheme, i.e. multiple-pair configuration.

A report presented by CIGRE's Study Committee No. 14 (AC/DC Converting Plant) 1974 has discussed various aspects of the d.c. network configurations (e.g. radial, meshed, and series connections) and requirements of the d.c. circuit breakers, control systems, and telecommunication systems for multiterminal operation. More recently, a survey of technical papers which are relevant to multiterminal systems' configuration and operation has been given by Reeve 1980. The survey and an IEEE Committee Report also list recent literature on d.c. circuit breakers.

With respect to the eventual implementation of digital convertor-station control and protection, some design features and requirements for multiterminal operation are summarized below:

- In general, multiterminal systems offer greater flexibility of power transmission as compared to separately applied two-terminal systems.
- The control scheme for multiterminal operation is generally an extension of that already described for the two-terminal systems.
in previous Section 2.4.1. A means of central control is normally required for coordination of current or power settings of the convertor stations. Thus a level of centralization generally leads to a system control hierarchy which comprises of valve group control, station (pole) control, area control, and overall a.c./d.c. system control at a load dispatch level. For example, a comparative computer simulation study has demonstrated that centrally coordinated power modulation of a four-terminal radial HVDC system can utilize d.c. overload capabilities more efficiently than decentralized modulation.

- Fast fault detection and protection against convertor and d.c.-line faults are required. Moreover, the discrimination of fault locations and coordinated protection strategies become more significant to minimize the effect of faults, and to ensure reliable a.c./d.c. system operation. For example, commutation failure at any inverter in a radial system can draw current from the other convertors connected in parallel.

- Fast and reliable two-way (duplex) telecommunications channels permit rapid power rescheduling and/or modulation following severe convertor faults or d.c.-line faults. For example, it has been realized that in a meshed multiterminal system the use of information such as voltage and current at the other end of transmission lines is required to determine the location of d.c. line faults. In this case, telecommunications delays will be significant since they have to be included in the time for detection of the line in which the fault has occurred.

- D.c. circuit breakers do not necessarily have to be used in multiterminal operation, however, they would be valuable to minimize the effect of d.c. line faults if fast control and
protection action by gate pulse firings were coordinated.\textsuperscript{(72)}

The requirements on the d.c. circuit breakers depend to a large extent on the fault detection principle and d.c. network configurations to be developed.
CHAPTER 3

DESIGN OF THYRISTOR CONVERTOR MODEL SUITABLE FOR
DIRECT DIGITAL CONTROL AND PROTECTION

3.1 INTRODUCTION

Based on the requirements for direct digital control and protection, the design of a scaled-down thyristor convertor and transmission model is described in Sections 3.2 to 3.5. Section 3.6 describes the design of a fault actuator for the implementation of a.c./d.c. disturbances. Finally the overall convertor characteristics are presented in Section 3.7.

3.2 DESIGN CONSIDERATIONS OF THE THYRISTOR CONVERTOR MODEL

3.2.1 Design Requirements and Main Characteristics

The design requirements and main characteristics of the convertor model are summarized below:

- Compatibility with an existing manually-controlled thyristor convertor, because some modules like harmonic filters and convertor transformers are exchangeable, so that the rating of the convertor model is kept the same.
- In order to study malfunctions of existing convertors with mercury-arc valves installed, a by-pass valve and an extra auxiliary valve are also provided in order to simulate arback disturbances in the main and by-pass valves.
- For flexibility to study the behaviour of analogue and digital controllers, the model includes an existing type of convertor controller, i.e. the predictive controller. A selection of the
appropriate automatic control mode, either analogue or digital, can be achieved by an external signal.

- Various transducers provide the necessary signals for a direct digital control and protection, i.e. commutating-voltage-zero crossings ($C_i$), ON/OFF states of each valve ($ON_i$), direct current ($I_d$), rate of change of direct current ($\frac{dI_d}{dt}$), and direct voltage ($V_d$).

- In order to investigate the interaction between convertor and power supply with different short circuit levels under various a.c. and/or d.c. faults and valve malfunctions, series reactors with different values of reactance are connected between the a.c. supply (regarded as an infinite busbar), and the convertor transformers.

3.2.2 Realization of the Convertor Model

3.2.2.1 Overall Configuration. The overall circuit configuration of the convertor model is diagrammatically shown in Fig. 3.1. A brief description of the model is given below:

- A three-phase supply is connected to three sets of series reactors, which represent a.c. system with different ratios of short circuit level at the a.c. busbars to the d.c. power, i.e. short circuit ratios (SCR) 2, 4, 5, 10 and 20.

- A.c. filters tuned to lower harmonic frequencies and higher frequencies are connected to the primary windings of convertor transformers.

- Up to 20% amplitude of voltage unbalance can be simulated by means of the transformer tap-changing switches.

- The model consists of a basic 6-pulse bridge plus a by-pass valve and an auxiliary valve. A series smoothing reactor and 6th and/or 12th tuned harmonic filters are connected to the d.c. side
Fig. 3.1 HIROLLAGA III Convertor Configuration
terminals of the bridge.

- Signal transformers provide commutating voltage-waveforms with thirty-degree phase-displacements with respect to the secondary phase (line-to-neutral) voltage of convertor transformers.

- The predictive controller provides minimum delay angle (MDA) control, constant current (CC) control and constant extinction angle (CEA) control. The value of CEA can be set and read by the digital angle display (module B-3).

- A reference direct current $-I_{ds}$ and current margin $\Delta I_{ds}$ can be set at the Input/Output module A-3. The module also permits the blocking of signals and provides control signals for the predictive controller.

- Direct current $I_d$, voltage $V_d$, and rate of change of direct current $\frac{dI_d}{dt}$ are measured and buffered by operational amplifiers for external processing. The lower pole of the d.c. line is supposed to have a ground potential. Thus the direct voltage is referred to that lower pole which has the common ground with d.c. supplies, i.e. + and -15 V and +5 V.

- Firing circuits combined with ON/OFF level-detection circuits are shown in Fig. 3.1 are D1 to D6, E7 and E8. ON/OFF states of each valve are derived from these circuits for external processing.

3.2.2.2 General Description of Individual Modules. As illustrated in Fig. 3.2, the model is of modular design to permit constructive components modelling, to provide accessibility to the components and facilitate maintenance and fault diagnosis.

Each module can be identified by three symbols, e.g. HR3, where H indicates the type of module, R the phase (Red, Yellow or Blue), if any, and 3 the type of convertor model (which in this case refers to the predictive controller.)

The model consists of the following nine major types of modules.
Fig. 3.2 Panel View of HIROLLAGA III Convertor
Scale 3/4
- Modules H (HR3, HY3 and HB3) represent the a.c. system.
- Modules I (IR3, IY3 and IB3) comprise harmonic filters.
- Modules J (JR3, JY3 and JB3) comprise Y-Y connected convertor transformers.
- Module A-3 is an Input/Output module for the predictive controller.
- Module B-3 includes the CEA generation and the digital angle display.
- Modules C (CR3, CY3 and CB3) comprise the predictive controller.
- Modules D (DR3, DY3 and DB3) comprise the 6-pulse bridge.
- Module E-3 comprises by-pass and auxiliary valves, transducers.
- Module G-3 comprises 6th and 12th harmonic filters.

A selection of short circuit ratios (SCR) can be achieved by means of a pair of 2-mm plug-connectors for each a.c. system phase. A location of arcback can be externally determined by connecting the auxiliary valve TH₈ across the particular valve selected and firing the auxiliary valve.

The main control signals and the outputs of various transducers can be monitored via 1-mm sockets placed in the front panels of the model.

Details of the electrical characteristics and operating procedures of the individual modules are described in Section 3.4.

3.3 DESIGN FEATURES OF THE CONVERTOR MODEL

3.3.1 Convertor Ratings

- AC Supply; 240 V, 3-phase plus neutral (earth)
- Average Direct Voltage; 50 V
- Average Direct Current; 1 A
- Average Direct Power; 50 W
3.3.2 AC System

The a.c. supply sees the convertor load as a source of harmonic current. Owing to the low power rating of the model, the supply system is virtually a zero impedance source, so that the harmonic voltage-drop is negligible and the supply waveform remains sinusoidal.

A simple representation of the a.c. system is shown in Fig. 3.3a, where \( R_s \) is the effective resistance and \( X_s \) the effective reactance of the a.c. system. From the viewpoint of system performance, the amount of damping in the a.c. system, i.e. the value of \( R_s \), is important. A useful criterion of damping is the impedance angle of the a.c. system, \( \phi \), defined at a particular frequency, i.e.

\[
\tan \phi = \frac{X_s}{R_s}.
\] (3.1)

The value of \( \phi \) depends on the electrical proximity of loads, if any, to the a.c. busbar and on the nature of the a.c. system. Each transformer between the load and the convertor a.c. busbar introduces inductance and reduces the effectiveness of the load in damping transients.

The a.c. system can be represented accurately at a single frequency by the simple circuit of Fig. 3.3a. However it is often required to represent the a.c. system over a range of harmonic frequencies, say from the fundamental to 5th harmonic for most purposes.

Although very extensive and complicated equivalent circuits can be used, the simple circuit of Fig. 3.3b can provide a network with an approximately constant impedance angle for a range of frequencies, which is more representative of a.c. system for lower harmonic frequencies. The value of \( L \) is chosen to obtain the required impedance and the value of \( R \) to obtain the required angle at a nominal angular frequency \( \omega_0 \).

The expected characteristic of a.c. system impedance is shown in Fig. 3.3c, where the angular frequency \( \omega \) is a parameter.
Fig. 3.3 Representation of AC System Impedance and Damping:
(a) Simple Circuit which is Accurate at a Fundamental AC System Frequency,
(b) AC System Equivalent Circuit for a Range of Low Frequencies,
(c) Impedance Characteristic of the AC System (b).
Due to a space limitation of module, the model has five different values of the short circuit ratio, i.e. 2, 4, 5, 10 and 20, with fixed impedance angles from 83° to 86°.

3.3.3 Harmonic Filters

Harmonic filters are normally installed in the form of parallel tuned branches, taking advantage of the power factor correction capacitors normally installed.\(^\text{(57)}\)

Typical filters for the three-phase bridge configuration consist of several branches of L, C, R components connected in series and tuned to lower order harmonics, (i.e. 5th, 7th, 11th, 13th) with a relatively high Q, and a high pass filter for the higher harmonic orders, (i.e. over 17th and 19th).

Switches are provided in the model to show the individual effect that each filter branch has on the voltage waveform.

The design and construction of harmonic filters have been done by Rimmer.\(^\text{(96)}\) Typical impedance-frequency characteristics of the a.c. harmonic filters in the model are shown in Fig. 3.4.

3.3.4 Convertor Transformers

A set of three single-phase transformers is used and up to 20% amplitude unbalance can be simulated by means of the transformer tap-changing switches placed in the front panel of the model. Thus the effect of voltage unbalance on the a.c. and d.c. waveforms can be studied.

A current-waveform of secondary winding can be monitored if a non-inductive shunt resistor with very low resistance is placed instead of the appropriate two 2-mm sockets in the front panel of the module, as shown in Fig. 3.5.

The ratings of two types of transformers are shown below.

(i) Three single-phase transformers for Y-Y connected convertor (Fig. 3.5a).
Fig. 3.4  Typical Impedance-Frequency Characteristics of the AC Harmonic Filters.
Fig. 3.5 Panel View of Transformer Modules:
(a) Transformer Module J for Y-Y Connected Convertor Model,
(b) Transformer Module K for Y-Δ Connected Convertor Model.
- Primary r.m.s. voltage; 240 V, nominal plus ±4%, ±8% and +12% taps
- Primary r.m.s. current; about 0.12 A
- Secondary r.m.s. voltage; 26 V, nominal
- Secondary r.m.s. current; 0.78 A, average

(ii) Three single-phase transformers for Y-Δ connected convertor (Fig. 3.5b).
- Primary r.m.s. voltage; 240 V, nominal plus ±4%, ±8% and +12% taps
- Primary r.m.s. current; about 0.12 A
- Secondary r.m.s. voltage; 45 V, nominal
- Secondary r.m.s. current; 0.45 A, average

The output voltage regulation characteristics of the sets of transformers (with 5 and 8% short-circuit impedances) are shown in Fig. 3.6.

The per-cent impedance of these transformers is constant over a wide range of secondary current as observed in Fig. 3.6.

### 3.3.5 Thyristor Valves

As mentioned above, the model consists of a basic 6-pulse bridge and a by-pass and auxiliary thyristors. The ratings of these eight thyristors are as follows:

- Repetitive peak OFF-state/reverse voltage; 400 V
- Continuous forward current; 5 A
- Surge ON-state current; 30 A

The sequential firing logic and the development of fast ON/OFF detection of each thyristor valve are discussed in Chapter 4.
Fig. 3.6 Output Voltage-Current Characteristics of Convertor Transformers:
(a) Convertor Transformers for $Y-Y$ connected Convertor,
(b) Convertor Transformers for $Y-\Delta$ connected Convertor.
3.3.6 Predictive Controller

A predictive controller is basically a special-purpose analogue computer solving a specific equation governing minimum delay angle (MDA) control, constant current (CC) control and constant extinction angle (CEA) control.\(^{(27,47)}\) The basic design of the controller has been achieved\(^{(97)}\) and some more features are added to the basic controller as follows:

- A reference current \(I_{ds}\) and current margin \(\Delta I_{ds}\), or the latter alone, can be blocked by logic commands or manual switches placed in the front panel of Input/Output module A-3 of the model.
- If the reference current is blocked by the logic command as mentioned above, a new reference current can be instantaneously provided from an external processor via A/D convertor to Input/Output module A-3.
- In order to assess the effect of firing unbalances under steady state conditions, firing angles at each valve can be set by a knob placed in the front panel of the control module C.
- All timing pulses of the predictive controller, i.e. \(T_1\) to \(T_6\), can be instantaneously blocked by a logic command, so that an alternative direct digital control and/or protection scheme is implemented either on temporary or permanent basis by using external processors. The predictive control could be resumed after a temporary period of direct digital control and/or protection, if required.

3.3.7 Transducers

Five different transducers are employed in the model as summarized below:

(i) Commutating-voltage-zero Crossings Cl to C6. Commutating voltage-waveforms are derived from a set of signal transformers.
which are connected to the nominal taps\(^{(24)}\) on the primary side of the convertor transformers. For the Y-Y connected convertor, the use of signal transformers with a \(\Delta\)-double \(Y\) configuration provides the thirty-degree phase-displacements required for the six commutating voltage-waveforms.

The six instants of commutating-voltage-zero crossings \(C_i\) are individually derived by squaring the commutating voltage-waveforms and triggering six one-shots from their edges. Due to the waveform distortion caused by the commutations, only the first voltage-zero crossing of the commutating voltage-waveforms is selected.

(ii) **ON/OFF States of Each Valve ON\(_1\) to ON\(_8\).** ON/OFF states of each thyristor valve are derived by an electronic circuit which senses the gate-to-cathode voltage. A very fast (within a few microseconds) and accurate ON/OFF detection of thyristor valve has been achieved.\(^{(98)}\) This is discussed in detail in Chapter 4.

The extinction angle of each valve, \(\theta_{Ei}\), is now a direct result of combination \(ON_i\) and \(C_{i-1}\) for a valve \(TH_i\) of the bridge.

(iii) **Direct Current \(I_d\).** A linear-type Hall IC, Hall-generator with differential amplifiers mounted in a small plastic package, is placed in a small gap of ferrite core with high permeability. The core itself has four turns of d.c. line, which add negligible reactance to the d.c. line.

Thus the linearity of the transducer is maintained, and the output of the Hall IC is amplified to a suitable level of voltage by means of operational amplifiers. Two \(I_d\) signals are produced, one for the predictive controller and the other, through external A/D conversion, for microprocessor control.

(iv) **Rate of Change of Direct Current \(\frac{dI_d}{dt}\).** A rate of change of direct current \(\frac{dI_d}{dt}\) is derived from the transducer which is
actually a transformer magnetically coupled with the d.c. line through the ferrite core mentioned above. The secondary output of the transducer, proportional to the primary and with good electrical insulation, is then amplified to the level required for external A/D conversion, for microprocessor control and protection.

(v) **Direct Voltage Vd.** The direct voltage is simply derived from a pair of shunt resistors connected across the d.c. terminals with the smoothing reactor. The voltage derived from the shunt resistors is then amplified to the level required for external A/D conversion, for microprocessor control and protection.

3.4 INDIVIDUAL MODULES OF THE CONVERTOR MODEL

3.4.1 **AC System Modules H**

The hardware model representation of the a.c. system consists of two variable (tapped) reactors in series with each phase of the three-phase supply. The centre-point of the two reactors is connected to the neutral by a shunt resistor R, which gives the desired impedance angle of a.c. system.

3.4.1.1 **Panel Design of Module H.** One of three 2-inch panels of module H is shown in Fig. 3.7. The module includes a fuse (5 A) and a neon indicator. The supply voltage and convertor a.c. system's voltage can be monitored through 1-mm sockets. The a.c. system line current can be monitored if one of the external 2-mm plug-connectors is replaced by an a.c. ammeter or a non-inductive shunt resistor combined with the use of a differential-type oscilloscope.

The typical voltage-current (or impedance) characteristics of a.c. system's reactor are shown in Fig. 3.8. Due to the space limitation of the 2-inch module, the reactance (slope) shows a gradual
Fig. 3.7 Panel View of AC System Module H.
Fig. 3.8 Voltage-Current Characteristics of Reactor in AC System Module H.

N.B. 50 Hz supply voltage is applied to one of reactors and the voltage across the reactor is measured.
reduction as the current increases due to saturation.

3.4.1.2 Short Circuit Ratios SCR. Theoretically the SCR is the ratio of short circuit level at the convertor a.c. busbars to the d.c. power-rating of the convertor. Due to the small power-rating of the model (i.e. 50 W), effects such as forward voltage-drop of thyristors and resistance of convertor transformers and smoothing reactor have to be taken into consideration when calculating the SCR.

The reactors of the module show reasonably good linearity over a wide range of a.c. current as shown in Fig. 3.8.

3.4.1.3 Impedance Angle of AC System. An equivalent circuit of the a.c. system for a range of low frequencies is shown in Fig. 3.9. A small series resistance \( r \) is introduced by the reactor's windings.

\[
Z_s = R_s + jX_s
\]

\[
\tan \phi = \frac{X_s}{R_s}
\]

The reactors of the module show reasonably good linearity over a wide range of a.c. current as shown in Fig. 3.8.

3.4.1.3 Impedance Angle of AC System. An equivalent circuit of the a.c. system for a range of low frequencies is shown in Fig. 3.9. A small series resistance \( r \) is introduced by the reactor's windings.

\[
Z_s = \frac{1}{R} + \frac{1}{\frac{R + j\omega L}{\frac{R^2 + 2rR + (r^2 + \omega^2 L^2)^2}{2rR^2 + (3r^2 + \omega^2 L^2)R + r(r^2 + \omega^2 L^2)}} + \frac{2\omega LR^2 + 2r\omega LR + \omega L(r^2 + \omega^2 L^2)}{R^2 + 2rR + (r^2 + \omega^2 L^2)}}
\]

(3.2)
The impedance angle of the a.c. system, $\phi$, is now,

$$\tan \phi = \frac{X_S}{R_S} = \frac{2\omega LR_S^2 + 2\omega L R + \omega L (r^2 + \omega^2 L^2)}{2r R_S^2 + (3r^2 + \omega^2 L^2)R + r (r^2 + \omega^2 L^2)}. \quad (3.3)$$

With known values of $r$ and $L$, the characteristics of the impedance angle, $\phi$, versus the value of $R$ are calculated at the power frequency, 50 Hz, and the results are shown in Fig. 3.10. From the figure it is clear that with a selected short circuit ratio the desired impedance angle, which approximately represents a state of a.c. loads, can be selected by varying the value of shunt resistor $R$.

Due to space limitation and also to high power dissipation in $R$, the value of $R$ is fixed at 5.0 k\Omega. The design of the a.c. system module is based on an SCR of 2.

The module provides impedance angles of about $84.3^\circ$ (SCR of 2), $84.9^\circ$ (SCR of 4 or 5), $84.0^\circ$ (SCR of 10) and $82.4^\circ$ (SCR of 20) at 50 Hz. It is suggested that in representing the damping of a rectifier station fed solely by generators with little local load, an impedance angle of $85^\circ$ should be used, which is probably pessimistically high. For an inverter station with substantial load relatively close to the a.c. busbar, it is suggested that an impedance angle of $75^\circ$ should be used; this value is again probably pessimistic, and depends principally on the a.c. configuration. \(^{(95)}\)

The impedance angles suggested above could be met for specific studies by altering the value of the shunt resistor $R$, except for SCR's of 10 and 20 which require smaller $r$.

3.4.1.4 Impedance Characteristics of the AC System. With known values of $r$ and $L$, the impedance of the module is calculated at various frequencies, and its characteristics are shown in Figs. 3.11 to 3.13. From these figures it is obvious that with this simple a.c. system representation the value of impedance and its angle are only correct at
Fig. 3.10 AC System Module H: Impedance-angle versus the Value of R at AC System Frequency 50 Hz.
Fig. 3.11 Impedance-Frequency Characteristics of AC System Module H: Calculated Results.
Fig. 3.12 Impedance Characteristics of AC System Module H with SCR of 2 and R of 5 kΩ:
Calculated Results.
Fig.5.13 Impedance Characteristics of AC System Module H with SCR of 5 and R of 5 kΩ:
Calculated Results.
a particular nominal angular frequency $\omega_0$, i.e. a substantial reduction of impedance angles occurs between the fundamental and 5th harmonic frequency. The variation of impedance angle with frequency is shown in Fig. 3.14.

Thus the lower harmonic components will be more damped in the module than those in a real a.c. system with an impedance angle substantially constant throughout the range of interest.

The experimental results of a.c. system module H are shown in Fig. 3.15. The impedance-frequency characteristics of the module show good agreement with the calculated results in Fig. 3.11.

3.4.2 Input/Output Module A-3

3.4.2.1 Design Features. The direct current $I_d$, measured in module E-3, is processed in module A-3. As a result, the error signal $\epsilon$, and the product $2\omega L \cdot I_d$, required for CEA control, are generated in this module. The outputs are fed to the predictive controller, i.e. modules C.

With reference to Fig. 3.16 the main design features of module A-3 are summarized below:

- The direct current $I_d$ is smoothed out by a 4th-order Butterworth low-pass filter ($^{99,100}$) and the product $2\omega L \cdot I_d$ is directly obtained from a buffer-amplifier.

- A specified current $I_{ds}$ ($-10$ V for 1 A of direct current), and current margin $\Delta I_{ds}$ ($+1$ V for 0.1 A of direct current), are manually set by two knobs in the front panel of the module.

- An error signal $\epsilon$, will be generated, if $I_d - I_{ds} + \Delta I_{ds} < 0$, otherwise it is null, because the blocking amplifier blocks the output of error signal generator.

- The reference current $I_{ds}$ and current margin $\Delta I_{ds}$, or the latter alone, can be blocked by either logic commands, BLKI$_{ds}$ and BLK$, the
**Fig. 3.14** AC System Module II:
Frequency Variation of Impedance Angle, Calculated Results.
Fig. 3.15 Impedance-Frequency Characteristics of AC System Module H: Experimental Results.

N.B. The corresponding broken lines show the calculated results shown in previous Fig. 3.11.
Fig. 3.16 Block Diagram of Input/Output Circuits for Predictive Automatic Control System: Module A-3.

N.B. Error Signal $\varepsilon \cong 0$, if $I_d - I_{ds} + \Delta I_{ds} \approx 0$, otherwise $\varepsilon = 0$. 
or manual switches placed in the front panel of the module.

- If the reference current is blocked by the logic command $BLKI_{ds}$, a new reference current $I_{ds}$ ($-10$ V for $1$ A of direct current) is instantaneously provided from external processors via A/D conversion.

- By replacing the error signal with a variable direct voltage, and grounding the $2\omega L I_d$ signal the convertor delay angle is set by manual control.

- Blocking of all firing-pulses $FP_1$ to $FP_6$ can be achieved by either a toggle switch in the front panel of the module or an external logic command $BLK_A$.

3.4.2.2 Panel Design and Operating Instructions. The panel design of the Input/Output module A-3 is shown in Fig. 3.17. Its operating instructions are summarized below:

- **Toggle Switch SW9:** turns on or off $\pm 15$ V (0.5 A $\text{max}$), $+5$ V (2 A $\text{max}$) d.c. power supplies and eight auxiliary d.c. power supplies to the thyristor gates.

- **Toggle Switch SW5:** blocks the reference current $I_{ds}$ and current margin $\Delta I_{ds}$.

- **Toggle Switch SW6:** blocks the current margin $\Delta I_{ds}$ only.

- **Variable Resistor VR3:** sets the reference current $I_{ds}$ between nought and 1.1 A ($-11$ V).

- **Variable Resistor VR5:** sets the current margin $\Delta I_{ds}$ between 0.1 A ($+1$ V) and 0.3 A ($+3$ V).

- **Variable Resistor VR7:** sets a control constant or a gain of CC control characteristics.

- **Toggle Switch SW7:** selects control modes either automatic (predictive) or manual for the convertor model.

- **Variable Resistor VR10:** manually sets a desired delay angle of
SW5
To Block Ids and ΔIds

VR3
Reference Current
(-10V/dc, A)
Ids=0 to 1.1A

Green Lamp

SW7
Control-mode Selection

VR10
Manual Control of Delay-Angle

A-3

SW6
To Block ΔIds only

VR5
Current Margin
(+10V/dc, A)
ΔIds=0.1 to 0.3A

VR7
CC Control Constant

SW8
To Block FF1 to FF6
Error Signal

Fig. 3.17 Panel View of Input/Output Module A-3.
convertor model, of which the minimum angle is about 3.5°.

- Toggle Switch SW8; manually blocks all the firing pulses FP₁ to FP₆, to the 6-pulse bridge.
- The error signal £ and the product 2ωL•Iₖ can be monitored by 1-mm sockets placed in the front panel of the module.

3.4.3 Digital Angle Display Module B-3

3.4.3.1 Design Features. A periodic logic signal with certain time-duration based on the a.c. system frequency, 50 Hz, can be displayed by module B-3 in electric degrees, down to a decimal number. The logic signal which sets the CEA of the predictive controller is also generated in this module.

With reference to the block diagram of Fig. 3.18, the main design features are summarized below:

- One of six delay-angles α₁ to α₆ can be selected by a 12-way double rotary switch and the angle displayed by the module.
- Any logic (non-inverted and periodic) signal can be also selected and displayed by the module, provided that the signal is connected to 1-mm socket in the front panel of the module.
- As shown in Fig. 3.18, the selection of an appropriate pair of signals is made by a 12-way double rotary switch, and the time-duration of pulses is set by an S-R Flip-Flop.
- The following six-stage ripple-counter picks up one cycle of selected pulses out of 64 cycles, so that the display shows the numeric angle every 1.28 s based on 50 Hz a.c. system frequency.
- The logic circuits which follow the ripple-counter provide the necessary commands to the display.
- The frequency of clock pulses is set at 180 kHz.
Fig. 3.18 Block Diagram of CEA Generator and Digital Display: Module B-3.
If desired, the decimal number of display can be rounded up to the nearest integer and the decimal nought blanked by sub-miniature switches inside the module.

The display is capable of measuring an angle between 0.1° and 999.9°.

3.4.3.2 Panel Design and Operating Instructions. The panel design of the angle display module B-3 is shown in Fig. 3.19. Its operating instructions are summarized below:

- Rotary Switch SW5; selects the periodic signal to be displayed.
- Variable Resistor VR3; adjusts the frequency of the clock-pulse generator. When the selected SW5 signal is "357°", the reading of the display is expected to be this figure.
- Variable Resistor VR1; sets a desired value of the CEA between 0° and 30°. With SW5 placed at "CEA", the display shows the present value of CEA setting, which will normally be over 10° in practice.
- 1-mm Socket "100 Vmax"; can be used to measure the duration of the positive-part of any periodic analogue signal, but the maximum peak-to-ground voltage of the signal should be less than 100 V.
- 1-mm Socket "Logic"; can be used to measure the angle of periodic logic signal, e.g. extinction angle EA₁ to EA₆, duration of valve conduction ON₁ to ON₆, etc.

3.4.4 Predictive Controller Modules C

3.4.4.1 Design Features. Main control circuits per phase are mounted in module C. Its schematic block diagram and corresponding waveforms (with reference to thyristor TH₁) are shown in Fig. 3.20.
Fig. 3.19 Panel View of Digital Angle-Display Module B-3.
Fig. 3.20  Schematic Block Diagram and Corresponding Voltage Waveforms of Predictive Control System.
The main design features are summarized below:

- One of six commutating voltage-waveforms, derived from signal transformers, is shown in Fig. 3.20a (broken line).

- Commutating-voltage-zero crossings $C_1$ to $C_6$ are derived by zero-crossing detectors $A$ and one-shots as shown in Figs. 3.20b and 3.20c.

- For CEA control, the commutating voltage-waveforms are integrated producing a $90^\circ$ phase-shift as a result. The output of the operational amplifier is clamped on to the virtual ground for the duration of CEA as shown in Figs. 3.20d and 3.20e.

- The error signal $e$, the product $2\omega L I_d$, the rate of change of direct current $\frac{dI_d}{dt}$, and the negative pulses $C_i$ are added together with the integrated output, so that the equation governing MDA, CC and CEA control is solved as shown in Fig. 3.20f. As previously shown in Fig. 3.20c, the minimum delay-angle (MDA) is already set as a pulse-width from the crossings $C_1$ to $C_6$.

- The logic command which initiates start of valve conduction, i.e. the timing pulses $T_i$ to $T_6$, is derived as shown in Fig. 3.20h.

- In order to prevent complete arc-quenchings (in the case of mercury-arc valve convertors) or intermittent misfires, and also to ensure the initial start of the 6-pulse bridge, firing pulses $FP_1$ to $FP_6$ of $120^\circ$ duration are formed by pairs of timing pulses, $T_i$ and $T_{i+2}$ as shown in Fig. 3.20i.

- The individual setting of delay-angle is achieved by altering a variable resistor of an additional one-shot, which is in fact gated with the output of zero-crossing detector $B$, though this is not shown in Fig. 3.20.

3.4.4.2 Panel Design and Operating Instructions. Various stages of the control signal development can be monitored through 1-mm sockets
mounted in the front panel of the module, as shown in Fig. 3.21.

Variable resistors VR7 are used for the manual setting of individual delay-angles $\alpha_1$ to $\alpha_6$. The actual value of delay angle can of course be read at the display module B-3. These knobs (VR7) can set the delay angles between $3.5^\circ$ and $170^\circ$; however, they should be set at the minimum reading ($3.5^\circ$), (when they are not used for individual setting of delay-angles), because the VR7 settings have priority over the predictive control.

3.4.5 Thyristor Modules D

3.4.5.1 Design Features. A block diagram of the thyristor module D is shown in Fig. 3.22 and the main design features are summarized below:

- When the predictive controller is operating, firing pulses FP$_1$ are formed by an S-R Flip-Flop and the outputs of which are fed to the firing circuit of the thyristor valve TH$_1$.
- Individual blocking of the firing pulses FP$_i$ can be achieved by the external logic command BLK$_i$.
- Total blocking of firing pulses FP$_1$ to FP$_6$ can be achieved by the external logic command BLK$_A$, which is common to all firing circuits.
- The firing pulses FP$_1$, provided to the thyristor gate G$_1$, are monitored at FP$_1$(m).
- ON/OFF states ON$_1$ to ON$_6$, end of valve conduction S$_1$ to S$_6$, and extinction angles EA$_1$ to EA$_6$ of thyristor valves TH$_1$ to TH$_6$ are derived in logic form in the modules D.
- For applications to digital control and protection, firing pulses FP$_1$ can also be formed by a pair of logic commands RP$_i$ ("Low" to pre-set S-R Flip-Flop) and CLR$_i$ ("Low" to clear S-R Flip-Flop). The additional command EDDC ("Low" to enable direct digital
Fig.3.21  Panel View of Predictive Controller Module C and Thyristor Module D (Red Phase).

N.B. VR's 7 are for setting individual delay-angles $a_1$ to $a_6$. 
Fig. 3.22 Block Diagram of Thyristor Module D:

TH_i: Thyristor Valve V_i (i=1 to 6),
T_i: Timing Pulses, Initiation of Conduction of TH_i,
FP_i: Firing Pulses to TH_i Gate,
PR_i: Pre-set FP_i, or Fire TH_i if not blocked,
CLR_i: Clear FP_i,
BLK_i: Block FP_i,
BLKA: Block all FP_i's, i.e. FP_1 to FP_6,
ON_i: Conduction State of TH_i,
EA_i: Extinction Angle of TH_i,
C_i: Commutating-voltage-zero Crossing,
S_i: End of Conduction of TH_i,
EDDC: Low to Clear T_i to T_6, Enable Direct Digital Control.

N.B. Priority over FP_i: BLK_i or BLKA > PR_i > CLR_i > T_i, T_i+2 in this order.
control) can clear all timing pulses $T_1$ to $T_6$ of the predictive controller and enable S-R Flip-Flop by $\overline{PR}_i$.

- There are three levels of priority in the logic of the firing pulses $FP_i$ and $FP_{i(m)}$ as follows:

$$BLK_i \text{ or } BLK_A > PR > CLR > T'_{i}, T_{i+2}.$$  \hspace{1cm} (3.4)

- In order to supply d.c. auxiliary power $EI$ to each firing/detection circuits of the module, isolated d.c. supplies are used.

3.4.5.2 Panel Design and Operating Instructions. The panel design of the thyristor module is shown in Fig. 3.23. In order to permit individual valve arcback/short-circuit simulation, a 2-mm socket is placed at the connection point of valve pairs $TH_1$ and $TH_4$, etc.

As shown in Fig. 3.23b, an auxiliary thyristor module is made available for substitution. Thus, valve current can be monitored if a non-inductive shunt resistor with very low resistance is connected between the sockets A and B (or C and D) in the front panel of the auxiliary module.

3.4.5.3 AC Voltage-waveforms and Logic Signals. The relationship between the a.c. voltage-waveforms of a 6-pulse bridge and its associated logic pulses is illustrated in Fig. 3.24 for the case of inverter operation. The positive and negative direct voltages with respect to the transformer neutral (Fig. 3.24a), and the voltages across valve $V_1$ and between the d.c. poles ($v_1$ and $v_d$ in Fig. 3.24b) are related to timing pulses $T_1$ and $T_3$ (Figs. 3.24c and 3.24d), which form the firing pulses $FP_1$ (Fig. 3.24e) for the thyristor gate $G_1$.

Fast ON/OFF detection of the thyristor valve is also obtained from this module; the ON/OFF states of valve $V_1$, i.e. $ON_1$, and the duration of extinction angle $EA_{1}$ are illustrated in Figs. 3.24f and 3.24h, respectively. The extinction angle $EA_{1}$ is measured as the interval
Panel View of Thyristor Module D:
(a) Standard Thyristor Module (Red Phase),
(b) Auxiliary Thyristor Module for Valve-current Monitoring.
Fig. 3.24 Relationship of the Typical Inverter AC/DC Voltage-waveforms (a) and (b), and the Logic Signals (c) to (h) in Thyristor Module D.
between the end of valve conduction $S_1$ (extinction) and the corresponding commutating-voltage-zero crossing $C_6$ (Fig. 3.24g), where the anode-to-cathode voltage becomes positive (Fig. 3.24b).

Some of the actual voltage-waveforms of the thyristor module D are shown in Fig. 3.25.

![Voltage-waveforms](image)

**Fig. 3.25** Typical Voltage-waveforms of Thyristor Module D Illustrated in Fig. 3.24.

$\alpha = 150^\circ$, $I_d = 0.5$ A, SCR = 10, 8 \% 2.

3.4.6 **By-pass Valve, Auxiliary Valve, and Transducers Module E-3**

3.4.6.1 **Design Features.** A block diagram of module E-3 is shown in Fig. 3.26 and its main design features are summarized below:

- **Firing/Detection Circuits.** By-pass and auxiliary valves have very similar firing and ON/OFF detection circuits to the previous thyristor module D, except that their firing pulses ($FP_7$ and $FP_8$) are single logic commands.
Block Diagram of Module E: By-Pass and Auxiliary Valves, and Transducers (Direct Current, Direct Voltage and Rate of Change of Direct Current).

N.B. 6th and 12th filters are mounted in Module G-3.
Simulation of Arcback. The simulation of arcback is carried out by an external connection of the auxiliary valve TH₈ across and in opposition to the selected valve, TH₄ to TH₇.

Direct Current $I_d$. The direct current is measured at the lower (common anode) pole of the convertor bridge. Because of the low current rating of the d.c. line, four turns of d.c. line, with negligible addition to d.c. line reactance, are used to produce a magnetic field directly proportional to the direct current. A linear-type Hall IC is placed in a narrow air-gap of ferrite core, so that complementary outputs of Hall IC, $Q₁$ and $Q₂$, are directly proportional to the direct current. The outputs of the Hall IC are then amplified to two different voltage-levels; one for supplying the $I_d$ signal to the Input/Output module A-3, and the other for driving an A/D convertor for the external processor. The Hall IC has its own d.c. supply (+5 V) regulated from +15 V. In order to avoid thermal instability of the Hall IC caused by a change of ambient temperature, the IC is sealed by silicon compound and plastic sheets.

Output Characteristics of Direct Line Current. Typical direct currents measured in the module are shown in Fig. 3.27. The output is calibrated to provide 10 V for the rated direct current (1 A). The output is linear throughout the range of interest and the tolerance is expected to be within about 0.3% of the measurement.

Rate of Change of Direct Current $dI_d/dt$. Additional windings around the ferrite core give the rate of change of direct current, which is buffered and amplified to a certain magnitude suitable for driving an A/D convertor for the external processing. Only the positive signal is derived to the predictive controller modules C.
Direct Voltage $V_{d}$. The convertor direct voltage $V_{d}$ is derived by a pair of shunt resistors connected across the d.c. terminals. The intermediate voltage of the shunt resistors is then amplified to a certain magnitude suitable for driving an A/D convertor for the external processing.

- **Smoothing Reactor.** Two smoothing reactors with equal reactance of 0.5 H are placed behind the module. Their typical voltage-current (impedance) characteristic is shown in Fig. 3.28. The small non-linearity, due to magnetic saturation of the reactor core, is representative of practical HVDC schemes. External arrangement of terminal connection enables a selection of reactance either 0.5 or 1.0 H.
Fig. 3.28 Voltage-Current Characteristic of 0.5H Smoothing Reactor:

N.B. 50 Hz supply voltage is applied to the reactor and the voltage across the reactor, $V_L$, is measured.
- 6th and 12th Harmonic Filters. Harmonic filters tuned to the 6th and 12th harmonics of the a.c. system frequency are mounted in the next module G-3. The filters consist of L, C, R components similar to the a.c. harmonic filters of modules I. Typical impedance-frequency characteristic of the 6th and 12th harmonic filters is shown in Fig. 3.29.

3.4.6.2 Panel Design and Operating Instructions. Fig. 3.30 shows the panel design of module E-3. Its operating instructions are summarized below:

- Six 1-mm sockets are used for monitoring the various outputs of the transducers.
- Four 2-mm sockets are used to simulate an arcing across one of seven valves TH₁ to TH₇.
- Due to thermal drift of the Hall IC's outputs, it is necessary to adjust the variable resistors VR7 (for pre-amp A) and VR10 (for pre-amp B). The outputs of both pre-amps A and B should be nought, if there is no direct current.

3.5 DC TRANSMISSION LINE MODULES

The model d.c. transmission line consists of a required number of Π-section modules to simulate overhead and/or cable transmission. As shown in Fig. 3.31, 10-miles cable and 50-miles overhead-line modules are individually constructed, where the line data are typically based on the Kingsnorth (38) and New Zealand (43) schemes.

3.6 FAULT ACTUATOR

In order to simulate a.c./d.c. system disturbances, a fast and duration-controllable switch or fault actuator is designed for the
Fig. 3.29 Typical Impedance-Frequency Characteristic of the 6th and 12th Harmonic Filters.
Fig. 3.30 Panel View of Module E-3.
3.6.1 Design Features

The fault actuator consists of a pair of back-to-back connected thyristors and a hinged armature circuit-breaker connected in series. A schematic block diagram is shown in Fig. 3.32 and the main design features are summarized below:

- A local switch SW1 generates a logic signal Enable-FA which can in turn either close or trip the circuit breaker CB. For example, when Enable-FA is "High", T (Toggle) Flip-Flop is enabled and S-R Flip-Flop is set, thus the CB closed.
An external logic command FA-Select is used to fire the thyristor pair, and ON/OFF level detection logic provides the status of the fault actuator. When FA-Select goes to "Low", T Flip-Flop is set and S-R Flip-Flop is reset, thus the CB tripped. At the same time the thyristors may cease conduction if the anode-to-cathode...
voltage becomes negative.

- A fault current can be monitored.

- The fault actuator can be used to simulate a valve arcback. In this case an additional switch SW2 normally short-circuits the CB, thus a short-duration pulse is adequate for the FA-Select command.

- Main circuit of the fault actuator is adequately isolated.

3.6.2 Panel Design and Operating Instructions

The panel design of the fault actuator module M is shown in Fig. 3.33. Its operating instructions are summarized below:

- Toggle Switch SW1; enables the fault actuator. It can also stop the fault by tripping the circuit breaker CB.

- Toggle Switch SW2; selects either a.c./d.c. fault (AC/DC) or arc-back (AB7). In the latter case the CB is kept short-circuited.

3.6.3 Maximum Ratings and Fault Level

Maximum ratings of the fault actuator are as follows:

- R.m.s. ON-state current; 8 A
- Peak one-cycle surge current; 80 A
- Repetitive peak forward and reverse voltages; 500 V
- Direct current breakage; 2 A
- Tripping delay of the circuit breaker CB; 2.5 ms

In order to achieve a required fault level within the maximum ratings described above, an adequate value of non-inductive resistor may be externally connected in series with the fault actuator.

The fault actuator is normally capable of simulating a single a.c. line-to-ground fault or d.c. line fault.
Fig. 3.33 Panel View of Fault Actuator Module M.

N.B. With SW1 "ON" the CB is initially closed, with SW2 at "AB7" the CB is short-circuited.
3.7 OVERALL CHARACTERISTICS OF THE CONVERTOR MODEL

The overall front view of the convertor model is shown in Fig. 3.34 together with part of the d.c. transmission line modules and the fault actuator. Typical modular constructions are shown in Fig. 3.35.

With reference to Section 2.4 basic control characteristics of the convertor model are measured, as shown in Fig. 3.36.

3.8 CONCLUSIONS

The convertor model described in this Chapter contains all the basic hardware needed for direct digital control and protection. The model also includes a predictive controller of the conventional type. A second convertor model has been provided with a conventional equidistant controller. These can be connected as a d.c. link and a fault actuator has been added which can apply duration-controlled short-circuit at either end of the link.

The complete circuit diagrams are separately documented in a convertor manual (101) which also includes d.c. power-supply circuits, edge connector configurations, and the interface circuits required to communicate with external microprocessors.
Fig. 3.34 Overall View of the Convertor Model together with Part of the DC Transmission Line Modules (Right-Bottom) and the Fault Actuator (Right-Top).

Fig. 3.35 Typical Predictive Controller Modules: From Left to Right CR3, DR3, E-3, G-3, A-3, and B-3.
Fig. 3.36 Typical Control Characteristics of the Convertor Model:
Direct Voltage $V_d$ versus Current $I_d$; $I_{ds} = 0.7 \, A$, Strong AC System.
CHAPTER 4

TRANSUDCERS

4.1 INTRODUCTION

The degree of controllability provided by static convertors is mostly determined by the speed and accuracy of information available from the transducers. In Section 4.2 two novel methods of fast ON/OFF detection of the convertor valve in particular the thyristor are described. The prospective applications of fast ON/OFF detection and its effect on convertor controllability are also discussed.

Section 4.3 very briefly discusses the fast direct current and voltage measurement required for direct digital implementations.

4.2 ON/OFF DETECTION OF CONVERTOR VALVES

4.2.1 Introduction

The prospective application of minicomputers and microprocessors to the control of static convertors can only materialize with the development of suitable transducers to extract a higher level of information from the convertor plant. Most of the information presently available consists of physical signals which, like the temperature in the human body, indicate the degree of "normality" of the system but cannot provide immediate diagnosis of the disturbance.

The discontinuous operation of the thyristor can provide useful information of the state of the system. Logical signals representing the ON and OFF commutation instants can be easily processed to provide continuous information of the conducting patterns. Deviations from the expected behaviour can then be used to detect small or large disturbances.
prior to the physical manifestation of their effect.

The large ratings of much of the convertor plant in existence justify the use of more sophisticated control and protection schemes. Moreover, as the rating of the thyristors increases, the relative cost of providing individual ON/OFF detection schemes reduces.

This section describes two detection schemes based on the current and voltage turn-on and turn-off characteristics of the devices.

4.2.2 Derivation of Conducting States from Current Detection

Fast monitoring of current buildup can be achieved by differential current detection. A practical method of deriving such information is illustrated in block diagram in Fig. 4.1.

Fig. 4.1 Block Diagram of ON/OFF Detection Circuit.

The rate of change of current through the thyristor valve is detected by means of a differentiating current transformer (DCT). In order to discriminate between ON and OFF conducting states, the output of the DCT is fed separately to two buffer, amplifier, and clipping stages. One of the outputs (Fig. 4.1e) is differentiated again prior to being driven to a one-shot stage (Fig. 4.1f). Due to the transient nature of the differential signal, it is also necessary to use an S-R Flip-Flop to provide continuous information of the ON and OFF states of the thyristor.
Fig. 4.2 shows a practical design suitable for use with a 6-pulse low-power convertor bridge of nominal 1 A and 50 V ratings such as the convertor model described in Chapter 3.

A bar conductor is used as the primary winding and a toroidal ferrite core of high permeability containing some 270 turns as the secondary winding.

The operation of the circuit is better explained with reference to the waveforms. The valve current is shown in Fig. 4.3a and the output from the DCT in Fig. 4.3b. Waveforms of Fig. 4.3c and 4.3e illustrate the clipped outputs of the ON and OFF operational amplifiers, respectively. The waveform of Fig. 4.3f shows the differentiated output of Fig. 4.3e. Finally, the positive-going edges of Fig. 4.3c and 4.3f are detected by dual one-shot IC which provides the ON of Fig. 4.3d and OFF of Fig. 4.3g signals, respectively.

A pair of NAND gates fed from the inverted outputs of the one-shot
Fig. 4.3 Corresponding Waveforms of ON/OFF Detection Circuits Shown in Figs. 4.1 and 4.2.

N.B. Delay Angle $\alpha = 10^\circ$, Direct Current $I_d = 0.8$ A.

units constitute an S-R Flip-Flop which provides information of the conducting states as shown in Fig. 4.3h.

4.2.2.1 Experimental Results. The results of ON/OFF detection tests carried out on the convertor model under various direct currents and firing delay angles are illustrated in Fig. 4.4.

The effects of varying the direct current for typical cases of rectification and inversion are illustrated in Fig. 4.4a and 4.4b, respectively. For currents higher than 0.2 A (about $\frac{1}{5}$th of the nominal), both ON and OFF valve detection is achieved within 10 $\mu$s. The existence
Fig. 4.4 Experimental Results of ON/OFF Detection Delay Shown in Fig. 4.2.
of spurious spikes in the DCT output caused by the commutation of other valves in the convertor makes faster discrimination difficult to achieve. For lower values of current, the output of the DCT reduces substantially, and the detection time increases. In fact, for very low currents (below 0.1 A), OFF detection cannot be achieved by this method.

The delay angle is shown to have a large effect in the case of OFF detection. For a direct current of 0.5 A, Fig. 4.4c indicates large delays of between 30 and 50 μs for most of the firing angle range. With very low currents (0.1 A in Fig. 4.4d), OFF detection is shown to be impossible for delay angles beyond 30°.

4.2.3 Derivation of Conducting States from Voltage Level Detection

4.2.3.1 Thyristor Firing Circuit. A description of the thyristor firing circuits is essential to the development of this method. The convertor model used as a basis for the tests is provided with the firing circuit shown in Fig. 4.5.

![Thyristor Firing Circuit](image)

Although in this case the voltage rating requires no special isolation between firing and power circuits, in practical convertors isolating pulse transformers or optically coupled circuits may have to be provided.
For generality, an optically coupled isolator has been included in the circuit of Fig. 4.5, i.e., the firing pulse is provided by a TTL circuit and transmitted by an optically coupled isolator consisting of a light-emitting diode LED1 and a silicon NPN phototransistor TR1.

In some applications there is no need for the battery E1 as the auxiliary power is obtained from the voltage across the thyristor. In the circuit of Fig. 4.5 when TR1 switches on (in about 1 μs), the battery is connected between gate and cathode through a current-limiting resistor R2, and the thyristor turns on. The purpose of transistor TR2 is to provide a negative blocking voltage at the gate during the nonconducting period, i.e., when TR1 is turned OFF, TR2 turns ON, thus providing a current path through R3 and R2 and a negative voltage between gate and cathode. The auxiliary power required in this firing circuit is very small; a 2 A·h mercury battery capacity can be used for 3000 h with the convertor model under test.

4.2.3.2 ON/OFF Level Detection. The gate-to-cathode voltage of the thyristor changes from a constant positive level to a constant negative level as the device passes from the conducting to the nonconducting state (refer to Fig. 4.9b). This fact can be used as the basis for the ON/OFF detection scheme.

Fig. 4.6 shows a modification of the firing circuit described above to provide ON/OFF detection. A bipolar transistor TR3, which is usually "ON", has been added with the base connected to the cathode of the thyristor through a resistor, R3. A diode D1 has been introduced in the path from the gate to cathode provided by resistors R2 and R4. The gate-to-cathode voltage is sensed by an N-channel silicon, depletion type, dual-insulated gate field-effect transistor TR4.

Finally, a second optically coupled isolator LED2-TR5 has been added to pass the detected information in logical form to the main control unit.
The switching states of all the transistors involved in Fig. 4.6 and the corresponding operating states of the thyristor are indicated in Table 4.1.

Fig. 4.6 Firing Circuit Combined with ON/OFF Level Detection.

TABLE 4.1 SWITCHING STATES OF TRANSISTORS IN FIG. 4.6.

<table>
<thead>
<tr>
<th>Thyristor Operation</th>
<th>States of Thyristor</th>
<th>TR1</th>
<th>TR2</th>
<th>TR3</th>
<th>TR4</th>
<th>TR5</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal Conduction</td>
<td>ON(^2)</td>
<td>ON(^1)</td>
<td>OFF(^2)</td>
<td>ON(^3)</td>
<td>ON(^4)</td>
<td>ON</td>
</tr>
<tr>
<td>Commutation</td>
<td>ON</td>
<td>OFF(^1)</td>
<td>ON(^2)</td>
<td>ON(^3)</td>
<td>ON(^4)</td>
<td>ON</td>
</tr>
<tr>
<td>Non-Conduction</td>
<td>OFF(^3)</td>
<td>OFF(^1)</td>
<td>ON(^2)</td>
<td>ON(^3)</td>
<td>OFF(^4)</td>
<td>OFF</td>
</tr>
<tr>
<td>Breakdown</td>
<td>ON</td>
<td>OFF</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
</tr>
<tr>
<td>Failure to Fire</td>
<td>OFF</td>
<td>ON(^1)</td>
<td>OFF(^2)</td>
<td>OFF(^2)</td>
<td>(OFF)</td>
<td>OFF</td>
</tr>
</tbody>
</table>

"ON" if TR3 is ON.

In each case, the decisive transistor state from the point of view of the ON/OFF detection has been underlined. The superscript numbers indicate a time sequence of the operating states. Transistor TR3 was
found necessary to prevent faulty indication. Without it, in the event of a failure to fire, the current through TR1 and R4 would have maintained a positive voltage between gate and cathode. With TR3 in, no current flows through R3 in such case, and, as a result, both TR3 and TR4 will turn off.

4.2.3.3 Logic Circuit for the ON/OFF Level Detection. Initially, a simple logic circuit was designed, shown in Fig. 4.7, for the detection of ON/OFF states.

Fig. 4.7 A Simple Logic Circuit for ON/OFF Level Detection.

The driver stage consisted of transistor TR6, resistors R8 and R9, and a diode D1. This scheme operated on direct information of thyristor conduction. However, the prolonged logical transition from LED2 to TR5 caused unacceptable delays (between 20 and 40 μs) in the case of OFF detection with very low values of direct current.

An improved version for faster OFF detection using an operational amplifier is shown in Fig. 4.8.
Fig. 4.8 An Improved Logic Circuit for ON/OFF Level Detection.

In this case the negative-going edge of the TR5, emitter-to-ground voltage is level-detected at its earliest stage.

Logical waveforms corresponding to the circuits of Figs. 4.6 and 4.8 are illustrated in Fig. 4.9.

If the ON/OFF signals are combined with the commutating-voltage-zero crossings signals, a simple S-R Flip-Flop can provide sufficient logical information to form the extinction angle of each thyristor.

4.2.3.4 Experimental Results. The results of tests carried out for the voltage level ON/OFF detection scheme are summarized in Fig. 4.10. These show a considerable improvement over the differentiating current transformer scheme results of Fig. 4.4.
ON and OFF detections are now possible over the whole range of direct current in about 3 and 8 µs, respectively, with a slight further delay in the case of OFF detection for very low values of current.

Considering that \(1^\circ\) of 50 and 60 Hz frequencies corresponds to 46.3 and 55.6 µs, respectively, the ON/OFF level detection scheme proposed provides the necessary information in a small fraction of one degree which is quite acceptable for all practical purposes.

It must be added that the detection delay is partly caused by the optically coupled isolator used. There are in the market faster units which could cut the detection delay by several microseconds.
Fig. 4.10 ON/OFF Detection Delay by Level Detection Circuits in Figs. 4.6 and 4.8.

4.2.4 Prospective Applications of the ON/OFF Level Detection

4.2.4.1 HVDC Thyristor Valves. A modern HVDC thyristor valve typically consists of 100 to 180 thyristors connected in series. With the ON/OFF level detection devised for each thyristor, the following
valve performances can be achieved.

- **Valve ON/OFF States.** ON/OFF states of the HVDC thyristor valve can be defined as a period where all of the thyristors are either conducting or non-conducting simultaneously. However, minor discrepancies of the transition from OFF to ON and ON to OFF states exist in practice among series-connected thyristors within the valve.\(^{(103)}\) Therefore, in order to derive the valve ON/OFF states, the ON/OFF signals of each thyristor (Fig. 4.9g) should be processed with an "AND" gate; the breakdown of a thyristor is indicated by a continuous ON state.

- **Extinction Angle (EA) Measurement.** Present methods of EA measurement are based on either voltage across the valve or alternating current on the valve side of converter transformers.\(^{(28,35)}\)\(^{(36)}\) The former is limited to normal inverter operation only and the latter has similar disadvantages as described in Section 4.2.2. Based on the ON/OFF level detection, however, fast EA measurement is achieved over the whole range of firing delay angles and direct currents.

- **Valve Protection.** Thyristor valves have very limited overcurrent capabilities over a certain period of time.\(^{(104,105)}\) Thus primary protection of each valve can be realized by directly measuring both valve conducting-period and magnitude of current.

- **Thyristor Monitoring.** From the early stages of thyristor-valve developments, the anode-to-cathode voltage of each thyristor is monitored for maintenance purposes.\(^{(15,102,103)}\) Moreover, with the quality control of modern thyristors, their modular design and preventive maintenance,\(^{(105,106)}\) the level of thyristor redundancy can be effectively reduced to 3 to 4% per valve.\(^{(82,107)}\) In the recent Nelson River Bipole-two\(^{(108)}\) and Skagerrak\(^{(82,109)}\)
1 1 8

schemes, intelligent redundancy and firing controls are achieved, i.e., depending on a number of the defective thyristors appropriate protection is taking place. The ON/OFF detection scheme proposed can provide high level information for these purposes.

4.2.4.2 Current-zero Detection in Industrial Convertors. The expansion of power electronics has been particularly manifested at the industrial level. In applications such as the reversing d.c. machine drive shown in Fig. 4.11, fast and reliable load-current-zero detection is of great importance to rapidly change over firing controls from one bridge to another. Present practice of the current-zero detection employs auxiliary diodes and/or thyristor in the load-current path.\(110,111\)

![Diagram of Three-phase Supply](image)

Fig. 4.11 Antiparalleled Industrial Convertors with Load Current-zero Detector.

N.B. Four quadrant operation without circulating current.

With the ON/OFF level detection devised for each thyristor, however, fast and reliable diagnosis of the bridge status can be directly obtained at a low power requirement on the detection components over the whole load-current range, and within self-contained bridge environments.
Moreover, if power transistors are used for the convertor bridges instead, (110, 112) the current-zero detector of Fig. 4.11 could consist of two back-to-back connected thyristors similar to the fault actuator described in Section 3.6.

4.2.5 Effects on Convertor Controllability

Most of the present static convertor plants use firing angle control schemes based on analogue techniques. Even under perfectly normal conditions, the individual firing angles cannot be accurately implemented, and variations of a few degrees are common.

With the use of fast ON/OFF detection schemes, it should be possible to introduce more accurate control of the firing instants by means of special-purpose digital hardware.

The higher level of information provided by the proposed monitoring scheme can also be used to improve the dynamic behaviour of the convertor plant during normal variations of system parameters. The information processing can be done by software, using minicomputers or microprocessors.

Moreover, the simultaneous availability of the conducting states of the various thyristors involved in the convertor plant, when processed together with other logical signals such as commutating-voltage-zero crossings, firing instants, etc., provides an accurate diagnosis of abnormal operating conditions.

4.2.6 Conclusions

Two methods for the ON/OFF detection of convertor valves have been described. The method based on the rate of change of current is not considered to be sufficiently fast for applications involving accurate direct digital control and protection; moreover, the OFF detection is unreliable at very low currents in this case. On the other hand, the method based on gate-to-cathode voltage level detection of the
thyristor provides fast and reliable ON/OFF information at all power levels and control angles. Present firing circuits can be easily modified to include the additional electronic components to provide ON/OFF detection. The nature of the information available meets the requirements of digital controllability in both HVDC and industrial applications.

4.3 DIRECT CURRENT AND VOLTAGE MEASUREMENT

From the early stages of HVDC applications transductor-type direct current transformers (DC CT) have been commonly used.\(^{(47)}\) Although the DC CT is suitable for rugged outdoor environments, current notches and inaccuracy caused by transductor nonlinearity are far from ideal for digital implementations. Among the proposed alternatives is the application of the Hall effect which can provide continuous and instantaneous measurement of the direct current or power with good linearity.\(^{(113,114)}\) In this case a rate of change of direct current \(\frac{dI_d}{dt}\) can be directly derived from the direct current measured.

The Hall IC has been used in the low-power convertor model (See Sections 3.3.7 and 3.4.6). Under laboratory environments an accuracy of 0.3% has been achieved, and 0.5% is found typical elsewhere.\(^{(115)}\) Moreover, some latest developments of integrated circuits are attractive for this application,\(^{(116)}\) e.g., the Texas Instruments’ Linear-type Hall IC TL173 employs voltage and current regulators as well as a precision amplifier. However, for practical HVDC applications good consideration should be given to the temperature stability, strain sensitivity, isolated power supply, etc.

Although the direct voltage transducer of the convertor model provides instantaneous measurement of the direct voltage \(V_d\), there is some time-delay in the response of the resistance-type voltage dividers. The time constant of the voltage divider presently used is about 50 to 100 ms.\(^{(47)}\)
CHAPTER 5

FAULT SIMULATION AND DATA ACQUISITION

5.1 INTRODUCTION

As reviewed in Chapter 2, the distinctive characteristics of HVDC thyristor valves have a direct effect on the convertor-station configurations and operations. Although comprehensive analysis of the convertor faults and their development are well documented in the literature, a fresh consideration is required to assess the behaviour of recent thyristor convertors under various faults encountered in practice. This is a specially demanding task because of the prospective implementations of direct digital convertor-fault detection and protection which require exact diagnosis of the convertor behaviour. In present protection schemes the 6-pulse bridge or bridges are regarded as a "black box", and the protection philosophy is solely based on external information such as the direct line current, alternating currents on the valve side of convertor transformers, etc.

The normal convertor operation is briefly discussed in Section 5.2, and various HVDC faults are analysed and classified in Section 5.3. This information is used in the remaining Sections for the development of a fault simulation scheme.

Section 5.4 describes two fault simulators based on hardwired logic, i.e. a comprehensive digital fault simulator designed for the evaluation of a direct digital control scheme and a simple fault simulator designed for the convertor model.

Recent developments in the microelectronics technology provide both adequate speed and the flexibility required for a comprehensive
fault simulator and data acquisition. Overall design considerations and the interactive role of microprocessor hardware and software are described in Section 5.5. A hardware design of a multimicroprocessor-based system is described in Section 5.6. The software development required for the fault simulation and data acquisition schemes is described in Sections 5.7 and 5.8, respectively. Finally some typical test results on the convertor model are presented in Section 5.9.

5.2 NORMAL HVDC CONVERTOR OPERATIONS

5.2.1 HVDC System Representation for Analysis

A typical 12-pulse thyristor convertor-station is represented in Fig. 5.1. The 6-pulse bridge circuit shown in Fig. 5.2 illustrates the notation adopted for analysis. In the Figure, the a.c. voltage source, assumed balanced and sinusoidal, is connected in series with balanced leakage inductance $L$, the smoothing inductance $L_d$ is assumed infinitely large and the valves forward resistance is ignored. The anode-to-cathode voltage of valve $V_i$ is denoted as the valve voltage $v_i$ which is normally "positive" when the valve fires and "negative" when the valve ceases conducting.

In the following description the commutating-voltage-zero crossing $C_i$ and/or valve $V_i$ are used as a reference for clarity. However, the reference can be made generally applicable to any crossing $C_i$ and valve $V_i$ in a cyclic manner.

5.2.2 Typical Rectifier and Inverter

Typical steady-state rectifier and inverter operations are schematically illustrated in Figs. 5.3 and 5.4, respectively. Regardless of the mode of convertor operation, the sequential valve firings indicated in the Figures are characteristic of normal convertor behaviour, with the top and bottom halves of the bridge valves being
Fig. 5.1  Schematic Configuration of Unit 12-pulse Thyristor Convertor under Main Consideration.

Fig. 5.2  Schematic Circuit Diagram of 6-pulse Bridge for Analysis.
Fig. 5.3 Typical 6-pulse Rectifier Operation:
(a) Positive and Negative Direct Voltages with respect to the Transformer Neutral,
(b) Direct Bridge Voltage $v_d$, and Voltage across Valve 1,
(c),(d) Valve Currents $i_1$ to $i_6$,
(e) AC Line Current of Phase $a$. 
Fig. 5.4  Typical 6-pulse Inverter Operation:
(a) Positive and Negative Direct Voltage with respect
to the Transformer Neutral,
(b) Voltage across Valve 1, and Direct Bridge Voltage $v_d$,
(c), (d) Valve Currents $i_1$ to $i_6$,
(e) AC Line Current of Phase a.
alternatively responsible for the phase-to-phase current commutations.

A comprehensive steady-state analysis of the convertor bridge is given by Kimbark.\(^{(47)}\)

5.2.3 Start-up

A typical rectifier start-up operation is schematically illustrated in Fig. 5.5, where the direct voltage is slowly raised by gradually retarding the minimum delay angle (MDA) limits. Conventionally all of the firing pulses are deblocked simultaneously at, for example, instant \(C\) in Fig. 5.5. In this case convertor valves \(V_1\) and \(V_6\) both start conducting at \(C\).

However, when sequential valve deblocking is implemented, one valve precedes conducting because the R-C dampers and resistance voltage dividers installed across the thyristors provide "positive" valve voltage, and charging current due to stray capacitance may well exceed the holding current of the thyristors. For example, starting from valve \(V_6\) (instant \(Z\) in Fig. 5.5), each valve is deblocked in sequence from the corresponding voltage-zero crossing on, thus at \(B\) valve \(V_6\) starts conducting as the hatched area indicates. It should be noted that the difference of the two deblocking methods, i.e. either simultaneous or sequential, only becomes apparent when ON/OFF signal detection is provided.

Simultaneously with the rectifier start-up, a by-pass pair is fired at the inverter end to provide a current path as soon as the direct voltage appears at the inverter's d.c. busbar. After a time delay, which is mainly determined by the rectifier start-up procedure and the d.c.-line time constant, normal inversion can resume. Typical inverter start-up operation is schematically illustrated in Fig. 5.6. For example, when all of the firing pulses are simultaneously deblocked at instant \(A\) in Fig. 5.6, valve voltage \(v_5\) is "negative" at \(B\) and normal
Fig. 5.5 Schematic Diagram of a Rectifier Start-up:
(a) Positive and Negative Direct Voltage with respect to the Transformer Neutral,
(b) Direct Bridge Voltage $v_d$,
(c),(d) Valve Currents $i_1$ to $i_6$ with ON1 and ON6 Signals.
Fig. 5.6 Schematic Diagram of an Inverter Start-up:
(a) Positive and Negative Direct Voltages with respect to the Transformer Neutral,
(b) Direct Bridge Voltage $v_d$,
(c), (d) Valve Currents $i_1$ to $i_6$. 

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**Diagram Description**

- **Positive and Negative Direct Voltages (a)**
  - $e_a$, $e_b$, $e_c$ with $e_a$ and $e_b$ shown.
  - Voltages $e_{ab}$ and $e_{ac}$ are distinguished.
  - Transformer neutral labelled $N$.
  - Voltages $v_{ab}$ and $v_{ac}$ shown.
  - Bridge voltage $v_d$ indicated.

- **Valve Currents (c), (d)**
  - Currents $i_1$ to $i_6$ shown.
  - Valve currents $i_d$ and $i_a$ highlighted.
  - Phase labeling $A$, $B$, $C$.

---

**Technical Details**

- The diagram illustrates the start-up process of an inverter, focusing on direct voltages and currents.
- It includes key components such as the transformer neutral and the bridge voltage.
- Valve currents are analyzed for phases $A$, $B$, and $C$.
- The schematic provides a comprehensive view of the inverter's operation during start-up.
commutation takes place at C, H, and so on. At instant F valve \( V_4 \) is already conducting.

When sequential valve deblocking is implemented, Fig. 5.6 can be interpreted such that the valve deblocking starts at instant \( Z \) for valve \( V_6 \) while valves \( V_1 \) and \( V_4 \) carry the direct current.

5.2.4 Power Reversal in Two-Terminal Systems

Ideal power reversal is schematically illustrated in Fig. 5.7, where the voltage polarity is gradually reversed under a firing angle control in two-terminal systems. Although the fastest voltage-polarity reversal can be achieved by simultaneous valve blocking and subsequent deblocking by digital means,\(^{78}\) retaining the normal firing sequence of convertor is desirable since the same convertor fault detection and protection scheme can be applied during the power reversal, and a firing angle control over the direct voltage is more flexible when a long overhead transmission or cable line is involved in the power reversal. With the availability of general purpose microprocessors, it is feasible to design a controller which is capable of altering the firing delay angles at a maximum rate of 20° to 30° per valve firing.\(^{91}\)

5.2.5 Shut-down

A convertor shut-down involves the transfer of the direct current to by-pass pairs. Temporary convertor by-passing is required during severe a.c. faults, e.g. 50% commutating-voltage reduction, as the firing circuitry power is derived from the anode-to-cathode voltage of a thyristor.\(^{117,118}\) In this Section 5.2.5 two basic microprocessor applications are discussed.

5.2.5.1 Sequential Convertor Shut-down. A typical sequential inverter shut-down is schematically illustrated in Fig. 5.8, where the shut-down sequence is carried out with reference to the commutating-voltage-zero crossings. For example, at instant A an inverter shut-down
Fig. 5.7 Schematic Diagram of Ideal Power Reversal in Two-Terminal Systems.
Fig. 5.8 Schematic Diagram of a Sequential Inverter Shut-down:
(a) Positive and Negative Direct Voltages with respect to the Transformer Neutral,
(b) Direct Bridge Voltage $v_d$,
(c) to (h) Valve Currents $i_1$ to $i_6$. 

(a) Positive and Negative Direct Voltages with respect to the Transformer Neutral,
request is recognized by a microprocessor and at instants D and G valves $V_2$ and $V_3$ are respectively blocked. Although valve $V_4$ can be fired at instant G as the thick broken-lines in Fig. 5.8 indicate, this is avoided because, depending on the firing delay and overlap angles, a three-phase short-circuit may develop due to four conducting valves. Thus at instant K valves $V_4$ and $V_1$ are fired (Note that at K valve $V_1$ is normally already conducting), and commutation from valve $V_6$ to valve $V_4$ completes at L. At instants N and Q valves $V_5$ and $V_6$ are respectively blocked. A possible delayed shut-down is illustrated by the thick dotted-lines from K to O. In order to avoid commutation failures during the convertor shut-down the nominal extinction angle (EA) setting should be temporarily increased.

The same sequential blocking can be applied to the rectifier as schematically illustrated in Fig. 5.9. The hatched area in Fig. 5.9b shows negative bridge voltage $v_d$ before valve $V_6$ commutates back to valve $V_4$ between instants I and J. The simplicity of this approach suits most HVDC transmission configurations. However, for back-to-back connected convertors, it may be preferable to fire valves $V_4$ and $V_1$ at instant $F$ as the thick broken-lines indicate. A possible delayed shut-down is also illustrated by the thick dotted-lines from I to L with increased negative bridge voltage.

Although the sequential method achieves the same valve ON/OFF sequence in any mode of convertor operation, it can take as much as half-a-cycle after the by-passing requested. This may be considered too slow with back-to-back connected convertors.

5.2.5.2 Fast Convertor Shut-down Based on Conducting States of Valves. A sequence of simultaneous blocking and delayed by-pass-pair firings based on hard-wired logic has been proposed for rectifier and inverter operation. The proposed sequence,
Fig. 5.9 Schematic Diagram of a Sequential Rectifier Shut-down: Unified Approach.
however, lacks flexibility regarding the convertor operating modes, and may only be applicable to strong a.c. systems. Presumably the delayed by-pass-pair firings, i.e. 1 ms after the by-pass request, is imposed so that the last commutation may complete within this time. A principle of by-pass-pair selections based on valve ON/OFF information has been proposed for normal and abnormal convertor operations.\(^{56}\)

Fresh consideration is given here involving microprocessors and taking into account unavoidable ON/OFF detection delay and the time required for serial processing.

Typical operation of a microprocessor-based inverter shut-down is schematically illustrated in Figs. 5.10 and 5.11. For example, at or a little later than instant Z in Fig. 5.10, the latest valve ON/OFF states are read and the non-conducting valves \(V_1', V_2', V_5\) and \(V_6\) are blocked. However, allowing some ON/OFF detection and processing delay, the incoming valve \(V_5\) can not be blocked in time. Hence, at instant A, three valves \(V_3', V_4\) and \(V_5\) are conducting. Then, for example, later at instant C the selected by-pass pair, i.e. valves \(V_2\) and \(V_5'\), is fired and simultaneously the rest of valves, i.e. including valves \(V_3\) and \(V_4'\), are blocked. At instants B and E, normal firing of valves \(V_6\) and \(V_1\) is blocked, respectively. In order to retain generality, some valves are successively blocked twice, but, the second blocking has no effect since the blocking signal is normally latched. Delayed by-pass-pair firing is also possible at instant F as the thick dotted-lines indicate in the Figure.

The same sequence can be applied to normal inverter operation, which results in faster by-passing. For example, in Fig. 5.11, the non-conducting valves \(V_1', V_5\) and \(V_6\) are blocked after instant Z, and later at instant A the selected by-pass pair, i.e. valves \(V_1\) and \(V_4'\), is fired and simultaneously the rest of valves are blocked.
Fast Inverter Shut-down Involving Normal Commutation at $C_1$:
(a) Positive and Negative Direct Voltages with respect to the Transformer Neutral,
(b) Direct Bridge Voltage $V_d$,
(c) to (h) Valve Currents $i_1$ to $i_6$.

Fig. 5.10

Fast Inverter Shut-down Based on Conducting States of Valves:

Fig. 5.11
Moreover, the same sequence can be equally applied to rectifier operation. For example, in the previous Fig. 5.9, if the non-conducting valves $V_2$, $V_3$, $V_4$ and possibly $V_5$ are blocked after instant B but before E, then at instants F, I, or K the selected by-pass pair, i.e. valves $V_1$ and $V_4$, is fired and simultaneously the rest of valves blocked.

![Diagram](image)

**Fig. 5.12** General Flowcharts of Fast Converter Shut-down Based on Conducting States of Valves:
(a) Shut-down Request Subroutine,
(b) By-pass Enforcement Subroutine.

General flowcharts are shown in Fig. 5.12. It is assumed that the data-word containing the valve ON/OFF states is promptly updated whenever any valve turns on or off. Initially two parameters or
control flags SHUT-DOWN and BY-PASS are reset to "False". When a convertor shut-down is requested, the flag SHUT-DOWN is set to "True" and appropriate non-conducting valves are blocked immediately. By setting the flag BY-PASS to "True", the following by-pass enforcement subroutine (Fig. 5.12b) is enabled. This arrangement ensures that Fig. 5.12b always follows after Fig. 5.12a. Thus, if the bridge is not by-passing as initially this must be (Fig. 5.12a), a subroutine is called so that the control flag SHUT-DOWN is reset to "False" and the criteria in look-up Table 5.1 are applied, i.e. only if two successive valves $V_i$ and $V_{i+1}$ are conducting within the crossing zones (thick blocks in Table 5.1), valves $V_{i+4}$ and $V_{i+1}$ are fired and simultaneously the rest of valves blocked. (A selection of the by-pass pair can be complementary, i.e. in Table 5.1 "Fire $V_{i+3}$ and $V_i$" instead of "Fire $V_{i+4}$ and $V_{i+1}$." If valve $V_{i+4}$ is defective, valve $V_{i+3}$ can be used.)

**TABLE 5.1 CRITERIA FOR FAST CONVERTOR SHUT-DOWN BASED ON CONDUCTING STATES OF CONVERTOR VALVES.**

<table>
<thead>
<tr>
<th>Two Conducting Valves</th>
<th>Commutating-voltage-zero Crossings</th>
<th>wt</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_1$ and $V_2$</td>
<td>$C_1$</td>
<td></td>
</tr>
<tr>
<td>$V_2$ and $V_3$</td>
<td>$C_2$</td>
<td></td>
</tr>
<tr>
<td>$V_3$ and $V_4$</td>
<td>$C_3$</td>
<td></td>
</tr>
<tr>
<td>$V_4$ and $V_5$</td>
<td>$C_4$</td>
<td></td>
</tr>
<tr>
<td>$V_5$ and $V_6$</td>
<td>$C_5$</td>
<td></td>
</tr>
<tr>
<td>$V_6$ and $V_1$</td>
<td>$C_6$</td>
<td></td>
</tr>
</tbody>
</table>

N.B. For complementary Table substitute "Fire $V_{i+4}$ and $V_{i+1}$" for "Fire $V_{i+3}$ and $V_i$."
In practice, the shut-down request subroutine Fig. 5.12a should be a part or whole of an interrupt service routine which attains immediate processing. On the other hand the by-pass enforcement subroutine Fig. 5.12b can be included in an interrupt service routine which is processed at each commutating-voltage-zero crossing, i.e. at about 30° intervals with 12-pulse bridges. Faster by-passing can be achieved with shorter intervals, e.g. 5° or 10°. (Note that mainly for explanation purposes Figs. 5.10 and 5.11 are drawn based on commutating-voltage-zero crossings.) The shortest interval is limited by a maximum valve ON/OFF detection delay and the time required for updating the ON/OFF information, e.g. about 10° in all. However, maximum intervals should not exceed successive crossing intervals of a 6-pulse bridge, i.e. about 60°.

It will be discussed in Section 5.3.2.3 that the above arrangement and Table 5.1 also serve to achieve the required by-passing in case of a failure of initial shut-down attempt(s) due to an incidental commutation failure with weak receiving a.c. systems.

5.3 CLASSIFICATION OF FAULTS

5.3.1 Introduction

Classification of HVDC faults falls into three major areas, i.e. convertor faults, d.c. line faults, and a.c. faults. From a viewpoint of convertor operation, both d.c. line and a.c. faults are regarded as "external" faults, which may be causes or effects of convertor faults. Therefore, a.c. faults practically include near or remote faults, i.e. near or beyond convertor transformers and a.c. busbar(s).

Convertor faults occur sometimes in the valves themselves due to malfunctions of the valves and/or their associated equipment. Depending on whether the cause is temporary or permanent, these faults may clear
themselves in one cycle (single faults) or persist for several or many cycles (repetitive or permanent faults). Although some faults seldom occur, most of the faults are of great importance to a design engineer. With modern thyristor convertors the most frequent and significant convertor faults are commutation failures in an inverter.

In the following graphic presentation, single fault is treated as a unit of fault, and persistent faults are indicated by thick dotted-lines. In order to show the commutation process clearly, overlap angles are slightly exaggerated.

5.3.2 Sequential Convertor Faults

5.3.2.1. Misfire. Misfire is the failure to fire a valve during a scheduled firing period, i.e., when the valve voltage is normally "positive" and sufficiently large to fire the series-connected thyristors simultaneously. It may be caused by various defects in the control and firing equipment, by erroneous blocking and by commutating-voltage reduction due to transient overvoltages or voltage disturbances; particularly in the receiving a.c. system. For simplicity, misfire of a valve $V_i$ is denoted as $MF_i$.

(i) Single Misfire in Rectifier. Fig. 5.13 schematically illustrates a single misfire ($MF_1$) in a rectifier. At instant $B$, valve $V_1$ fails to conduct, thus valve $V_5$ goes on conducting. Between instants $C$ and $D$ the direct current $I_d$ commutates from valve $V_6$ to valve $V_2$, and then between instants $E$ and $F$ the current commutates back from valve $V_5$ to valve $V_3$. Normal firing sequence is resumed after instant $G$. If the cause of misfire persists, misfire $MF_1$ repeats from instant $H$ as the thick dotted-lines indicate in the Figure. When ON/OFF signal detection is provided, an abnormal firing sequence can be recorded at instants
Fig. 5.13 Single Misfire of Valve V₁ in Typical Rectifier.
C, D, E and F, i.e., four times per single misfire. However, since the valve voltage $v_1$ (thick broken-line in Fig. 5.13b) is sufficiently "positive" between B and E, the anode-to-cathode voltage of each thyristor is usually monitored and, if required, an additional firing pulse may be sent to the thyristor(s).\(^{(103,108)}\) This arrangement also assists the rectifier to recover from valve-current extinction due to transient over-voltages entering into the upper bridge.\(^{(104,119,120)}\)

(ii) Single Misfire in Inverter. Fig. 5.14 schematically illustrates a single misfire (MF\(_1\)) in an inverter. At instant $A$, valve $V_1$ fails to conduct and valve $V_5$ goes on conducting because at $E$ valve voltage $v_3$ is "negative", thus valve $V_3$ cannot be fired. At instant $H$, valve $V_5$ is already conducting. If the cause of misfire persists, misfire MF\(_1\) repeats from instant $I$ as the thick dotted-lines indicate. Unlike the misfire in rectifier, the valve voltage $v_1$ (thick broken-line in Fig. 5.14b) is gradually decreasing at a time of scheduled firing (instant $A$). Thus, upon commutating-voltage reduction at the inverter, normal firing or re-firing may not succeed. In practice, the direct current $I_d$ transiently increases after the occurrence of inverter misfire because of the simultaneous conduction of valves $V_2$ and $V_5$ (i.e., by-passing) between instants $D$ and $F$.\(^{(84,117,121)}\)

(iii) Double-Successive Misfire in Rectifier. Fig. 5.15 schematically illustrates double-successive misfire (MF\(_1\) and MF\(_2\)) in the rectifier. At instants B and C, valves $V_1$ and $V_2$ fail to conduct, respectively. If the cause of misfire persists, misfire MF\(_1\) and MF\(_2\) repeat from instant $H$ as the thick dotted-lines indicate in the Figure. If valve $V_3$ further fails to conduct (triple-successive misfire MF\(_1\), MF\(_2\) and MF\(_3\)), negative bridge
Fig. 5.14 Single Misfire of Valve V1 in Typical Inverter.
Fig. 5.15 Double-Successive Misfire of Valves $V_1$ and $V_2$ in Typical Rectifier.
voltage $v_d$ prolongs to instant $F$. If more than four valves fail to conduct successively or the bridge is erroneously blocked, the whole commutating voltage $e_{cb}$ (BY) appears across the bridge as the thick broken-line indicates in Fig. 5.15b.

(iv) **Double-Successive Misfire in Inverter.** Fig. 5.16 schematically illustrates double-successive misfire ($MF_1$ and $MF_2$) in the inverter. Following the first misfire $MF_1$ at instant $A$, valve $V_2$ may also fail to conduct at $B$ because of the similarly decreasing valve voltage $v_2$ as the thick broken-line indicates in Fig. 5.16b. At instants $C$ and $D$ valves $V_3$ and $V_4$ can not be fired, respectively, because valve voltages $v_3$ and $v_4$ are "negative". At instants $E$ and $F$ valves $V_5$ and $V_6$ are already conducting, respectively. If the cause of misfire persists or the bridge is erroneously blocked, the whole commutating voltage $e_{cb}$ (BY) continues appearing across the bridge as the thick dotted-lines indicate in the Figure.

(v) **Double-Not-Successive Misfire in Rectifier.** With respect to the previous Fig. 5.13, if valve $V_3$ fails to conduct at instant $E$, the bridge continues by-passing until instant $G$. If valve $V_4$ fails to conduct at instant $G$ instead, valves $V_2$ and $V_5$ by-pass the bridge again, i.e., positive bridge voltage appears intermittently in every half cycle.

(vi) **Double-Not-Successive Misfire in Inverter.** With respect to the previous Fig. 5.14, if valve $V_4$ fails to conduct at instant $F$, the bridge continues by-passing until instant $I$. In this case the bridge may be kept by-passing as far as the cause of misfire $MF_1$ and $MF_4$ persists. However, misfire $MF_3$ at instant $E$ is insignificant, and misfire $MF_5$ can not occur at instant $H$ since valve $V_5$ is already conducting.
Fig. 5.16 Double-Successive Misfire of Valves $V_1$ and $V_2$ in Typical Inverter.
5.3.2.2. **Firethrough.** Firethrough is the failure to block a valve during a scheduled blocking period, i.e., when the valve voltage is sufficiently "positive". It may be caused by various defects in the control and firing equipment, by erroneous firing, and by transient overvoltages exceeding thyristor-valve ratings; particularly at the inverter. For simplicity, firethrough of a valve $V_i$ is denoted as $FT_i$.

(i) **Firethrough in Rectifier.** Fig. 5.17 schematically illustrates single firethrough ($FT_1$) in a rectifier. As the valve voltage $v_i$ is indicated by the thick broken-line in Fig. 5.17b, valve $V_1$ fires through as soon as the valve voltage becomes sufficiently "positive" at instant $A$, i.e. before the scheduled firing instant $B$. If the cause of firethrough persists, firethrough $FT_1$ repeats from instant $D$ as the thick dotted-lines indicate in the Figure. In this case the remaining valves become operating at some increased delay angles, e.g. $20^\circ$, because of the direct current controller installed. The defective valve $V_1$ conducts longer than normal, and the preceding valve $V_5$ shorter. If more valves fire through, the bridge may eventually become an uncontrolled rectifier.

(ii) **Single Firethrough in Inverter.** Fig. 5.18 schematically illustrates an example of single inverter firethrough ($FT_1$) at instant $B$. If the cause of firethrough is repetitive, e.g. due to noise in the firing circuit, firethrough $FT_1$ recurs at instant $J$. As the valve voltage $v_1$ is indicated by the thick broken-line in Fig. 5.18b, however, valve $V_1$ fires through at any time after instant $A$, but before the scheduled firing instant $F$. If the cause of such firethrough persists, permanent firethrough $FT_1$ occurs once per cycle after instant $G$ as the thick dotted-lines indicate in the Figure. (This firethrough can be the case when...
Fig. 5.17 Single Firethrough of Valve $V_1$ in Typical Rectifier.
Fig. 5.18 Single Firethrough of Valve V1 in Typical Inverter.
valve $V_1$ fires through soon after instant A instead of B.) In fact, such firethrough FT$_1$ after instant G (or A) is equivalent to a commutation failure from valve $V_1$ to valve $V_3$, although the cause is different. (123)

(iii) **Double-Successive Firethrough in Inverter.** Fig. 5.19 schematically illustrates an example of double-successive inverter firethrough (FT$_1$ and FT$_2$) at instant B. Valve voltage $v_2$ becomes "positive" at instant A. Valves $V_1$ and $V_2$ are already conducting at instants F and G, respectively. If the cause of firethrough is repetitive, firethrough FT$_1$ and FT$_2$ recurs at J. If the cause persists, however, permanent firethrough FT$_1$ and FT$_2$ occurs once per cycle after instants H and I, respectively, as the thick dotted-lines indicate in the Figure.

5.3.2.3 **Commutation Failure.** A commutation failure is the commonest misoperation of an inverter. It results in either premature extinction of the outgoing valve due to a lack of sufficient de-ionization time or incomplete transfer of the direct current before the commutating voltage becomes "positive". Thus, the incoming valve fails to take over the direct current. A true commutation failure is not due to any misoperation of the valves involved, but to a.c./d.c. disturbances outside the bridge or to inadequate control of the firing time. It may be caused by commutating-voltage reduction, increased direct current, late firing, or a combination of these.

In the following analysis, a commutation failure is assumed to result from late firing of the incoming valve, which is equivalent to early appearance of the commutating-voltage-zero crossing. Further for simplicity, a commutation failure from valve $V_i$ to valve $V_{i+2}$ is denoted as CP$_{i,i+2}$. 
Fig. 5.19 Double-Successive Firethrough of Valves $V_1$ and $V_2$ in Typical Inverter.
(i) Single Commutation Failure. Fig. 5.20 schematically illustrates a single commutation failure (CF\textsubscript{1,3}). Valve V\textsubscript{3} is fired at instant B instead of normal firing instant A. Since the commutating voltage $e_{ab}$ (RY) becomes positive after instant C, the incoming valve V\textsubscript{3} eventually ceases conducting at E, and the direct current commutates back to the preceding valve V\textsubscript{1}. (Valve V\textsubscript{1} may cease conducting shortly before C. In this case valve V\textsubscript{3} temporarily carries the full direct current across over instant C.) When valve V\textsubscript{4} is fired at instant D, three-phase short-circuit develops until E, because of the four conducting valves V\textsubscript{1} to V\textsubscript{4}. However, since the commutating voltage $e_{ac}$ (RB) is normally negative at instant D, the preceding valve V\textsubscript{2} can complete to transfer the direct current to the incoming valve V\textsubscript{4} at instant F. Valve V\textsubscript{5} can not be fired at instant G because valve voltage $v_{5}^{d}$ is "negative". The inverter bridge is completely by-passed between instants F and H, i.e., there are no alternating currents through convertor transformers and the direct current increases in practice. However, after normal commutation from valve V\textsubscript{4} to valve V\textsubscript{6} between instants H and I, the bridge voltage $v_{d}^{d}$ is gradually re-established. At instant J valve V\textsubscript{1} is already conducting. If the cause of commutation failure persists in a cyclic manner, the commutation failure CF\textsubscript{1,3} may recur after instant K, as the thick dotted-lines indicate in the Figure. In practice, other types of commutation failure are likely to occur, because of the voltage and current disturbances caused by the initial failure.

(ii) Double-Successive Commutation Failure. Fig. 5.21 schematically illustrates a double-successive commutation failure (CF\textsubscript{1,3} and CF\textsubscript{2,4}). If the cause of the initial commutation
Fig. 5.20 Single Commutation Failure from Valve V1 to Valve V3 in Typical Inverter.
Double-Successive Commutation Failure from Valve $V_1$ to Valve $V_3$ and Valve $V_2$ to Valve $V_4$ in Typical Inverter.
failure $CF_{1,3}$ persists, the immediately following commutation from valve $V_2$ to valve $V_4$ may also fail to be completed before the cross-over instant $F$. In this case successive valves $V_1$ and $V_2$ are left conducting because, at instants $G$ and $H$, the corresponding valve voltages $v_5$ and $v_6$ are both "negative". At instants $I$ and $J$, valves $V_1$ and $V_2$ are already conducting, respectively. Therefore, the bridge voltage $v_d$ is reversed for nearly a half cycle after instant $G$. During this time, the direct current increases rapidly, because the inverter bridge works as a rectifier. The following commutations are also likely to fail, i.e. $CF_{1,3}$ and $CF_{2,4}$ as the thick dotted-lines indicate in the Figure. This persistent failure is a most likely consequence of a phase-to-phase short-circuit fault in the receiving a.c. system, as shown by field test-results in the Cabora Bassa-Apollo scheme. (124)

(iii) Double-Not-Successive Commutation Failure. Fig. 5.22 schematically illustrates a double-not-successive commutation failure ($CF_{1,3}$ and $CF_{4,6}$). Until instant $H$, the fault development is the same as the single commutation failure $CF_{1,3}$ described in paragraph (i) (Fig. 5.20). If the cause of $CF_{1,3}$ persists, however, the following commutation from valve $V_4$ to valve $V_6$ may fail to be completed before the cross-over instant $J$. At instant $K$ valve $V_1$ is already conducting. At instant $L$ valve $V_2$ can not be fired, because valve voltage $v_2$ is "negative". The inverter bridge is further by-passed by valves $V_1$ and $V_4$ between instants $K$ and $M$, after which normal commutation from valve $V_1$ to valve $V_3$ takes place. If the cause of commutation failure persists, however, this commutation may fail to be completed again as the thick dotted-lines indicate in Fig. 5.22. Another type of double-not-successive commutation failure ($CF_{1,3}$ and $CF_{6,2}$) is schemat-
Fig. 5.22 Double-Not-Successive Commutation Failure from Valve $V_1$ to Valve $V_3$ and Valve $V_4$ to Valve $V_6$ in Typical Inverter.
ically illustrated in Fig. 5.23. After the initial commutation failure $CF_{1,3}$ and temporary recovery of the bridge voltage $v_d$, commutation from valve $V_6$ to valve $V_2$ may fail to be completed before cross-over instant $I$. Thus, between instants $J$ and $M$, the bridge is by-passed again by valves $V_3$ and $V_6$. Moreover, depending on the development of preceding commutation failure and also on the subsequent voltage and current disturbances, a double-successive commutation failure ($CF_{5,2}$ and $CF_{1,3}$) and additional commutation failure(s) (e.g. $CF_{1,3}$) may occur, as the thick dotted-lines indicate in Fig. 5.23. In practice, such multiple commutation failures are observed during a single phase-to-ground fault in the receiving a.c. system in the Cabora Bassa-Apollo scheme.\(^{(84)}\)

(iv) Commutation Failure during Inverter Start-up. Fig. 5.24 schematically illustrates a single commutation failure ($CF_{4,6}$) during inverter start-up operation. Initially the inverter bridge is by-passed by valves $V_1$ and $V_4$. After the commutation failure $CF_{4,6}$ the same valves $V_1$ and $V_4$ continue to carry the direct current. At instant $H$ valve $V_2$ can not be fired, because valve voltage $v_2$ is "negative". After normal commutation from valve $V_1$ to valve $V_3$ between instants $I$ and $J$, the bridge voltage $v_d$ is gradually established. At instant $K$ valve $V_4$ is already conducting, and the normal firing sequence of inverter starts from instant $L$. Due to the initial commutation failure $CF_{4,6}$ the bridge is by-passed for an additional half cycle. Further commutation failures can be found identical with the previous types of commutation failures already described in paragraphs (i) to (iii).
Fig. 5.23 Double-Not-Successive Commutation Failure from Valve V1 to Valve V3 and Valve V6 to Valve V2 in Typical Inverter.
Fig. 5.24  Single Commutation Failure from Valve $V_4$ to Valve $V_6$ during an Inverter Start-up,  
(a) Positive and Negative Direct Voltages with respect to the Transformer Neutral,  
(b) Direct Bridge Voltage $v_d$,  
(c),(d) Valve Currents $i_1$ to $i_6$.
(v) Commutation Failure during Sequential Inverter Shut-down.

An incidental commutation failure may occur during the inverter shut-down operation described in Section 5.2.5.1 (Fig. 5.8). For example, a single commutation failure CF,1 and direct current transfer from valve V6 to valve V4 may occur simultaneously over instant D, as schematically illustrated in Fig. 5.25. From instant F successive valves V4 and V5 are left conducting so that the full commutating voltage $e_{ca}$ (BR) appears across the inverter bridge. A similar fault development is likely if a single commutation failure CF,5 occurs after instant A, and thus valves V3 and V4 are conducting at instant D (not shown in Fig. 5.25). In this case valves V3 and V4 will be left conducting after instant F. When ON/OFF signal detection is provided, however, an appropriate by-pass pair (e.g. valves V2 and V5 at instant I in Fig. 5.25) can be selected as described in Section 5.2.5.2 (Table 5.1).

5.3.3 Consequential Inverter Faults

As analysed in the previous Section 5.3.2, an initial inverter fault may cause a transient rise of the direct current and subsequent voltage and current disturbances in practice. Persistent a.c. faults in the receiving a.c. system may also cause voltage and current disturbances due to the effects of harmonic filters, nonlinearity of convertor transformers, characteristics of the a.c. faults, etc. Since the inverter is susceptible to these disturbances, consequential inverter faults are likely to occur in practice as follows:

(i) Misfire and Consequential Commutation Failure. Fig. 5.36 illustrates an initial misfire MF,1 at instant A followed by a commutation failure CF,2 after instant D. Valve voltages $v_3$ and $v_4$ are "negative" at instants E and F, respectively. If the
Fig. 5.25 Single Commutation Failure from Valve V5 to Valve V1 during a Sequential Inverter Shut-down.
Fig. 5.26 Cosequential Commutation Failure from Valve V6 to Valve V2 Following Single Misfire of Valve V1 in Typical Inverter.
cause of misfire persists, misfire MF_1 and commutation failure CF_{6,2} may recur after instant I, as the thick dotted-lines indicate in Fig. 5.26. Alternatively, as illustrated in the following Fig. 5.27, a commutation failure CF_{2,4} may occur at instant G after the initial misfire MF_1 at instant A. At instants D and I, valve voltages v_3 and v_6 are "negative", respectively, and misfire MF_1 may repeat at instant J. Similarly, Fig. 5.28 illustrates the effect of a commutation failure CF_{4,6} after instant J. In this case, if the cause of the initial misfire MF_1 persists, full commutating voltage e_{ca} (BR) appears across the inverter bridge after instant I, as the thick dotted-lines indicate in Fig. 5.28.

(ii) Commutation Failure and CONSEQUENTIAL MISFIRE. If the commutating-voltage disturbance persists and the valve voltage is insufficient or "negative" at the time of valve firing, a consequential inverter misfire occurs. For example, with respect to previous Fig. 5.21, misfire MF_4 may occur at instant D (or E) instead of the commutation failure CF_{2,4}. Similarly, misfire MF_6 may occur at instant H (or I) in Fig. 5.22, and also misfire MF_2 at instant H in Fig. 5.23. In such cases the bridge voltage v_d is only slightly different from, or exactly the same as, the corresponding waveforms in Figs. 5.21 to 5.23. However, the difference of valve ON/OFF states becomes significant when ON/OFF signal detection is provided.

(iii) Firethrough and CONSEQUENTIAL Commutation Failure. Fig. 5.29 schematically illustrates an example of initial firethrough FT_1 at instant B and consequential commutation failure CF_{4,6} at instant F. At instant H valve voltage v_2 is "negative". If the cause of firethrough persists, permanent firethrough FT_1 occurs
Fig. 5.27 Consequential Commutation Failure from Valve $V_2$ to Valve $V_4$ Following Single Misfire of Valve $V_1$ in Typical Inverter.
Consequential Commutation Failure from Valve V₄ to Valve V₆ Following Single Misfire of Valve V₁ in Typical Inverter.
Fig. 5.29 Consequential Commutation Failure from Valve V₄ to Valve V₆ Following Single Firethrough of Valve V₁ in Typical Inverter.
once per cycle after instant $K$ as the thick dotted-lines indicate in Fig. 5.29. A further commutation failure $\text{CF}_{1,3}$ may instead occur after instant $K$. Moreover, as schematically illustrated in the following Fig. 5.30, a consequential commutation failure $\text{CF}_{6,2}$ may occur after instant $I$. In this case, a permanent fire-through $\text{FT}_1$ at instant $M$ results in full commutating voltage $e_{ab}$ (RY) across the inverter bridge, as the thick dotted-lines indicate in Fig. 5.30.

(iv) Firethrough and Consequential Misfire. Although less likely, with respect to previous Fig. 5.29, a consequential misfire $\text{MF}_{6}$ may occur at instant $D$ (or $E$) instead of the commutation failure $\text{CF}_{4,6}$. Similarly, misfire $\text{MF}_{2}$ may occur at instant $G$ (or $H$) in Fig. 5.30 instead of the commutation failure $\text{CF}_{6,2}$.

5.3.4 Internal AC/DC Short-Circuit Faults

Due to various overvoltages mainly originating on the a.c. system and d.c. transmission line, the convertor bridges and their associated apparatus are subject to short-circuit (flashover) faults. Fig. 5.31 shows possible locations of the internal a.c./d.c. short-circuit faults in 12-pulse thyristor convertor. Although such faults seldom occur, the most severe overcurrent appears during rectification in the conducting valve which forms the phase-to-phase short-circuit involving the flashover across a non-conducting valve (Fig. 5.31a). The worst instant of short-circuit is soon after the extinction of an outgoing valve (e.g. valve $V_1$ in Fig. 5.31) at small firing delay angles. Thus, the incoming valve (valve $V_3$ in this example) starts carrying a forward current of large amplitude which is only limited by the leakage reactance of the convertor transformers and the sending a.c. system impedance. The short-circuit current itself is similar to the arcback current in main mercury-arc valves, as
Fig. 5.30 Consequential Commutation Failure from Valve \( V_6 \) to Valve \( V_2 \)
Following Single Firethrough of Valve \( V_1 \) in Typical Inverter.
Possible Locations of Internal AC/DC Short-Circuit Faults in Typical 12-pulse Thyristor Convertor:

(a) Faults across a Non-Conducting Valve,
(b) Faults across Bridge Terminals,
(c) Faults across AC Phases on the Valve Side of Convertor Transformer,
(d) Ground Faults at a DC Terminal of a Bridge,
(e) Ground Faults at an AC Phase on the Valve Side of Convertor Transformer,
(f) Ground Faults at the Station Pole or DC Busbar.
comprehensive analysis is given by Kimbark°) and Uhlmann.® In recent HVDC schemes, thyristor valves are designed to withstand the surge ON-state current.(102,105,126-129)

Other severe internal faults include flashover faults across the rectifier bridge-terminals (Fig. 5.31b), (130,131) or across the a.c. phases on the valve side of convertor transformers (Fig. 5.31c).

Ground flashover faults can occur at a d.c. terminal of a bridge (Fig. 5.31d) or at an a.c. phase on the valve side of convertor transformers (Fig. 5.31e). A ground fault of a rectifier at a d.c. station-pole (busbar) normally results in transient overcurrent and subsequent current control.(104) These ground faults may be caused by deterioration of the insulators, by failure of a.c./d.c. lightning arresters, or by misoperation of the earthing switches installed at the a.c./d.c. terminals.

5.3.5 AC Faults

Various types of a.c.-system faults commonly occurring in practice include single phase-to-ground, phase-to-phase, and three-phase faults. The most common of these is the single phase-to-ground fault which is widely applied to study the controllability of inverter.(35,36,45,84)

A CIGRE survey (50-54) shows various levels of a.c. faults which have occurred within the convertor stations in commercial operation. Most of the faults reported are caused by failure of a.c. terminal apparatus and measuring/protecting equipment. The severity and duration of all possible a.c. faults become significant to an HVDC design engineer.

5.3.6 DC Line Faults

D.c. line-to-ground faults commonly occur due to flashovers in overhead transmission lines or to cable failures.(50-54) Travelling
waves generated by a low-impedance overhead-line fault\(^{(132,133)}\) are usually detected at an early stage of the fault development.\(^{(47,48,84,117)}\) However, high-impedance faults detection requires a differential comparison of d.c.-line currents.\(^{(84,117)}\) From a viewpoint of fault simulation on a scaled-down convertor model, the fault duration should be specified, because several restart attempts are usually made with possibly reduced line voltages at certain de-energization intervals, e.g. 150 to 500 ms.\(^{(47,84,117,134)}\) However, d.c. lines consisting wholly of cables are not normally reenergized, because cable faults are nearly always permanent.

D.c. line open-circuits may be caused by erroneous opening of d.c.-busbar switch(es) before the rectifier start-up or by failure of the inverter start-up. Although d.c. open-circuits are much rarer than short-circuit faults, they result in large overvoltages at the d.c. busbar and at the end of the disconnected d.c. line, because of the peak rectification effect,\(^{(135)}\) i.e., stray capacitance may be charged up to the maximum ripple voltage due to the small leakage currents. If the a.c. harmonic filters and shunt capacitors remain connected at the time of the d.c.-line open-circuit, even larger overvoltages will result.

5.4 DIGITAL FAULT SIMULATORS BASED ON HARDWIRED LOGIC

5.4.1 Digital Fault Simulator

A comprehensive digital fault simulator has been designed for the dynamic testing of a direct digital convertor control.\(^{(38,44)}\) One of the four basic types of convertor faults can be specified by the single fault simulator schematically shown in Fig. 5.32; a second similar unit is used for the simulation of double faults. The specification of the required parameters is carried out on the mimic panels of modular design.
Fig. 5.32 Schematic Block Diagram of Single Fault Simulator Based on Hardwired Logic.

The basic concepts of the fault simulation design are summarized below:

- An appropriate pair of fault-simulation control signals I and J is selected from among the commutating-voltage-zero crossings $C_i$ and firing pulses $FP_i$ by the trigger selector (Fig. 5.32a).

- When a fault simulation is requested locally or by a remote signal, the trigger unit (Fig. 5.32b) sends two signals, i.e. a trigger pulse TRG to a recording instrument and a fault initiation signal START$_i$, immediately after counting over a predetermined number of cycles up to 15. A specified type of fault can be single, repetitive, or permanent. Moreover, the fault duration can be independently specified by a timer such that the fault simulation is terminated by generating a signal STOP$_j$.

- Misfire is simulated by blocking a selected firing pulse in the misfire unit (Fig. 5.32c).

- Commutation failure is simulated by delaying a selected firing instant by a certain amount of time which is adjustable within
the commutation failure unit (Fig. 5.32d).

Application of firethrough or arcback can be further delayed from the instant of fault initiation signal $\text{START}_1$. Thus, a digital point-on-wave selection of fault instant is provided up to $63^\circ$ with a step increment of $1^\circ$ (Fig. 5.32e). An auxiliary thyristor $\text{TH}_8$ is provided for the arcback simulation.

5.4.2 Design of Simple Fault Simulator

5.4.2.1 Main Design Features. A simpler fault simulator has been designed for the convertor model described in Chapter 3. It can simulate either a misfire or firethrough of valves $V_1$, $V_2$, and $V_3$. The duration of the fault can be made single or permanent. In spite of its simplicity, the simulator can provide the precise instants for a.c./d.c. or arcback fault application to the fault actuator described in Section 3.6.

As schematically shown in Fig. 5.33, the simulator operates based on the firing pulses $FP_1$ to $FP_3$ which are derived from either the convertor model or a multimicroprocessor-based system. As explained in Section 3.4.5, a selection of the analogue or digital control mode is made by the signal $\text{EDDC}$. Hence, the simulator operates on either of the two convertor control modes.

5.4.2.2 Panel Design and Operating Instructions. The panel design of the fault simulator module L is shown in Fig. 5.34. A toggle switch $\text{SW}5$ is used to select either misfire or firethrough and the valve(s) involved should be specified by means of switches $\text{SW}1$, $\text{SW}2$, and/or $\text{SW}3$. Switch $\text{SW}7$ is provided to specify the use of the fault actuator.

The related logic signals are schematically shown in Fig. 5.35. Normally valve $V_1$ (thyristor $\text{TH}_1$) is fired at instants B, E, J, etc. Thick dotted-lines indicate a "permanent" fault, which is selected by
Detailed Logic Diagram for the Convertor Model, Fault Actuator and Simple Fault Simulator Interfacing with Multimicroprocessor-based System.
Fig. 5.34. Panel View of Simple Fault Simulator Based on Hardwired Logic.

N.B. Scale 3/2.
Fig. 5.35  Schematic Time-chart of Simple Fault Simulator Module L:

(a) Fault Initiation Signal Generated by Switch SW6 "on",
(b) Trigger Pulse Output TRG,
(c) Fault-Duration Control Signal with Switch SW4 either "single" or "permanent",
(d) Firing Pulse FP1 to Simulate Misfire MF1,
(e) Firing Pulse FP1 to Simulate Firethrough FT1,
(f) Fault Instant of Fault Actuator (Trailing Edge) when Switch SW5 at "FT" and Plug PLG Open-circuited,
(g) Fault Duration of Fault Actuator with Setting (f),
(h) Fault Duration of Fault Actuator when Switch SW5 also at "FT" but Plug PLG Connected to Socket ON1,
(i) Fault Instant of Fault Actuator (Trailing Edge) when Switch SW5 at "MF",
(j) Fault Duration of Fault Actuator with Setting (i).
The main operating instructions are summarized below:

- As soon as switch SW6 is turned "on", the fault initiation signal is generated at instant A (Fig. 5.35a). About $240^\circ$ later a trigger pulse TRG (Fig. 5.35b) is sent to the output socket for recording purposes. Further, about $345^\circ$ later a fault duration control signal (Fig. 5.35c) is generated so that the pre-fault operating condition can be recorded for about one cycle.

- Misfire is simulated by blocking the specified firing pulse(s), e.g. FP₁ (Fig. 5.35d). Firethrough occurs as soon as the specified valve voltage(s) become "positive", e.g. sometime earlier than instant J for valve $V_1$ (Fig. 5.35e).

- When switch SW5 is set at "FT", the start of the fault actuator can be set within a 4.7$^\circ$ to 75.4$^\circ$ delay after instant G (Fig. 5.35f) by a knob VR4. If switch SW4 is set at "single" (Fig. 5.35g), the fault duration can be set by a knob VR5 between 43$^\circ$ and 720$^\circ$ (i.e. a single fault). If switch SW4 is set at "permanent", however, a repetitive logic signal (pulse) can be specified, where the pulse width can be set between 43$^\circ$ and 358$^\circ$. Beyond the maximum repetitive setting (i.e. 358$^\circ$), the logic signal (Fig. 3.35g) results in continuously "High" state, because of the retriggerable one-shot used (Texas Instruments' SN74123).

- When switch SW5 is also set at "FT" but plug PLG is connected to socket ON1 (Fig. 5.34), the start of the fault actuator is automatically set at the end of valve $V_1$ conduction, i.e. instant H (Fig. 5.35h).

- When switch SW5 is set at "MF" instead, the start of the fault
actuator can be set within a $4.7^\circ$ to $75.4^\circ$ delay after instant D (Fig. 5.35i). In this case switch SW4 and plug PLG have no effect on the setting (Fig. 5.35j).

Before actually applying the fault actuator, these signals Figs. 5.35f to 5.35j should be monitored through sockets ABI and ABD (Fig. 5.34). At this stage, repetitive signals can be directly measured by the digital angle display module (See Section 3.4.3).

The complete circuit diagram and edge connector configurations are included in the convertor manual. (101)

5.4.3 Advantages and Limitations

The main advantages of hardwired logic are its high speed and straightforward design. For example, the propagation delay time of a standard TTL gate is typically 10 ns. For simple tasks, such as signal blocking and timing, the delay time is negligible in practice. Designing such a system is straightforward since a designer can usually follow a signal flow or processing sequence. Most of the logic components with specific functions are readily available as basic building blocks.

However, as system requirements become more complex, it becomes important to consider other design factors such as operating procedures, compatibility with other system functions, noise immunity against signal interference, overall size, power dissipation, maintenance, flexibility of system modifications, and so on. In the simple fault simulator described in the previous Section 5.4.2, the fault specification is achieved manually by switches and knobs placed in the front panel. However, depending on the type of fault, prior knowledge of the convertor operating conditions is essential to select an appropriate pair of signals, e.g. I and J in Fig. 5.32. Moreover,
the indication of the state of fault simulation is very limited.

5.5 DESIGN CONSIDERATIONS OF THE MULTIMICROPROCESSOR-BASED FAULT SIMULATION AND DATA ACQUISITION SYSTEM

5.5.1 Design Requirements and Main Characteristics

The main design considerations of a microprocessor-based fault simulator are to try and keep (or improve) the advantages of hardwired logic described in the previous Section 5.4, and to transfer the required complexity and sophistication from hardware to software, i.e. computer programmes, as far as practical. Under software controls, the required processing should be met on request by one or more microprocessors. By minimizing the required hardware implementation, maximum design flexibility and operating reliability can be achieved.

It is also important to provide a fast and co-ordinated data acquisition scheme for convertor operation monitoring and fault analysis. Moreover, in order to accomplish flexible system utilization and easy maintenance, a modular approach of both the software and hardware development should be preferred.

With respect to these basic considerations and the needs of modern HVDC schemes, the following design requirements are laid down for the development of a multimicroprocessor-based fault simulation and data acquisition system.

- In order to develop and test sophisticated fault detection and protection schemes, a compatible fault simulator is required.
- The fault simulator should permit comprehensive tests at the commissioning stage to check the reliability of the installation under different types of convertor fault. After successful commissioning, similar tests may be required to check or modify the installation during forced and scheduled maintenance periods.
Specification of fault types and related parameters should be carried out by means of a VDU terminal, so that simple and effective man/machine interaction can be achieved.

Adequate convertor-state information should be readily available to an operator throughout the progress of fault simulation.

All the fault information should be immediately available for display and also for transmission to the other convertor station or dispatch centre via an appropriate telecommunication channel.

A hierarchical structure of multiple mini/microcomputers is required for the HVDC station and bridge controllers. The developed fault simulation and data acquisition system should eventually become an integral part of the overall system which includes other system functions such as convertor control and protection.

5.5.2 Realization of the Multimicroprocessor-based System

5.5.2.1 Selection of the Main System Components. A general purpose microprocessor is being used in systems of high complexity at low cost. Intel's 8085A microprocessor (an upgraded version of 8080A) is one of the most widely used 8-bit general-purpose microprocessors. It has 80 basic instructions based on byte manipulation, and can directly access up to 64 K bytes (words) of memory (Note that 1 K = 2^{10} = 1024). A maximum of 256 input/output ports (devices) can be handled by the 8085A microprocessor. The execution speed and interrupt handling capability of the 8085A microprocessor have also been taken into account in the selection for the real-time application. Moreover, a complete range of support circuits is available for interfacing with the 8085A microprocessor.\(^{(136,137)}\)

The 8-bit word size is convenient to store the convertor-state
information such as the positive/negative states of three commutating voltages and the ON/OFF states of six valves strictly in digital form, since each state can be represented by either "1" or "0" within the 8-bit word.

Although designing a microcomputer system from the chip (IC) level may be advantageous as regards cost-effectiveness and design flexibility, a prefabricated single board microcomputer eliminates the need for much of the hardware implementation. From the design requirements considered in the previous Section 5.5.1 and at the time when the design had to be made, Intel's single board computer iSBC 80/30(138) was selected as the main system component. The iSBC 80/30 includes the 8085A microprocessor, 16 K bytes of dynamic random-access read/write memory, one serial communication device, three programmable interval timers, one programmable interrupt controller, and bus control logic upon a single printed-circuit assembly. Provisions are made for flexible selection of the on-board functions by jumper connections, and for installation of programmable read-only memory. A considerable amount of read/write memory is required to permit a large application programme, and is indispensable for prototype development and future system modification.

In order to provide simple and effective operator/system interaction, a standard VDU terminal (Heath/Zenith H19)(139) has been installed. It includes a standard alphanumeric keyboard and a 12-inch cathode-ray-tube capable of displaying 95 ASCII characters at 80 columns in 25 lines. Together with 33 graphic symbols such as arrows and blocks, the total 128 characters can be displayed in either normal or reverse video mode. (Note that, in the reverse video mode, the background column is illuminated instead of the displayable character itself.) Under an operating condition the operator normally provides
VDU-key commands, or the interconnected system may prompt the operator by requesting commands or parameter values.

Fig. 5.36 Basic Configuration of Multimicroprocessor-based Fault Simulation and Data Acquisition System Interfacing with VDU Terminal and the Convertor Model.

5.5.2.2 Basic System Configuration and Function. The basic configuration of the multimicroprocessor-based fault simulation and data acquisition system is diagrammatically shown in Fig. 5.36. Two single board microcomputers share all the required processing, and are connected to the thyristor convertor model via short ribbon cables. According to their major functions, one microcomputer is referred to as
an "interactive controller", and the other as a "process controller". The former is connected to the standard VDU terminal by a serial communication link. Each microcomputer has a basic hardware structure including 16 K bytes of random-access on-board read/write memory; it has also its own additional hardware which is dedicated to analogue-to-digital (A/D) conversion, interrupt requests generation, convertor-state data-input/output interface, and interval timers control.

Together with the two microcomputers, a 16 K-bytes random-access read/write memory-board is installed in a system chassis and interconnected by a modular termination motherboard; the termination provides Intel Multibus interface which practically allows several microprocessors to have free access to all of the available read/write memory locations and common (off-board) input/output ports interfaced with (i.e. a multiple master distributed-system). Having shared a specific block of the random-access read/write memory as a common data base, the multiple microprocessor system can interactively perform the overall system function in real time. By allocating various processing tasks to a different microprocessor, it can also achieve high system throughput and great modularity.

In order to fully enhance such system characteristics, each time-critical task is typically requested by an input/output device on an occurrence of convertor-state changes, e.g. commutating-voltage-zero crossing instant, valve ON/OFF instant, timer count-over, etc. At each of these instants a corresponding interrupt request signal is generated and directed to a particular microprocessor. Therefore, upon the recognition of interrupt request(s), an appropriate interrupt service routine is selected and immediately executed by the microprocessor (i.e. an interrupt-driven system). In order to arbitrate several interrupt requests occurring concurrently, a multilevel priority
interrupt structure is internally established for each microcomputer, so that the input/output device with the highest assigned priority is serviced first.

With reference to Fig. 5.36, the functional features of the two microcomputers are summarized below:

- **The interactive controller** is assigned all the interactive man/machine operating tasks such as VDU display control and fault specification. It is also assigned to normally display the convertor operating information such as control angles, direct voltage and current. In conjunction with programmable interval timers and the process controller, normal or abnormal convertor-valve ON/OFF sequences can be recorded and made available for display.

- **The process controller** is assigned the measurement of control angles, diagnostic convertor operation monitoring, and fault simulation. Primarily it updates the convertor-state information such as positive/negative states of commutating voltages and valve ON/OFF states. It also sends digital command signals and a trigger (TRG) pulse to the convertor model for fault simulation purposes.

5.5.2.3 Basic System Implementation and Programming Languages

The hardware and software implementation of the multimicroprocessor-based system is characterized by a structured or modular design. Essentially, the total system function, identified by "top-down design", is partitioned into subfunctions of less complexity. Appropriately partitioned subfunctions are typically A/D conversion, valve ON/OFF-states data-input port (hardware modules), and interrupt service routines (programme modules). Each programme module can be written and debugged (verified) separately with a minimum amount of interaction.
(i.e. modular programming). In order to achieve the overall system operation, a main programme is provided to each microprocessor.

A selection from the available programming languages is of great importance for the real-time application. Although difficult to write and debug, assembly language ASM-80 is used for all of the interrupt service routines in the multimicroprocessor-based system, since the speed and/or timing are very critical in such processing. Usually, memory requirement is the smallest with the assembly language. Most of the programme modules are written using the ASM-80 for the process controller in Fig. 5.36.

On the other hand, when processing time is not critical and adequate memory space is available, a structured high-level (procedure-oriented) language PL/M-80 is used in practice. The PL/M language is similar to PL/1 (Programming Language 1), developed for Intel microprocessors. It is block oriented and contains typical programme statements such as:

- IF Condition = True THEN DO Block-A;
- ELSE DO Block-B; (conditional structure),
- DO CASE Block-Number-i; (select structure), and
- DO WHILE Condition = True; (loop structure).

For example, the PL/M-80 is used for the operator/system interaction, since software development time is significantly reduced and the structured programme is almost self-documenting, i.e. easy to debug and maintain for a system change.

In order to test and debug the developed hardware and software in real time, a stand-alone multimicroprocessor-based microcomputer development system (Intellec MDS Model 230) is used in conjunction with In-circuit Emulator ICE-85. All of the required software development is carried out by the microcomputer development system.
which provides the complete diskette operating system including programme editor, assembler, compiler, linker, relocater, loader, etc.

5.5.3 **Main Design Features of the Fault Simulator**

5.5.3.1 **Basic Fault Simulator Design.** The fault simulation methodology of a software-based fault simulator can be derived from the hardwired-logic-based fault simulators described in the previous Section 5.4. Special consideration must be given to the difference between the two types of information processing; namely, the hardwired-logic-based fault simulators are fast to perform simple tasks requiring both serial and parallel signal processings, while the software-based fault simulator is primarily restricted to serial data processing within a single processor. This is because the digital processor is essentially a sequential machine. Although faster and more powerful microprocessors are being continually developed, it is common to find that a typical general-purpose microprocessor requires a few microseconds to evaluate the control parameter(s) and reach a simple decision. Therefore, the serial data-processing nature of the digital processor should be considered in both the hardware and software design for the real-time application. From the viewpoint of processing speed, the system hardware is supportive of the software and an interactive coordination of the two is very important within the overall system.

Subject to the digital processing restriction, a fault simulation programme has been developed for the interrupt-driven multiple microprocessor system. The programme is divided into two major subprogrammes, i.e. fault specification subprogramme and fault simulation subprogramme. The former is assigned to the interactive controller, and used to specify fault type(s) and related parameters. The latter is assigned to the process controller, and used to control a fault simulation sequence and to actuate the specified fault.
Hence, the fault simulation subprogramme consists of two major routines, i.e. fault-simulation control routine and fault-simulation service routine, respectively.

A general time-chart of the fault simulation subprogramme is illustrated in Fig. 5.37, and the corresponding structure diagram is shown in Fig. 5.38. The fault simulation subprogramme is executed at each commutating-voltage-zero crossing $C_i$ as a part of the process controller's interrupt service routine $P$-INT2. As shown in both Figs. 5.37 and 5.38, the fault-simulation control routine further consists of four control subroutines, i.e. pre-TRG, post-TRG, fault-duration, and fault-interval control subroutines. The fault-interval control subroutine is executed only if the specified fault is to be repeated at a certain interval.

As shown in Fig. 5.37, the fault-simulation control routine is executed in sequence and in a cyclic manner. The commutating-voltage-zero crossing $C_1$ is taken as a key reference. Crossings $C_5$ and $C_6$ are directly related to the execution of the fault-simulation control routine. For example, sometime before instant $A$ (Fig. 5.37), the appropriate fault type(s) and related parameters are specified by the fault specification subprogramme. Within a cycle before instant $A$, the fault simulation is requested by specifying a coded control parameter $FS$-STATE in a common data base. At instant $A$, the process controller recognizes this parameter and, therefore, the pre-TRG control subroutine is enabled to count down a specified number of cycle(s). At the end of count-over (e.g. at instant $B$), an external timer is loaded to initiate a fault-data acquisition at about $10^0$ before instant $D$ (crossing $C_1$), and a control parameter TRIGGER is also set so that a trigger pulse (inverted) is sent at instant $D$. At instant $C$ (crossing $C_6$) the control sequence is transferred to the post-TRG
Fig. 5.37 General Time-chart of Multimicroprocessor-based Fault Simulator:
(a) Sequential Time-chart of Four Control Subroutines,
(b) Trigger Pulse (TRG Output).

Fig. 5.38 General Structure Diagram of Fault Simulation Subprogramme: Part of Process Controller's Interrupt Service Routine P-INT2.

N.B. Initially parameters FS-CTLO = 00B, FS-STATE = 0000B, and REPEAT = False.
control subroutine which is used to retain a pre-fault condition for a few specified cycles. At instant E the post-TRG control is terminated. Therefore, from instant F (crossing C_1), the specified fault is actuated for the set duration by the fault-simulation service routine, which essentially provides a required fault start-stop control at each crossing C_i, as indicated by "φ" in Fig. 5.37a. The overall fault duration (e.g. two cycles in Fig. 5.37) is determined by the fault-duration control subroutine. Hence, at instant G (crossing C_6), the fault duration control is terminated so that the fault-simulation service routine is executed to cease the simulated fault within the following cycle (as indicated by "x" in Fig. 5.37a) and the trigger pulse is restored at instant H. Several control parameters are also re-initialized for the next fault simulation. Moreover, under the optional fault-interval control, the same fault can be repeated after instant I. One of three repeating modes, corresponding to three restarting instants A, C and E, can be specified.

In order to cope with the required processing time, fault-simulation-related subroutines, including the four control subroutines, are distributed to each crossing C_i as "Task-i". For example, Task-1 is used to manipulate the trigger pulse (Fig. 5.37b) by acting on the control parameter TRIGGER, and Task-4 to initialize a set of control parameters. Therefore, the fault simulation subprogramme, including each Task-i, can be executed by the 8085A microprocessor within a few electric degrees at each crossing C_i.

As shown in Fig. 5.38, a general algorithm of the fault simulation subprogramme is related to three main control parameters, i.e. FS-CTLO, FS-STATE, and REPEAT. Initially the three parameters are zero. When the appropriate fault type(s) and related parameters are specified by the fault specification subprogramme, FS-STATE = 1000B.
(Note that "B" denotes a binary number.) At this stage no action is taken place. When the fault simulation is requested and accepted by, e.g., the interactive controller, FS-STATE = 1100B; therefore, the pre-TRG control subroutine (Task-5) is executed. If the pre-TRG control is terminated, then FS-STATE = 1010B; therefore the post-TRG control subroutine (Task-6) is executed. If the post-TRG control is terminated, then FS-STATE = 1001B and also FS-CTLO = 11B; therefore, the fault-simulation service routine is requested (bit-0 of FS-CTLO is "1"), and the specified fault is actuated (bit-1 of FS-CTLO is "1"). As shown in Fig. 5.38, the fault-simulation service routine is executed before the fault-simulation control routine (Task-i) at each crossing C_i, since the Task-i is less critical in processing time. (Only Task-5 and Task-6 are included in Fig. 5.38.)

If the fault-duration control is terminated, then FS-CTLO = 01B; therefore, the specified fault is stopped by the fault-simulation service routine within the following cycle. When the specified fault is completely cleared, the used control parameters are re-initialized, i.e. FS-STATE = 1000B and FS-CTLO = 00B. If the specified fault is to be repeated, however, REPEAT = 1B (True) and the FS-STATE remains the same, i.e. FS-STATE = 1001B; therefore, the fault-interval control subroutine (Task-6) is executed. When the fault-interval control is terminated, an appropriate branching is made to repeat the specified fault.

5.5.3.2 Basic Fault Simulator Operation. The fault simulator operation is displayed on the VDU terminal. A main part of the screen-based fault specification and fault-simulation monitoring format is shown in Fig. 5.39. The top-half screen (lines 1 to 12) is used to monitor the convertor operating state before and during the fault simulation. Various messages can be displayed on line-25, which is
Please specify Fault Type(s) and related parameters for New Fault Simulation.

--- Welcome to our Realistic and Comprehensive HVDC Fault Simulation Scheme!

<table>
<thead>
<tr>
<th>Type: O</th>
<th>NewFS, Q Quest FS, R Return, S Stop FS/Log, T Tell</th>
</tr>
</thead>
<tbody>
<tr>
<td>PreTRG:</td>
<td>m 10.0s (500Cy) 2PostTRG: 2Cy 3 4 5 6 2nd Misfire 1 2 3 4 5 6</td>
</tr>
<tr>
<td>V 1</td>
<td>2Interval: 0Cy 3 4 5 6</td>
</tr>
<tr>
<td>W 1st Misfire</td>
<td>1 2 3 4 5 6 2nd Misfire</td>
</tr>
<tr>
<td>X 1st Firethru</td>
<td>1 2 3 4 5 6 2nd Firethru</td>
</tr>
<tr>
<td>Y 1st CommFailr</td>
<td>51 62 13 24 35 46 2nd CommFailr</td>
</tr>
<tr>
<td>Z 1st AC/DC/AB7</td>
<td>1 2 3 4 5 6 2nd AC/DC/AB7</td>
</tr>
</tbody>
</table>

* Please specify Fault Type(s) and related parameters for New Fault Simulation.

---

Fig. 5.39 Convertor Operation Monitoring Format (Top-half Screen) and Main Part of Screen-based Fault Specification and Monitoring Format (Bottom-half Screen).
also used to enter alphanumeric parameter values such as valve number(s), fault duration in cycles, "Y" for "Yes", and so on. (Line-25 acts like a single-line screen independent of the main screen which includes lines 1 to 24.) The reverse video mode is used to emphasize varying parameter values and some particular specifications in the bottom-half screen (lines 13 to 24), and to distinguish the line-25 (not shown in Fig. 5.39). A flickering horizontal arrow "〜", initially placed in column-5 of line-14, is used to indicate the current selection entered by the operator and to draw the operator's attention during the fault simulation.

From the viewpoint of basic screen design, the main command selections are included in lines 16 to 20. VDU keys "O" to "T" are used for major command selections (line-16), and line-17 is used to monitor the state of fault simulation. Three types of first and/or second convertor faults, i.e. misfire, firethrough and commutation failure, can be independently selected by VDU keys "W" tp "Y" (line-21 to line-23). A multiple misfire (e.g. MF₁, MF₂ and MF₃) can also be specified, but the same valve (or its corresponding commutating-voltage-zero crossing) is not subjected to two different fault types or to a second fault of the same type. Moreover, the a.c./d.c. fault (line-24) can only be either a first or second fault, since only one fault actuator is made available at present. (The second fault can be delayed for a number of cycles after the first fault.) The fault specification includes a 'fool-proof' mechanism to prevent misoperation. Selected fault type(s) are left indicated by a graphic symbol "• (oval)" (not shown in Fig. 5.39).

The corresponding algorithm of the fault specification sub-programme is shown by the main structure diagram in Fig. 5.40. The initial set-up includes all the preparatory work including external wiring of recording instrument(s) and the fault actuator (if required),
as well as calling the fault specification subprogramme. If no fault specification has been made before, initial fault parameters are printed out in a complete format similar to Fig. 5.39. Otherwise, the previously specified fault type(s) and related parameters are printed out onto the bottom-half screen. The interactive controller continually displays the present state of fault simulation and prompts the operator to type a key to assign the functions briefly summarized below:

- "P" pre-sets initial fault parameters, and clears the fault type(s), if already specified.
- "Q" requests to initiate the specified fault simulation.
- "R" returns to a point of call in a main programme.
- "S" stops a current fault simulation at any stage in progress and re-initializes the used parameters for a fresh fault simulation.
- "T" continually displays the convertor operating state on the top-half screen as Fig. 5.39.
- "U" and "V" are used to specify various control parameters, e.g. "U" and then "5" to specify a fault duration in cycles. "0 (zero)" is used to exit the current selection "U" after the sub-selections "1" to "5".
- "W" to "Z" are used to specify fault type(s), e.g. "Y", "1", and "1" to specify the commutation failure CF_{5,1} as a first fault.

5.5.4 Main Design Features of the Data Acquisition Scheme

In order to study the effect of a simulated fault, conventional recording instruments can be operated by using the trigger pulse TRG (Fig. 5.37b). Multichannel recorders and oscilloscopes are useful for a comparative analysis of the fault. Digital instruments are also available with varied capabilities. However, an on-line integration of the fault-data acquisition scheme into the overall control and monitoring system can enhance the assessment of system performance, by providing accurate diagnosis of the fault behaviour which can also be communicated immediately to the other convertor station or dispatch centre under a computer-aided control. As the detailed classification of convertor faults indicates in Section 5.3, the recorded convertor-valve ON/OFF states are indispensable to know an exact type of convertor fault, as well as to assess the valve(s) involved, fault instant, duration, consequential effects caused by the initial fault, etc.

From the above considerations, a fault-data acquisition
programme has been specifically developed for the multimicroprocessor-based fault simulator scheme. Primarily, the process controller updates the positive/negative states of the three commutating voltages $e_{ac}$ (RB), $e_{ba}$ (YR) and $e_{cb}$ (BY), and the ON/OFF states of the six convertor valves as two 8-bit data in a common data base. A few cycles before actuating the specified fault (about $10^\circ$ before instant D in Fig. 5.37b), the interactive controller starts sampling these data at a regular interval of $2.5^\circ$ based on 50 Hz a.c.-system frequency. (Minimum usual resolution is therefore about $2.5^\circ$.) A block of read/write memory is provided to store about 14-cycle worth data in a pre-defined format and in sampled sequence. Other convertor operating data are also sampled at the end of every cycle. These include convertor control angles and instantaneous direct voltage and current. Two interrupt service routines (I-INT65 and I-INT55) are executed under the combined control of two programmable interval timers. Based on the VDU terminal, the recorded data can be displayed for analysis.

Moreover, as a practical mode of operation, the free-running fault-data acquisition can be terminated immediately when any abnormal sequence of the convertor valve(s) is recognized by the process controller. By providing a memory manipulation programme, the pre-fault condition can be also retained for a few specified cycles. Therefore, the developed fault-data acquisition programme has such a scope that it can also be used in actual convertor-fault recording. The recorded data are sorted out for the common memory format so that the same fault-data display subprogramme is used.

Fig. 5.41 shows a main part of the fault-data display format on the bottom-half of the screen (lines 13 to 24). Positive/negative states of the three commutating voltages are displayed from line-15 to line-17, while valve ON/OFF states (ON) from line-18 to line-23. In
Fig. 5.41 General Format of Pre-programmed Valve ON/OFF Sequences (Top-half Screen) and Main Part of the Display Format Designed for Multimicroprocessor-based Data Acquisition Scheme (Bottom-half Screen).

N.B. "m" denotes "positive" part of commutating voltages RB, YR and BY, and "n" denotes "conducting" state of each valve $V_i$. 
this case, a typical rectifier (Fig. 5.3 in Section 5.2) is chosen, and 72 columns are equivalent to one-and-half cycles (i.e. 8 columns per 60°). "m" denotes the positive part of the commutating voltages and "n" a valve ON-state, however, the actual display appears like a horizontal bar/line chart, because a graphic symbol "= (half-block)" is used instead of both "m" and "n" in the Figure. VDU keys "H" to "K" (line-13) are assigned to specify the indicated cycle-length per 72 columns. ("J" is selected in this example and a total of 76 columns is used for the bar/line chart.) VDU keys "L" to "Q" (line-14) are assigned to shift the entire bar/line chart to the right or left within the recorded 14 cycles. A cycle location of column-5 is exactly at the beginning of the 11th cycle. This is indicated on line-24 as "Loc 10.0Cy". (Note that the cycle number is counted from 0 to 13.) VDU key "S" (line-14) is used to print out six pairs of firing delay angles and extinction angles on special line-25 (not shown in Fig. 5.41). Part of line-24 is used to display a firing delay angle (α₁), overlap angle (α₁,₃), direct voltage (Vₕ) and current (Iₕ), which are sampled at the end of the indicated cycle location (i.e. 11th cycle). Moreover, the top-half screen can be independently used to display the same recorded-data from a different cycle location for a varied length. Therefore, a maximum of four cycles can be displayed on the full screen or the details of interest can be separately displayed with 2.5° resolution (i.e. 24 columns per 60°). VDU key "R" is always assigned to return to a point of call in a main programme.

Fig. 5.41 also includes a complete format of pre-programmed valve ON/OFF sequences which can only be displayed on the top-half of the screen (lines 1 to 12). The display format is very similar to that of recorded fault data (bottom-half screen in Fig. 5.41), except that line-6 is used to indicate corresponding crossings C₁ with reference to
the selection "H" to "K" on line-1. (Crossing C₁ is fixed at column-5.) The pre-programmed sequences include normal rectifier ("L" as in Fig. 5.41), normal inverter ("M"), single rectifier misfire MF₁ ("N"), single inverter misfire MF₁ ("O"), single inverter firethrough FT₁ ("P"), and commutation failure CF₁ ("Q"). Although limited in the selection, the pre-programmed sequences provide the comparative information to the operator on the same screen.

5.6 HARDWARE DESIGN OF THE MULTIMICROPROCESSOR-BASED FAULT SIMULATION AND DATA ACQUISITION SYSTEM

5.6.1 Realization of the Interrupt-driven Multiple Microprocessor System

Having selected Intel 8085A microprocessor and 8085A-based single board microcomputer iSBC 80/30 as the main system components, a wide scope is provided for interactive multiprocessing among Intel microprocessors. Based on the modular design, the developed hardware and software modules can be readily integrated into a total system. Intel Multibus interface allows up to sixteen parallel microprocessors with the Multibus-access priorities fixed from the highest to the lowest. Each microprocessor can be selected from the Multibus-compatible iSBC microcomputer family, so that the latest 8- and 16-bit microprocessors (e.g. Intel's 8088, 8086) can be used for the same task or other high-level tasks.

In the realization of an interrupt-driven system, generation of concurrent interrupt-request signals becomes important; i.e. each signal should be generated promptly by an input/output device (port) and then cleared immediately by the corresponding interrupt service routine (software) via decoding logic provided for the input/output device. Hence, the interrupt request-acknowledgement relationship ensures prompt
service for the multiple interrupts by the requested microprocessor. After having considered software requirements such as processing priorities and time, and also available interrupt levels (i.e. a maximum of twelve levels with the iSBC 80/30), the multilevel priority interrupts are distributed to an appropriate microprocessor. If required, however, each input/output device can be rearranged for a system expansion by a simple wiring alteration to the Multibus. (It is practically assumed that the number of input/output devices is small in comparison to the maximum 256 input/output ports that the 8085A microprocessor, or a compatible microprocessor, can directly access.)

5.6.1.1 Overall System Configuration. Corresponding to the basic configuration in Fig. 5.36, an overall block diagram of the interrupt-driven multiple microprocessor system is shown in Fig. 5.42. Although the single board microcomputer iSBC 80/30 has a common hardware feature, only the relevant components are included in the Figure, together with the interrupt-request structure and memory allocations. In order to initialize each microcomputer upon the system set-up, appropriate initialization routines are individually programmed in the on-board (local) erasable-programmable read-only memory (EPROM). A dual-port controller provides the feature in which the on-board read/write memory (RAM) can be accessed by the on-board 8085A microprocessor or by another microprocessor via the Multibus. (The on-board microprocessor has RAM access priority over a Multibus request.) Multi-master arbitration logic is provided to prevent a Multibus contention by indicating which microprocessor is currently having access to the Multibus. (13B)

Two on-board timers (PIT) use a 1.2288 MHz clock and locally generate the highest interrupt-request signals OUT0 and OUT1 which are directly connected to the central processing unit (CPU) through its
pins RST6.5 and RST5.5, respectively. (RST6.5 has higher priority than RST5.5.) The on-board programmable interrupt controller (PIC) can directly handle a maximum number of eight interrupt-request signals IR0 to IR7, and generates the lowest interrupt-request signal INT which is connected to the CPU through its pin INTR. The priority of these low-level interrupts is fixed from the highest IR0 to the lowest IR7, though not all the interrupts are in use.

As shown in Fig. 5.42, several interrupt-request signals are externally generated by the input/output devices interfaced with the Multibus. Appropriate 8-bit port addresses are specified for each input-output device so that it can be accessed by any microprocessor, e.g. CPU-I and CPU-P. (Note that "I" denotes the interactive controller and "P" the process controller.) All of the interrupt-request signals are positive level-triggered, i.e., the signal is active while it is in the "High" state.

With reference to the interactive controller, the main design features are summarized below:

- The VDU terminal is connected to the programmable communications interface (USART-I) through the voltage-converting RS 232 C interface. A baud rate of the asynchronous serial link is generated by the on-board timer-I2 and set at 9,600 baud (bits/s). (Intel's PIT 8253 consists of three independent 16-bit timers.)

- The two on-board timers I0 and I1 are used to sample the fault data at a regular interval. Two interrupt service routines I-INT65 and I-INT55 are requested by the timers I0 and I1, respectively.

- External timer-22 is used to start the fault-data acquisition from an appropriate instant. Usually, the process controller
CPU-P loads the timer-22. At the instant of count-over, the interrupt-request signal OUT2 (i.e. IRO) goes "High", and an interrupt service routine I-INT0 is immediately executed by the interactive controller CPU-I.

- Six analogue signals are separately derived from the convertor model. Usually, the parallel (simultaneous) A/D conversion is started by the process controller CPU-P. At the end of the A/D conversion, an interrupt-request signal IRI goes "High", and an interrupt service routine I-INT1 is executed by the interactive controller CPU-I. It can read part or all of the converted 8-bit data. More details are to be described in Section 5.6.3.

- The 16 K-bytes on-board read/write memory (RAM) is addressed from 4000H to 7FFFH.

With reference to the process controller, the main design features are summarized below:

- In order to simulate the specified fault, the process controller CPU-P sends appropriate digital command signals to the programmable peripheral interface (PPI-P). Two latched 8-bit output-ports E8 and EA are used to manipulate the convertor model, fault actuator, and recording instrument(s). Input port E9 is not used for the fault simulation.

- The two on-board timers P0 and P1 are used to provide a point-on-wave capability for the first and second faults, respectively. Two corresponding interrupt service routines P-INT65 and P-INT55 are responsible for simulating firethrough(s) and commutation failure(s), and for requesting the fault actuator. Because of this design arrangement, the second fault is completely independent of the first.
Free-running external timer-20 is used to measure the converter control angles. Its 16-bit count is incremented by referring to a 1.8 MHz clock. (A count of 100 is equivalent to 1.0°.)

Timer-21 is used to provide an external fault duration control independent of the a.c.-system voltage-waveforms. At about every 20 ms (i.e., equivalent to a cycle) the specified fault duration is evaluated in an interrupt service routine P-INT3. The external timer control is optional, and mainly designed for simulating very severe a.c. faults.

At any change of the converter valve state, an interrupt service routine P-INT1 is requested and it is promptly executed by the process controller CPU-P. More details are to be described in Section 5.6.2.

Positive/negative states of the three commutating voltages are updated at each voltage-zero crossing instant by executing an interrupt service routine P-INT2, which also includes the fault simulation subprogramme (Fig. 5.38). The three zero-crossing detectors are of conventional type with diode clippers and differential amplifiers (inverting).

The 16 K-bytes on-board read/write memory (RAM) is addressed from 8000H to BFFFH.

The 16 K-bytes read/write memory board is addressed from C000H to FFFFH. The overall memory map is briefly described in Appendix A1, which includes the programme module names and their allocations.

5.6.1.2 8085A-based Single Board Microcomputer iSBC 80/30. The 8085A microprocessor used for the single board microcomputer iSBC 80/30 is operated on a constant system-clock frequency of 2.7648 MHz, marginally smaller than the maximum 3.125 MHz. Based on this system
clock (i.e. 2.7648 MHz), the fastest CPU register-to-register transfer instruction "MOV" requires 4 clock cycles (i.e. 1.45 μs), and the slowest "CALL" instruction 18 clock cycles (i.e. 6.51 μs). Since each 8085A instruction requires a set number of clock cycles, the total processing time can be calculated from the instructions actually applied for the interrupt service routines. The calculated time can thus be used for providing an accurate point-on-wave capability by adjusting the count number of a programmable timer. This is because, when the timer is loaded, several instructions have been already executed since a reference instant (e.g. C). The calculated (or estimated) time is also important to determine the distribution of the required interrupt service routines to an appropriate microprocessor. As a conservative estimation, the 8085A microprocessor can execute more than a thousand basic instructions within 60°. (A latest version of the 8085A, i.e. 8085AH-1, can be operated up to a 6 MHz system-clock frequency. Therefore, it can double the above estimation.)

A complete set of iSBC 80/30 circuit diagrams and related programming information is fully documented in an iSBC 80/30 reference manual.

5.6.2 Generation of Microprocessor Interrupts

As briefly described in the previous Section 5.6.1, the generation of the timer-based interrupt request signals is straightforward, since each programmable timer can be manipulated independently. Initially, a timer is set with a timer control mode, i.e. PIT 8253 Interrupt Mode 0. When the timer is loaded with an either 8- or 16-bit count, the timer output (i.e. the interrupt request signal) remains "Low". With reference to the timer clock used, the counting duration is determined and, at the instant of count-over, the timer output goes "High". This enables the execution of the corresponding
interrupt service routine, which immediately clears the timer output either by re-loading the timer count or by re-setting the timer with the same timer control mode. The former method is used to regularly repeat the same interrupt service routine (e.g. I-INT65 and P-INT3), and the latter to simply acknowledge the interrupt request (e.g. I-INT55, I-INT0, P-INT65 and P-INT55).

Generation of other interrupts requires special hardware. The block diagram of three valve-ON/OFF-data input/output ports is shown in Fig. 5.43, which also includes a co-ordinated generation of the process controller's interrupt P-INT1. Data-in port 2A of the programmable peripheral interface PPI-20 (Intel's 8255A) is used to read the valve ON/OFF states through the bi-directional data-bus driver (Intel's 8226, inverting). Bit-0 to bit-5 of the port 2A (i.e. PA0 to PA5) correspond to the digital values ON_1 to ON_6, which are then stored as 8-bit data ON-STATE in a common data base. (Bit-6 and bit-7 of the ON-STATE are not in use.) Port 2B is used to promptly acknowledge the interrupt request, and port 2C to initially mask (disable) the request. The two output ports are latched. Decoding logic in Fig. 5.43 is dedicated to select the specified PPI-20 port and to control the direction of data transfer (i.e. either input to or output from the microprocessor CPU-P) via the Multibus. Additional TTL gates are used to manipulate the P-INT1 request signal.

Upon a system set-up, all of the six exclusive-OR gates are cleared by two successive 8085A port-read/write instructions, i.e. "IN Port-2A" and "OUT Port-2B". (For example, when no valves are conducting, ON-STATE = 0000000B. If the same data are sent to the interrupt acknowledgement port 2B, each of the exclusive-OR gates is set to "Low".) The interrupt request signal is then enabled by sending 1111111B to the mask port 2C; i.e. PC0 to PC5 are kept "High". Therefore, any change of the valve ON/OFF states immediately sets the interrupt request
Valve ON/OFF Information From Convertor Model

From/To MULTIBUS

Bi-Directional Data-Bus Driver
(Two 8226)

CS DIEN

IOJC IOWC

XACK

ADR2_7

ADR1

ADR0

INIT

Dat0-7

Dat0-7

Directional Control

Decoding Logic

Chip Select

PA0

DO to D7

Data-In Port 2A

PA5

PB0

RD

WR

Acknowledgment Port 2B

PB5

PC0

Mask Port 2C

PC5

A1

A0

RESET

Programmable Peripheral Interface PPI-20
(Intel's 8255A)

Fig. 5.43 Block Diagram of Valve ON/OFF Data Input/Output Ports Combined with Generation of Process Controller's Interrupt P-INT1.
signal "High", and it is promptly re-set by the two successive 8085A instructions in the interrupt service routine P-INT1.

A very similar circuit is applied to the interrupt P-INT2 which reads positive/negative states of the three commutating voltage. In this case, bit-0 to bit-2 of 8-bit data C-STATE are defined to store positive/negative states of the \( e_{ac} \) (RB), \( e_{ba} \) (YR), and \( e_{cb} \) (BY) in this order. (Bit-3 to bit-7 of the C-STATE are not in use.) For example, at a crossing \( C_1 \) the C-STATE is updated from 011B (i.e. \( C_6 \)) to 010B (i.e. \( C_1 \)) by the process controller. (Note that a "positive" state is denoted as "0".)

5.6.3 Analogue-to-Digital Conversion

In the main functional description given in previous Section 5.6.1, six A/D convertors are used in parallel to obtain 8-bit data of the \( e_{ac} \) (RB), \( e_{ba} \) (YR), \( e_{cb} \) (BY), \( I_d \), \( \frac{dI_d}{dt} \), and \( V_d \). The block diagram of one conversion channel (i.e. Port BC) is shown in Fig. 5.44, which also includes the overall A/D conversion control logic and I-INT1 request generation. Decoding logic is dedicated to initiate the simultaneous A/D conversion and to select one of the six data-in ports. A sampling duration of the sample and hold device (National Semiconductor's LF398) is determined by a pulse width of one-shot A; i.e. 15 \( \mu \)s for 0.5% sampling accuracy. The low-cost and medium-speed A/D convertor (National Semiconductor's MM5357B) uses a successive approximation technique. With reference to the 922 kHz clock, it takes a maximum of 40 clock cycles (i.e. 43.4 \( \mu \)s) to complete the A/D conversion.

Initially, the I-INT1 request signal is re-set by 8085A instruction "IN Port-BC" where the port address BCH is used to clear the Toggle-type Flip-Flop through the decoding logic in Fig. 5.44. In
order to initiate the A/D conversion, 8085A instruction "OUT Port-BC" must be executed by any microprocessor interfaced with the Multibus. Upon the execution, the A/D conversion request signal is sent to the one-shot A, so that the six analogue inputs are simultaneously sampled. At the end of sampling (i.e. 15 µs later), a short pulse is generated by the cascaded one-shot B and given to the six A/D convertors to start the A/D conversion. When all of the six A/D convertors complete the conversion, their signals EOC0 to EOC5 are set from initial "Low" to "High" so that the I-INT1 request signal is set "High" by the T Flip-Flop. Therefore, the interactive controller reads part or all of the
converted data by executing 8085A instructions such as "IN Port-BC".
(Note that this instruction must be included in the interrupt service routine I-INT1 so that the I-INT1 request signal is cleared to allow next A/D conversion.) A range of the analogue input, i.e. -5 V to +5 V, can be converted to the digital equivalents 0 to 255, respectively.

5.7 SOFTWARE DESIGN OF THE MULTIMICROPROCESSOR-BASED FAULT SIMULATION SCHEME

5.7.1 VDU Terminal Manipulation Programme

In order to provide reliable parameter-values specification and VDU-key selection, various procedures have been programmed in a VDU-terminal manipulation module VDU-TML.PLM and made available for the interactive controller. The programme module also includes several procedures responsible for displaying the parameter values in various formats. These procedures fall into three major categories as the main features are summarized below.

5.7.1.1 Parameter Values Display. In general, a string of ASCII characters can be sent to the VDU terminal (Procedure MSG). A message can be printed out starting from a specific screen column (Procedures STRING-OUT and STRING-OUT-TO-24THLINE). Similarly, a numeric value can be printed out from the 10000th decimal value to the successive value(s) specified (Procedure ADR-TO-STRING). In this case preceding zero(s) can be deleted, i.e. replaced by "space" character(s) for a better readability. A 16-bit integer value is converted to a meaningful angle with a decimal point appropriately placed (Procedure ADR-TO-ANGLE). An 8-bit value can be sequentially printed out from a pre-specified high-bit to a low-bit in a digital form, i.e. as 1's and 0's (Procedure ADR-TO-BIT-PATTN). Several more procedures are available to erase part
of the VDU screen, and to manipulate the cursor, e.g. "turn on the
cursor", "use a block cursor", etc.

5.7.1.2 Numeric Values Specification. A numeric value can
be specified within the minimum and maximum values, inclusive
(Procedure GET-NUM). The absolute minimum is 0 and the maximum is
limited up to 65529. In the latter case, a further entry of a numeric
character 0 to 9 is rejected beyond the current number 6553. An entry
of non-numeric characters is simply rejected with a "bell" sound.
Below the minimum specification or beyond the maximum specification or
65529, the erroneous number is indicated near the end of line-25 (e.g.
"N was: 6553") while the operator is prompted for a fresh specification.
Therefore, only an acceptable number is returned to a point of call in
an application programme. This capability is essential in some cases to
protect the programme against a total destruction which is otherwise
inherent due to the microprocessor's memory structure and CPU 'stack'
operation or to a limited processing speed.

Moreover, only one zero can be entered as the first numeric
character and the operator can delete the preceeding decimal(s) during
the specification.

When this procedure is called, adequate space should be available
from the cursor location to the end of the line. If the special line-25
is not used for the specification, an appropriate error message will be
given on this line.

5.7.1.3 Character Selection. A displayable ASCII character can
be selected from within the specified character string (Procedure
SELECT-CHAR). This procedure is normally used in a loop structure. If
no VDU key is entered by the operator, zero is returned to a point of
call. However, if and only if the character selection is acceptable
(e.g. "Y" amongst "A" to "Z"), it is immediately returned.
As an option, the acceptable character can be printed out temporarily. It can be deleted for correction within about five seconds or be returned by typing the carriage-return (CR) key or returned automatically due to expiration of the time.

5.7.2 Interactive System Operation

As briefly mentioned in Section 5.5.2.3, the overall system operation is achieved by providing two main programmes I-MMAIN.PLM and P-MMAIN.PLM for the interactive and process controllers, respectively. The former is primarily responsible for the operator/system interaction at various stages of the system operation. Since sufficient processing time is available other than for the interrupt service routines, several processing assignments are distributed between the two controllers. In essence, these main programmes have the lowest level in processing priority. However, this does not normally restrain the effective system operation, because a human interaction is relatively slow; e.g. about 0.2 s may be required for a new key entry after recognizing a change on the VDU screen.

5.7.2.1 Interactive Programme Selection. A complete format of the initial programme selection is shown in Fig. 5.45, together with the convertor-operation monitoring format. The corresponding algorithm of the main programme I-MMAIN.PLM is shown by the general structure diagram in Fig. 5.46. After the system set-up, the VDU-key selection parameter SELECT is initially set to "C". Before entering the loop "Main", the system interrupts are enabled. Under SELECT = C the initial format in Fig. 5.45 is given. Then, by using SELECT = F, the convertor operating state is monitored and the operator is prompted to select the VDU key within "A" to "I". At this stage VDU keys "J" and "K" are disabled, but, they can be easily enabled to evaluate user test-programme(s) or to add new programme(s). As shown in Fig. 5.46, VDU key "L" is
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### Line:

1. Timer: 21m50.7s 50.0Hz
2. Inv Vd: 50.0V Id: 1.00A
3. Convertor Valve Vi
4. Firing Delay Angle ai
5. Overlap Angle ui,i+2
6. Extinction Angle EAi

#### Following keys are assigned for HVDC Fault Simulation, Analysis and Monitoring

- **A** To analyse recorded data with pre-programmed valve ON/OFF sequences,
- **B** To bid special functions,
- **C** To clear main parameter values, and come back to this display,
- **D** To display recorded data,
- **E** To exit to our Monitor Program,
- **F** Fault Simulation Program has been loaded, and convertor state is monitored,
- **G** To go ahead for Fault Simulation!
- **H** To help Fault Simulation procedures,
- **I** To input parameter values. N.B. Initially "F" is selected.

---

**Fig. 5.45** Convertor Operation Monitoring Format (Top-half Screen) and Interactive Programme Selection Format (Bottom-half Screen) Initially Displayed.
Fig. 5.46 General Structure Diagram of the Interactive Controller: Interactive Programme Selection.

N.B. Within the loop "Main", the interrupts (I-INT's) are enabled.
internally used to retain the current VDU screen. Namely, \texttt{SELECT = L} is used when returned from the programmes selected by "A", "B", "D", and "G" to "I". In this case, a message is printed out on line-25 to ask a new SELECT. An essential feature of the main programme is therefore that these selections are "re-entrant", i.e., the once selected/specifed parameter values are retained until they are re-set or re-initialized by the operator.

As an additional feature, a state of fault-data acquisition is made available within the main programme (Procedure \texttt{SORT-SQ-MSG}). Usually, an appropriate message is printed out on line-25. However, if the top-half screen is not used for convertor-operation monitoring, the recorded fault data are immediately displayed upon completion of the acquisition. This is equivalent to automatically selecting "D", besides, an exact location of the first convertor sequential fault (if any) is given at the 37th column(s) within the two cycle-length.

With reference to Figs. 5.45 and 5.46, the main VDU-key selections and related programmes are briefly summarized below:

- "A" is used to display the pre-programmed valve ON/OFF sequences as described in previous Section 5.5.4. (The data base is defined in module \texttt{F-PATTN.ASM} and Procedure \texttt{DISPLAY-F-PATTN} in module \texttt{SHOW-FP.PLM} is called.)

- "B" is used to execute special functions such as built-in test programmes. Two blocks of the fault-data base defined in module \texttt{F-OFSEQ.ASM} can be exchanged or copied to either block. This enables that the latest or previous fault data be retained for a comparative study when new fault-data acquisition is made. The copied fault data can be displayed over the full screen, as mentioned in previous Section 5.5.4. Moreover, one test programme \texttt{TEST65.PLLM} is dedicated to manually enforce the
fault-data acquisition. Upon a recognition of any sequential convertor fault, the recorded fault data can be immediately displayed, as mentioned above.

- "C" reproduces the full screen as Fig. 5.45. Main parameters selected in "A" and "D" are re-initialized.

- "D" is used to display the recorded fault data as generally described in previous Section 5.5.4. (The data base is defined in module F-OFSEQ.ASM and Procedure DISPLAY-F-OFSEQ in module SHOW-SQ.PLM is called.)

- "E" is used to exit the loop "Main" and return to the monitor programme. It is normally responsible for parameter values transfer such as loading CPU programme counters (PC). However, part of the memory contents can be displayed or altered. (145)

- "F" is used to continually monitor the convertor operating state on the top-half screen as shown in Fig. 5.45. The relevant data are displayed in every 0.4 s. (Procedure DISPLAY-ANGLES in module DISPLY.PLM is regularly called within the loop "Main".)

- "G" calls the fault specification and monitoring subprogramme (Procedure FAULT-SPECN in module F-SPECN.PLM), as generally described in Section 5.5.3.2.

- "H" gives interactive operating information on the top-half screen. (Procedure HELP-MAIN-PROCEDURES in module HELP-FS.PLM is called.)

- "I" is used to specifically alter the parameter values which are initially defined. These include the minimum de-ionization time of thyristors MIN-ION (initially set to 3°), and the parameter LD-TIMO which determines a regular interval of fault-data sampling between 1.8° and 5.3°. (Normally LD-TIMO = 60 for 2.5° sampling.)
5.7.2.2 Process Controller Assignments. The interrupt service routines of the process controller CPU-P typically require 15 to 20% of the total processing time. Therefore, two main assignments are given to the process controller, as shown by the structure diagram in Fig. 5.47. This may impose some delay in execution of the interrupt(s) which have just been requested, since the current instruction related to the loop "Main" has to be executed before the interrupt(s) are acknowledged by the CPU-P. However, because the execution delay (several microseconds) is insignificant in practical applications such as HVDC control and protection, the CPU-P is not put at a 'halt (HLT)' state, which would allow the CPU-P to immediately acknowledge the requesting interrupt(s).

![General Structure Diagram of the Process Controller](image)

**Fig. 5.47** General Structure Diagram of the Process Controller.

N.B. Within the loop "Main", the interrupts (P-INT's) are enabled.

With reference to Fig. 5.47, the two main assignments are summarized below:

- If the fault-data acquisition is internally terminated by recognizing a sequential convertor fault in the interrupt service
routine P-INT1, sorting is required to retain the pre-fault condition within the common memory format defined in module P-OFSEQ.ASM. This is achieved by calling Procedure SORT-P-OFSEQ in module CP-SORT.PLM with a coded parameter SORT-SQ = 1. The sorting takes up to a maximum of 2 s.

The fast convertor shut-down subroutines described in previous Section 5.2.5.2 have been programmed in module P-INT0.ASM (Appendix A2). They are primarily called within the interrupt service routines P-INT1 and P-INT2, and kept requested. Therefore, this arrangement in the loop "Main" is effective when non-conducting valves are immediately blocked by the shut-down request subroutine and if the last commutation takes place over a certain period of time, which is mainly determined by the magnitude of the direct current and commutating reactance of the convertor. In this case, originating from the loop "Main", the by-pass enforcement subroutine is called as soon as the two successive valves are left conducting. (The sorting of the recorded fault-data is required well after this occurrence.) The convertor is kept by-passing until an appropriate measure is taken.

5.7.3 Main Fault Simulation Algorithm

As the main design features of the software-based fault simulator are described in Section 5.5.3, the fault simulation subprogramme requires accurate information of the commutating-voltage-zero crossings. Any change of positive/negative states of the three commutating voltages generates the P-INT2 request signal, as described in Section 5.6.2. Since no filters are used to smooth out the commutating-voltage signals which normally contain commutation notches, triple crossings normally occur when the delay angle is about 60° and 120°. (Conventional active
low-pass and notch filters were found impractical because of unacceptable phase shift at the main a.c.-system frequency. Low-Q resonant band-pass filters were more practical for a narrow a.c.-system frequency range.) Moreover, various voltage disturbances in the sending/receiving a.c. system may result in multiple crossings. Therefore, it is essential to provide an adequate diagnostic routine before processing the appropriate routines related to each valid crossing $C_i$.

![General Structure Diagram of the Interrupt Service Routine](image)

**Fig. 5.48** General Structure Diagram of the Interrupt Service Routine P-INT2 Executed at any Change of Positive/Negative States of the Three Commutating Voltages.

The interrupt service routine P-INT2 is shown by the general structure diagram in Fig. 5.48. Whenever the interrupt P-INT2 is requested and acknowledged by the process controller CPU-P, the C-STATE is updated and, according to its value, an appropriate crossing $C_i$ is selected. Normally, the C-STATE is traced in order to check the sequence of the crossings, i.e. C-STATE = 011B ($C_6$), 010B ($C_1$), 100B ($C_2$), etc. (As explained in Section 5.6.2, a "positive" state is denoted as "0".) Moreover, in order to detect triple crossings, the
previous two crossings are stored in a common data base. For example, a voltage dip on the a.c.-system voltage $e_a$ soon after crossing $C_1$ may result in the triple crossings such as C-STATE = 011B (i.e. $C_6$), 010B (i.e. $C_2$), 011B (i.e. $C_6$), 010B (i.e. $C_2$), 100B (i.e. $C_2$), etc. In such case, the second $C_6$ and $C_1$ are both rejected and further processing prevented. The first crossing $C_1$ is taken as valid and normal processing of the interrupt service routine P-INT2 resumes from the $C_2$. Very severe a.c. faults may produce different crossing sequences, but in such cases, other interrupts (e.g. P-INT1) should be activated to shut down the convertor.

With reference to Fig. 5.48, the main functions of the P-INT2 are briefly summarized below:

- First of all, the extinction angle $EA_{i+1}$ is measured at each crossing $C_i$. Within the interrupt service routine P-INT1, the free-running timer-20 has been temporarily latched when the valve $V_{i+1}$ turns off, and its count is stored in a common data base. Hence, the difference between the latched and current counts is measured as the extinction angle. (A very similar technique is used to measure the delay and overlap angles according to their definitions.)

- As described in Section 5.5.3.1, the fault simulation service routine and distributed Task-i are then executed in this interrupt service routine P-INT2. More details are described in the following Section 5.7.3.1.

- The fault classification study described in Section 5.3 has already explained that valve $V_i$ should not normally be conducting after crossing $C_{i-1}$ in any convertor operating mode. This condition is therefore used to grade the severity of convertor faults and to apply the fast convertor shut-down. More details
are given in Section 6.4.

- Convertor operating modes (e.g. by-passing, blocking) can be derived by regularly evaluating the valve ON/OFF states at, say, 60° intervals. Similarly to the C-STATE validity check, an abnormal operating mode is usually declared first in the interrupt service routine P-INT1 by tracing the valve ON/OFF sequence. More details are given in Sections 5.8.2.4 and 6.3.

5.7.3.1 Fault Simulation Service Routine. The fault simulation service routine is shown by the main structure diagram in Fig. 5.49. Essentially, the fault start and stop controls have similar structures, except that the second fault (if specified) may be enabled a number of cycles later than the first fault by means of the fault-duration control subroutine (Task-6). A coded parameter FS-TYPi is defined by the fault specification subprogramme and used to select a type of first/second fault. (In addition, a coded parameter FIRST is used to identify either the first or second fault.) Bit-0 (least-significant-bit) of the FS-TYPi is used to identify the misfire MF_i, since the valve V_i should be blocked/de-blocked as soon as possible. (Decoding bit-0 by means of the 8085A 'rotate' instruction "RRC" is the fastest method to achieve the one-out-of-two selection. (143) In practice, a misfire can only be simulated when the delay angle is greater than 3.8°. This experimental value is perfectly adequate since the minimum delay angle is practically limited to 5° to 7° (See Section 2.3.4.4).

Other fault types are selected by using the 8085A register-indirect jump instruction "PCHL". (141,143) The fault simulation principle of these fault types is basically the same as the hardwired-logic-based fault simulators described in Section 5.4. This is described in the following Section 5.7.4 with specific examples and additional features.
Fig. 5.49 Main Structure Diagram of the Fault Simulation Service Routine.
5.7.4 Fault Simulation and Monitoring

To complement the main design features of the fault simulator described in Section 5.5.3, more specific fault specification and operating instructions are described in the following Sections 5.7.4.1 to 5.7.4.4, together with corresponding screen formats.

5.7.4.1 Fault Specification and Operating Instructions. A complete fault-specification format is shown in Fig. 5.50a. Initially, no fault types are specified and a non-repeating single (i.e. one-cycle) fault is assumed. If, at this stage, the fault simulation is requested by typing VDU key "Q", the request is rejected and an error message is printed out on line-25, since no fault type(s) are specified. If, however, any fault type is specified (i.e. "FSis:Set!" in line-17 of Fig. 5.50b) and "y" is typed; the operator is prompted to answer if the equipment is "Ready". If the answer is "Y" for "Yes" (i.e. "Ready:Y" in line-17 of Fig. 5.50b), the fault simulation is started. The equipment readiness can be independently reported by typing "T" and answering either "Y" or "N" (for "No").

In addition to the manual operation, it is possible to remotely operate the fault simulator by providing additional signal lines (or input port) to the multimicroprocessor-based system; by setting a parameter FS-REQUEST by, e.g., the interactive controller, the fault simulation can be automatically started. (VDU key "[" simulates this case by setting FS-REQUEST = True.) An equipment readiness signal may be included which is derived from appropriate testing equipment in the field so that a parameter FS-READY is set or re-set. (VDU key "]" simulates an equipment failure by re-setting FS-READY = False.) In order to handle an equipment failure or an additional fault-simulation request or inadequate fault-type specification, several checking routines are included in the pre-TRG control subroutine (Task-5), so that the
Welcome to our Realistic and Comprehensive HVDC Fault Simulation Scheme!

Type: Opt PrevLog, P Reset NewFS, Q Quest FS, R Return, S Stop FS/Log, T Tell

Ready: N FSis: New ConvFault: 0 AbortedFS: N ReptFS: Non MinIon: 3d SampleK: 60

U 1 PreTRG: m 10.0s (500Cy) 2PostTRG: 2Cy 3Del-1: 5d 4Del-2: 5d 5Dur: 1 Cy
V 1 SecFDel: 0 Cy 2 Interval: 0 Cy 3 ExtDurC: N 4 Implicit: N 5 CFM: Mod: Min 6 Del: 7.5 d
W 1st Misfire 1 2 3 4 5 6 2nd Misfire 1 2 3 4 5 6
X 1st Firethru 1 2 3 4 5 6 2nd Firethru 1 2 3 4 5 6
Y 1st CommFailr 51 62 13 24 35 46 2nd CommFailr 51 62 13 24 35 46
Z 1st AC/DC/AB7 1 2 3 4 5 6 2nd AC/DC/AB7 1 2 3 4 5 6

Type: Opt PrevLog, P Reset NewFS, Q Quest FS, R Return, S Stop FS/Log, T Tell

Ready: Y FSis: Set! ConvFault: 0 AbortedFS: N ReptFS: BGN

U 1 PreTRG: m 0.0s (0 Cy) 2 PostTRG: 7 Cy 3 4 5Dur: 2 Cy
V 1 SecFDel: 1 Cy 2 Interval: 50 Cy 3 ExtDurC: Y 4 Implicit: Y 6
W 1st Misfire 1 2 3 4 5 6 2nd Misfire 01 02 03 4 5 6

X 1st Firethru 01 2 3 4 5 6 2nd RFirethru 01 02 3 4 5 6

Y 1st CommFailr 51 62 01 3 24 35 46 2nd CommFailr 51 62 13 24 03 5 46

Z 1st AC/DC/AB7 1 2 3 Del-1: 5d 4Del-2: 90d 5

3Del-1: 5d 4Del-2: 90d 5

Screen-based Fault Specification and Monitoring Format (Bottom-half Screen):
(a) Initial Format, (b) Misfire Specification, (c) Firethrough Specification,
specified fault will not be actuated. When the fault simulation is terminated prematurely, a coded number is indicated in column-46 of line-17 such as "AbortedFS:1". A "bell" sound is given and an appropriate error message is printed out on line-25. Moreover, a current fault simulation can be remotely stopped at any stage in progress by setting a parameter STOP-FS = True. (This is basically equivalent to typing VDU key "S".)

As mentioned in Section 5.7.2.1, two blocks of the fault-data base in module F-OFSEQ.ASM can be copied to either block. Whenever the fault simulation is requested and accepted by the interactive controller, the latest fault data are normally retained. However, by typing VDU key "0" and answering "Y", the previous fault data can be retained, instead. This is indicated by an oval in column-6 of line-16 as shown in Fig. 5.50b. While the fault simulation is in progress, access to VDU key "0" is prevented; access is also prevented for keys "Q" and "U" to "Z".

With reference to the pre-TRG, post-TRG, and fault-duration control subroutines in Section 5.5.3, three parameter values can be specified in cycles as shown in line-19 of Figs. 5.50a and 5.50b, i.e. "U-1", "U-2", and "U-5", respectively. The corresponding minimum and maximum values are shown by the schematic time-chart in Fig. 5.51a. It should be noted that, in the case of post-TRG specification, the actual specification is limited to between 1 and 12 cycles in order to record the pre-fault condition for 0 to 11 cycles, respectively. A fault duration lasting many cycles may be regarded as a "permanent" fault in practice. Since a maximum pre-TRG time of more than twenty minutes has been specified, the operator can communicate with a field operator by telephone before actuating the a.c./d.c. fault. Co-ordinated fault simulation may be carried out at both ends of an HVDC link.
Fig. 5.51 Schematic Time-chart of Fault Simulation (Non-repeating):

(a) Sequential Time-chart,
(b) Trigger Pulse (TRG Output),
(c) First Fault,
(d) Second Fault.

Moreover, a second fault can be delayed up to 255 cycles from instant C as shown in Fig. 5.51d. The second-fault delay can be specified in cycles as shown in line-20 of Fig. 5.50b, i.e. "V 1SecFDel: 1Cy".

(i) Misfire Simulation. Fig. 5.50b also shows an example of a first multiple misfire (MF₄, MF₅, and MF₆) followed by a second multiple misfire (MF₁, MF₂, and MF₃). In this example, the second misfire is delayed by one cycle, and because of this, the fault duration can only be set to at least two cycles. (The duration "2" is indicated in column-78 of line-19, Fig. 5.50b). The hatched areas in Figs. 5.51c and 5.51d indicate where the corresponding valves V₄ to V₃ are to be blocked in sequence.

(ii) Firethrough Simulation. Fig. 5.50c shows an example of
double-successive firethrough (FT_1 and FT_2) specification. Both first and second firethrough can be delayed between 5° and 180° from the corresponding crossings, e.g. C_1 and C_2, respectively. The former limit is due to the processing time required to actuate the fault, and the latter limit corresponds to a half cycle where the corresponding valve voltage is "positive". (Note that a letter "d" following after the numbers denotes electric degrees, e.g. 5° and 90°.) When VDU key "X" is typed and either the first or second firethrough selected, the operator is prompted to further select a "permanent" or "repetitive" fault mode. In the former mode, the corresponding valve is kept fired from the firethrough instant, and in the latter mode, a short firing pulse (of about 29 μs) is generated to fire the valve at each firethrough instant. For example, no indication is given in column-8 of line-22 for the first permanent firethrough FT_1, however, "R" is printed out in column-47 of line-22 for the second repetitive firethrough FT_2 (Fig. 5.50c). (A by-passing mode is available at the second firethrough as described in Section 5.7.4.3.)

(iii) Commutation Failure Simulation. Fig. 5.50d shows an example of double-not-successive commutation-failure (CF_1,3 and CF_3,5) specification. Essentially, commutation failure is simulated by late firing of the incoming valve, e.g. V_3 and V_5. There are two modes of commutation-failure simulation available, i.e. minimum de-ionization ("Min") and additive delay ("Add") modes. Initially, the minimum de-ionization mode is selected, i.e. "CFMod:Min" in line-20 of Fig. 5.50a. In this mode, the incoming valve is blocked for 180° less the specified minimum de-ionization
time, e.g. \(180^\circ - 3^\circ = 177^\circ\) (the delay angle of the incoming valve becomes \(177^\circ\)). The corresponding parameter MIN-ION can be altered between \(0^\circ\) and \(30^\circ\) as described in Section 5.7.2.1 to increase the flexibility of the fault simulator operation.

If, however, the additive delay mode is selected (i.e. "CFMod: Add" in line-20 of Fig. 5.50d), 2.56° to 25.6° of firing delay is added to the corresponding delay angle actually measured a cycle before actuating the specified commutation failure in the post-TRG control subroutine (Task-6). The amount of additive delay can be specified in 2.56° step increments, e.g. "Del:12.5d" in line-20 of Fig. 5.50d. Since only arithmetic and logic instructions are used in combination with a look-up table P-W-TABL in module TRNSFR.ASM, and also the on-board timers PO and PI use a 1.2288 MHz clock available (instead of a 1.8 MHz clock desirable), the calculated blocking period (i.e. new delay angle) has a minimum resolution of 1.28°. (16-bit multiplication/division takes considerable time, e.g. 2 to 3 ms, and is impractical for the interrupt service routine P-INT2; the lower seven bits of the measured delay angle are therefore ignored.) Furthermore, it is possible to introduce the additive delay to two firing angles.

(iv) AC/DC Fault Simulation. Fig. 5.50e shows an example of first a.c./d.c. fault specification. The fault instant can be delayed between \(5^\circ\) and \(180^\circ\) from the selected crossing, e.g. \(30^\circ\) from \(C_1\). Whenever the fault actuator is applied, it should be re-set by switch SW1 (See Section 3.6). An appropriate fault level should also be set up.

As mentioned in Section 5.6.1, the timer-21-based fault duration control (interrupt service routine P-INT3) can be used for this
purpose, i.e. "ExtDurC:Y" in line-20 of Fig. 5.50e. Moreover, upon the recognition of any sequential convertor fault, fault-data recording can be terminated if an 'implicit' mode of data acquisition is specified, i.e. "Implicit:Y" in line-20 of Fig. 5.50e. More details about this recording mode are described in Section 5.8.2.

5.7.4.2 Repeating Modes of the Fault Simulation. As described in Section 5.5.3.1, the specified fault can be repeated from one of the three repeating instants under the fault-interval control (Task-6). Corresponding to previous Fig. 5.51, the three repeating modes, Mode 1 ("BGN"), Mode 2 ("TRG"), and Mode 3 ("IMD") are shown by the schematic time-charts in Figs. 5.52a, 5.52b, and 5.52c, respectively. Note that TRG pulse is set from "High" to "Low" at instant B in Figs. 5.52a and 5.52b, as shown in Fig. 5.51b. Usually, the fault-simulation interval

![Diagram](image-url)

**Fig. 5.52** Three Repeating Modes of Fault Simulation:

(a) Mode 1 to repeat from the beginning (BGN),
(b) Mode 2 to repeat from the Trigger stage (TRG),
(c) Mode 3 to repeat immediately (IMD).
can be specified between 1 and 65529 cycles (Fig. 5.52a). However, if the timer-21-based duration/interval control (P-INT3) is specified, the interval is automatically incremented by two cycles, i.e., the resultant interval becomes 3 to 65531 times 20 ms. This is a precaution against prolonged voltage-waveform disturbances due to very severe a.c.-system fault(s) simulated.

When the fault simulation is to be repeated from the beginning (i.e. instant A in Fig. 5.52a), the pre-TRG specification is limited to 500 cycles at least. This is because sorting of the fault data may require considerable time as mentioned in Section 5.7.2.2.

The repeating mode itself is automatically entered if the interval is specified other than 0 (zero). For example, when the interval is set to 50 cycles (line-20 in Fig. 5.50b), the operator is prompted to select one of the three repeating modes. The selected mode is then indicated in line-17 such as "ReptFS:BGN" (Fig. 5.50b). The operator is further prompted to specify a number of additional repetition(s) between 1 and 254. The total number of the fault simulation events is therefore limited to 255. In the case of a.c./d.c. faults, it is necessary to re-close the circuit breaker CB; this operation only requires a short pulse of about 12 μs (FA-Select) which is generated at the end of the fault-interval control (See Section 3.6).

5.7.4.3 Sequential Convertor Shut-down. In order to demonstrate the sequential convertor shut-down described in Section 5.2.5.1, a by-passing mode is made available at the second firethrough (Paragraph ii in Section 5.7.4.1). This mode, discussed with reference to a multiple valve blocking (specified as 'misfire'), is shown as an example in Fig. 5.53a. If this mode is selected, "B" is printed out in column-57 of line-22 (Fig. 5.53a). If the earliest firethrough instant
**Fig. 5.53** Screen-based Fault Specification and Monitoring Format (Bottom-half Screen):

(a) Sequential Converter Shut-down Specification,
(b) Parameter-Values Monitoring during Fault Simulation.
is selected (i.e. 5° after the appropriate crossing C₃), the corresponding by-pass pair, i.e. valves V₃ and V₆, is fired at this instant. At the start of the demonstration, a sequential blocking of valves V₁, V₂, V₄, and V₅ in the same cycle is specified, since the second fault (i.e. permanent firethrough FT₃ and FT₆ at C₃) is not delayed. When the fault duration control is terminated, the six valves are de-blocked in sequence as in a normal convertor start-up.

If the by-passing mode is selected for crossing C₄ and the first multiple misfire (i.e. valve blockings, MF₂, MF₃, MF₅, and MF₆) specified, the results are very similar to previous Figs. 5.8 and 5.9. Because the by-passing mode can be specified with reference to different first faults, various by-passing sequences can be simulated; a delayed by-passing can be also demonstrated as described in Section 5.2.5.1.

5.7.4.4 Monitoring. As described in Sections 5.5.3.2 and 5.7.4.1, various parameter values are continually displayed during the fault simulation. This is shown for a specified fault in lines 17 to 24 of Fig. 5.53b. It is assumed that the fault simulation has just been requested and accepted as indicated by the horizontal arrow in column-37 of line-16. The equipment is "Ready" and the fault simulation is "ON" (line-17). A convertor-fault event counter CONV-FAULT is described in Section 5.8.2.4, which starts from 0 (line-17). (The fault counter can be re-set to 0 by typing VDU key "N".) Because line-17 indicates "AbortedFS:N", the fault simulation is not prematurely terminated.

Normally, the specified cycle numbers are counted down to zero and immediately re-set to the specified values (line-19 and line-20). The operator can normally observe which control subroutine is in action, although a change in a few cycles may not be recognized, e.g. 5 cycles (line-20).

In this example, the specified fault is to be simulated for the
maximum 255 times (line-17); the number is decremented to 0 and then
the specified repeating mode ("BGN", "TRG", or "IMD") immediately
printed out, since the fault simulation is completed. At this later
stage, fresh simulation can be started ("FSis:Set!", line-17).

5.8 SOFTWARE DESIGN OF THE MULTIMICROPROCESSOR-BASED DATA ACQUISITION
SCHEME

5.8.1 Convertor Operating-State Monitoring

As mentioned in Sections 5.5.3.2 and 5.7.2.1, the top-half
screen is used to continually monitor the convertor operating state.
Figs. 5.39 and 5.45 show typical rectifier and inverter operations under
balanced a.c.-system conditions. Figs. 5.3 and 5.4 illustrate the
theoretical waveforms corresponding to these display examples. The
frame, units, and notations are initially printed out and the current
values are displayed in sequence from line-1 to line-9. It takes about
4 to 5 ms to display each angle.

A 21-minutes timer is run based on the a.c.-system frequency. A
16-bit cycle counter CYCLE-K is incremented at each crossing C₁(Task-1).
Normally, the timer is freely running, but it is re-set to zero whenever
the fault simulation is started. The maximum indication is given in
line-1 of Figs. 5.39 and 5.45.

The a.c.-system frequency is measured based on the period of
commutating-voltage \( e_{ob} \) (BY); i.e. starting at each crossing \( C_3 \), the
period CY-PROD is measured by means of external timer-20 (Task-3) and
it is linearly interpolated around the nominal frequency (i.e. 50 Hz)
within 1.5% deviation (module DISPLY.PLM). To be more accurate, the
three commutating voltages (i.e. periods) should be calculated by an
independent microcomputer such as Intel's 8041A/8741A.\(^{138}\) Instead of
this arrangement, a digital frequency meter may be directly interfaced
through additional input port(s).

The direct voltage and current are converted to the digital equivalents at every crossing (P-INT2) and promptly displayed in the formats shown in line-2 of Figs. 5.39 and 5.45 (module DISPLY.PL). These variables have maximum ranges of ±140 V and 2A and the corresponding resolutions are 1.09 V (i.e. 2.18% of the rated voltage) and 15.6 mA (i.e. 1.56% of the rated current), respectively. 10- or 12-bit A/D convertors are practically required for much finer HVDC convertor control.

5.8.1.1 Normal Convertor Operating Modes. Under the normal convertor-operating condition, three operating modes, i.e. "Rec" (rectifier), "Trn" (transition), and "Inv" (inverter), are displayed in columns 1 to 3 of line-2 (Figs. 5.39 and 5.45).

These modes are derived in two stages in Task-2 (P-INT2). Firstly, each mode is tentatively declared, by calculating the average of the three firing angles $\alpha_1$, $\alpha_3$, and $\alpha_5$, as follows:

- If the average angle is less than 60°, declare "Rec".
- If the average angle is between 60° and 120°, declare "Trn".
- If the average angle is between 120° and 180°, declare "Inv".

In the above calculation, the absolute error of the average angle is 2.56° (256 count from the 1.8 MHz clock), since only the most significant byte of the three firing angles, actually measured, is used for simplicity.

Secondly, a changeover from the current operating mode is allowed only if the same mode is declared over one cycle.

Moreover, the display of these operating modes is suppressed if other convertor operating-modes are declared, as explained in Section 6.3.
5.8.2 Data Acquisition under Normal and Abnormal Converter Operations

To complement the main design features of the data acquisition scheme described in Section 5.5.4, a specific algorithm and details of data recording modes are described in the following Sections 5.8.2.1 to 5.8.2.4.

5.8.2.1 Memory Organization and Recording Principle. Fig. 5.54 shows in block diagram the main part of the fault-data based defined in module F-OFSEQ.ASM (Appendix A1). Each block-section (i.e. record) is addressed from CYCLE00 to CYCLE14 in sequence and consists of 288 bytes of the read/write memory to store one-cycle worth recorded-data, i.e. C-STATE and ON-STATE. Extra memory is also provided to store convertor control angles and direct voltage and current. These variables are sampled at the end of every cycle, i.e. at instants A to N in the Figure, and the cycle counter CYCLE-NUM is incremented at those instants. The sample pointer SAMPLE-PTR, initially set to the starting address CYCLE00, is incremented whenever the latest C-STATE and ON-STATE are sampled in the interrupt service routine I-INT65 at 2.5° intervals. Appropriate initial values are given by the interrupt service routine I-INT0 which is executed before the I-INT65 is enabled. About 10° after starting the data recording, TRG pulse is set from initial "High" to "Low".

There are two modes of data recording available, i.e. 'explicit' (data logging) and 'implicit' (fault recording) modes. In the former mode the recording is completed when CYCLE-NUM = 14, i.e. at instant N (Fig. 5.54a). The pre-fault period is determined by the post-TRG specification POST-TRG, e.g. 3. In this case, when a fault is simulated, any first sequential convertor fault would occur in the third cycle and this is indicated by an asterisk "*" in Fig. 5.54a. The fault location
Fig. 5.54 Memory Organization for the Converter Data Acquisition: Part of the Fault-Data Base Defined for the Interrupt Service Routine I-INT65.

(a) 'Explicit' Mode, (b) 'Implicit' Mode.
F-LOCATION is also recorded as the current value of sample pointer SAMPLE-PTR by the process controller (P-INT1).

The 'implicit' mode of data recording is similarly initiated, but it allows continuous recording under normal convertor operation; i.e. at instant N in Fig. 5.54b, cycle counter CYCLE-NUM is re-set to zero and sample pointer SAMPLE-PTR re-initialized to the starting address. (The memory block is used like a ring.) As described in following Section 5.8.2.4, the data recording is normally terminated when any sequential convertor fault is recognized by the process controller. For example, a control parameter END-CYCLE is initially set to other than 0 to 13, i.e. 255. When the fault is first recognized in the P-INT1, this value is calculated, e.g.

\[ \text{END-CYCLE} = \text{CYCLE-NUM} - \text{POST-TRG} = 7 - 3 = 4. \]

(14 is added if END-CYCLE becomes a negative value.)

Since, at each instant A to N, END-CYCLE is compared for equality with CYCLE-NUM before it is incremented, the data recording continues from the following instants H to N and back to A. However, at instant E, \( \text{END-CYCLE} = \text{CYCLE-NUM} = 4 \), therefore, the recording is terminated while retaining the pre-fault condition specified by the POST-TRG.

If for example SAMPLE-PTR = CYCLE05 (instant E), all the recorded data is rotated upward by 5 cycles until a common memory format similar to Fig. 5.54a is obtained. (This is achieved by calling Procedure SORT-F-OFSEQ in module CP-SORT.PLM.)

5.8.2.2 Fault-Data Recording Algorithm. Based on the pre-defined memory format and recording principle, a fault-data recording algorithm has been developed, which combines the two recording modes as shown by the detailed structure diagram of Fig. 5.55. A complete listing of the interrupt service routine I-INT65 is documented in Appendix A3.
Fig. 5.55 Detailed Structure Diagram of the Interrupt Service Routine I-INT65: Convertor Data Recording.
Until one-cycle worth sampling is completed, the latest C-STATE and ON-STATE are regularly sampled (EXIT10 in Fig. 5.55). This part of the routine is referred to as "critical sampling path", which determines the minimum sampling interval. This interval includes the processing time required to acknowledge the interrupt I-INT65 and to execute 22 related instructions (One 'jump' instruction is programmed in module I-INTJT.ASM to call the I-INT65.) The experimental evaluation of the sampling interval is given in the following Section 5.8.2.3.

When one-cycle worth sampling is completed, the interrupt service routine I-INT55 is enabled and the equality 'CYCLE-NUM = END-CYCLE' is checked in order to terminate the 'implicit' mode of recording. (If terminated, a coded parameter SORT-SQ is set to 1.) After the CYCLE-NUM is incremented and provided that the end of the memory block (i.e. instant N in Fig. 5.54) is not reached, the recording continues (EXIT20). In this case, the on-board timer 10 is loaded with an adjusted (i.e. normally reduced) count, since, in comparison to the critical sampling path, extra instructions are executed.

If CYCLE-NUM =14 and the 'explicit' mode is specified, the recording is completed. If the 'implicit' mode is specified instead, further check takes place to confirm if the recording is stopped by an operator's intervention, i.e. STOP65 = True. If not intervened, the 'implicit' mode of recording is directed to continue (EXIT20).

5.8.2.3 Minimum Sampling Interval. Fast sampling is required to achieve fine resolution of the recorded valve ON/OFF sequence and also to relieve the interactive controller CPU-I for other processing tasks related to the I-INT55, I-INT1, and main programme. Inherently, processing speed is limited by the system-clock frequency (i.e. 2.7648 MHz) operating the 8085A microprocessor, and by the instruction set
available for a given processing task. However, some processing time is saved by sequentially organizing the parameters defined in a common data base, and by using a register-indirect addressing method.\(^{(141,142)}\)

The minimum number of CPU registers is used to save processing time (the registers have to be reserved in advance by "PUSH" instructions and then restored by "POP" instructions within the interrupt service routine, Appendix A3). In order to achieve the fastest possible execution, 'jump' instructions are minimized and, instead, the same subroutine is repeated, although more memory is required for the repetition.

Having complied with the above requirements on speed-conscious programming, the sampling interval characteristic is measured against the count of on-board interval timer 10, as shown in Fig. 5.56. The timer 10 (a down counter) uses a 1.2288 MHz clock and only the 8-bit count LD-TIMO is loaded to re-enable the I-INT65. The sampling interval is measured based on the 50 Hz a.c.-system frequency, and the slope in Fig. 5.56 is therefore $1.46^\circ$ per 100 count.

The maximum interval (i.e. $5.29^\circ$) is simply determined by the maximum 8-bit count, i.e. 255. The minimum interval (i.e. $1.75^\circ$) is determined by the minimum permissible count, i.e. 10, since the last three 8085A instructions (i.e. "POP PSW (restore processor-status-word)", "EI (enable interrupts)", and "RET (return)" ) have to be executed before the I-INT65 is re-enabled owing to the timer count-over. In this case, the processing time of the interactive controller is almost fully devoted to the execution of the critical sampling path which requires about $1.5^\circ$ (i.e. 84 μs).

Based on the experimental result obtained, a nominal count of 60 has been chosen to achieve a $2.5^\circ$ sampling interval. This interval not only gives the adequate resolution required to analyse the recorded
valve ON/OFF sequences, but also leaves sufficient time for other related processing. Furthermore, 2.5° sampling (i.e. 144 samplings per cycle) provides a high level of screen-display manoeuvrability by the fault-data display subprogramme in module SHOW-SQ.PLM (See Section 5.5.4). This is because the duodecimal number system is superior to the octal and decimal systems, in the sense that it has a maximum number of common multiples. For example, 144 can be divided by 2, 3, 4,
6, 8, etc., where the corresponding display resolutions per column become $5^\circ, 7.5^\circ, 10^\circ, 15^\circ, 20^\circ$, etc.

Judging from the latest development of the microelectronics technology available, it may be practical to sample other convertor control-variables at $2.5^\circ$ intervals.

5.8.2.4 Convertor Fault Recording. The interrupt service routine P-INT1 is shown by the general structure diagram in Fig. 5.57. As described in Section 5.6.2, the P-INT1 is executed at any change of the valve ON-OFF states; i.e. the interrupt request is immediately acknowledged and the ON-STATE is updated. Similarly to the C-STATE validity check (Fig. 5.48 in Section 5.7.3), the normal sequence of the valve ON/OFF states is traced, i.e. ON-STATE = 110000B ($S_4$), 110001B ($P_1$), 100001B ($S_5$), 100011B ($P_2$), 000011B ($S_6$), 000111B ($P_3$), etc. (As explained in Section 5.6.2, bit-0 to bit-5 of the ON-STATE correspond to ON to ON, respectively.) If the new ON-STATE is the expected one, in order to branch to an appropriate ON- or OFF-state subroutine (V-ONi and V-OFFi in Fig. 5.57), use is made of an odd/even parity check of the ON-STATE (8085A flag 'PO (parity odd)' condition) and of the register-indirect jump instruction "PCHL". For example, when valve $V_1$ turns on normally, a new ON-STATE = 110001B is read and its parity is 'odd' (i.e. there are three 1's), therefore the subroutine V-ON1 is selected to measure the firing delay angle $\alpha_1$.

If, however, an overlap angle is very small (e.g. $1^\circ$ or less), there exists a processing mismatch between the P-INT1 request originated by a valve turn-on and the ON-STATE updated. For example, if following ON-STATE = 110000B (i.e. $S_4$), ON-STATE = 100001B (i.e. $S_5$) is read, it is judged that 110001B (i.e. $P_1$) is 'skipped' due to a short commutation overlap between the valve $V_1$ turn-on ($P_1$) and the valve $V_5$ turn-off ($S_5$). (This condition is recognized by means of a logic-OR instruction, i.e.
Fig. 5.57 General Structure Diagram of the Interrupt Service Routine P-INTI Executed at Any Change of the Valve ON/OFF States.
110000B OR 100001B equals 110001B.) Therefore, immediately after processing the subroutine V-ON1, subroutine V-OFF5 is executed. Due to the processing time involved, the overlap angle measurement is limited to 2.9°.

If neither the normal sequence is traced nor the small overlap condition recognized, it is judged that an abnormal sequence has occurred during the convertor operation (branch SEQ-ERR in Fig. 5.57). At first, the 16-bit fault counter CONV-FAULT is incremented by one for monitoring and detection/protection purposes. As explained in previous Sections 5.8.2.1 and 5.8.2.2, the F-LOCATION is recorded once if the fault-data recording is enabled. The END-CYCLE is also calculated if the 'implicit' mode is specified.

Based on a relative increment of the fault counter CONV-FAULT, the fast convertor shut-down routine P-INT0 can be applied. This is included in the fault simulation scheme, as described in Section 6.4.

In conjunction with the P-INT2 briefly described in Section 5.7.3 (Fig. 5.48), the convertor operating mode (e.g. blocking, faulty) is derived immediately in the P-INT1 (routine DEC-C-ST in Fig. 5.57). This is described in Section 6.3.

5.8.3 Display Facilities

To complement the main design features of the fault-data display facility described in Section 5.5.4, Fig. 5.58 shows the complete format on the bottom-half of the screen. A single rectifier misfire MF1 of Fig. 5.13 (Section 5.3.2.1) is chosen as the fault example. The instants A to H in Fig. 5.13 are included in Fig. 5.58 from column-5 to column-55. Normal rectifier operation is also shown on the top-half of the screen for comparison.

Within the recorded 14 cycles, the entire bar/line chart (lines 15 to 23) can be shifted to the left (VDU key "L" in line-14) or right
Fig. 5.58 General Format of Pre-programmed Valve ON/OFF Sequences (Top-half Screen) and the Format Designed for Multimicroprocessor-based Data Acquisition Scheme (Bottom-half Screen): Instants A to H Correspond to Single Rectifier Misfire MF1 of Fig. 5.13.

N.B. "m" denotes "positive" part of commutating voltages RB, YR and BY, and "n" denotes "conducting" state of each valve V_i.
by one column. The current cycle on display can be replaced by
the next ("N") or previous ("P") cycle. By typing "O" and specifying
the cycle location between 0 and 13, the corresponding cycle can be
promptly displayed starting from column-5. For intermediate selection
the use of key "Q" is recommended, because it shifts the chart to the
left by 60°.

VDU key "S" is used to print out six pairs of firing delay
angles and extinction angles on line-25. The operator can select the
angles for the current cycle or the adjacent two cycles, if available.

With reference to the cycle location in line-24 (e.g. "1.0Cy")
the corresponding memory address is indicated in columns 12 to 15 (e.g.
"288"). Following this indication, the fault location F-LOCATION is
given in columns 19 to 22 (e.g. "348"). In this case, the F-LOCATION
corresponds to column-15 (instant C). The fault counter CONV-FAULT
(not shown in Fig. 5.58) is incremented at instants C, D, E and F, i.e.
four times per single rectifier misfire.

A coded fault-type parameter CF-TYPE is set to zero
when the fault simulation is started. This parameter is coded by the
process controller (P-INT2) and indicated in columns 29 to 31 of line-24
(e.g. "Type:000"). The coding conditions and screen indications are
described below:

- If valve $V_i$ is conducting after crossing $C_{i-1}$ for the first time,
  the valve number "$i" is recorded and indicated in column-31. A
  level of fault severity is set from "0" to "1" and indicated in
  column-29.

- If the above condition is met for the second time in the same or
  the following cycles, the valve number is recorded and indicated
  in column-30. The level of fault severity is incremented to "2".

- If the first condition is met for the two successive valves at
the two corresponding crossings, the first and second valve numbers are recorded and indicated in column-31 and column-30, respectively. The level of fault severity is set to "3" and indicated in column-29.

5.9 EXPERIMENTAL RESULTS

5.9.1 Introduction

In order to evaluate the basic capabilities of the multimicroprocessor-based fault simulation and data acquisition system, the convertor model is connected to a constant direct-voltage source (+70 V) through the four 50-miles overhead-line and four 10-miles cable modules (Section 3.5). From a fault simulation point of view, the manual firing angle control is used throughout, since it provides fundamental phenomena of an unprotected convertor without impinging undue HVDC system representation. In addition, the convertor control variables (e.g. firing delay angle, direct voltage and current) can be clearly indicated before and during the fault simulated.

Numerous evaluation tests have been carried out during the system hardware and software development, and typical test results are documented in the following Section 5.9.2. These results are included in graphic form at the end of this Section, i.e. Figs. 5.59 to 5.70. Various parameter values and fault-simulation modes are chosen in order to demonstrate the varied capabilities of the scheme. However, those parameters are not necessarily suited to the fault type(s) specified.

5.9.2 Typical Test Results

5.9.2.1 Convertor Operating-State Monitoring and P-INT1/P-INT2 Generation. Fig. 5.59 shows the convertor operating-state displayed on the top-half of the screen. Normal inverter operation "Inv" is indicated in line-2, in the reverse video mode.
The normal C-STATE and ON-STATE sequences, shown on the bottom-half of the screen, are printed out by a built-in test programme TEST12.PLM. Crossings are decoded such as "C-1" for C₁. The test programme is used to demonstrate the execution of the interrupt service routines P-INT1 and P-INT2, in the processed sequence, from line-14 and from left to right. It can be seen that after crossing C₁ (P-INT2), valve V₅ turns on (P-INT1), then valve V₃ turns off (P-INT1), and so on (See Fig. 5.4).

Since VDU key "B" has been used to print out the processed sequence in the main programme I-MMAIN.PLM, the operator is prompted to select a new key among "A" to "I" (line-25).

5.9.2.2 Misfire Simulation. Fig. 5.60 shows a multiple misfire specification as a second fault which is delayed by one cycle. The timer-21-based duration/interval control and 'implicit' mode of data recording are also specified (line-20).

The fault simulation has been carried out during rectification with the receiving end short-circuited. The result is shown on the top-half of the screen in the Figure. It can be seen that this particular simulation represents a case of unprotected rectifier blocking, since the two successive valves V₅ and V₆ are left conducting over a cycle. Because the related commutating voltage $e_{cb}$ (BY) becomes "negative" after crossing C₂ (column-70), the valves cease conducting when the direct line-current $I_d$ becomes zero (See Fig. 5.15 in Section 5.3.2.1).

The fault event counter CONV-FAULT is incremented to two when the two valves cease conducting and then to three when the fault duration (i.e. 500 cycles) expires and normal rectification is resumed.

The coded fault type CF-TYPE is "365" (line-12), because valve V₅ continues conducting after crossing C₄ (column-47) and V₆ after C₅ (column-52). The level of fault severity is set to "3", since at C₅
only two successive valves $V_5$ and $V_6$ are left conducting.

5.9.2.3 Firethrough Simulation. Fig. 5.61 shows a specification of a permanent firethrough $FT_1$ followed by a repetitive firethrough $FT_2$ (line-22) in the same cycle. The fault duration is set to one cycle. Both first and second firethroughs are delayed by the minimum $5^0$ from the corresponding crossings $C_1$ and $C_2$ respectively (line-19). The fault-simulation interval is initially set to a minimum of three cycles (i.e. 60 ms), as required by the timer-21-based duration/interval control (line-20). One of the three repeating modes (e.g. Mode 3 "IMD") is selected, and the fault simulation events are set to a maximum of 255 (not shown in Fig. 5.61).

The fault simulation has been carried out during rectification and the result is immediately displayed on the top-half of the screen and this is stated on line-25. It can be seen that valve $V_1$ is kept fired over a cycle and the first abnormal sequence is recognized when valve $V_4$ turns on normally (column-37). The recorded F-LOCATION is "450" (line-12), which corresponds to the calculated screen column, i.e. column-37. The coded fault type CF-TYPE is set to "101", because valve $V_1$ is kept conducting after crossing $C_6$ (column-47). The direct current is commutated from valve $V_1$ to valve $V_3$ (column-31). Valve $V_2$ fires a little earlier than normal, though this can not be noticed because of the resolution of the display, i.e. $10^0$ per column (line-12).

Fig. 5.61 is actually taken during the fault simulation by temporarily retaining the screen. The fault-simulation interval is currently counted down to "1" (line-20) and from that stage on the fault is continued for the additional "181" times (line-17). Line-17 shows that the fault simulation is "ON", and the fault-event counter CONV-FAULT is incremented by six per single permanent firethrough $FT_1$.

Fig. 5.62 shows a specification of double-successive repetitive
firethrough, FT₁ and FT₂ (line-22), in the same cycle. The fault duration is also set to one cycle, but the repeating mode is not specified, since the interval is set to "0" (lines 17 to 20). The first firethrough FT₁ is delayed by 60° from crossing C₁ and the second firethrough FT₂ by 90° from C₂ (line-19).

The fault simulation is carried out during inversion and the result is shown on the top-half of the screen. It can be seen that valves V₁ and V₂ are fired at the specified instants, i.e. column-33 and column-43, respectively. The fault-event counter CONV-FAULT is set to "3" (line-17), i.e. when valve V₁ fires through, valve V₆ turns on normally (column-36), and valve V₄ turns off (column-37). It is not further incremented, since valve V₅ turns off (column-42) before valve V₂ fires through.

5.9.2.4 Commutation Failure Simulation. Fig. 5.63 shows a specification of commutation failure CF₁₂ (line-23) for two cycles (line-19). The additive delay mode "Add" is specified and its value is set to 15.0° (line-20).

The fault simulation has been carried out with a delay angle of 150°, and the result is immediately displayed on the top-half of the screen. It can be seen that valve V₅ fails to commutate the current to the incoming valve V₁ due to the late firing. Valve V₅ therefore fires through the two specified cycles and this is indicated by the coded fault type CF-TYPE, i.e. "255" (line-12). The first abnormal sequence is recognized when valve V₂ turns on normally (column-37), and the fault event counter CONV-FAULT is incremented by six per cycle (line-17). The calculated firing angle, i.e. 166°, printed out on line-19, is used to delay valve V₁ firing.

Valve V₃ is fired as normal (columns 43 and 78), since valve V₁ prolongs conduction after crossing C₄ (column-34) due to increased direct line-current. Namely, valve voltage v₃ is "positive" because of
the simultaneous conduction of valves $V_1'$, $V_2'$, and $V_5'$. Further three-phase short-circuits occur when valves $V_3$ and $V_4$ turn on (columns 43 and 49, respectively).

Fig. 5.64 shows a specification of a single commutation failure CF$_{5,1}$ and a misfire MF$_3$ (i.e. valve $V_3$ blocking) in the same cycle.

The minimum de-ionization mode "Min" is specified in line-20, and the minimum de-ionization time ($5^\circ$) is altered and set in line-17. The calculated firing angle, i.e. $175^\circ$, is given in line-19.

The fault simulation has been carried out and the result is immediately displayed on the top-half of the screen. As described in Section 5.3.2.3 (Fig. 5.20), this example displays a case of incomplete transfer of the current to the incoming valve $V_1'$. Line-17 shows that the fault-event counter CONV-FAULT is set to "5". The coded fault type CF-TYPE, i.e. "105", is indicated in line-12.

The same result is reproduced on the bottom-half of the screen in Fig. 5.65 and a pre-programmed commutation failure CF$_{5,1}$ sequence is displayed on the top-half of the screen. Although the selected display resolution is $10^\circ$ per column, the recorded fault sequences can be clearly evaluated.

Line-24 in Fig. 5.65 and line-12 in Fig. 5.64 show that the recorded delay angle $\alpha_1$ is $175^\circ$ in the simulated second cycle. The display also shows an increase in direct current $I_d$ (from 0.42 A to 0.54 A) and a decrease in direct (terminal) voltage $V_d$ (from 62.1 V to 25.0 V) per cycle.

Fig. 5.66 shows a specification of double-successive commutation failure CF$_{5,1}$ and CF$_{6,2}$. The second commutation failure is delayed by one cycle, and the specified minimum de-ionization mode applies to both commutation failures.

The simulated result, shown on the top-half of the screen, clearly illustrates that the first commutation failure CF$_{5,1}$ occurs in
the first cycle followed by the double successive commutation failure \( \text{CF}_{5,1} \) and \( \text{CF}_{6,2} \) in the second cycle.

It should be mentioned that the sampling interval is deliberately set to 3.3°, i.e. 13° per column instead of the normal 10°. This is indicated in line-17, i.e. "SampleK:120".

5.9.2.5 Sequential Convertor Shut-down. Figs. 5.67 and 5.68 show a specification of a by-passing mode of firethrough \( \text{FT}_4 \) and a multiple misfire (i.e. valve blockings, \( \text{MF}_2 \), \( \text{MF}_3 \), \( \text{MF}_5 \), and \( \text{MF}_6 \)) in the same cycle.

The demonstration has been carried out during rectification and inversion and the corresponding results are shown on the top-half of the screen in Figs. 5.67 and 5.68, respectively. Delayed by-passings have also been tested. Those test results completely agree with the theoretical waveforms described in Section 5.2.5.1.

5.9.2.6 AC Fault Simulation and Fast Convertor Shut-down. Figs. 5.69 and 5.70 show the test results of an a.c. fault followed by a fast convertor shut-down demonstrated by a built-in test programme TEST65.PLM. The fault actuator is connected to the red-phase at the convertor busbar in series with a non-inductive resistor of small value. The short-circuit-ratio of the receiving a.c. system is set to 10. The a.c. fault is applied during inversion and the shut-down is ordered about three cycles after the application of the a.c. fault (shown in Fig. 5.70). The programme includes the 'implicit' mode of data recording and the recording is kept going before the a.c. fault application, and the convertor operating-state is monitored.

Because of the relatively strong a.c. system represented in this case the a.c. fault causes no consequential convertor faults. When the shut-down is applied, the fault recording is terminated. The recorded valve ON/OFF sequences are shown on the bottom-half of the screen in Fig. 5.69, and the pre-fault convertor state is retained on the top-half
of the screen. The relevant voltage waveforms, i.e. a.c. voltage $e_d$ and direct bridge voltage $v_d$ are shown in Fig. 5.70. It can be seen that the fast shut-down (P-INT0) is applied shortly after valve $V_3$ turns on (column-51 in Fig. 5.69) or valve $V_1$ turns off (column-52). In either case the fast shut-down is applied when valves $V_2$ and $V_3$ are left conducting in column-52. Provided that all valves are operating normally, the by-pass pair $V_3$ and $V_6$ is selected. If the fast shut-down is applied when only two successive valves are conducting, the shut-down processing takes a minimum of $3^\circ$ (167 $\mu$s).
Fig. 5.59  Convertor Operating-State Monitoring (Top-half Screen) and Typical C-STATE and ON-STATE Sequence Printed out by a Built-in Test Programme TEST12.PLM (Bottom-half Screen).

Fig. 5.60  Multiple Misfire Simulation during Rectification: Unprotected Rectifier Blocking while DC-Line Charged and the Receiving End Short-circuited.
**Fig. 5.61** First Permanent- and Second Repetitive-Firethrough Simulation: Repeating.

**Fig. 5.62** Delayed Repetitive Firethrough Simulation: Non-Repeating.
**Fig. 5.63** Two-cycle Commutation Failure Simulation: Additive Delay Mode "Add".

**Fig. 5.64** Single Commutation Failure Simulation and Valve V3 Blocking: Minimum De-ionization Mode "Min".
Fig. 5.65 Comparison between the Pre-programmed Commutation Failure Sequence (Top-half Screen) and the Simulated Result in Fig. 5.54 (Bottom-half Screen).

Fig. 5.66 Delayed Double-Successive Commutation Failure Simulation: Minimum De-ionization Mode "Min", "SampleK (LD-TIM0): 120". N.B. Data recording interval is deliberately set to 3.3 degrees.
Fig. 5.67 Sequential Rectifier Shut-down Demonstration:
By-passing Mode of Firethrough "B", and Multiple Valve Blocking.

Fig. 5.68 Sequential Inverter Shut-down Demonstration:
By-passing Mode of Firethrough "B", and Multiple Valve Blocking.
Fig. 5.69 Fast Inverter Shut-down during a Receiving AC-System Fault Demonstrated by a Built-in Test Programme TEST65.PLM.

(a) $e_a$ 200V/div.

(b) $v_d$ 30V/div.

Time Scale 2 cycles/3 divs.

Fig. 5.70 AC-System Voltage-waveform (Red Phase) and Direct Voltage Waveform at the DC Terminal:
SCR = 10, 18% Peak-voltage Reduction.
5.10 CONCLUSIONS

The normal HVDC convertor operation has been summarized and a detailed sequential convertor shut-down method described and demonstrated on the convertor model. Under the normal operating condition, the shut-down method provides a smooth reduction of the direct voltage. However, its application may be limited during severe a.c./d.c.-system disturbances. Based on the conducting states of convertor valves, an alternative shut-down method has been demonstrated.

A comprehensive analysis and classification of HVDC faults has been carried out with detailed indication of the ON/OFF sequences. In addition to the convertor faults normally found in HVDC schemes, consequential inverter faults have been included with expected valve ON/OFF sequences stated. The classified faults provide the bases for a comprehensive fault simulation scheme, as well as direct digital fault detection and protection schemes.

A simple hardwired fault simulator unit has been designed for the convertor model. This has provided the basis to assess the advantages and limitations of hardwired-based fault simulators and has led to the development of the multimicroprocessor-based scheme.

Based on the classified HVDC faults, an interrupt-driven multiple microprocessor system has been set up for fault simulation and data acquisition. The system is capable of efficient operator/system interaction as required for the fault simulation and graphic display of the recorded data in real time. The software-based fault simulator fulfils most of the requirements set aside for the development of new or alternative digital HVDC control and protection schemes.

A fast and interactive data acquisition scheme has also been developed. In addition to monitoring the convertor operating-state on a regular basis, the scheme allows displaying the recorded fault-data
upon the immediate recognition of any sequential convertor fault. The speed and resolution of the sampled interval, i.e. $2.5^\circ$, is quite adequate for the analysis of abnormal ON/OFF sequences.

Complete programme listings are separately documented in a programme manual (146) which also includes system set-up procedures, input/output ports specification, and summary of the parameter values specification and fault simulation modes.

The complete circuit diagram and detailed operating instructions of the simple fault simulator is also included in the convertor manual (101).
CHAPTER 6

POTENTIAL APPLICATIONS OF MICROPROCESSORS IN THE
DETECTION AND PROTECTION OF HVDC CONVERTOR FAULTS

6.1 INTRODUCTION

Present HVDC protection systems (46-48) are greatly influenced by the relay-based protection philosophy of a.c. systems with a few exceptions like the case of a d.c.-line short-circuit, which relies on fast firing angle control. Although electromagnetic relays have been gradually replaced by faster and more reliable solid state relays in recent HVDC schemes, (57,69,84,117,118) the present practice of convertor protection is primarily based on continuous monitoring of voltages and currents on both sides of the convertors. This trend has continued with the thyristor-based HVDC technology. In spite of the extensive development of high-powered thyristor schemes, (102,103,105,107) little attention has been given to detailed diagnostic protection of the convertor plant.

However, an early research project (by Morales) (56,147) demonstrated the possibility of eliminating the by-pass valve, and a digital detection scheme was proposed by Reeve. (123,148) Further work by Arrillaga and Galanos demonstrated the need for fault-history memory storage in order to provide exact diagnosis of convertor faults. (11,149) With recent development in the microelectronics technology the prospects for direct digital protection schemes have improved considerably. With this aim a basic multimicroprocessor-based system has been described in Chapter 5.

Some special applications, illustrating the great potential of the new technology, are described in this Chapter with reference to
HVDC convertor protection.

6.2 COMMUTATING VOLTAGE INTEGRAL FOR PREVENTION OF INITIAL COMMUTATION FAILURES

The significant role played by the commutating voltage integral has already been described in Section 2.3.2.1 (Fig. 2.5).

In order to minimize the probability of commutation failures during inversion, a predictive triangular approximation of the commutating-voltage integral (Fig. 2.7) has been used in the ASEA's HVDC control system (Section 2.3.3.2). A more exact real-time voltage integral can be achieved by means of fast A/D convertors together with an interrupt-driven microprocessor-based system and this can be incorporated in a direct digital control scheme.

The voltage integral relevant to the proposed technique is shown by the hatched area in Fig. 6.1. Equidistant firing angle control is assumed and angle $\alpha_3$ is subjected to a required firing adjustment (i.e. an early firing) due to a sudden reduction in the commutating voltage $e_{ab}(\text{RY})$ governing extinction angle $\text{EA}_1$. The decision is made at instant B. To eliminate the effect of commutation notches, the voltage integral between Z and A is not used. Instead, that time interval could be used to execute any initialization routine required prior to enabling an interrupt service routine at instant A; however, if the processing time required for this initialization routine is larger than the overlap angle, that time interval has to be increased.

The structure of the required interrupt service routine should be similar to the I-INT65 used for the fault-data recording described in Section 5.8.2.2. Namely, it should read the A/D-converted commutating voltage at short and regular intervals, say, 1° to 2°. In order to minimize the calculation time of the voltage integral, a
Fig. 6.1 Typical 6-pulse Inverter under Equidistant Firing Angle Control with Trapesoidal Approximation of a Voltage Integral:

(a) Positive and Negative Direct Voltages with respect to the Transformer Neutral,
(b) Voltage across Valve V1, and Commutating Voltages,(c), (d) Valve Currents \(i_1\) to \(i_6\).
multi-step trapezoidal approximation \(^{(150)}\) should be used in real-time microprocessing.

After several sampling intervals, the current value of the voltage integral is compared with the value stored in the previous cycle. The comparison should be repeated two or three times between instants A and B in Fig. 6.1, and the difference should be used to provide the appropriate firing advance.

6.3 ABNORMAL CONVERTOR OPERATING MODES

6.3.1 Operating-Mode Declaration Routine

To complement the normal convertor operating modes described in Section 5.8.1.1, a further routine has been developed and included in the interrupt service routines P-INT1 and P-INT2. This is shown by the detailed structure diagram in Fig. 6.2. An additional coded parameter is used to declare the appropriate mode.

Part of the convertor operating-mode declaration routine, i.e. Fig. 6.2a, is executed whenever the sequential convertor fault is recognized by the process controller, as described in Section 5.8.2.4 (Fig. 5.57). First of all, the latest ON-STATE is read in and checked. If no valves are left conducting, it is immediately declared that the convertor is in the "blocking(BLK)" state. This is because the P-INT1 will not be executed until any valve(s) start conducting. By checking a convertor-blocking request signal, it should be possible to declare whether the convertor is erroneously blocked.

Any abnormal conduction pattern which does not include a by-pass pair is immediately declared as a "faulty(FLT)" state. The absence of by-passing is included because convertor misfires and commutation failures usually involve this condition within a cycle. Therefore, the by-passing mode is separately declared based on the commutating-voltage-
Fig. 6.2 Detailed Structure Diagram of Converter Operating-Mode Declaration Routine:
(a) Part of the Declaration Routine in P-INT1,
(b) Part of the Declaration Routine in P-INT2.
zero crossings in the P-INT2, as follows.

The complementary part of the convertor operating-mode declaration routine, i.e. Fig. 6.2b, is executed near the end of the P-INT1, as described in Section 5.7.3 (Fig. 5.48). First of all, the latest ON-STATE is read in and the existence of by-passing is checked. If it exists (subroutine YES-BYP in Fig. 6.2b), a "by-passing" state is tentatively declared and the relevant by-pass pair is stored, i.e. a parameter BYPASSING is set to 001001B (i.e. by-pass pair V_1 and V_4), 010010B (i.e. V_2 and V_5), or 100100B (i.e. V_3 and V_6). The "by-passing(BYP)" mode is confirmed if the same by-pass pair is still conducting after three successive crossings (i.e. half a cycle). By checking a convertor-bypass request signal, it should be possible to declare whether the convertor is erroneously by-passed. Erroneous by-passing can be caused by a double-not-successive inverter misfire MF_1 and MF_{i+3}, as described in paragraph (vi) of Section 5.3.2.1. In such case, the convertor is kept by-passing for more than five crossings through valves V_{i+1} and V_{i+4}.

The following processing stage involves the declaration of a normal state condition. This is done first by eliminating the "blocking(BLK)" state in the presence of conducting valves (subroutine NO-VALV in Fig. 6.2b). This declaration subroutine acts as a back-up, since the blocking state is declared first in the P-INT1 (subroutine DEC-BLK in Fig. 6.2a).

In the next stage the possibility of a "faulty(FLT)" state is eliminated. Namely, if the fault-event counter CONV-FAULT is incremented between the two successive crossings C_{i-1} and C_i and also the existence of either by-passing or blocking is excluded, the "faulty(FLT)" state is immediately declared (subroutine FAULTY in Fig. 6.2b). This subroutine is also selected if valve V_{i+1} is conducting at crossing C_i.
If none of the conditions stated above are met, a "normal" state is tentatively declared. If this state is held over a cycle (i.e. six successive crossings) the "normal(NOR)" mode is confirmed. This delay is necessary because the "by-passing" mode declaration requires a minimum of three crossings and the possibility of double-not-successive misfires can not be excluded. A faster normality declaration would be possible if the ordered operating mode was confirmed by other means, e.g. by a supervisory convertor-operation controller.

6.3.2 Typical Test Result

Although the normal and abnormal convertor operating-modes are derived independently, the software-based fault simulator is used to demonstrate the "faulty(FLT)" state in line-2 of Fig. 6.3. Two commutation failures $CF_{1,3}$ and $CF_{5,1}$ are specified in the additive delay mode. The fault simulation, carried out during inversion, is illustrated in Fig. 6.3 while the fault is on. (Note that if the first commutation $CF_{5,1}$ occurs, the second commutation $CF_{1,3}$ does not.)

The data recording has been completed (line-25) while the convertor operating-state is monitored on the top-half of the screen. It can be seen that the "faulty(FLT)" state is indicated in line-2 instead of the normal operating mode "Inv". In this case the parameter BYPASSING is tentatively set to 010010B (i.e. valves $V_2$ and $V_5$) due to the commutation failure $CF_{5,1}$ (not shown in Fig. 6.3).

The alternative declaration, i.e. "BLK" or "BYP" if appropriate, would be shown instead of "FLT" in Fig. 6.3.
6.4 SEVERITY ASSESSMENT OF CONVERTOR FAULTS FOR THE FAST CONVERTOR SHUT-DOWN

6.4.1 Fault-Severity Assessment Routine

Although an exact discrimination of sequential convertor faults is not provided, it has already been shown in Chapter 5 that the relative increment of the fault-event counter CONV-FAULT provides a good indication of fault severity. By imposing a limit on the number of fault events, various repetitive and/or permanent faults can be detected to decide whether the convertor should be shut down. Assuming that the convertor valves are already protected against various mal-operations, this technique should be capable of providing back-up protection.

The abnormal conduction of valve $V_{i+1}$ after $C_i$ should be used
as the highest level of protection because this fault condition could lead to either a large reduction of the direct voltage or to the appearance of a.c. fundamental component on the d.c. side. The latter condition is typically caused by a double-successive convertor fault.

In order to demonstrate fast convertor shut-down under various fault conditions and to evaluate the two protection principles mentioned above, a fault-severity assessment routine has been included in the interrupt service routines P-INT1 and P-INT2. The required parameter specification for such routine must be carried out during the fault specification described in Sections 5.5.3.2 and 5.7.4.1. Namely, by typing VDU key "M" and answering "Y" for "Yes", the fast convertor shut-down is requested and then enabled when the fault simulation is started.

The operator must specify the limit FK-SPEC for the relative increment of the fault-event counter CONV-FAULT between 1 and 99. The specified number is printed out in columns 17 and 18 of line-21 (refer to Fig. 6.5 in Section 6.4.2).

The relevant algorithm of the fault-severity assessment routine is shown by the main structure diagram in Fig. 6.4. Part of the routine, i.e. subroutine CHCK-SD in Fig. 6.4a, is executed whenever an abnormal convertor sequence is recognized in the P-INT1, as described in Section 5.8.2.4 (Fig. 5.57). When the specified fault is simulated and the fast convertor shut-down is requested and enabled as mentioned above, the relative increment of the fault-event counter is compared with the specified limit FK-SPEC. When the specified limit is reached, the fast convertor shut-down is applied and kept reinforced until the fault simulation is terminated. Further request of the subroutine CHCK-SD (Fig. 6.4a) is disabled. Since the process controller is used for two different tasks, i.e. blocking and firing the relevant valves through the same input/output ports, the fault service routine relevant to the
Fig. 6.4 Main Structure Diagram of Fault Severity Assessment Routine:

(a) Part of the Fault Severity Assessment Routine in P-INT1 (Fig. 5.57),
(b) Part of the Fault Severity Assessment Routine in P-INT2 (Fig. 5.48).
convertor fault(s) must be disabled. Provided that all valves are operating normally, this should cause no difficulty whenever a single processor is used for the protection tasks. The application of the fault actuator should only be cancelled when the fault simulation is terminated.

Another part of the routine, i.e. subroutine CKSEQ1 in Fig. 6.4b, is executed at each crossing C_i in the P-INT2, as described in Section 5.7.3 (Fig. 5.48). First of all, the latest ON-STATE is read in and the conducting state of valve V_{i+1} is checked. If the specified valve is conducting, the fault-type parameter CF-TYPE is set up according to the coding conditions described in Section 5.8.3. Furthermore, if two successive valves V_i and V_{i+1} are conducting after crossing C_i, it is judged that a double-successive fault has occurred. Similarly to the subroutine CHCK-SD in Fig. 6.4a, the fast shut-down is only applied if it is requested and enabled (APLY-SD in Fig. 6.4b).

6.4.2 Typical Test Result — Fault Event Limit

A typical test result of a commutation failure CF_{5,1} has been described in Section 5.9.2.4 (Fig. 5.63). A similar type of fault is demonstrated in Fig. 6.5 with a two-cycle duration. The limit specified for the number of fault events, i.e. FK-SPEC = 3, is indicated in line-21, in the reverse video mode.

The demonstration has been carried out during inversion and the result is immediately displayed on the top-half of the screen. It can be seen that the fault-event counter CONV-FAULT, initially set to zero, is incremented by one when valve V_2 turns on and again when valve V_6 turns off (column-37). Therefore, when valve V_3 turns on normally (column-43), the specified fault-event limit is reached. For this conduction pattern (i.e. valves V_1, V_2, V_3, and V_5) the look-up table
BP-TABL in Appendix A2 selects the by-pass pair $V_2$ and $V_5$. In this case the by-passing state is established within $10^0$ (column-44).

The fault event counter is further incremented when the shut-down takes place. Due to the rapid increase in the direct current, a commutation failure occurs when the convertor is re-started (the re-start is not shown in Fig. 6.5). The final count "10" is indicated in line-17.

It has been confirmed that, by varying the fault-event limit FK-SPEC between 1 and 99, the fast convertor shut-down can be applied at various stages of non-successive repetitive/permanent fault developments. The FK-SPEC is limited to "99" simply because most of the bottom-half of the screen space is used for the fault simulation purposes.
6.4.3 Typical Test Results — Double Successive Fault

A typical test result of a double-successive commutation failure \( CF_{5,1} \) and \( CF_{6,2} \) has been described in Section 5.9.2.4 (Fig. 5.66). A similar type of fault is demonstrated in Fig. 6.6 with a two-cycle duration. The fault-event limit FK-SPEC is deliberately set to the maximum value, i.e. "99".

The demonstration has been carried out during inversion and the result is immediately displayed on the top-half of the screen. The relevant voltage waveforms, i.e. a.c. voltage \( e_a \) and direct bridge voltage \( v_d \), are shown in Fig. 6.7. In this case the fast convertor shut-down is enforced by the subroutine CKSEQ5 in the P-INT2 (Fig. 6.4b) as follows.

At crossing \( C_4 \) (column-32 in Fig. 6.6) valve \( V_5 \) is conducting due to the first commutation failure \( CF_{5,1} \). This is recognized by the subroutine CKSEQ4 in the P-INT2. At the following crossing \( C_5 \) (column-38) valve \( V_6 \) is also conducting due to the second commutation failure \( CF_{6,2} \). (This is indicated by the coded fault type "265" in line-12.) Since two successive valves \( V_5 \) and \( V_6 \) are conducting after \( C_5 \) and the convertor shut-down (already requested) is enabled, the shut-down subroutine (APLY-SD in Fig. 6.4b) is immediately applied. The by-pass pair \( V_2 \) and \( V_5 \) is then selected among the four conducting valves, i.e. \( V_1, V_2, V_5, \) and \( V_6 \) by the look-up table BP-TABL in Appendix A2.

Although valves \( V_2 \) and \( V_5 \) are kept fired while the others are blocked, after crossing \( C_5 \) the anode-to-cathode voltage of valve \( V_2 \) becomes "negative" and as a result the direct current is commutated back from valve \( V_2 \) to valve \( V_6 \). Therefore two successive valves \( V_5 \) and \( V_6 \) are left conducting and the phase-to-phase voltage \( e_{cb} \) (BY) appears across the d.c. terminals for about half a cycle, as shown in Fig. 6.7b.
Fig. 6.6 Fast Inverter Shut-down due to Double-Successive Commutation Failure Simulated.

(a) $e_a$ 200V/div.

(b) $v_d$ 50V/div.

Time Scale 10ms/div.

Fig. 6.7 AC-System Voltage-waveform (Red Phase) and Direct Voltage Waveform at the DC Terminal: SCT = 10, Simulated Fault Duration = 2 Cycles.
During this period, the gate-to-cathode voltage (of valve $V_2$) does not provide sufficient information to detect this condition, as shown by the apparent continuous conduction of valve $V_2$ in the top-half of the screen (line-7). In this particular case it is thus necessary to add anode-to-cathode voltage information to the firing circuit if the interval of current discontinuity is to be recognized. A final commutation from valve $V_6$ to valve $V_2$ takes place immediately after crossing $C_2$ (column-56) and the by-passing state is established in column-58. The convertor is re-started when the specified fault duration is over (Fig. 6.7).

Fig. 6.8 shows a specification of a.c./d.c. fault for five cycles with the fault-event limit set to "99". The fault actuator is connected to the red-phase at the convertor busbar and the short-circuit-ratio of the receiving a.c. system is set to 5. The a.c. fault is delayed from crossing $C_1$ by $5^\circ$.

The demonstration has been carried out during inversion and the result is immediately displayed on the top-half of the screen. The relevant voltage waveforms, i.e. a.c. voltage $e_a$ and direct bridge voltage $v_d$, are shown in Fig. 5.9. Line-3 of Fig. 6.8 shows a triple crossing caused by a voltage dip at the initial stage of the a.c. single-phase fault. The second and third crossings are ignored (column-18 and column-19, respectively). It can be clearly seen that due to the delayed firing caused by the distorted waveform a consequential commutation failure $CF_{5,1}$ occurs first which is followed by a misfire $MF_6$. Because two successive valves $V_4$ and $V_5$ are conducting after $C_4$ (column-38) and the convertor shut-down (already requested) is enabled, the shut-down routine (APLY-SD in Fig. 6.4b) is immediately applied. The by-pass pair $V_2$ and $V_5$ is then selected by the look-up table BP-TABL in Appendix A2.
Fig. 6.8 Fast Inverter Shut-down due to Commutation Failure CF_5,1 and Misfire $M_F^6$ Caused by AC Single-phase Fault.

(a) $e_a$ 200V/div.

(b) $v_d$ 50V/div.

Time Scale 10ms/div.

Fig. 6.9 AC-System Voltage-waveform (Red Phase) and Direct Voltage Waveform at the DC Terminal: SCR = 5, 22% Peak-voltage Reduction.
Similarly to the case of Fig. 6.6, there is a temporary commutation from valve V₂ to valve V₄ not shown in Fig. 6.8 (line-7). The by-passing state is finally established when commutation from valve V₄ to valve V₂ takes place immediately after crossing C₁ (column-56).

6.5 CONCLUSIONS

Several examples of convertor abnormal operating conditions have been demonstrated in this Chapter, to illustrate the detailed information provided by the multimicroprocessor-based system. The results have highlighted the need to incorporate anode-to-cathode voltage information (already provided in actual HVDC schemes) within the protection logic. Without it, some cases of temporary current discontinuity can pass undetected. The very fact of its detection illustrates the great potential of the proposed interactive microprocessor system as a development tool.

Since the OFF state is indicated by negative gate-to-cathode voltage, the firing pulse must be removed whenever the anode-to-cathode voltage becomes negative. This facility can be easily incorporated in the firing logic of the experimental convertor model.
CHAPTER 7

CONCLUSIONS

The first part of the thesis has described the development of a scaled-down model of an HVDC convertor, which, besides the basic convertor components, includes many other features essential for the purpose of the investigation, e.g. a.c. and d.c. harmonic filters, variable a.c. system strength, duration-controllable fault actuation, etc. Because of its experimental nature, the model has been provided with extra flexibility to accommodate various types of manual and automatic analogue, digital (hard-wired logic) and microprocessor controls. This has been achieved partly by the use of a modular design and partly by the provision of many accessible points in the front panels.

In view of the main prospective application of the model, namely microprocessor control and protection, much effort has been devoted to the design of suitable transducers. In particular a novel principle of the state of each valve, i.e. ON and OFF level detection, has been thoroughly investigated and the measure of success achieved described in detail.

In the second part of the thesis, the scaled-down model has been complemented with an interrupt-driven multiple microprocessor system. Prior to its use as an HVDC controller, considerable work has been done on the development of monitoring facilities which include the normal and abnormal convertor states, indication of the operating modes, i.e. rectification, inversion, blocking, by-passing, as well as the various voltages and currents. The multiprocessing scheme has been applied to the classification, simulation and assessment of HVDC convertor disturbances and many tests have been carried out to demonstrate its performance in
this area. Perhaps the main contribution has been the real-time processing of information and the development of comprehensive interactive sampling, specifically designed to provide a clear intuition of the convertor behaviour as well as highly accurate information of the development of convertor disturbances.

A comprehensive software package of typical convertor, a.c. and d.c. system faults is now available which can be used as a standard test set to assess the performance of alternative control and protection schemes. With the prospective addition of further parallel processors and the use of more powerful microprocessor developments, such as the Intel's 8088 and 8086, the present system can be extended to provide completely integrated direct digital control and protection facilities.

Moreover, the flexibility of the hardware model and of the microprocessor software provide an ideal development system for the investigation of new ideas in the field of HVDC control and protection.

Finally, the high level of information locally derived at each convertor, being already in digital form, can be easily transmitted to other terminals to provide a co-ordinated control of the overall HVDC system.
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Santa Clara, California, October 1979.


APPENDIX A1

Memory Map of the Multimicroprocessor-based Fault Simulation and Data Acquisition System

N.B. Increment of the address scale is arbitrary.

**iSBC 80/30 On-Board EPROM's**

<table>
<thead>
<tr>
<th>Address</th>
<th>Memory Contents</th>
<th>Functions</th>
</tr>
</thead>
</table>
| 0 0000H | Monitor Programmes | Interactive Controller Monitor
| 1K 0400H |                  | Process Controller Monitor |
| 2K 0800H |                  | Not in use. |
| 8K 2000H |                  | Not available. |
| (3FFFH) |                  |           |

**iSBC 80/30 Interactive Controller Board 16 K RAM**

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<th>Functions</th>
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<td>16K 4000H</td>
<td>I-INTJ.ASM</td>
<td>Vectored Interrupt Jump Table, Stack and Data Segment for Monitor</td>
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<td>403FH</td>
<td>I-INTJ.ASM</td>
<td></td>
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<td>4100H</td>
<td>I-BEGIN.ASM</td>
<td>Initialization Routines</td>
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<td>I-INT0.ASM</td>
<td>To Start Fault-Data Acquisition</td>
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<td>I-INT1.ASM</td>
<td>To Read Converted 8-bit Data</td>
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<td>To Sample Sequential Fault Data</td>
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<td>To Record Convertor-State Data</td>
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<td>I-MMMAIN.PLM</td>
<td>Main Programme</td>
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<tr>
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<td>DISPLY.PLM</td>
<td>Convertor-State Monitoring</td>
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<td>F-SPECN.PLM</td>
<td>Fault Specification Subprogramme</td>
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<tr>
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<td>To Show Pre-programmed Sequences</td>
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<td>SHOW-SQ.PLM</td>
<td>To Show Recorded Fault Data</td>
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<td>XCHG-SQ.PLM</td>
<td>To Exchange Two Memory Blocks</td>
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<td>TEST-65.PLM</td>
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<td>TEST-12.PLM</td>
<td>To Test ON1 and Ci Sequences</td>
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<td>To Give VDU Screen Information</td>
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<td>D-BASEI.ASM</td>
<td>Common Data Base</td>
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### iSBC 80/30 Process Controller Board 16 K RAM

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<td>P-IN3 .ASM</td>
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**16K RAM Memory Board**

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<td>FSPECN-FRAME</td>
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<td>64K (FFFFH)*</td>
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Interrupt Service Routine P-INTO

$ TITLE ('Process Controller; Fast By-passing Based on Valve "ONi")
$ MACROFILE MOD85

;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
; Process Controller                      Vn.1.1   22 May, 1982
; Module PINTO                            Power Systems Group, UC
; ============
;
; This module is related to Fast By-passing Operation based on
; valve ON/OFF states (OF-STAT) which are read-in from the Port 2A.
;
; The module is designed as an interrupt service routine INT0,
; however, it is practically used as a procedure which can be called
; elsewhere by the Process Controller.
; ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;
; NAME PINTO
PUBLIC INT0, INIT0

EXTRN FASTSD, FASTBP, PERROR ; Stored in Common Data Base

; ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
; GLOBALS ; To equate the Names to actual values
;
EOI      EQU 020H ; Non-Specific End of Interrupt
ICNTRL   EQU 028H ; On-Board Interrupt Controller 8259A Control Port
IMASK    EQU 029H ; PIC-P 8259A Interrupt Mask Port
PORT2A   EQU 0C4H ; External PPI-20 8255A OF-STAT Data Input Port 2A
BPRTEB   EQU 0B8H ; Port E8 for BLK1/ TRG & AB7/ Output Signals
FPRTEA   EQU 0EAH ; Port EA for PRI/ FP7/ & EDDC/ Output Signals

; ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;
CSEG ; Code Segments
;
; To set up the Mode to Receive Interrupt Level 0
;
INIT0:
; IN    IMASK ; Enable PIC-P 8259A Interrupt Level 0
; ANI   NOT 1B
; OUT   IMASK ; N.B. Now suspended.
RET
To process Interrupt Level 0 (Interrupt Service Routine P-INT0)

`INTRO:`
PUSH PSW ; Save register A and Processor Status Word
PUSH D ; Save register pair D, E
PUSH H ; Save register pair H, L

`BPENFC:`
LDA FASTBP ; Is Fast Bypass-pair Firing requested ?
DCR A ; i.e. FAST-BP = 01B ?
JNZ SDREQT ; No, check if Fast Shut-down is requested
; Yes, at first find out a correct By-pass Pair
STA FASTSD ; Re-initialize FAST-SD = 0B (False), (A) = 0

IN PORT2A ; Read present Valve ON/OFF States OF-STAT
ANI 00111111 ; Conditioning for ONi, i.e. clear Bits-6 & -7
; N.B. OF-STAT = ON-STATE in the main text.
LXI H, BPTABL ; Find out an appropriate By-pass Pair
MOV E, A
XRA A ; (A) = 0
MOV D, A ; (D, E) = (0, OF-STAT)
DAD D ; (H, L) = .BP-TABL + OF-STAT (Offset)
; N.B. "BP-TABL" denotes the address value.
MOV A, M ; Find out the coded number, (A) = 1, 2, 3 or 0
DCR A ; Is it 1 ?
JZ BPTK14 ; Yes, (A) = 1: Fire Valves V1 and V4
DCR A ; Is it 2 ?
JZ BPTK25 ; Yes, (A) = 2: Fire Valves V2 and V5
DCR A ; Is it 3 ?
JZ BPTK36 ; Yes, (A) = 3: Fire Valves V3 and V6
JMP ENDNOW ; No, (A) = 0: No Firing/Blocking required
; N.B. Normal Valve Firing/Blocking assumed.

`BPTK14:`
IN FPRTEA ; Read-in the present Firing Port EAH states
ANI 00000011B ; Retain Signals FP7/ and EDDC/
ADI 10010000B ; i.e. (A) = 100100??B
OUT FPRTEA ; Fire V1 and V4 only

IN BPRTE8 ; Read-in the present Blocking Port E8H states
ANI 00000011B ; Retain Signals TRG and AB7/
ADI 01101100B ; i.e. (A) = 011011??B
OUT BPRTE8 ; Block other valves, i.e. V2, V3, V5, & V6
JMP ENDNOW

`BPTK25:`
IN FPRTEA ; Read-in the present Firing Port EAH states
ANI 00000011B ; Retain Signals FP7/ and EDDC/
ADI 01001000B ; i.e. (A) = 010010??B
OUT FPRTEA ; Fire V2 and V5 only

IN BPRTE8 ; Read-in the present Blocking Port E8H states
ANI 00000011B ; Retain Signals TRG and AB7/
ADI 10110100B ; i.e. (A) = 101101??B
OUT BPRTE8 ; Block other valves, i.e. V1, V3, V4, & V6
JMP ENDNOW
BPTK36:

IN BPRTE8 ; Read-in the present Blocking Port E8H states
ANI 00000011B ; Retain Signals TRG and AB7/
ADI 11011000B ; i.e. (A) = 110110??B
OUT BPRTE8 ; Block other valves, i.e. V1, V2, V4, & V5
JMP ENDNOW

; << Shut-down Request Subroutine >>

SDREQT:

LDA FASTSD ; Is Fast Shut-down requested ?
RRC ; i.e. FASD-SD = 1B (True) ?
JNC ERROR5 ; No, erroneous call was made!
; Yes, proceed for immediate blocking

IN PORT2A ; Read present Valve ON/OFF States OF-STAT
ANI 00111111B ; Conditioning for ONi, i.e. clear Bits-6 & -7

LXI H, BKTABLE ; Find out the non-conducting valves:
MOV E, A ; Use a Look-up Table BK-TABL
XRA A ; (A) = 0
MOV D, A ; (D, E) = (0, OF-STAT)
DAD D ; (H, L) = BK-TABL + OF-STAT (Offset)

IN BPRTE8 ; Read in the Blocking Port E8H States
ORA M ; Reserve the TRG (Bit-1) and AB7/ (Bit-0) states
OUT BPRTE8 ; Block the selected non-conducting valves, now!

MVI A, 01B ; Enable the By-pass Enforcement Subroutine for
STA FASTBP ; a next call, i.e. FAST-BP = 01B

; ENDNOW:

POP H ; Protected end of the Interrupt 0
POP D

; MVI A, EOI ; Reset the ISR bit of On-board PIC-P 8259A
; OUT ICNTRL ; N.B. Now suspended.
POP PSW
RET

; ERROR5:

MVI A, 5 ; Set a flag for the erroneous call of INTRO
STA PERROR ; i.e. P-ERROR = 5 (Coded)
JMP ENDNOW
DSEG ; Data Segments for Control Transfer

BKTABL: ; Look-up Table for the valves to be blocked

; OF-STAT = 000000B 000001B 000010B 000011B 000100B
DB 11111100B, 01111100B, 10111100B, 00111100B, 11011100B
; Block V3-V6

; ON1 & ON2
DB 000101B 000110B 000111B 001000B 001001B
DB 01011100B, 00111100B, 11111100B, 01111100B, 10111100B

; DB 001010B 001011B 001100B 001101B 001110B
DB 01010100B, 01010100B, 10010100B, 00010100B, 11010100B

; DB 001110B 001111B 100000B 100001B 100010B
DB 01000100B, 1000100B, 0001000B, 11000100B, 01000100B

; DB 100011B 100100B 100101B 100110B 10011B
DB 0011000B, 1101100B, 0101100B, 1001100B, 0001100B

; DB 101000B 101001B 101010B 101011B 101100B
DB 1110100B, 01110100B, 10110100B, 00110100B, 11101100B

; DB 101101B 101110B 101111B 110000B 110001B
DB 0100100B, 1000100B, 0001000B, 11110000B, 01110000B

; DB 110010B 110011B 110100B 110101B 110110B
DB 0110000B, 1011000B, 0011000B, 1101000B, 0010000B

; DB 110110B 111000B 111001B 111010B 111011B
DB 0001000B, 1110000B, 0110000B, 1010000B, 0010000B

; DB 111100B 111101B 111110B 111111B
DB 1100000B, 0100000B, 1000000B, 0000000B
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END
APPENDIX A3

Interrupt Service Routine I-INT65

$TITLE ('Interrupt Level 6.5 to Record Convertor Operating Information')
$ MACROFILE MOD85

; Parameters STRT-SQ to CY-NUM are defined in sequence in Data Base
; Initially SPL- PTR = STRT-SQ = .CY00C1,
; SAMPL-K = CY-NUM = STOP65 = 0, and ENDCY = OFFH (255).

RWT0MD EQU 0DH ; On-board 8253 Timer 0 Read/Write Port for INTR65
RWT0MI EQU 0DDH ; On-board 8253 Timer 1 Read/Write Port for INTR55
TIM0MD EQU 10H ; 00-01-000-0B Timer 0, L.S. Byte only, Mode 0, Binary
TIM1MD EQU 50H ; 01-01-000-0B Timer 1, L.S. Byte only, Mode 0, Binary

CSEG ; Code Segments

INIT65: ; Initially,
MVI A, TIM0MD ; Set up On-board Timer 0, LSB only, Mode 0
OUT TIMCNT
MVI A, TIM1MD ; Set up On-board Timer 1, LSB only, Mode 0
OUT TIMCNT
RET ; End the Timers 0 and 1 Initialization
To Process Interrupt Level 6.5 (Interrupt Service Routine I-INT65)

N.B. In order to achieve smallest possible sampling resolution (i.e. 1.8 electric degrees) a register pair D,E is not used, and Timer Count TIM-ADJ is adjusted external to a critical sampling path.

INTR65:

```assembly
PUSH PSW ; Save Register A and Processor Status Word
PUSH H ; Save Register Pair H, L

LHLD SPLPTR ; Load Sample Pointer into (H,L), directly
LDA VCSTAT ; Load Commutating-voltage-zero Crossing States
MOV M, A ; Store current VC-STAT at address SPL-PTR
 ; N.B. VC-STAT = C-STATE in the main text.
INX H ; Then increment Sample Pointer in (H,L) by one
LDA OFSTAT ; Load Valve ON/OFF States into (A), and
MOV M, A ; Store it at the incremented address SPL-PTR
 ; N.B. OF-STAT = ON-STATE in the main text.
INX H ; Further increment Sample Pointer in (H,L)
SHLD SPLPTR ; i.e. SPL-PTR = SPL-PTR + 1, and
LXI H, SAMPLK ; Store it for next sampling when IINT65 called
INR M ; Increment Sample Counter by one,
 ; i.e. SAMPL-K = SAMPL-K + 1

MVI A, 144 ; Is SAMPL-K reached one-cycle worth sampling ?
CMP M ; i.e. 144 - SAMPL-K = 0 ?
JNZ EXIT10 ; No, immediately exit for next sampling
MVI M, 0 ; Yes, reset Sample Counter, i.e. SAMPL-K = 0

MVI A, 1 ; Enable Interrupt Level 5.5 to record angles
OUT RWTIM1 ; On-board Timer I1 is used for this purpose
 ; N.B. Interrupt Level 5.5 must be completed
 ; within a cycle or about 20 ms.

LDA ENDCY ; Load End of Cycle Number END-CY into (A)
INX H ; Load Adr. of Cycle Number CY-NUM into (H,L)
CMP M ; Is End of Cycle Number reached ?
 ; i.e. END-CY - CY-NUM = 0 ?
JZ IMPSQ ; Yes, end up sampling by this INTR65
INR M ; No, increment Cycle Number by one
 ; i.e. CY-NUM = CY-NUM + 1
 ; N.B. For 'Implicit' Recording END-CY is
calculated in P-INT1.

MVI A, 14 ; Is Cycle Number reached its absolute maximum ?
CMP M ; i.e. 14 - CY-NUM = 0 ?
JNZ EXIT20 ; No, repeat sampling next cycle, too
MVI M, 0 ; Yes, reset Cycle Counter, i.e. CY-NUM = 0

LDA IMPLCT ; Is Recording Flag specified for 'Implicit' ?
DCR A ; IMPLCT = 1/0 for Implicit/Explicit Recording
JNZ EXPSQ ; No, proceed for ending the Explicit Recording
 ; Yes, process for Implicit Recording
```
IMPREC:
LDA STOP65 ; Is the Implicit Recording forced to end now?
DCR A ; i.e. STOP65 = 1 ?
JZ STOPSQ ; Yes, stop Implicit Recording, now!
LHLD STRTSQ ; No, continue the Recording from CY-NUM = 0
; i.e. STOP65 = 0
MOV A, L ; First store L. S. Byte into SPL-PTR
STA SPLPTR
MOV A, H ; Then store M. S. Byte into SPL-PTR
LXI H, SPLPTR
INX H
MOV M, A ; Thus Sample Pointer is re-initialized
; i.e. SPL-PTR = STRT-SQ = CY00C1
EXIT20:
POP H ; << End of a Cycle-worth Sampling >>
LDA TIMADJ ; Save Registers used in this Level 6.5
OUT RWTIMO ; Load Timer 10 with an adjusted timer count
POP PSW
EI ; Enable all Maskable Interrupts including this
; Return to an interrupted instruction/programme
RET
EXIT10:
POP H ; << End of the Critical Sampling Path >>
LDA LDTIMO ; Restore Registers used in this Level 6.5
OUT RWTIMO
POP PSW
EI ; Enable System Interrupts including this INTR65
; Return to an interrupted instruction/programme
; N.B. Re-entering INTR65 is prevented until
; the completion of INTR65.
;
IMPSQ:
MVI A, 1 ; Set SORT-SQ = 1 for Implicit Recording, thus
JMP END65 ; Procedure SORT-POFSEQ will be called
;
STOPSQ:
MVI A, 3 ; If stopped, set Flag SORT-SQ = 3 for "I-MMAIN"
JMP END65
;
EXPSQ:
MVI A, 2 ; Set SORT-SQ = 2 for Explicit Recording, thus
; "I-MMAIN" reports the completion of Recording
END65: STA SORTSQ ; Now store SORT-SQ, i.e. SORT-SQ = 1, 2, or 3
;
RIM ; Reserve current Masks 7.5 and 5.5
ANI 00000101B
ORI 1010B ; Set Mask 6.5
SIM ; Thus this Level 6.5 is masked (disabled)
;
POP H ; Restore Registers used in this Level 6.5
POP PSW
EI ; Enable System Interrupts including this INTR65
RET ; Return to an interrupted instruction/programme
;
END