Zinc Oxide MESFET Transistors

by

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Abstract

Zinc oxide is a familiar ingredient in common household items including sunscreen and medicines. It is, however, also a semiconductor material. As such, it is possible to use zinc oxide (ZnO) to make semiconductor devices such as diodes and transistors. Being transparent to visible light in its crystalline form means that it has the potential to be the starting material for so-called 'transparent electronics', where the entire device is transparent. Transparent transistors have the potential to improve the performance of the electronics currently used in LCD display screens.

Most common semiconductor devices require the material to be selectively doped with specific impurities that can make the material into one of two electronically distinct types – p- or n-type. Unfortunately, making reliable p-type ZnO has been elusive to date, despite considerable efforts worldwide. This lack of p-type material has hindered development of transistors based on this material.

One alternative is a Schottky junction, which can be used as the active element in a type of transistor known as a metal-semiconductor field effect transistor, MESFET. Schottky junctions are traditionally made from noble metal layers deposited onto semiconductors. Recent work at the Canterbury University has shown that partially oxidised metals may in fact be a better choice, at least to zinc oxide.

This thesis describes the development of a fabrication process for metal-semiconductor field effect transistors using a silver oxide gate on epitaxially grown zinc oxide single crystals. Devices were successfully produced and electrically characterised. The measurements show that the technology has significant potential.

Chapter 1 - Introduction

1.1 Overview of Semiconductors and Transistors

Semiconductor materials and transistors have become so pervasive in modern life, that most people, at least here in New Zealand, own thousands of pieces of semiconductor material, and billions of transistors. Yet strangely, most of those people have little idea how many they own, or even that they own them at all, and even fewer have any idea of how they work. Even less familiar is the concept of a compound semiconductor, even though very recent developments in this area have made pervasive changes in our lives.

Gallium nitride – a compound semiconductor which was only commercialised less than 20 years ago, has enabled the development of high power blue and white LEDs and lasers. These are now found everywhere – Blu-ray™ players, car dashboards, torches and personal headlights, keyring lights, even Christmas decorations. This chapter will give a brief overview of what semiconductors are, how they work, and then go into more detail of one specific area of semiconductor research – MESFET transistors made from zinc oxide. This type of transistor may have potential applications in such diverse fields as optical displays, space electronics, or geothermal monitoring.

So what is a semiconductor? A semiconductor is literally that – a partial conductor. It has an electrical conductance partway between that of a metal, which has a high conductance, and an insulator, which has a very low conductance. There are only a handful of elements which are semiconductors – for example silicon, germanium, tin and carbon (in the diamond form) which are in group four of the periodic table of the elements. The very high bandgap of diamond means that in pure form it is an insulator at room temperature, but it can be made semiconducting when doped or heated.

Silicon is by far and away the most commonly used semiconductor material, largely due to the fact that it is relatively easy to form its oxide – silicon dioxide, which is also extremely stable, and a very good insulator. That high quality insulator makes it very easy to make reliable electronic devices out of silicon. There is also a considerable amount of knowledge about the properties and processing of this material, that enables fabrication of devices. However, silicon does have some limitations – primarily due to a property called its bandgap – which is a characteristic of semiconductor materials. The bandgap of silicon is relatively small, (equivalent to light in the infra-red portion of the optical spectrum) and also 'indirect'[1]. The same is true of germanium, the only other elemental semiconductor which has been widely commercialised.

There is, however, another group of semiconductors known as 'compound' semiconductors. Compound semiconductors consist of two or more elements – usually from a pair of columns of the periodic table either side of group four: e.g. gallium arsenide is a III-V semiconductor, and zinc oxide is a II-VI semiconductor. The primary advantage of compound semiconductors is that a wider range of bandgaps are available, and more importantly, the bandgap is tunable by choosing different elements, and mixing them in different quantities. However, that added flexibility comes with an added cost, and that cost is added complexity – both in making and processing that material.

One other important property of a semiconductor, other than bandgap, is the carrier mobility. When a semiconductor conducts current, it does so by free electrons and holes moving through the material. A hole is conceptually the 'lack' of an electron, and a hole can carry current, as nearby electrons can fall into the hole, and the hole therefore moves along. Mobility is a measure of how easily those current carrying particles, or 'carriers' can move through the material. In general, a very pure material with a very regular single crystal structure will have a higher mobility, and a less pure material, with many defects or grains in the crystal, will have a lower mobility. In a perfect material, the mobility will be limited by the properties of the crystal itself, and the mobility becomes a property of that material.

A pure 'perfect' semiconductor material will have relatively few electrons or holes available in the material for carrying current. The number of these carriers can be substantially increased by adding

impurities into the material. An atom that has more than four electrons in the outer shell will provide an extra electron to a column IV semiconductor that will be available for carrying current. Such an atom is known as a donor. Material with an excess of electrons is known as n-type material. Conversely atoms that have less than four electrons in the outer shell will provide a hole in column IV semiconductors. Such atoms are known as acceptors, and material with an excess of holes is known as p-type material. Imperfections in the crystal can also sometimes act as donors or acceptors, and make the material n- or p-type.

So what is a transistor? A transistor is an electronic device made from semiconductor materials. The name is a conjunction of the phrase 'transfer resistor'. A transistor has at least three connections, or terminals. An electrical signal applied to one of the terminals can be used to control the current that flows through one or more of the other terminals. There are many types of transistor, which can be based on several different modes of operation. If a transistor is appropriately designed and constructed, it can 'amplify' the control signal, or be used to switch large amounts of current on and off.

If many of these switching transistors are connected together, in different ways, they can be used to perform different logic tasks. Those combinations of logic can be as simple as a basic boolean operation, or as complex as a complete computer, if enough individual transistors are used. These transistors are rarely connected up individually nowadays. The fabrication techniques used to make transistors have evolved so that billions of transistors can be made at once on one chip of semiconductor material, including the 'wiring' that is used to connect them together in the correct way. This collection of electronic devices is known as an 'integrated circuit'. The transistors described in this thesis are simply individual, or so-called 'discrete' transistors.

This thesis describes the development of one specific type of transistor, known as a MESFET. These transistors are made from part of a thin layer of zinc oxide, which was grown on a wafer of sapphire. The details of the process used to fabricate these transistors is described, and the electrical characteristics of the resulting working devices are presented. With some modification, these

transistors could be made visually transparent, which makes them of particular interest for developing so-called 'invisible electronics'.

1.2 Transistor History

The first proposed devices similar to what we now call transistors were proposed in the 1930s by Lilienfeld [2] and Heil [3]. It is arguable whether the devices proposed would have ever worked. There is also no evidence that either of these devices were ever actually fabricated. They were, however, quite similar in concept to what we now know as a Field Effect Transistor (FET), and the inventors generally are credited with originating the concept.

The materials suggested for these early devices were often compound semiconductors such as copper sulphide, cuprous oxide, or lead salts. At that time, workers were more familiar with the properties of such materials. Later in the 1940s, there was a shift in emphasis from compound to elemental semiconductors, as there was a belief that these would be simpler to purify and analyse. It was not until considerably later in the century that materials research went full circle, and went back to considering the compound semiconductors again.

During the war years, there was considerable work done on trying to find alternatives to the large, power hungry, high-maintenance, unreliable vacuum tubes that were being used for the simple electronic devices and computers in use at the times. There was also a demand for high-speed devices for radar applications. These potential applications led to work at Bell labs and Purdue University on germanium diodes [4]. It also led to greater understanding of the properties of semiconductors.

The first working transistor was made by Bardeen and Brattain at Bell Labs in 1947 [5]. The background technology for this device was the work done on germanium earlier. This transistor was made with point contacts, but quickly led to development of the bipolar junction transistor (BJT). The development of the junction transistor largely shifted effort away from work on field-effect devices, although some work continued, and Shockley went on to invent the junction FET (JFET) [6].

The electrical characteristics of these junction FETs were obviously measured as they were made. Theories were developed to explain the operation of these devices at that time, and those theories are still relevant to many FET devices today. Only in very small devices with channel lengths of less than 1-2 μm is it necessary to modify that theory to adequately model device behaviour.

During the early 1950s the majority of work focussed on developing BJTs and JFETs. It was not until the 1960s that significant milestones were made on other FET devices. In 1960 Dawon Kahng and John Atalla created the first practical Metal Oxide Semiconductor FET (MOSFET) [7,8]. They had discovered that oxidising the surface of silicon reduced the effect of surface states that would otherwise prevent the field from the gate electrode modulating the carrier density in the channel [9].

In 1966 Carver Mead made the first working Metal Semiconductor FET (MESFET) [10]. A MESFET uses a Schottky diode – a rectifying metal-semiconductor structure, to modulate current flow through the device. Mead's device was fabricated from epitaxial n-type gallium arsenide on a semi-insulating gallium arsenide substrate, and used tin-tellurium Ohmic contacts and an aluminium gate. All these materials were familiar, as they were in use in other device types at the time. Although the transistor curves were presented, parameters such as transconductance were not explicitly calculated. Mead recognised that Schottky barriers provide useful high quality rectifying junctions to wide-bandgap semiconductors.

Earlier in 1962 Weimer made successful Thin Film Transistors (TFTs) [11]. Unlike most semiconductor devices, TFTs are generally not made with very pure, single-crystal material. They are instead made by deposition of the semiconductor onto a relatively cheaper substrate such as glass or plastic. Consequently the deposited semiconductor material is usually polycrystalline or amorphous. Non-crystalline semiconductor material usually has considerably lower mobility than single-crystal material, and transistors made from these materials have correspondingly lower performance figures than those made from high-quality monocrystalline material, but they are considerably cheaper to manufacture.

Weimer's TFTs were made with cadmium sulphide on a glass substrate, and used gold electrodes. CdS was used because of its relatively wide bandgap, and also because it had been used extensively for photoconductive devices at that time. Gold is hardly a cheap metal to use, but was presumably used for convenience, and its chemical inertness. The shadow-masked patterning used is certainly quick and cheap. His device transconductances were up to 25 mA/V.

1.3 Transistor application areas

So where are these billions of transistors that we each own? What do they do?

By far and away the most common and numerous are the transistors in our computer processors. The Pentium®, Phenom™, Athlon™, Xeon®, etc. chips in our computers are packed with literally billions of transistors, each under 100 nm in size, and made with the most advanced mass production technology available. These transistors work at incredibly fast speeds – currently 2-3 GHz, or 2-3 billion switching cycles per second. But it is not just our computers that have processors. IPods, GPS units, cellphones, our cars, even our car stereos – all are controlled by processors, and each processor is made up of millions or even billions of transistors.

In each of these units, there is not just the processor. There are usually other chips as well that make up the device. I/O controllers, display controllers, network controllers, and memory chips are all often used, usually to interface the controller with other parts of the device. Peripheral devices such as flash memory cards have yet more chips. Each of these has thousands or millions more transistors adding to the count.

The next most numerous application area is one that has only recently become so – that of flat panel displays. These are LCD computer monitors, LCD and plasma television screens, even the LCD displays on cellphones and other portable devices. Each pixel of the display, and in fact each of the three colours of each pixel of a colour display is controlled by a transistor. Unlike the transistors in a processor chip, these transistors do not need to be extremely small, or extremely fast. What these

transistors need to be is cheap, reliable and able to be made on large, inexpensive glass or plastic substrates.

Another increasingly common use of transistors is for power electronics. Like the transistors used in displays, these devices do not need to be small or fast. What they need to be able to do is handle the large currents and voltages involved in switching power on and off. They need to be able to do that efficiently, and without failing prematurely. They also need to be able to handle the high temperatures that can be generated under these conditions.

Power transistors would typically be found in computer power supplies, cellphone chargers, and laptop power supplies. There are also other application areas where their use is likely to increase hugely in the next decade or two. Electric and hybrid vehicles use power electronics to control the current flowing from their batteries to the electric motors to drive them. Even the relatively humble compact fluorescent light bulb uses power electronics to control the operation of the lamp. All these power applications place slightly different but highly stringent requirements on the transistors that make them work.

The group of devices that has the most demanding requirements is that of high frequency or radio frequency (RF) devices. These are the transistors that power the radars that keep us safe in the skies, the transistors that our cellphones use to send our signals to the cellphone towers, and also those towers themselves. Wireless networks represent another growing area. The transistors in these devices need to fulfil the combined requirements of two of the above application areas. They need to work at the extremely high frequencies that are used in computer chips, while doing so with the efficiency of power electronics.

1.4 The motivation for investigating new materials

The diverse requirements for transistors in the various application areas detailed above cannot usually be satisfied by one material alone. There are also many other semiconductor devices such as diodes, semiconductor diode lasers, and solar cells that have even more varied ideal properties. There are

therefore considerable gains that can be made by finding and developing compound semiconductor materials that satisfy as many of these application requirements as possible.

Beyond certain infrared applications, a wide (>1eV) bandgap is a generally desirable property for a semiconductor material. Materials with high bandgaps can work at higher temperatures, and diodes fabricated from wide bandgap materials typically have lower leakage currents. In power devices, wide bandgap materials are useful as they enable devices to be made with higher breakdown voltages [12]. This is due to the lower impact ionisation coefficients in these materials.

Semiconductor materials absorb the energy from light that passes into the material if the energy associated with that light is greater than the bandgap energy. This is why materials such as silicon and germanium, which have narrow bandgaps, are not transparent to visible light, and appear somewhat metallic. Wider bandgap materials will transmit light of correspondingly higher energy – i.e. materials with a bandgap wider than that equivalent to visible light will appear transparent to visible light. Zinc oxide has a wide bandgap of 3.4 electron volts (eV) [13], which means that ZnO is transparent to visible light.

Transistors made from transparent semiconductor materials could be particularly useful in display technologies, as the transistor would no longer block the light from part of the pixel. Additionally, visible light will not generate carriers in the material if the energy is less than the bandgap, making devices light-insensitive. This could reduce the need to shield display transistors from the emission coming from backlights.

High mobility is also a particularly useful property for semiconductor materials. High mobility means that the material is less resistive, and therefore there is less power loss due to resistive heating. This can translate into power devices needing less cooling and heat sinking. Battery powered devices will last longer with more efficient devices. More importantly, transistors made from materials with high mobilities generally have better properties than those made from lower mobility material.

One of the most important concerns for manufacturers is the cost of the material, and the cost of processing it. Substrates must be cheap, and also high quality. This is particularly true for very large devices such as flat panel displays. For large flat panel displays, a semiconductor substrate would be astronomically expensive, so glass substrates are typically used. Materials used for transistors must therefore be able to be deposited onto glass substrates, and processed at temperatures that can be withstood by the glass. These requirements mean that such transistors are particularly poor in terms of quality compared to those designed for use in other applications. Transistors for displays are therefore very much a specialist type of device.

The number of types of devices that can be made with only either of p-type or n-type material is very small. It is therefore very desirable that a semiconductor material can be made and selectively processed to be either p- or n-type. The combination of p- and n-type allows the fabrication of junction diodes and bipolar transistors, and also means that junction isolation can be used to make electrically isolated transistors on the same substrate. Selective conversion from p-type to n-type and vice versa is typically done by ion implantation or diffusion. Diffusion involves depositing a dopant material on the surface, and then thermally driving the dopant into the semiconductor. Ion implantation is generally achieved by making an ionised source of dopant material, which is accelerated by a high voltage. The resulting high energy ions will travel a short distance into the material before coming to rest.

As was mentioned previously, one of the most important reasons that silicon is extensively used as a semiconductor material is because of its chemically and thermally stable, high-quality, readily-formed oxide. Alternative semiconductor materials should therefore ideally be compatible with some form of insulating material. This material could be some form of insulating oxide or nitride that could be grown or deposited on the material. It would need to have very high resistance, be thermally and chemically stable, and have low amounts of trapped charge both in the bulk of the material, and at the interfaces.

Many compound semiconductors such as arsenides, selenides, and tellurides are extremely toxic, and hence special precautions must be made when manufacturing or processing these materials. Workers

must take precautions, and their health must be monitored constantly. If there is a large amount of material, it would be necessary to put precautions in place for safe end-of-life disposal of the product containing that material. It is therefore best to avoid toxic semiconductors if possible, and use a non-toxic material such as zinc oxide instead.

1.5 Properties of zinc oxide

The most obvious desirable property of ZnO is its wide bandgap of ~3.4 eV at room temperature. This corresponds to a wavelength of 365 nm – which is in the near UV region. ZnO is therefore transparent to visible wavelengths. It is also a direct bandgap material, and so it can efficiently radiate photons when an electron moves from the conduction to the valence band. This is particularly useful for optical applications. Other materials with similarly wide bandgaps are gallium nitride (GaN) which has a bandgap of 3.5 eV, and silicon carbide (SiC) with a bandgap of 3.23 eV in the 4H polytype. Only GaN however is also a direct bandgap material.

As a bulk chemical, ZnO itself is both reasonably inexpensive and relatively abundant. Unfortunately, this does not mean that pure, monocrystalline substrates are necessarily affordable. At present, there are several techniques used to produce semiconductor quality bulk ZnO crystals – however these are slow and therefore expensive, so the available substrates are also expensive. It is possible that in future, alternative growth methods will be developed that are considerably more economical. Presently, however, very little device development makes use of bulk ZnO substrates despite their quality and availability. Devices are usually made from layers of ZnO grown heteroepitaxially on other crystalline substrates.

ZnO is non-toxic. As a sunscreen, it is known as just 'zinc' – and is very popular with sports-people such as cricketers. It is also one of the main constituents of calamine lotion [14], which was a very common anti-itching lotion. ZnO can also be used as a wound dressing [15] due to its mildly antibacterial properties. From an electronic perspective, these properties may prove useful at some point given the increasing attention to hybrid biological-semiconductor device concepts.

The one property that distinguishes ZnO from other high bandgap materials such as GaN is its high exciton binding energy of 60 meV. The high exciton binding energy should allow ZnO to be a particularly efficient photon emitter material at room temperature and above. Although the exciton binding energy is not particularly relevant to transistor properties and operation, it is potentially very useful for applications where the ZnO could be used for both transistors and optical components on the same substrate.

The chemical reactivity of ZnO could be regarded as either an advantage or a disadvantage, depending on the desired processing. ZnO is amphoteric, which means that it reacts in both acidic and basic solutions. This is an advantage in that it is generally very easy to etch ZnO. The disadvantage is that it is therefore difficult to process other materials that might be desirable to use on or with ZnO, as any etchant that could be used to etch the other material would also etch the ZnO as well. It therefore has poor selectivity.

The relatively low mobility of ZnO is arguably its Achilles heel. At around 200 cm^2/Vs [16] the typical maximum room temperature electron mobility is lower than that of most conventional compound semiconductors. Many transistor figures of merit improve with higher mobility. It is therefore unlikely that ZnO would replace any of the traditional semiconductor materials for devices where high performance is the only criterion. If, however, other criteria such as transparency, radiation insensitivity, and high temperature operation are important, ZnO devices may then have a substantial part to play.

1.6 Previous Work on zinc oxide transistors

Current work on ZnO transistors roughly falls into two broad areas:- TFTs and high-speed heteroepitaxial structures. TFT research appears to be aimed at the display market, assumedly capitalising on the transparency of ZnO to visible light, and also the fact that visible light does not induce carriers in the material. The heteroepitaxy research effort is less commercially focussed at

present. Typical devices reported include MESFETs [17-20], MOSFETs [17] and high electron mobility transistors (HEMTs) [21-23].

As mentioned in section 1.2, TFTs were first suggested in the 1930s, and the first working devices were fabricated in the 1960s. It was not until the 2000s that significant reports appeared using ZnO as the semiconductor material for TFTs [13]. This work was apparently inspired by the realisation that wide bandgap materials could be used to fabricate transparent transistors. Hoffman gives a very good review of work on ZnO TFTs up until 2005 [13]. However, at that time, there were not many papers, and in fact Hoffman himself said that they were "rather limited in number" [13].

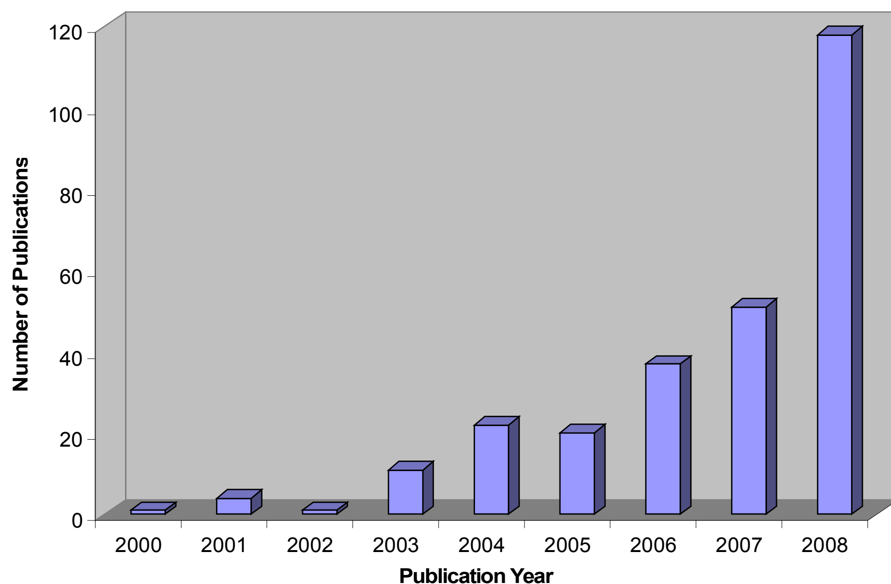

Figure 1.1: ZnO TFT publications by year from Web of Knowledge. Date: 24/5/2009
Query: TS=(Zinc Oxide or ZnO) and TS=(TFT or Thin Film Transistor)

As can be seen in Figure 1.1, the situation has changed dramatically since then. The data for 2009 (31) was omitted due to the fact that at the time it was a partial year, and there is a probable lag in capturing recent publications. Nonetheless, there has been a huge increase in the amount of work currently being done. Much of the recent work appears to be coming out of research groups in Asia, particularly Japan and Korea. Many of these groups have ties to companies in the display industry.

Not all work on ZnO TFTs is aimed purely at the display market. Bayraktaroglu et al. [24] fabricated high frequency TFTs using pulsed laser deposition (PLD) onto silicon dioxide coated substrates. The devices had cutoff frequencies of 450 megahertz. They also had field effect mobilities of 110 cm^2/Vs, which approaches the Hall mobility of high quality bulk ZnO. This is a particularly surprising result for polycrystalline materials, which typically show considerably lower mobilities than bulk materials.

There has been considerably less work done on ZnO transistors fabricated on single crystal material. Successful MESFET devices had been hindered by the lack of high-quality Schottky contacts, until Allen et al. developed successful nonstoichiometric Ag_xO Schottky contacts [25]. There are still very few reports of ZnO MOSFET devices [17] other than devices based on nanowires [26-28]. This is possibly due to the difficulty of producing a stable, low charge interface between the ZnO and the gate insulating material.

The most successful single-crystal devices to date have in fact been HEMT devices, based on a ZnO/ZnMgO heterojunction [21-23]. A HEMT should ideally provide transistors with the highest possible channel mobility, as the active area is away from the surface. Surface roughness and traps will tend to reduce the effective mobility of the semiconductor material near the surface. There has even been recent work using ZnO/ZnMgO HEMTs as biosensing elements [29,30].

1.7 Thesis overview

This thesis starts by introducing semiconductors and transistors. It then goes on to discuss the development of transistors, and work on investigating new semiconductor materials. This leads into a discussion of the properties of ZnO, and work on ZnO transistors.

The second chapter details the physics behind FET transistors. Several different FET types are described. This chapter details the equations that have been developed to describe FET characteristics, and discusses some performance measures. Some illustrations of typical transistor structures are shown.

The third chapter describes the design and fabrication of a ZnO MESFET. Details of the layout of the chip are provided. Some problems encountered during the design and fabrication are discussed, as well as the rationale behind some of the process flow decisions.

The fourth chapter discusses electronic testing of the transistors. Measured characteristics are presented, and key characteristic features are analysed. Deviations from ideal behaviour are noted and investigated. Device figures of merit (FOM) are calculated and tabulated.

In the fifth chapter, the limitations of the fabricated MESFETS is discussed, and the measured results of these MESFETs are compared to similar devices. The origin of the parasitic conduction path is considered, and some initial efforts to clarify its origin are presented and discussed.

In the final chapter, a summary of the key results is presented, and suggestions for further work are discussed.

Chapter 2 - Field Effect Transistors

2.1 Principles of Operation

The general principle of operation of a FET is to modulate current flow in a channel by applying a voltage to a gate. The electric field resulting from the applied voltage on the transistor gate repels (or attracts) carriers from (or into) the nearby channel, depending on the polarity of the field and the type of carrier present in the channel. Repelling carriers establishes a depletion region, which limits the current that can flow in the channel, and thereby limits the current that can flow between the terminals at either side of the gate (commonly known as the source and drain). Conversely, attracting carriers into the region under the gate will increase conduction, or alternatively invert the carrier population.

A simple physical analogue to a transistor would be a kitchen tap, where the flow of water through the tap is regulated by the handle. A more accurate analogy for a FET would be pinching a hose from the outside. The external pressure on the hose flattens the hose down, and reduces how much water can flow through. If enough squeeze pressure is exerted, the hose will flatten completely, shutting the flow of water entirely.

For a FET to be useful, the gate needs to be electrically isolated from the channel region. This is so that the gate voltage controls the channel current, but that neither the channel current, nor the drain/source voltages affect the gate voltage. There also needs to be a defined channel area that can be fully controlled by the gate – i.e. there are no uncontrollable parallel conduction paths. There are several ways of achieving this isolation; each gate isolation method effectively denotes a different transistor type.

The junction FET (JFET) was the first FET type to be successfully fabricated. As it was originally realised, the JFET consists of a bar of doped semiconductor material. This bar has a region of material doped with the opposite type of dopant on either side. The dopant is diffused into the bar, forming diode junctions on either side. These two diffused regions are referred to as gates, as they are capable of modulating the channel. The two gates on opposing sides of the device are electrically connected together. When the diodes are reverse biased with respect to the channel that is formed between them, a depletion region forms around each gate.

This depletion region performs two functions. Firstly – it effectively isolates the gate regions from the channel regions. Secondly, it is these depletion regions that modulate the volume of the channel that is available for current to flow between the ends of the bar. As the reverse voltage on the gate is increased, the extent of the depletion region decreases. As the depletion region on either side of the bar increases, the remaining channel thickness decreases, hence limiting the drain-source current.

Diffusing junctions into isolated bars does not lend itself to cheap or efficient fabrication. Instead, most semiconductor devices these days are made using planar technology. Although a top junction would be easy to diffuse in, the lower one would not. The lower junction could be made instead by counter doping, or alternatively by using epitaxy to create a junction by depositing oppositely doped material for the channel on top of a substrate which becomes one gate. However, this is unnecessarily complicated as alternative device structures exist, and for that reason, JFETs are largely of purely historical interest.

Rather than using diode junctions to provide the required isolation between the gate and channel, a MOSFET (metal oxide semiconductor FET) uses an insulating layer to physically isolate the gate from the channel. The electric field resulting from applied gate voltages directly modulates the carrier density in the channel. Although the acronym implies that it should be oxide, in practise the insulator can be any high-quality insulating material. The acronym MISFET is sometimes used to be more accurate. This high quality insulator means that the gate presents an effectively infinite DC impedance

to its driving circuit. The MOSFET is today the most ubiquitous transistor type, as it is used in most high-end microelectronic devices, such as processor chips.

The MOSFET took several years before it could be successfully commercialised. This was primarily due to problems with interface charges and with mobile charges in the oxides that were able to be grown at the time. These charges caused large and uncontrolled changes in the threshold voltages of the transistors. Once these problems were isolated and solved, the MOSFET went on to become the success that it is today. Those problems were solved in the silicon – silicon dioxide system, but have not necessarily been solved in general. Any new material system may have similar problems, and these would have to be overcome to make stable MOSFET (or MISFET) devices using that new material system.

The term MOSFET generally refers to devices made from single-crystal material. As mentioned previously, the term 'thin film transistor' (TFT) refers to devices where the active semiconductor is deposited onto a low-cost, non-crystalline substrate. The active area of the device is therefore generally amorphous or polycrystalline material, and is therefore lower quality than the equivalent single-crystal material. However, the principle of operation is generally the same as one or other of the above transistor types. Most TFTs being made currently are structurally similar to MOSFET devices.

FETs are known as unipolar devices, since the current that flows is carried only by one carrier type – either electrons or holes, but not both. This is in contrast to bipolar devices such as BJTs, where both holes and electrons carry current. However, like a BJT, in a JFET or a MOSFET fabricated using bulk semiconductor material, it is necessary to be able to make both p- and n-type material to achieve isolation between the source and drain. This isolation prevents conduction below, and around the gate area. In silicon this is simple and commonly done. However in some material systems, where it is difficult to make both p- or n-type material, this is a definite problem. In the specific case of ZnO, only n-type conduction can be reliably achieved.

Junction isolation not only prevents lateral conduction paths, but it also allows enhancement mode devices to be fabricated. If the channel is doped with the opposite polarity to the source and drain, there is also no conduction path through the gate. A voltage must be applied to the gate which inverts the polarity of the carriers in the gate region, and only then will the transistor conduct. A 'normally off' transistor is very desirable for efficient circuit design, because there would be no standing current flow through the device unless it was intentionally turned on.

As an example, consider a device where the source and drain are n-type, and the channel is p-type. No current can flow from source to drain. If a positive voltage is now applied to the gate, electrons will be attracted to the channel under the gate. If the voltage is sufficiently high, the dominant carrier type will invert from being holes to electrons. Consequently, a current can flow from source to drain through the contiguous electron-rich source-channel-drain path.

An alternative isolation method for situations where junction isolation is not feasible, is to use epitaxial growth techniques to grow layers of substantially different conductivities. If the substrate is sufficiently resistive, negligible current can flow through the substrate, limiting the parasitic conduction. The epitaxial material would be made considerably more conducting by doping. The substrate could either be a full insulator, such as sapphire, or could be a high resistivity semiconductor, such as semi-insulating gallium arsenide.

As mentioned above, the gate insulator is a critical component of a MOSFET. In some semiconductor materials, it may not be feasible to deposit or grow a good quality oxide on the semiconductor. There may be uncontrollable and/or unstable charges in the insulator, or at the interfaces, which cause large and uncontrollable changes in the threshold voltage of the transistor. Or, in the case of ZnO, the chemical reactivity of the semiconductor means that it can be extremely difficult to use etching techniques to pattern a gate insulator material.

One solution is the metal-semiconductor FET (MESFET). Some metals, particularly those with high work functions such as gold, silver and platinum, can produce highly rectifying junctions when

applied to the surface of a semiconductor material. If this junction is of sufficiently high quality, the leakage current when it is reverse biased is minimal. Since low leakage produces an appropriate level of gate-channel isolation, it can enable fabrication of a MESFET transistor, eliminating the need for a gate insulator.

There is a considerably more complicated device, and it has many names. It is variously called the heterojunction FET (HFET), the high electron mobility transistor (HEMT), the modulation doped FET (MODFET) or the two-dimensional electron gas FET (TEGFET). Some of these names refer to slightly different construction, or modes of operation; the general concept of all of them, however, is much the same. In such a device, a junction is formed between two different materials with substantially different band gaps; this forms what is known as a heterojunction. A very thin 'sea of electrons' forms near the junction in the low-bandgap material, due to band bending near the interface. The conductivity of this high-carrier-density quantum well can also be modulated similarly to any other FET.

A suitable high-bandgap material that could be used in conjunction with ZnO to make a HFET is zinc magnesium oxide (ZnMgO). $Zn_xMg_{(1-x)}O$ can be made with various mole fraction (x) values, which give substantially different bandgap differences to ZnO, due to the very high bandgap (~7.7eV at room temperature [31]) of MgO. $Zn_xMg_{(1-x)}O$ also has a reasonable lattice match to ZnO, so the heterojunction is reasonably straightforward to fabricate. Some groups have already fabricated successful $ZnO/Zn_xMg_{(1-x)}O$ HEMT devices [13].

2.2 FET Geometry

As stated previously, the most common type of FET is the MOSFET. A schematic representation of a generalised device is shown in Figure 2.2. A MOSFET typically has a source and a drain which are doped with a dopant of opposite polarity to the channel. This provides isolation between the source and drain. A layer of high quality insulating material provides isolation between the gate electrode and

the channel. In modern MOSFET devices, the gate is often made of highly doped polycrystalline silicon, or a silicide, rather than an actual metal.

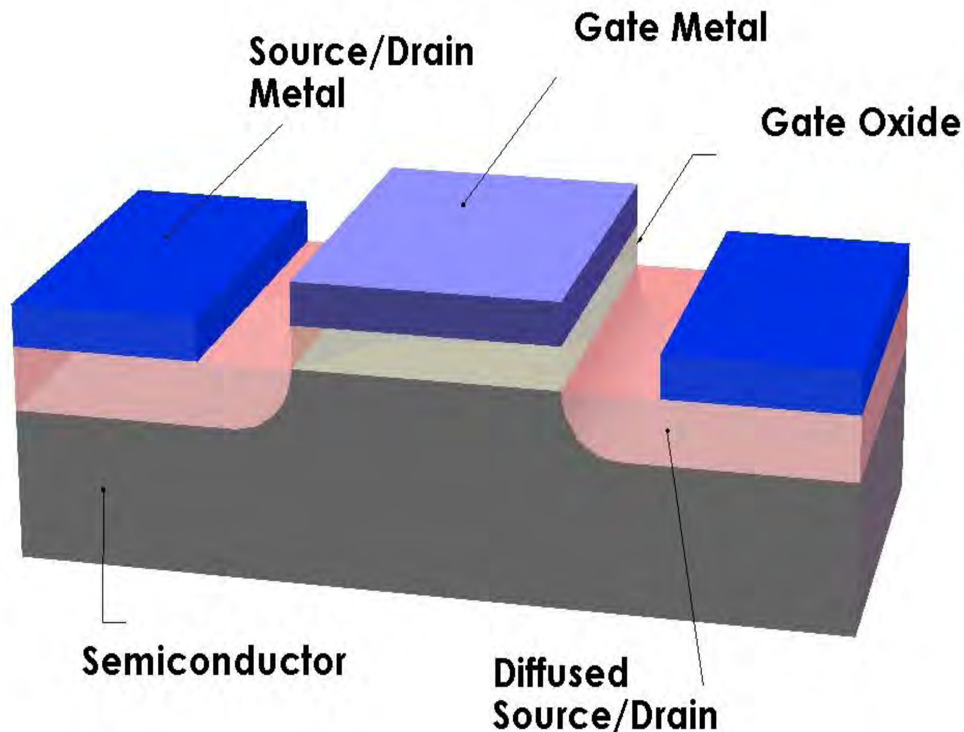

Figure 2.1: Diagram illustrating typical components of a MOSFET

MOSFETs are typically fabricated from bulk semiconductor material, using dopant diffusion to form the source and drain regions. The path between the source and drain consists of alternately p-n-p or n-p-n material, and therefore there is always a reverse biased diode preventing source-drain conduction, until a potential applied to the gate induces a conducting channel under the gate. This diffused structure also means that all potential parallel conduction paths around the gate laterally, and well below the gate cannot conduct, as there is always a reverse biased junction blocking the current.

Like the MOSFET, the TFT also has an insulating layer between the channel and the gate. It is not, however, fabricated from bulk semiconductor material like the MOSFET, but is instead made from semiconductor material deposited onto a substrate. The substrate is usually insulating, preventing parallel conduction paths below the channel. It is necessary to physically restrict the channel material laterally, to prevent uncontrolled lateral conduction paths. A typical structure is shown in Figure 2.2.

worth noting is that the channel does not extend sideways past the gate, and in fact the gate would probably go past the channel on either side, to allow for any misalignment.

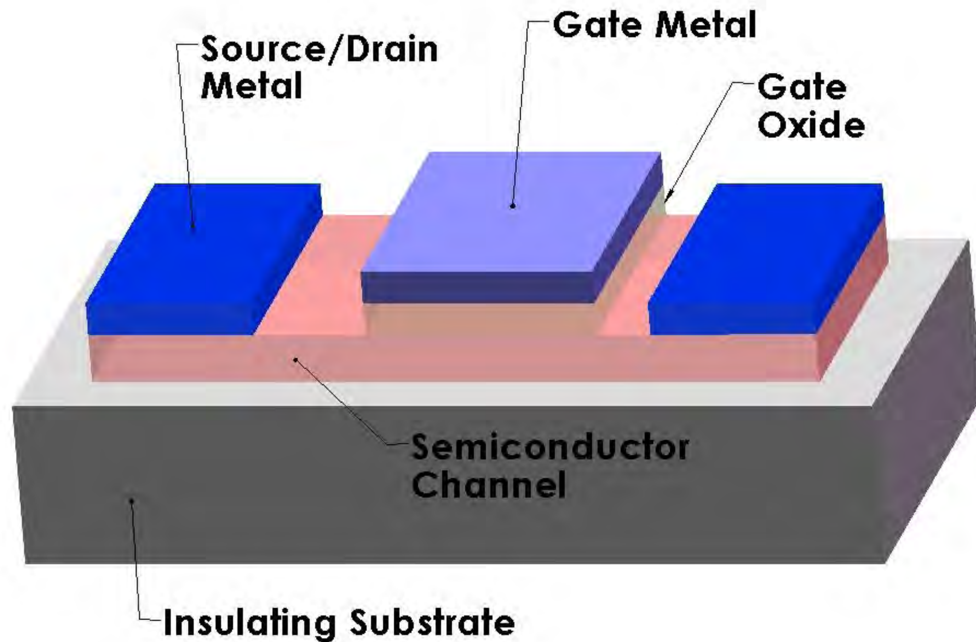

Figure 2.2: Schematic diagram of a generalised thin film transistor (TFT) structure

The TFT is an increasingly common transistor, as it is used extensively in active-matrix LCD displays as a pixel driver. Each coloured pixel in an active matrix LCD has a corresponding TFT transistor. The insulating substrate would typically be simple, cheap glass. Although many materials have been used for the semiconductor, the most commonly used at the moment is hydrogenated amorphous silicon [32]. For a TFT, the most important factor is cost, rather than performance.

The MESFET is structurally similar to the basic TFT, except that the insulated gate dielectric is replaced by the Schottky junction between the gate metal and the channel semiconductor. This is illustrated in Figure 2.3. Again, like the TFT, it is necessary to isolate the channel so that it is fully covered by the gate.

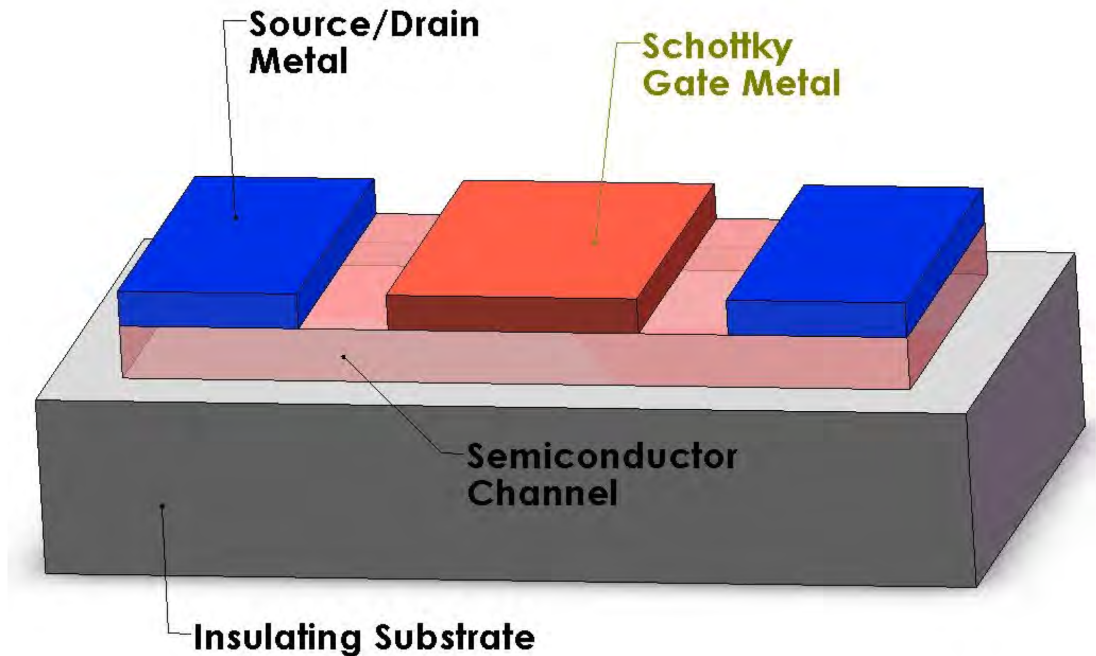

Figure 2.3: Schematic diagram illustrating the main components of a typical MESFET

Although the metal layers in figures 2.1 - 2.3 are schematically represented as homogeneous blocks of material, in practice they typically consist of multiple layers. The material contacting the semiconductor would be selected to have good contact properties to the semiconductor, whereas the top layer would be selected to have a low resistance. There might be additional layers to prevent alloying of the two outer layers. There might also be a layer to prevent oxidation or degradation of the underlying layers as well. For these reasons, the design of metallisation schemes is a entire technology area in itself.

In this work, the single-crystal ZnO channel material was grown epitaxially. This means that the substrate in this case must also be a single-crystalline material. For this application, it must additionally be insulating, which is why a substrate material such as sapphire was chosen. If it is possible to make good Schottky junctions, it would also be possible to make MESFET devices using channel material which is non-crystalline. In this case, the substrate would not need to be single-crystal material either.

2.3 MESFET Model

As a consequence of the similarity of the operation of these types of transistors, the current-voltage (I/V) characteristics of the various devices are also very similar. The simple model of the JFET developed in the 1950s by Shockley [6] can be easily adapted to the other variants of the FET, and it is reasonably valid for larger-sized devices. To model very small devices with channel lengths of less than 1-2 µm, the model must be adapted to allow for other effects such as 'short channel' effects. For the devices in this thesis, such issues are not relevant however. Let us start with the simple model of a MESFET, the cross-section of which is shown in Figure 2.4(a)

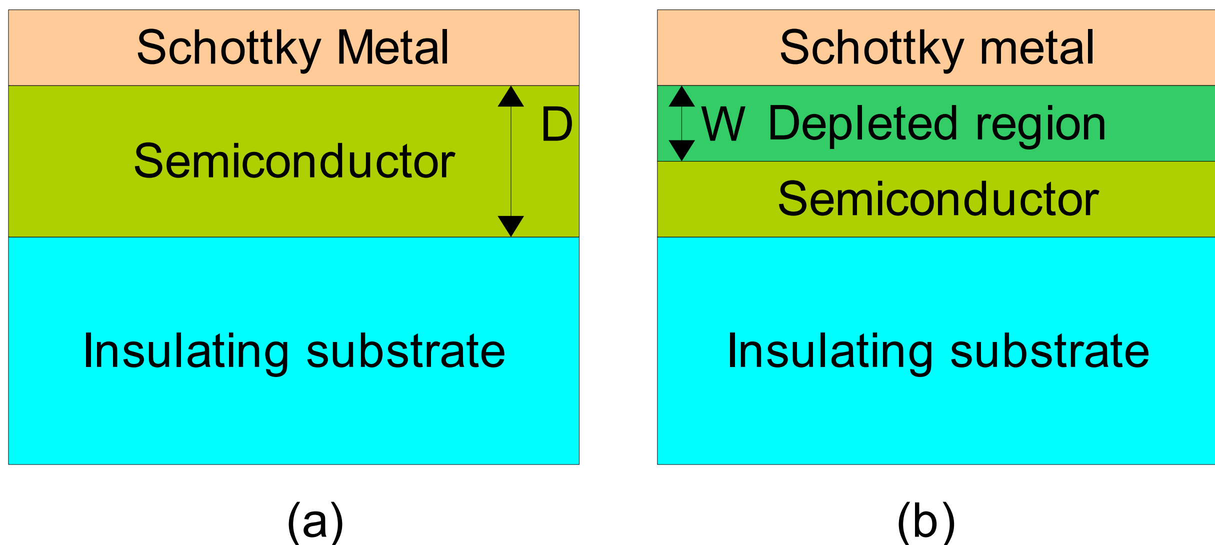

Figure 2.4: Schematic diagram of depletion in the channel of a MESFET. (a)showing the physical model of the layers; (b)showing the depleted region under the gate due to gate bias

Following the one-dimensional mathematical model of a MESFET described by Sze [1] we consider the case of a layer of n-type semiconductor. Only the material directly under the gate is considered.

First, consider the effect of the gate voltage V_G on the depletion region W under the gate, as shown in Figure 2.1(b). A positive V_G will forward bias the junction, so V_G would normally be negative. With both the drain and source grounded, there is no current flowing in the channel. V_G will be offset by the built-in voltage of the Schottky junction V_{bi}. W is given by:

$$W = \sqrt{\frac{2\varepsilon_s(V_{bi} - V_G)}{qN}} \tag{2.1}$$

where ε_S is the permittivity of the semiconductor, q is the electronic charge, and N is the density of electrons in the semiconductor.

The case when W = D, i.e. the depletion region just extends across the thickness of the semiconductor material, is referred to as threshold. The gate voltage at this point is referred to as the threshold voltage. If the gate voltage is made more positive than this voltage, there are undepleted regions in the channel, and current can flow between the drain and source. At gate voltages more negative than threshold, the channel is completely depleted, and no current can flow. Solving for V_T, the voltage at threshold:

$$V_T = V_{bi} - \frac{qND^2}{2\varepsilon_s} \tag{2.2}$$

Note that the threshold voltage depends on both the built-in voltage V_{bi} of the Schottky contact, and the channel thickness D. If the channel is thin, the threshold voltage will be negative. This means that the gate voltage must be driven positive to allow current to flow. This is known as an enhancement mode device. Since the range of positive gate voltages that may be applied before the gate starts to conduct is rather limited, these devices have a very limited gate voltage range.

When current flows in the channel, there will be a voltage drop in the channel between the drain and the source. At the higher voltage source, the gate-channel voltage, and therefore the depletion depth, is a maximum. The Shockley model predicts that the depletion width will vary linearly between the source and the drain, as shown in Figure 2.5. To see this, consider a narrow slice of channel, between y_1 and y_2, where $dy = y_1 - y_2$.

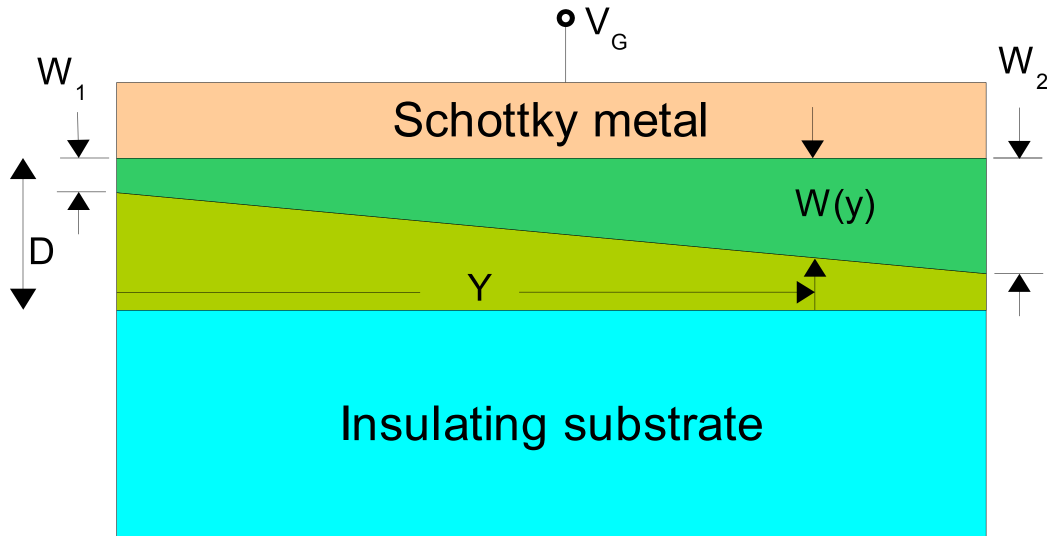

Figure 2.5 The linearly graded depletion region in a MESFET with finite drain-source bias

The resistance of this slice will be dR:

$$dR = \frac{\rho l}{A} = \rho \frac{dy}{Z[D-W(y)]} = \frac{dy}{q\mu N Z[D-W(y)]} \tag{2.3}$$

where Z is the channel width, and ρ is the resistivity of the material, which is inversely proportional to q, N and μ (the mobility of the material).

Generalising Eq. 2.1 to express the depletion width as a function of the distance along the length of the channel when there is a finite drain-source current gives:

$$W(y) = \sqrt{\frac{2\varepsilon_s(V_{bi}-V_G+V(y))}{qN}} \tag{2.4}$$

or:

$$[W(y)]^2 \frac{qN}{2\varepsilon_s} = (V_{bi}-V_G+V(y)) \tag{2.5}$$

Since the current flowing in the channel (I_d) is constant along the length of the channel, the voltage drop across the slice of resistance of Eq. 2.3 will be:

$$dV = I_d dR = I_d \frac{dy}{q\mu N Z[D-W(y)]} \tag{2.6}$$

Differentiating Eq. 2.5 also yields an expression for dV:

$$dV = \frac{qN}{\varepsilon_s} WdW \tag{2.7}$$

If we substitute this expression for dV into Eq. 2.6 we obtain:

$$I_d \frac{dy}{q\mu N Z[D-W(y)]} = \frac{qN}{\varepsilon_s} WdW \tag{2.8}$$

which when rearranged yields:

$$I_d dy = \frac{q^2 N^2 \mu Z}{\varepsilon_s}[D-W(y)] WdW. \tag{2.9}$$

Integrating from y = 0 to y = L gives an expression for the drain current:

$$I_d = \frac{1}{L}\int_{W_1}^{W_2} \frac{q^2 N^2 \mu Z}{\varepsilon_s}[D-W(y)] W\, dW \tag{2.10}$$

Since W is linear with y, the integration is trivial:

$$I_d = \frac{q^2 N^2 \mu Z}{2\varepsilon_s L}\left[D(W_2^2-W_1^2)-\frac{2}{3}(W_2^3-W_1^3)\right] \tag{2.11}$$

If we substitute in expressions for W at the source and drain from Eq. 2.4, the equation becomes ungainly. However, we can rewrite Eq. 2.11 in terms of a 'pinch-off' voltage V_p and current I_p:

$$I_d = I_P\left[\frac{V_d}{V_P}-\frac{2}{3}\left(\frac{V_d+V_G+V_{bi}}{V_P}\right)^{3/2}+\frac{2}{3}\left(\frac{V_G+V_{bi}}{V_P}\right)^{3/2}\right] \tag{2.12}$$

where

$$I_P = \frac{q^2 N^2 \mu Z D^3}{2\varepsilon_s L} \qquad V_P = \frac{q N D^2}{2\varepsilon_s} \tag{2.13}$$

Note that we can therefore rewrite Eq. 2.2 as

$$V_T = V_{bi} - V_P \tag{2.14}$$

Which is a simpler and more intuitive way of expressing this fundamental relationship.

2.4 Figures of Merit

It is common practise to develop 'figures of merit' which allow comparison between different devices and technologies. These figures of merit will often convolve critical terms or properties that are particularly appropriate to common uses. Many of the common ones used to characterise FET devices refer to the high-frequency operational parameters of these devices. As the devices fabricated and tested in this work were not specifically designed for operation at high frequencies, high frequency figures are not relevant here. However, there are several figures of merit that can be used to make useful comparisons.

The transconductance g_m of a FET is a critical parameter for circuit designers. g_m is defined as the change in drain current as a function of gate voltage, where the drain voltage is held constant. The transconductance of a FET limits the gain of a circuit using that FET. The transconductance is of limited use however for comparing different material systems and technologies, as it is strongly dependent of the physical size of the device.

When comparing different technologies for transistor fabrication, one particularly useful parameter is the channel mobility. The channel mobility is calculated by taking the theoretical expressions for the drain current (such as Eq. 2.12), and rearranging these expressions to make the mobility the unknown quantity. The measured voltages and currents, the physical dimensions, and physical constants can then be used to calculate what the effective mobility of the material in the channel is. This would typically be done in either the linear or saturation region, where simplifications can be made to the

form of the equation. Device parameters are strongly dependent on mobility – the higher the mobility, the better the device.

Chapter 3 - ZnO MESFET Fabrication

3.1 Introduction

This chapter describes the specific fabrication techniques used to make prototype ZnO FETs. It is assumed that the reader is familiar with standard photolithographic techniques and these will not be described in great detail, except where the specifics are particularly relevant. Readers unfamiliar with standard fabrication techniques and fabrication equipment will find an introductory text on microelectronic fabrication, such as [33] a useful reference.

3.2 Mask Design and Fabrication

The first step in fabrication is to design a layout using a computer aided design (CAD) package. A layout is a computer representation of features that will appear on the different masks. The CAD package allows the designer to specify the shape and location of those features. Figures 3.4 and 3.5 show typical sections of a layout. Unlike standard design and drawing software such as Autocad®, Visio® or CorelDRAW®, a CAD package intended for designing microelectronic devices will enable the designer to work with multiple layers representing the different masks needed to specify the device, and additionally support hierarchical design techniques. These allow the designer to design graphical structures, and then use these low-level structures as part of higher-level structures. This type of CAD package is commonly known as a 'layout editor'.

The software package L-Edit from Tanner Research [34] was chosen to design the layout. L-Edit is powerful and relatively intuitive. It is capable of outputting data directly in different formats suitable for mask-making, using various mask-making techniques. These include GDS which is a file format commonly accepted by electron beam lithography tools, and also CIF and DXF which are more

commonly accepted by optical mask-making tools. The Electrical and Computer Engineering Department at the University of Canterbury has multiple licenses on a license server, which means that it can be used anywhere within the campus.

Before one can design a layout, it is necessary to decide what masks are needed, and how these can be represented by graphical layers in the layout editor. For the devices in this thesis, this was a simple process, with a simple 1:1 correspondence between the layout and the masks. Three mask layers were defined :

- Isolation areas – defining the areas of ZnO to be removed to isolate the transistors.
- Schottky metal areas – this mask defines the transistor gate and gate connection pad.
- Ohmic metal areas – this mask defines the areas where the source and drain connections will be made.

The masks were written using a Heidelberg model µPG101 mask writer [35]. The µPG101 uses a UV laser diode and a computer controlled stage to write the CAD pattern onto a chrome and photoresist-covered mask plate. The µPG101 is capable of writing with a lateral resolution of 5 µm, which is far from 'state of the art' – but more than adequate for these devices. The patterns were subsequently transferred into the chrome layer using chrome etch, and then the photoresist was stripped using acetone. The chrome etch used consisted of ceric ammonium nitrate, perchloric acid and water.

Traditional lithography designed for mass production uses an array of the same pattern on a mask, and one mask per layer. In this application, where the devices were being made on a single 5 mm square die, using three different masks would be unnecessarily wasteful. All three designs were therefore patterned on the one mask, in a horizontal line. The design of the mask holder on the Süss MA6 Mask Aligner [36] is such that the mask can be moved slightly sideways, allowing each separate layer to be placed at the centre of the mask holder, for patterning each layer on the chip.

3.3 Mesa Isolation

For any form of integrated circuit, multiple transistors are normally needed. The active areas of each transistor must be electrically isolated from each other, so that the state of other nearby transistors do not affect each other's operation. In materials such as silicon, this can be done using junction isolation, where alternating p- and n- regions form back-to-back diodes. One of the diodes will be reverse-biased, and therefore provides the needed isolation. Occasionally this structure can form parasitic thyristor-type devices, but careful design can reduce their significance.

In ZnO devices, the lack of p- type material means that junction isolation is not an option. Some other form of isolation must therefore be utilised. Since the sapphire substrate used as a template for the epitaxial growth of the ZnO is an insulator, it can inherently prevent any conduction below the active areas of the devices. It is therefore only necessary to prevent lateral conduction through the ZnO layer. The simplest method to do this is to simply remove the ZnO around the active device to prevent conduction. This technique is called ‘Mesa Isolation’ – where etching is used to remove the conducting material – leaving isolated mesas of conductive material as the active areas.

3.4 Zinc Oxide Etching

In the microelectronic industry, etching is usually performed using either ‘dry’ or ’wet’ etching. Wet etching refers to the use of aqueous alkaline or acid etches to remove the material. Dry etching refers to etching in a reactive plasma. In a plasma, etching occurs when the plasma contains ions that will form volatile compounds when they react with the material that is required to be etched. Since they are volatile, they can be pumped away by the vacuum system as by-products.

For dry etching of ZnO, it is possible to use chlorine based chemistries such as BCl_3 or $SiCl_4$. However, to achieve adequate etch rates, it is generally necessary to use an inductively coupled plasma (ICP) etcher. In ICP, magnetic fields are used to substantially increase the density of active species in

the plasma. As we do not have access to such a machine at Canterbury, it was necessary to find an alternative etching method.

Fortunately, zinc oxide etches easily in many acidic solutions. A common etch that is used is dilute hydrochloric acid (HCl). However, the problem with using HCl for patterning is controlling the etch rate. Typically HCl etches very fast, and etches laterally under the masking material – this is known as ‘undercut’. Fast etching makes it difficult to estimate the time to etch. Excessive, uncontrolled undercut makes it difficult to control the width of resulting lines, and in extreme cases, the line will be undercut completely, and disappear. Figure 3.1 shows an example of bad undercut as the result of HCl etching. The white areas are areas of undercut. In finer structures such as the test structures near the top, the photoresist has been completely undercut, and has lifted off.

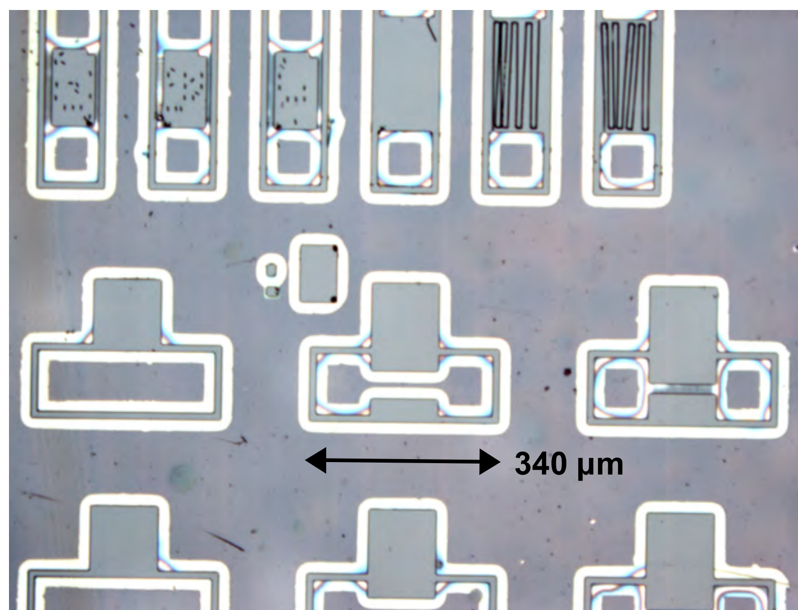

Figure 3.1: Micrograph showing the result of a badly undercut dilute HCl etch.

A solution to this problem was suggested by Chang, Hicks and Laugal [37]. Instead of using HCl, they employed ammonium chloride (NH_4Cl). The chloride ions form soluble zinc chloride, and the self-dissociation of the water provides a very low controlled concentration of H^+ ions which attack the ZnO. This etchant produced a controlled and reproducible etch rate, and also minimal undercut.

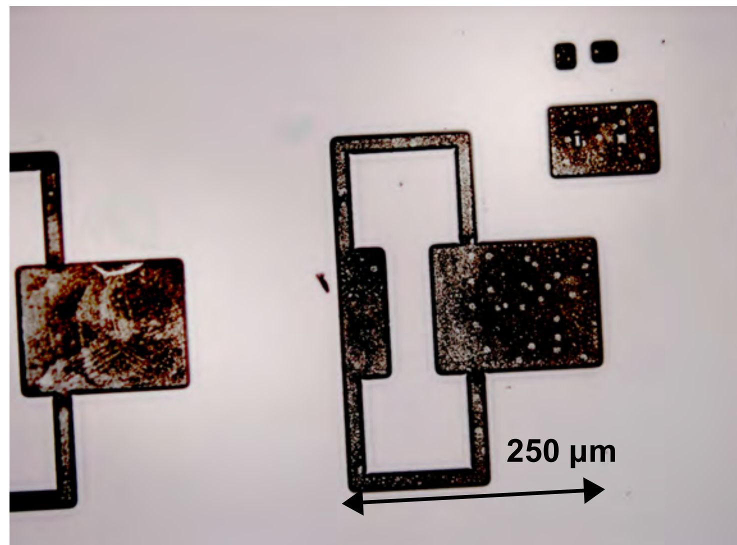

Figure 3.2: Uneven etching that occurs without oxygen plasma etch prior to NH_4Cl wet etching

The problem with this etch however, is that there appears to be some sort of etch blocking effect at the surface of the ZnO. Chang et. al. reported that etching with just NH_4Cl produced a textured uneven surface. They used a short oxygen plasma etch before the NH_4Cl etch. This made a dramatic difference to the etch – the resulting etch was smooth and even.

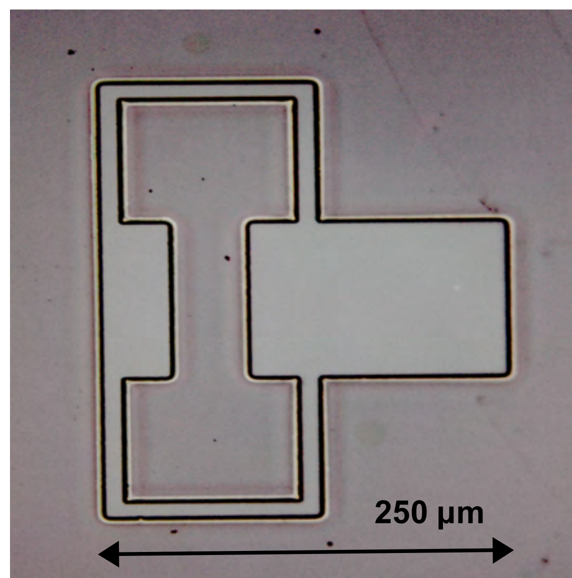

Figure 3.3: A good etch leaves a clean surface with minimal undercut.

In this work, similar results were observed. Etching in NH_4Cl only produced a very rough and uneven etch, as shown in Figure 3.2. The blackish areas are where there is an uneven layer of ZnO remaining. A 30 s etch at 400W in a barrel oxygen plasma before the NH_4Cl etch resulted in a smooth and even etch, as shown in Figure 3.3. The ZnO in this case has been cleanly and evenly etched, and there is also an acceptable amount of undercut.

The fact that the surface layer on zinc oxide produces a blocking effect, and that once the surface layer is modified/removed by a plasma etch, NH_4F etching proceeds evenly through the bulk of the ZnO material has significant implications to studies of ZnO properties that measure the surface. The properties of the surface layer may in fact not be representative of the bulk of the material.

3.5 Metal Lithography

Metal contact layers are often patterned using etching. After the metal is deposited, using evaporation or sputtering, a photoresist layer is spun on, exposed, and developed. In areas covered by photoresist, the metal layer is protected during etching. In areas where there is no photoresist, the metal is removed. When the etch has proceeded down to the substrate, the etch is complete. However, for metal deposition on ZnO, etching is not a suitable patterning method. Most wet metal etches are acidic, and would therefore attack the ZnO, because it is amphoteric. Dry etching would have very poor selectivity to the ZnO, making it difficult to terminate the etch without excessively etching the ZnO as well. Another patterning method must therefore be used.

Lift-off was chosen as the patterning method for the metal layers for these devices. To perform a lift-off, a photoresist layer is applied and patterned directly onto the substrate. The metal is then deposited over the photoresist layer. The substrate is then immersed in a solvent which will dissolve the photoresist, such as acetone. The metal which was deposited on the photoresist will 'float away', whereas the metal which was deposited directly onto the substrate will remain, assuming good adhesion exists.

Lift-off works best when the sidewall profile of the photoresist is tapered, with the top being wider than the base. This allows a shadowing effect to occur, preventing bridging from occurring between the metal attached to the substrate, and that on the photoresist. Bridging can prevent the material on the photoresist from being washed away. It is also desirable to use a method for depositing the metal in which the layer is deposited unidirectionally and perpendicularly to the substrate, which also helps to limit bridging. Non-perpendicular deposition will lead to coating on the sidewalls of the photoresist, which also causes bridging.

Achieving a tapered profile in photoresist is possible using techniques such as a chlorobenzine soak [38] prior to development. However this process is difficult to perform reliably, and also reasonably time-consuming. As long as the photoresist is considerably thicker than the metal layer, it is usually possible to achieve a reliable lift-off without having a tapered profile. If minor bridging does occur, it is usually possible to still remove the unwanted metal regions using methods such as ultrasonic agitation, or forceful squirting of solvent directly onto the surface.

3.6 Schottky Materials

The theory of Schottky contacts predicts that Schottky contacts should be formed between semiconductors and metals with high work functions [39]. Metals with high work functions such as gold, silver and platinum have been used to make good Schottky contacts to many semiconductor materials. Many workers have tried to make Schottky contacts to ZnO using those, and other metals, however the results have been generally disappointing, with large diode ideality factors, high reverse leakage currents, and low barrier heights.

Recent work by Allen et al. [25] at Canterbury University has shown that high quality Schottky contacts to ZnO can be fabricated using non-stoichiometric silver oxide (Ag_xO), rather than metallic silver. These Schottky diodes are considerably better than any others made on ZnO. The Ag_xO is deposited using reactive sputtering of metallic silver in an oxygen-argon plasma in an Edwards Auto 500 deposition system. The success of these diodes was a large motivating factor in this present work.

After deposition of the Ag_xO, a capping layer of platinum (Pt) was added using electron beam evaporation in the same chamber as the sputtered Ag_xO. This capping layer provides a low sheet resistance contact to the actual Schottky contact. It also provides scratch resistance, and a good surface for probing or wire bonding.

Between the deposition of the Ag_xO and the Pt the chamber was briefly opened to reposition the substrate from above the sputter gun, to above the electron beam hearth. The Ag_xO deposition, being sputtered, is not ideal for lift-off, due to the relatively wide range of arrival angles at the substrate. However, Ag_xO is a brittle material, and unlikely to produce as many problems with lift-off as a more ductile material. Electron beam evaporation is a better choice for lift-off, as it is extremely directional. The small hearth yields a metal flux with a very limited range of arrival angles at the substrate. It is therefore necessary to accurately position the substrate directly above the hearth in order to limit deposition on the sidewalls of the photoresist masking material.

3.7 Ohmic Materials

The connections to the source and drain of a transistor should be Ohmic contacts. The Ohmic contacts should provide a low resistance contact, to prevent unnecessary heating of the device, and maximise the device efficiency. Ohmic contacts also ensure that the connections to the channel material have linear behaviour.

There are many schemes that have been used to make Ohmic contacts to ZnO. The review by Özgür et al. [31] is a useful reference. These schemes vary from simple single layer metallisations [40], to complicated multilayer structures [See, for example: 11]. The individual layers in these multilayer structures each have different functions. The layer nearest the surface provides a low-barrier height contact to the ZnO. The next layer might be a physical (diffusion) barrier, to prevent the formation of inter-metallic alloys between two other layers. The topmost layer is typically a low-resistivity material, which provides the low sheet resistance necessary for low resistance connections between devices. These structures also often need to be annealed to achieve optimal performance.

Not only are different metallisation schemes used, but also many different pre- and post- deposition treatments may be used. Plasma treatments are sometimes used before deposition to improve contacts. The most common post-deposition treatment is a thermal annealing step. Annealing typically reduces resistivity by allowing metal grains to move, and change size. However, overheating can result in alloying and interdiffusion, which have the opposite effect.

The design of an optimised multilayer metallisation scheme can clearly be a major project in itself. Although previous research can be used as a starting point, differing deposition equipment and conditions mean that the results will often not be the same, necessitating considerable experimentation to optimise the process. Given the cost and difficulty of obtaining ZnO samples, it was decided to instead employ a simple platinum metallisation. Platinum provides a hard, scratch resistant, oxidation-resistant contact.

3.8 Array Layout

At the time of design of the transistors, the anticipated characteristics of the devices were to some degree unknown. It was therefore desirable to be able to fabricate a range of different sized transistors. This range of sizes maximised the chances of making a device with ideal, or at least measurable performance. It would also allow other parameters to be extracted, by plotting the transistor characteristics as a function of dimensions. The two critical dimensions of a FET are the length and width of the channel. To simplify the measurement and interpretation of the devices, the transistors were laid out in a grid pattern as shown in Figure 3.4. Devices of the same channel length were in one row, and those of the same width were in one column. Channel widths and gate lengths were varied from 5 μm to 100 μm.

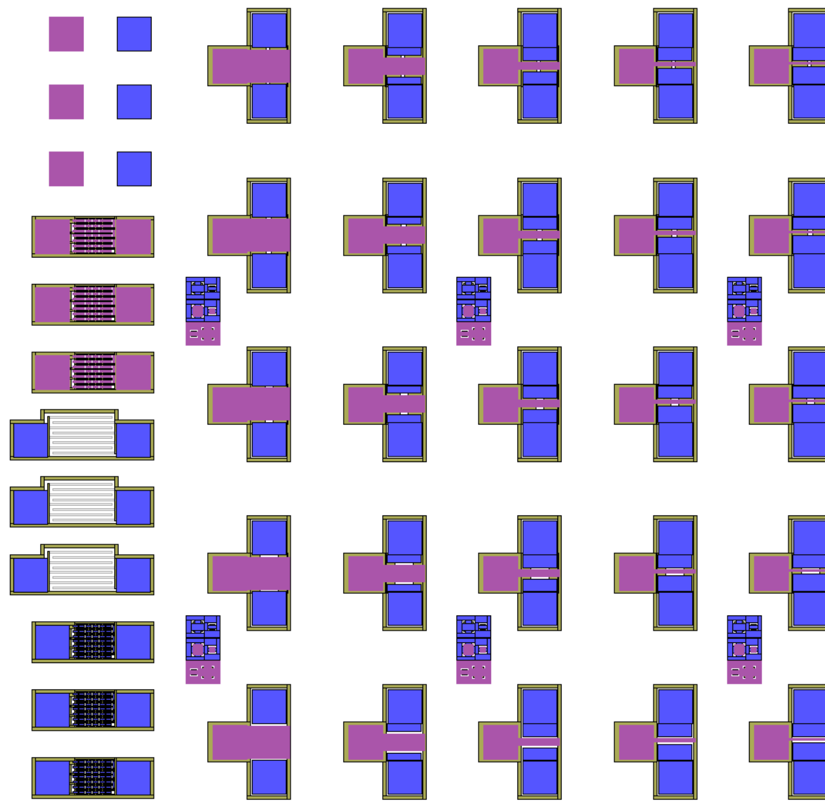

Figure 3.4: Schematic layout of the chip, showing test structures, alignment marks, and the array of transistors.

The transistors were all laid out with the same physical arrangement of contact pads. The gate, drain and source were all equally spaced on all devices. This allows simpler device testing. When the devices are being probed to measure their characteristics, it is only necessary to set up the probe positions once. Subsequent measurements can be made by simply lifting the probes, moving the substrate, and re-lowering the probes on a new device.

Figure 3.5 shows an individual transistor. The olive colour represents the 'moat' where the ZnO is etched away. The purple represents the Schottky metal area, consisting of the gate finger and a contact pad. The blue represents the Ohmic metal contacts to the source and drain. The white 'dog-bone' shape is the active area. The part which is covered by the purple gate finger is the actual transistor.

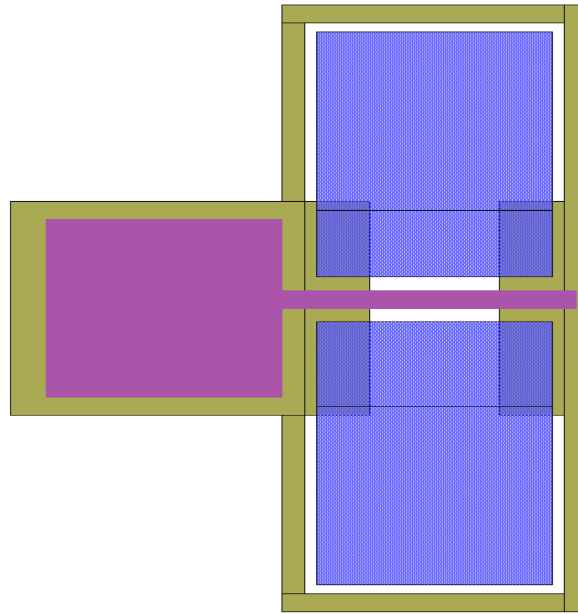

Figure 3.5: Schematic layout of one transistor

3.9 Test Structures

In addition to the array of transistors, test structures were also designed on the chip. These test structures included contact chains, serpentine resistors, and diodes. These test structures provided diagnostic capability for some aspects of the processing. These simple tests provide some confidence in the interpretation of measurements of more complicated devices such as transistors. They would also quickly indicate a problem, and save wasting time on lengthy testing of faulty devices.

The contact chains provided a means to test the reliability of contacts between the Ohmic metal and the ZnO. The contact chain consisted of 32 islands of ZnO connected by strips of Ohmic metal. Continuity between the pads at the ends of the chain would mean that all 64 Ohmic contacts were intact, and also that there was adequate metal coverage over the step up from the sapphire substrate to the ZnO surface.

The serpentine resistor was a narrow etched serpentine path of ZnO. This resistor provided additional information about the sheet resistance of the ZnO, as the serpentine shape forces current to flow along the resistor, as long as the isolation is adequate. The serpentine shape was also useful as a test of the

fidelity of the ZnO patterning and etching. Any distortions such as corner rounding would be obvious in a serpentine structure.

The diodes consisted of 3 adjacent pairs of contact pads made of Ohmic and Schottky metal. These allowed a simple test of continuity between the Ohmic pads, and a test of the diode characteristics of the Schottky contact, without any complications due to nearby isolation etches. The Ohmic contact also provided a reference contact to the bulk of the ZnO which allowed testing of the isolation etch.

3.10 Completed device

Figure 3.6 is a micrograph that shows the completed device. The Schottky contacts are a slightly pinkish colour compared to the Ohmic ones. Note that several of the Ohmic contacts are either damaged, or missing entirely. This was due to a poor lift-off. It was very unfortunate that the one occasion when this failed was the worst possible one. Nonetheless, many devices still had enough contact available to enable useful measurements to be made.

Note also the effect the poor lift-off has had on the test structures. Only the Ohmic and Schottky contacts at the top are intact. The metal contacts in the middle of the contact chains have completely disappeared in all but one structure. On that structure, none of the metal has lifted off, leaving a complete short.

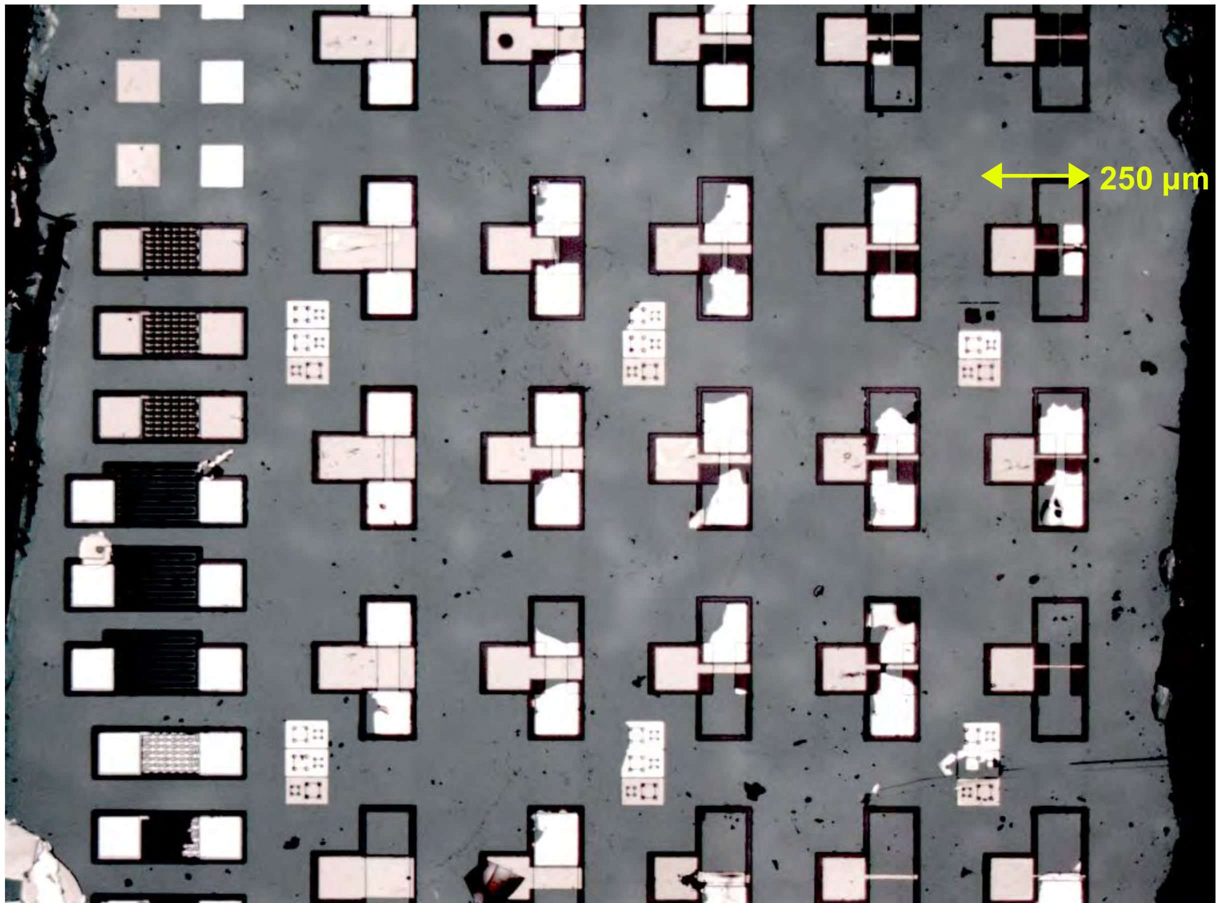

Figure 3.6: Micrograph of a fully fabricated chip. All layers are clearly visible, as is damage due to poor lift-off. Compare to the schematic in Figure 3.4

Chapter 4 - Device Characteristics

4.1 Introduction

In previous chapters, the design and fabrication of prototype hetero-epitaxial ZnO MESFET transistors has been described. This chapter describes the electrical characterisation of the devices that were fabricated.

First, the measured characteristic curves of the devices are presented, and then compared to the theory developed in Chapter 2. Discrepancies between the measured and expected behaviour are explored in some depth, and explanations proposed. Critical parameters are extracted from the measurements, which will allow these devices to be compared to other similar devices.

4.2 Experimental setup

Current-voltage (IV) measurements were made using a Hewlett Packard 4155B semiconductor parameter analyser. The 4155 has four independent built-in source-measurement units, or SMUs. Each SMU is capable of programmably sourcing voltage or current, and measuring the resultant current or voltage. The SMUs are capable of a maximum of 100 mA and 100 V, and by default will autorange down to the resolution limits of 10 fA or 2 μV. Typically an SMU is set up to sweep voltage or current from a specified starting value to a specified end value, with a given step size.

For transistor testing, one SMU can be set up as a primary sweep, and another as a secondary sweep -e.g. the primary one would sweep the drain-source voltage over the given range, then the secondary one would step to the next value of gate voltage. At each measurement point the current and voltage of

each SMU is recorded. These measurements can be plotted directly on-screen, or can be saved to a 1.44 MB 3 1/2" floppy disk for transfer to a PC.

The HB 4155B was connected to a Micromanipulator brand probe station, equipped with four manual probe manipulators. The probe station is set up inside an aluminium box which acts as a Faraday cage to reduce ambient electrical noise. The probes used are an excellent example of economy: They are stainless steel beautician's electrolysis needles, which cost well under $1 each. Figure 4.1 shows the prober set up to measure transistors on the chip; Figure 4.1(a) includes the manipulators and the Faraday shielding box. Figure 4.1(b) shows a better detail of the probe needles and the actual die. The arrow indicates the actual die, which being transparent, is difficult to see.

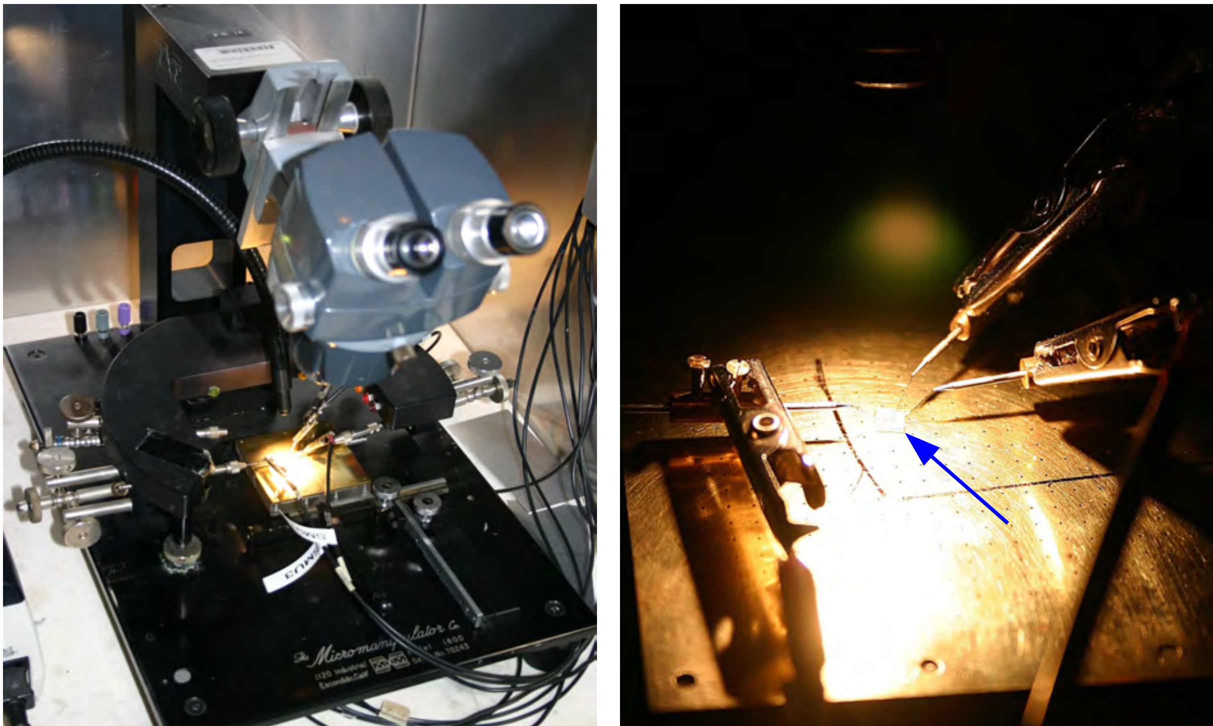

Figure 4.1(a) Prober overview showing probe station and Faraday cage; (b) showing detail of probe needles, and die being probed. The blue arrow indicates the actual die.

4.3 Gate diode characteristics

Since the performance of the MESFET depends strongly on the characteristics of the gate, it is reasonable to first consider the electrical properties of the gate. The gate is a Schottky junction, the

characteristic equation for which is derived partly from thermionic emission theory. The derivation of this equation is beyond the scope of this thesis, so it will simply be stated. Readers interested in the derivation are referred to a semiconductor physics text, such as reference [42].

$$J = J_s\left(e^{\frac{qV}{kT}} - 1\right) \tag{4.1}$$

where J is the current density flowing across the junction, V is the applied bias, T is the junction temperature, q is the charge of an electron, k is the Boltzmann constant, and J_s is the saturation current density. J_s is given by:

$$J_s = A^* T^2 e^{\frac{-q\phi_{Bn}}{kT}} \tag{4.2}$$

where A^* is the effective Richardson constant, and φ_{Bn} is the Schottky barrier height between the metal and an n-type semiconductor. φ_{Bn} in an ideal contact is the work function difference between the metal and the semiconductor, but in practice is usually quite different, and affected by surface states at the material interface.

The characteristics of the Schottky gate diodes are measured by applying a voltage and measuring the resultant current. The start point is a moderate reverse voltage, in this case -2 V, which is not sufficient to drive the diode to breakdown. The voltage is swept through to 1 V forward voltage. Since the forward current of a diode rises exponentially, that current quickly becomes limited by series resistances in the material, and no more useful information on the diode itself can be gained by measuring at higher voltages. A typical I-V plot is shown in Figure 4.2. This plot shows the data for one of the 100 μm square diodes which is part of the test structures.

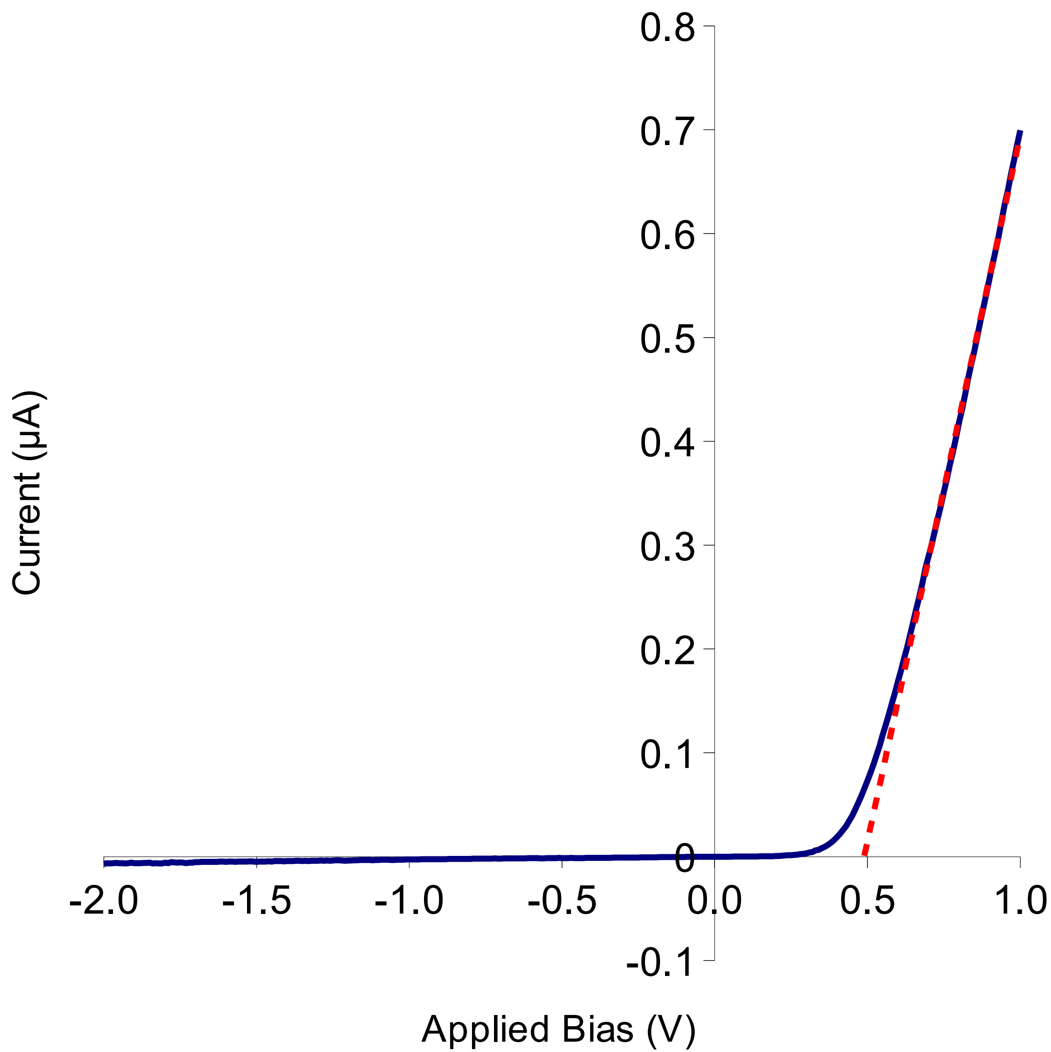

Figure 4.2: Current-voltage plot of test structure Schottky diode becomes essentially linear. The dashed line is a least-squares fit to the linear forward region.

The I-V characteristic certainly shows typical diode asymmetry, although there are a few points to note. At higher forward biases (~0.7-1.0 V) the current becomes linear with voltage, instead of rising exponentially. In this regime, current is being limited by series resistance in the circuit, which is due to both resistance in the ZnO layer, and also the contact resistance of the Ohmic contact. The red line in Figure 4.2 shows a linear regression to this section of the curve, the equation of which is

$$i = \frac{(v - 0.49)}{7.4\text{x}10^5} \quad \frac{A}{V} \tag{4.3}$$

The inverse slope of the line corresponds to the total series resistance, in this case 740 kΩ. This is quite a large resistance, which is why the effect is so noticeable. Further experiments would need to be done to quantify whether a significant improvement can be made by improving the resistance of the contacts. As mentioned previously, the composition of the contacts has not been optimised for low resistance.

Less obvious in Figure 4.2 is the fact that the reverse current is both large and non-ideal. Figure 4.3 shows the reverse current at a different scale to Figure 4.2. It is now clear that the reverse current in fact increases substantially with increasing reverse bias, rather than saturating as an ideal diode current would. The red line shows a linear fit to the reverse current. The slope of this line is 0.26 GΩ. This parameter would enable a simple comparison to be made to other diodes. At lower voltages, the current appears more like the theoretical exponential form.

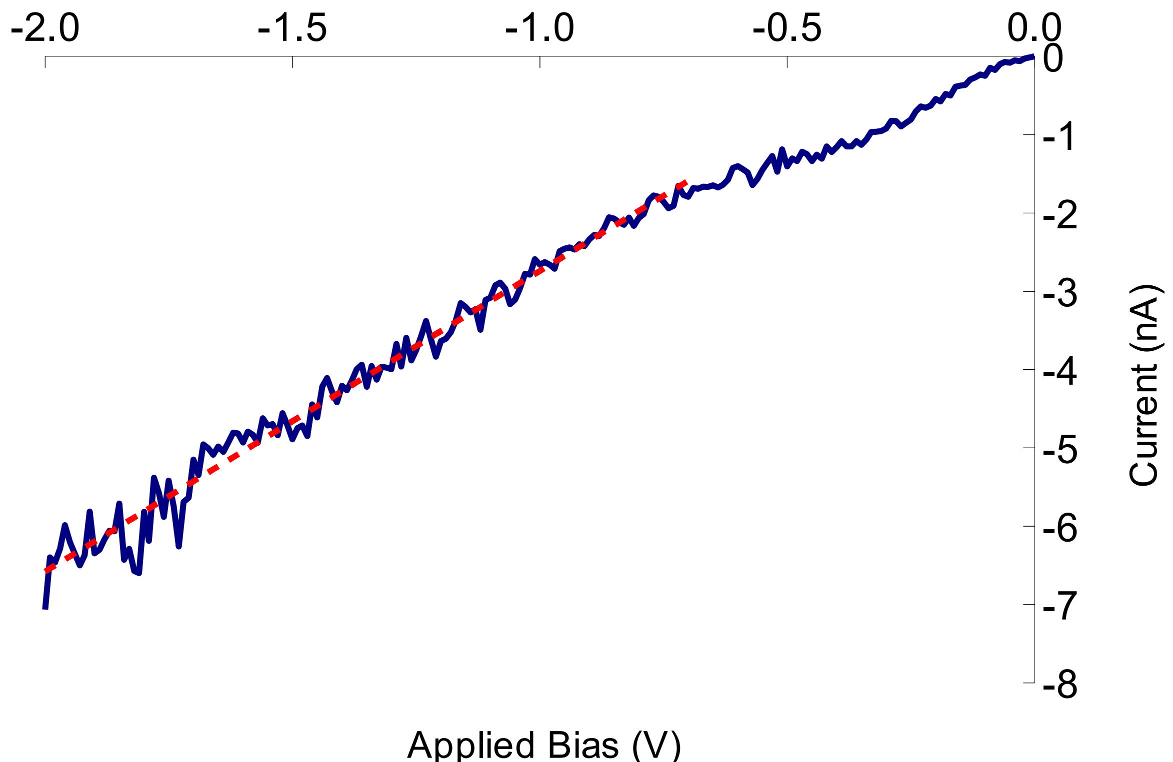

Figure 4.3: Linear plot of diode reverse current. This is an expanded scale of the same data as Figure 4.2. The red line is a least-squares fit to the linear region.

A linear plot of diode current does not provide significant quantitative information about the ideal diode parameters, which are the dominant characteristic in the curved region from 0 V to 0.6 V of forward bias. The most useful tool to analyse this region is a log-linear plot, otherwise known as a semi-log plot, such as that shown in Figure 4.4. For the region where the diode current follows ideal diode behaviour, the data will appear as a straight line. Fitting a line to this region allows extraction of the critical current and the ideality factor for the diode. These parameters correspond to the y-intercept, and slope of the regression line.

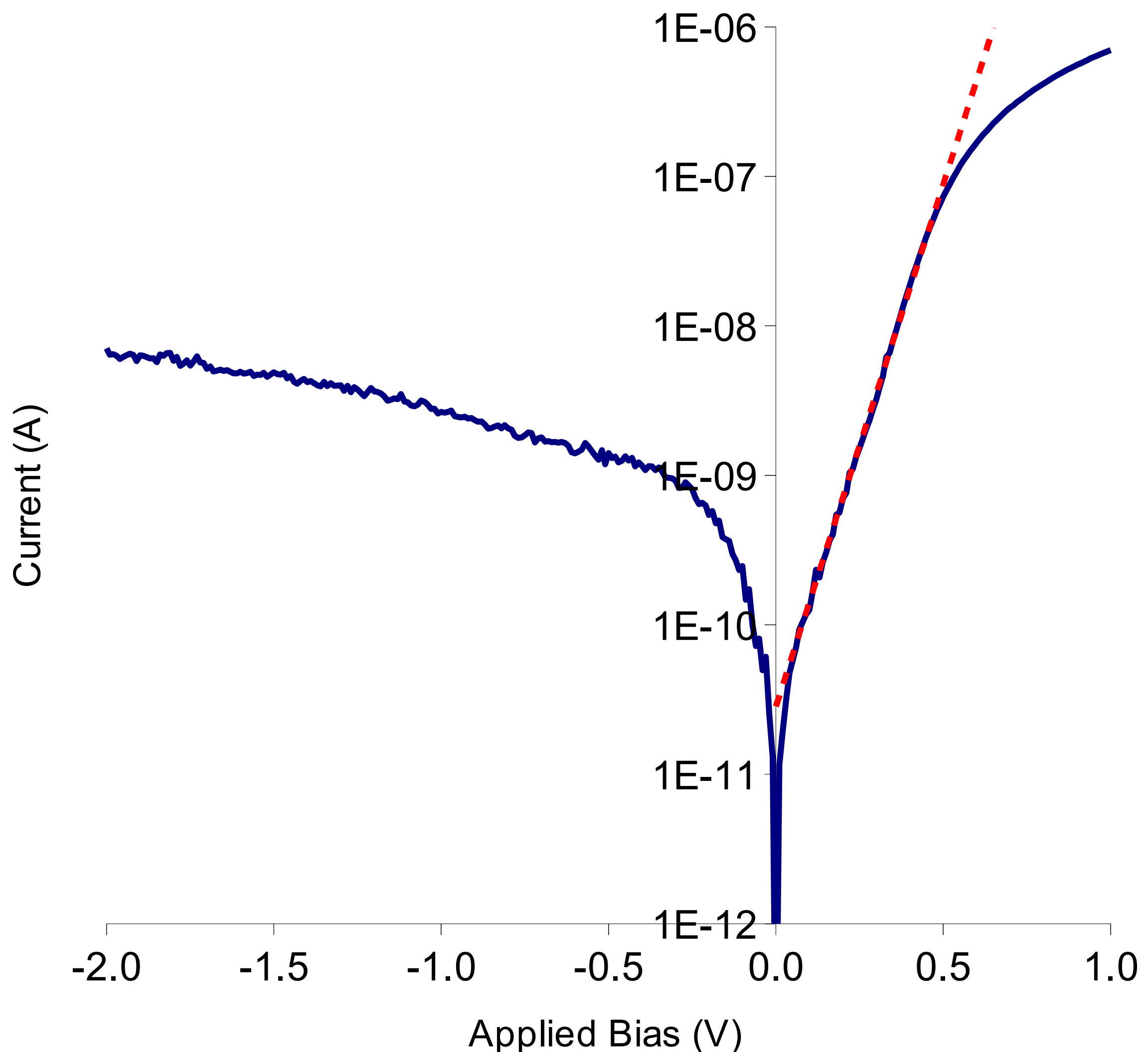

Figure 4.4: Semi-log plot of diode current. The red line is a least-squares fit to the linear region where Eqn. 4.1 is valid.

The slope of the semi-log plot for an ideal diode as described in Eqn 4.1 will be q/kT. The ratio between the semi-log slope of a measured diode and q/kT is referred to as the 'ideality factor'. The ideality factor is a measure of simply that – how ideal a diode is, or how closely the IV curve follows that predicted by thermionic emission theory. An ideal diode has an ideality factor of 1. High levels of defects will make the diode less ideal, and increase this factor, as will other effects such as lateral inhomogeneity, field emission and image force lowering [43]. The slope of the line in Figure 4.4 is 16.09 V^{-1}. This corresponds to an ideality factor of 2.5.

The intercept of the slope with the y-axis gives the saturation current I_s. If we divide by the contact area, we get J_s – the saturation current density. Using Eqn. 4.1, and using the theoretical Richardson constant of 32 $Acm^{-2}K^{-2}$, we can calculate the barrier height φ_{Bn}. This theoretical Richardson constant is calculated by substituting the ZnO effective electron mass of $0.27m_e$ [42] into a version of Richardson's equation that describes thermionic emission in semiconductor materials [44]. This yields a barrier height of 0.75 V.

The parameters extracted above are summarised in Table 1. The φ_{Bn} value is similar to other diodes fabricated on MBE-grown material, but somewhat less than those grown on bulk material [25]. The ideality of 2.5 is relatively high compared to diodes grown on bulk ZnO. This suggests some lateral inhomogeneity in the contacts, or the presence of current transport mechanisms other than simple thermionic emission [45].

Table 1: Summary of diode parameters

Diode Parameter	**Value**
Diode Area	100 x 100 μm = 10^{-8} m^2
Forward Resistance	740 kΩ
Reverse Leakage	260 MΩ
Saturation Current	$2.84\text{x}10^{-11}$ A
Saturation Current Density	$2.84\text{x}10^{-3}$ Am^{-2}
Ideality Factor	2.5
Barrier Height	0.75 V

4.4 Transistor characteristic curves

The usual way of graphically displaying the characteristic curves of a FET is to plot the drain current as a function of drain-source voltage. This is done for various values of gate voltage, which results in a continuous line for each gate voltage. The curves for a theoretical transistor based on Eq. 2.12 is plotted in Figure 4.5. This data is generated by substituting a pinch-off voltage of 3.2 V, a pinch-off current of 100μA, a built-in voltage of -0.6 V, and the parametric gate and drain voltages into Eq. 2.12. These values were randomly chosen to generate a plot with typical characteristics. It should be noted that Eq. 2.12 is only valid for the region below pinch-off. For all drain-source voltages above pinch-off, the constant saturation drain current is plotted.

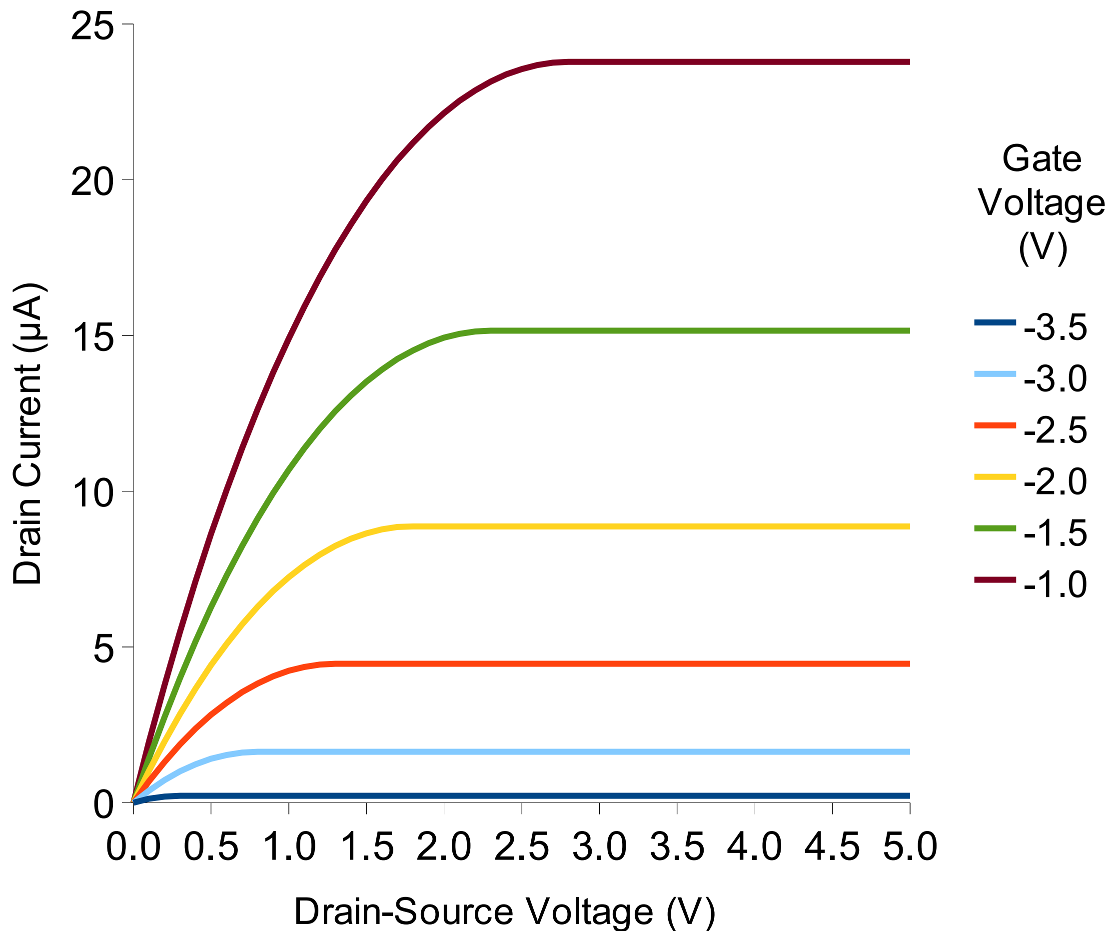

Figure 4.5: Theoretical MESFET transistor curves generated by substituting typical parameters into Eq. 2.12

There are three general characteristics of most FET devices, each of which is evident in Figure 4.5:

- When the channel is turned off, no current can flow between the source and drain, so the current is zero. All gate voltages that are such that they do not turn the channel on result in essentially zero drain current.

- There is a linear region at low drain-source voltages. The drain current is proportional to the drain-source voltage. The slope depends on the applied gate voltage.

- At higher drain-source voltages, the drain current becomes 'saturated'. The current is no longer proportional to the drain-source voltage, and instead becomes almost constant. This current is however strongly dependent on the gate voltage.

The measured characteristics of one of the fabricated ZnO transistors are shown in Figure 4.6. The drain-source voltage was varied from 0 to 2 V. The gate voltage was varied from -0.2 to 0.7 V in steps of 0.1 V. No time delays were introduced in the measurements. Note that at high gate voltages, and low drain-source voltages, the characteristics do not intersect the origin. This is because the gate is conducting under these conditions, and the resultant gate current appears superimposed on the drain or source current. The corresponding curve for $V_g = 0.5$ V has been plotted with symbols to illustrate that one data point has been affected by noise, or a bad contact.

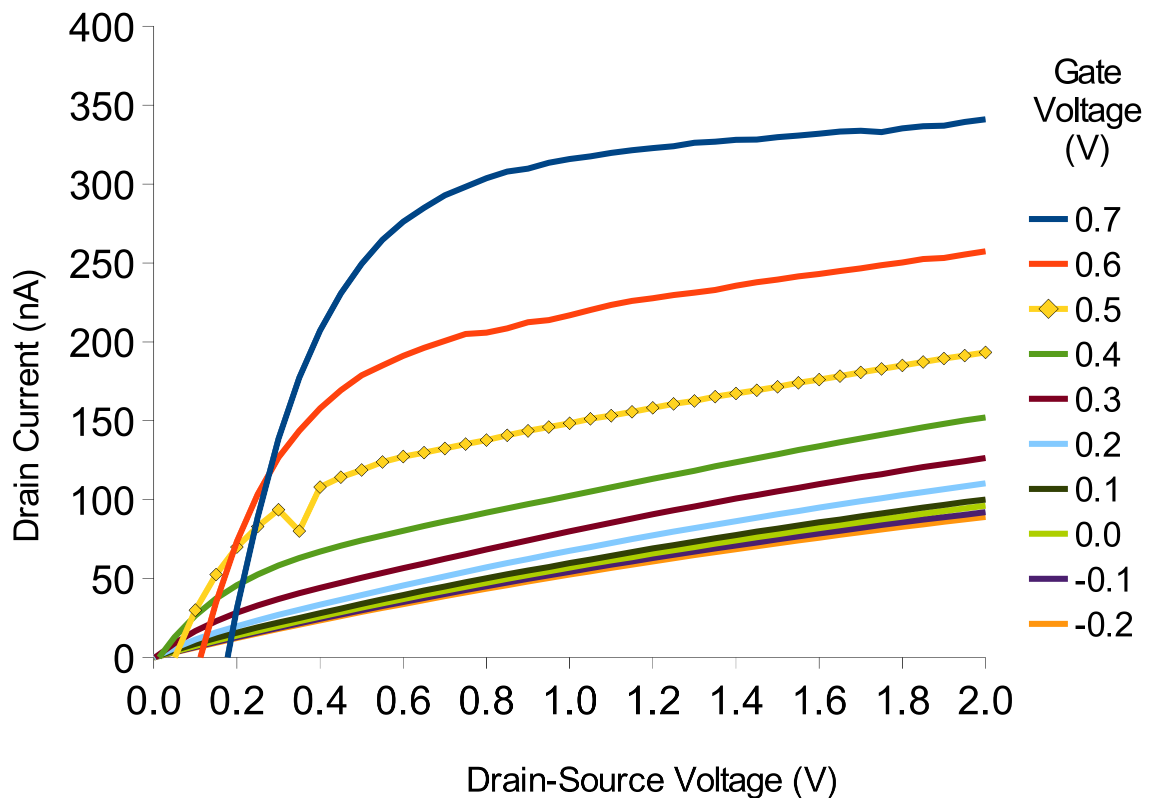

Figure 4.6: Measured curves for a nominal 25 µm wide x 5 µm long transistor.

It is clear by comparing Figures 4.5 and 4.6 that the measured data generally show the expected characteristics. At all gate voltages below threshold, the drain current is the same as at threshold. There is a clear linear region at low drain-source voltages. Above pinch-off, the linear region curves over, and limits at a current which is an essentially constant value above the 'turned off' value.

4.5 Deviations from ideal behaviour

By comparing the experimental and theoretical curves in Figures 4.5 and 4.6, it is clear that the predominant difference between them is that for each drain-source sweep, above pinch-off, the drain current continues to increase linearly, rather than reaching a saturation value. The curves for any gate voltage are all largely parallel – i.e. they have the same slope. This linear IV relationship is equivalent to a simple resistive parasitic conduction path between the source and drain. In addition, at higher reverse gate voltages where the transistor should be turned off, the IV relationship becomes purely linear. This indicates that the transistor has in fact been turned off, and all current flow is due to a parasitic conduction path.

There are various possible mechanisms for this parallel conduction. As part of the growth of the ZnO, a low-temperature buffer layer is initially grown on the sapphire substrate. This buffer layer is grown to reduce strain between the sapphire and the high quality main ZnO growth. This layer is often conducting, due to a high defect density. It is also possible that the surface of the ZnO is conductive, as several groups have reported a conducting surface layer on ZnO [46,47].

To further examine and quantify this conduction, an analysis was made of the parasitic conductivity of transistors of different geometries. The conductivity of different sized transistors may give information as to the parasitic conduction mechanism. In addition, by quantifying the parallel conduction, it is then possible to model the transistor / resistor combination. This will allow transistor parameters to be extracted more reliably and accurately.

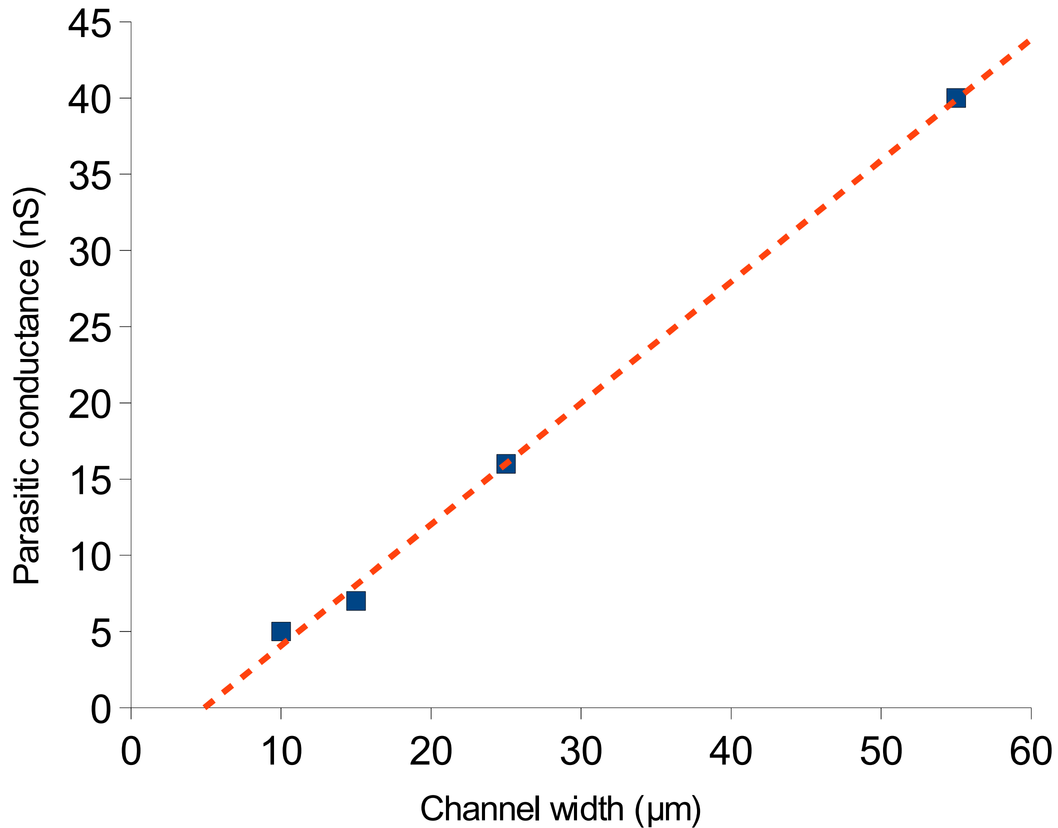

Figure 4.7: Parasitic conduction vs. channel width for 95 µm long transistors

As described in Chapter 3, the chip was designed with an array of transistors of various gate lengths and widths. For each transistor of a given width and length, a least-squares fit was made to to the I_d/V_d data. The gate was driven below threshold voltage. In Figure 4.7 the parasitic conduction of transistors with a nominal gate length of 95 µm is plotted as a factor of the as-drawn channel width. It is clear that the conduction is proportional to the channel width. The x-intercept of around 5 µm correlates reasonably well with the reduction in channel width due to undercut of the channel etch. The parasitic conduction of transistors with a channel width of 25 µm was plotted against their as-drawn gate length. There appeared to be an inverse relationship to gate length. This data is plotted in Figure 4.8 against reciprocal gate length, and shows a reasonably linear relationship. The dashed line is a least-squares regression fit to the data.

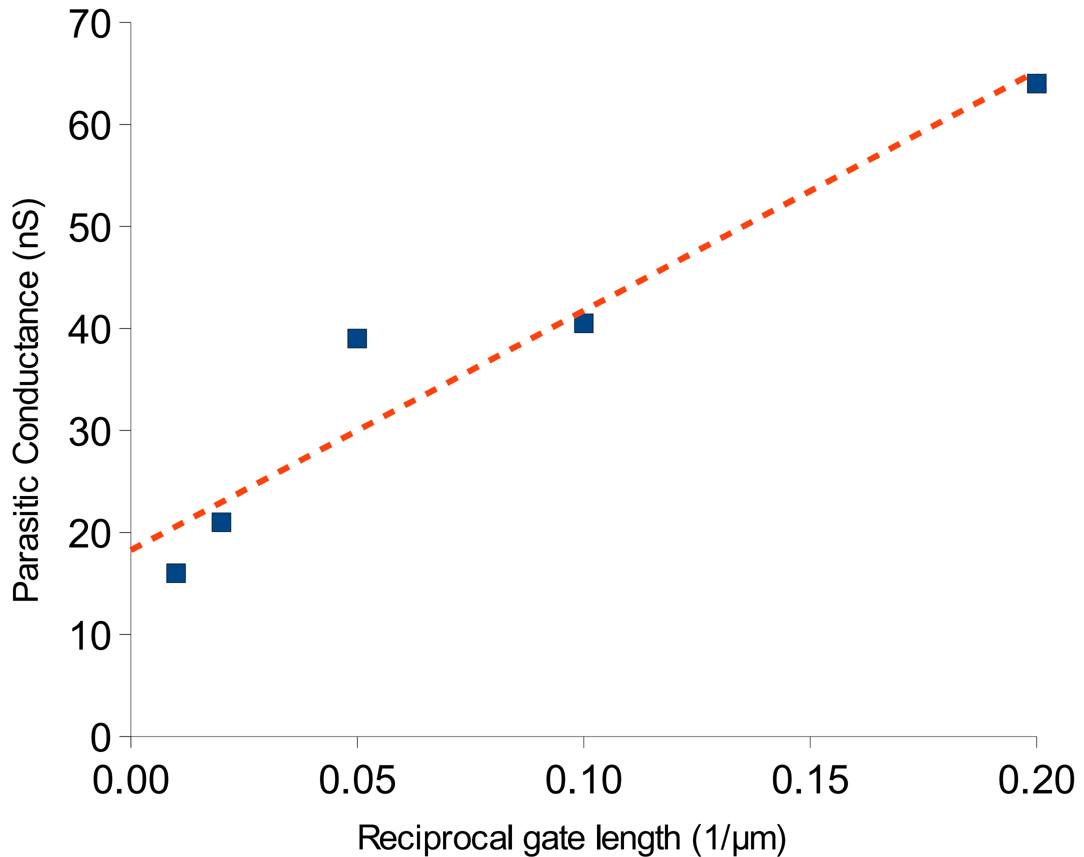

Figure 4.8: Parasitic conductance of 25 µm long transistors

A linear relation between channel width and parasitic conduction, and an inverse relation between gate length and conduction indicates that the parallel conduction is through the etched channel, and has a constant sheet conductance. Measuring the slope of the two linear curves, substituting in the appropriate values for sizes, and adding 5 µm to the nominal/as-drawn channel width to allow for the undercut due to the ZnO etch, allows the estimation of a sheet conductance or resistance value for the parasitic conductance. The two curves give rather different values for this parameter. These are 75.6 and 11.7 nS/□, or 13.2 and 85.2 MΩ/□, respectively, as summarised in Table 2.

Table 2: Calculation of parasitic conductance

Gate Length	**95 µm**	**Channel Width**	**25 µm**
Effective length	95 µm	Effective width	20 µm
Slope	$7.96 x 10^{-10}$ S/µm	Slope	$2.35 x 10^{-7}$ S/µm
Sheet conductivity	$7.56 x 10^{-8}$ S/☐	Sheet conductivity	$1.17 x 10^{-8}$ S/☐
Sheet resistance	$1.32 x 10^{7}$ Ω/☐	Sheet resistance	$8.52 x 10^{7}$Ω/☐

Note that the two points at the right in Figure 4.8 are those for the shortest gate lengths. Small errors in the measurement of these lengths would have a considerable relative effect on their position along the axis. They also have a disproportional weight in the fitting of the regression line. This data is therefore considerably less accurate than that in Figure 4.7. Considering the leftmost 3 points, which are very collinear, the resulting sheet resistance is 34.4 MΩ/☐, which is considerably closer to the 13.2 MΩ/☐ figure obtained from Figure 4.7.

Closer examination of the curves at high gate voltages and high drain-source voltages in Figure 4.6 show that there is a slight droop. The current does not stay at a constant offset from the below threshold current, but in fact drops slightly. This is not expected in the ideal model. It would be useful to establish the origin of this droop.

One mechanism for droop in FET devices is the effect of temperature. High drain-source currents can cause heating, due to resistive losses in the device. The elevated device temperature results in a lower device gain, which consequently reduces the drain-source current. Self-heating is a slow process due to the thermal mass of the substrate. One way to overcome this is to use a pulsed I-V measurement scheme. By pulsing the current, the device has chance to cool between measurement points, and therefore the self-heating effect can be reduced.

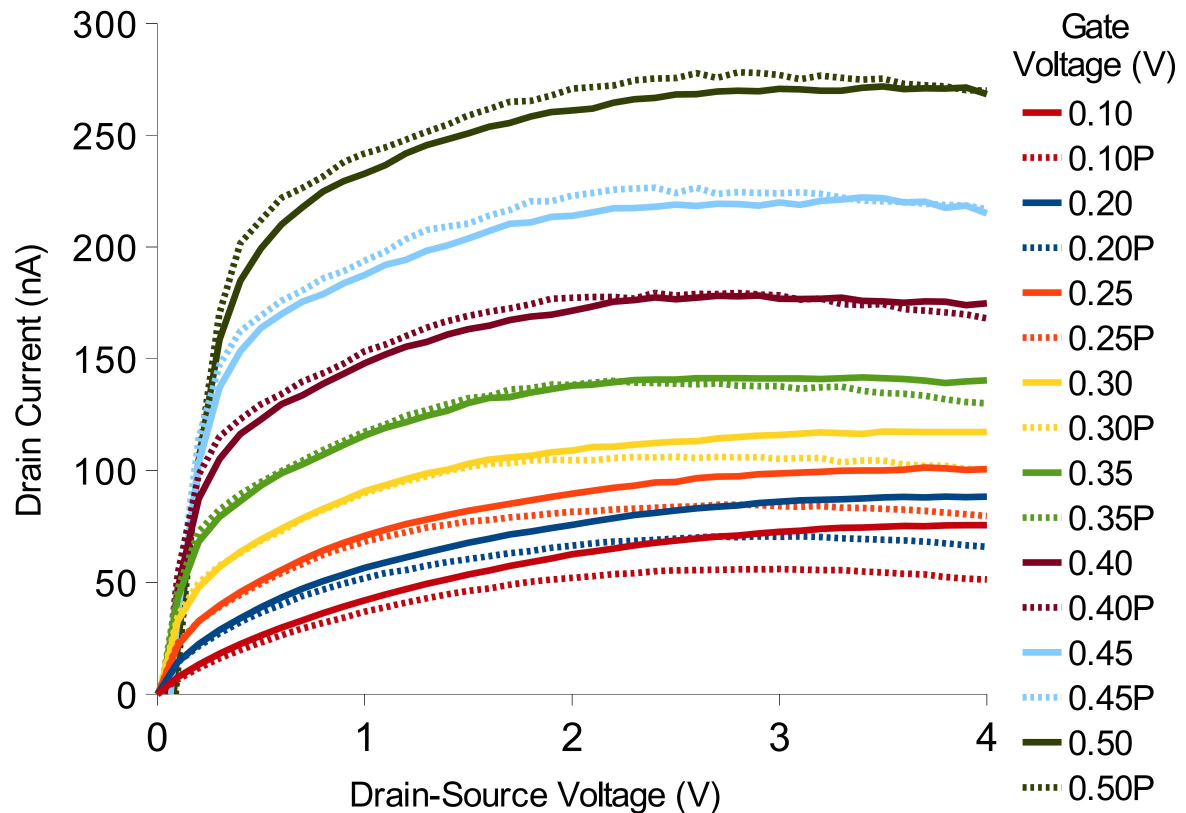

Figure 4.9: Transistor curves showing effect of pulsed measurements

Figure 4.9 shows a comparison between a normal continuous I-V sweep, and a pulsed I-V sweep. For the pulsed I-V, the current was on for 5 ms out of a total period of 100 ms. The pulsed measurements are shown with dotted lines, and both curves for a given gate voltage are the same colour. The graph shows that there is a difference between the two curves, but in fact the pulsed measurements show more droop that the continuous ones. It would therefore appear that self-heating is not the mechanism for this droop.

Another possible explanation for droop at high currents is the effect of the source resistance. From the diode measurements in Section 4.3, there are clearly substantial resistances in either the Ohmic contacts, or the ZnO itself. At higher drain currents, this resistance would result in a voltage drop between the point of application of the voltage at the drain contact and the voltage at the channel itself. This would result in an effective lowering of the gate voltage. This would result in a droop, as we have seen.

4.6 Transistor parameters

The threshold voltage of a transistor is the critical value of gate voltage above which the transistor starts to conduct. It is quantified by plotting the square root of the drain current against the gate voltage, at a constant drain-source voltage corresponding to the saturation region. This plot will have curved regions at low currents, and also at high currents, if series resistance is significant. At midrange currents, the square root of the current will be proportional to the gate voltage. A line fitted to this linear region will have an x-intercept at the threshold voltage. This data is plotted in Figure 4.10.

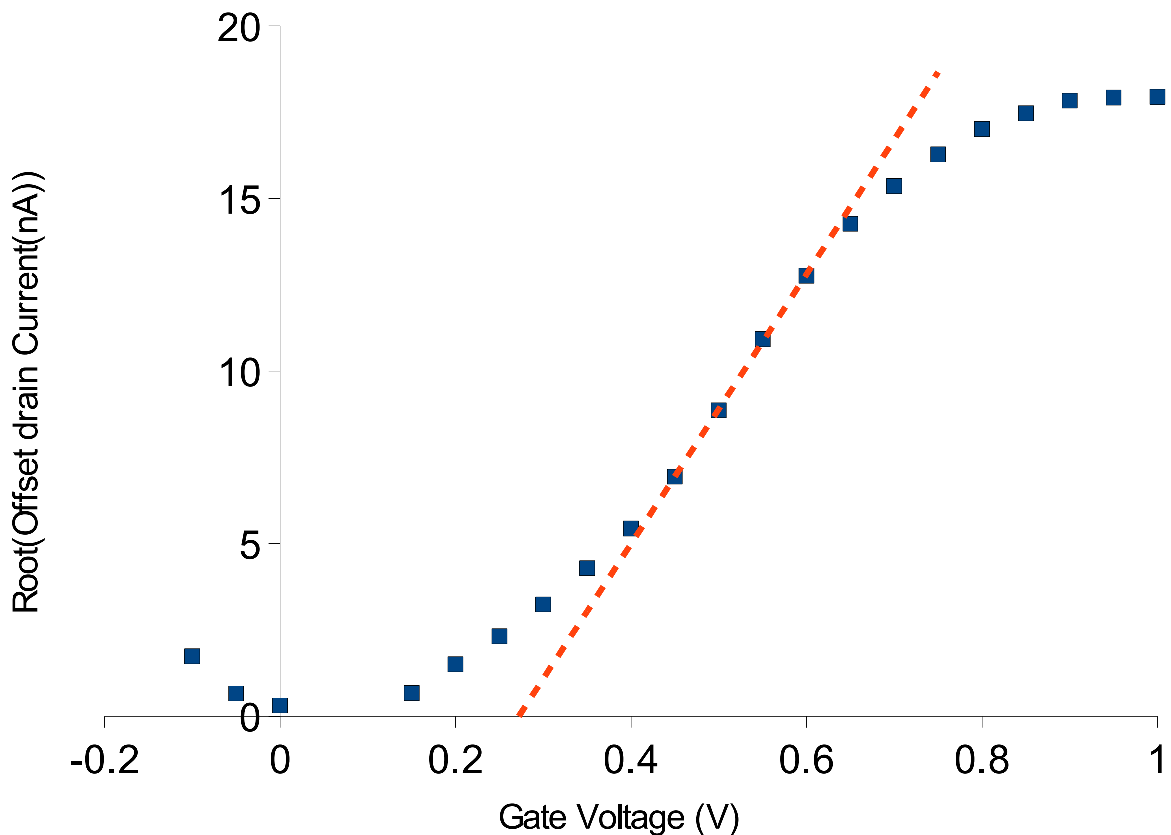

Figure 4.10: Plot used for threshold voltage extraction. The x-intercept gives the threshold voltage. The slope of the line can be used to calculate the channel mobility.

The drain currents were in nA, and have had a fitted parasitic conductance removed. The linear region is small, but recognisable. The threshold voltage is 0.27 V. This value correlates with the fact that the curves for I_d only start to obviously deviate from the parasitic current at gate voltages above this value.

The fundamental problem with these devices is the fact that this threshold voltage is so high. There is an extremely limited range of gate voltages (around 0.3 V) which are above threshold, and yet have a minimal forward gate current. Ideally, the threshold voltage would be at least 1 V lower than the present value, in order to increase the usable gate voltage range, and to increase the drain current.

Channel mobility is a concept that is commonly used to compare different materials that can be used to make transistors. It can also be used as a check that the performance of fabricated transistors are as good as they can be. To extract the channel mobility, measured data are substituted into the transistor equations, and the mobility is extracted as an unknown. This value can be compared to the mobility measured by other techniques such as Hall effect measurements. A significant reduction in effective mobility may mean that the transistor processing has degraded the material in the channel.

The channel mobility can be easily measured in either of two regions of the characteristic curves. These are the saturation region, or the linear region. The mobilities measured in these two regions will usually be slightly different, mainly due to second-order effects. In the saturation region, the channel mobility can be calculated from the slope of the fitted linear line in Figure 4.10, since in the saturation region, where $V_d > V_g$ equation 2.12 can be simplified to [39]:

$$I_{d_{sat}} \approx \frac{Z \mu \varepsilon}{2 D L} (V_g - V_T)^2 \tag{4.4}$$

Or, rearranging:

$$\mu \approx \frac{2 D L}{Z \varepsilon} \left(\frac{\sqrt{I_{d_{sat}}}}{(V_g - V_T)} \right)^2 \tag{4.5}$$

The term in braces in Equation 4.5 is the slope of the line in Figure 4.10. The slope of 39.1 for currents displayed in nA corresponds to a slope of 1.1×10^{-3} $A^{0.5}/V$. This value when substituted into Equation 4.5 yields a mobility of 24.6 cm^2/Vs. This is somewhat lower than the Hall mobility of 57 cm^2/Vs that was measured on other pieces of the same wafer. This suggests that there was some degradation in material properties due to the device fabrication.

The transconductance, which is usually denoted g_m, is a particularly useful parameter for circuit designers for establishing the DC characteristics and operating point of a FET. The transconductance is the ratio of the rate of change of drain current to the rate of change of gate voltage – or dI_d/dV_g. It is probably clear from looking at the spaces between the gate voltage lines in Figure 4.6 that the transconductance varies substantially with both gate voltage and drain-source voltage. The value which is of most significance would depend on the application area – i.e. in which regime the transistor is going to be operated. The value of g_m as a function of these two parameters is shown in Figure 4.11.

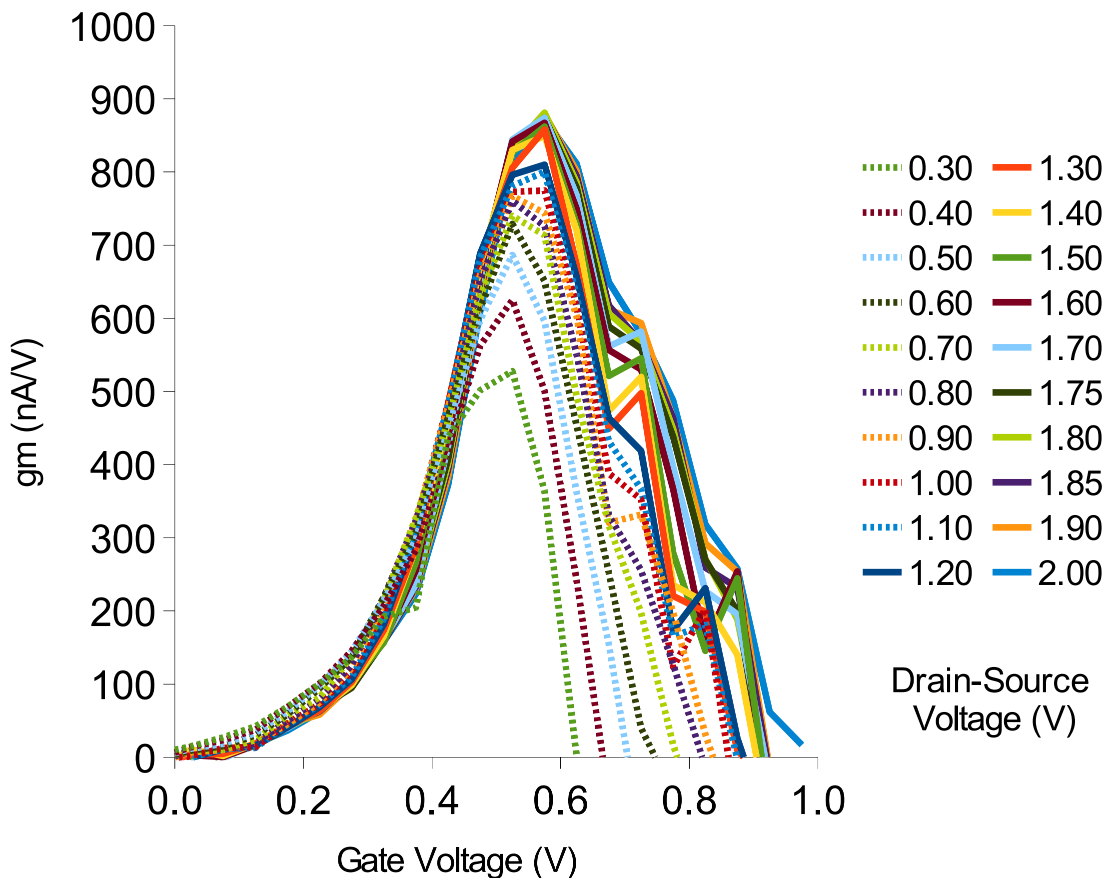

Figure 4.11: Transconductance as a function of gate and drain-source voltages.

Figure 4.11 shows that the maximum value for g_m is 880 nS and occurs at a gate voltage around 0.6 V, and a drain-source voltage of 1.8 V. Since the device had a gate width of 20 μm, this yields a

transconductance per unit length of 44 mS/m, or 0.44 mS/cm. This peak is similar for a range of drain-source voltages, as would be expected since this is the saturation region. The noise that is evident in the data of Figure 4.6 shows up even more in this graph, resulting in sizeable spikes and jumps, however the general form of the data is clear. Above threshold, g_m increases with increasing V_g until it is limited – presumably by series resistance.

Chapter 5 - Discussion

5.1 Device performance

In this chapter, the performance of the fabricated devices will be discussed, and put in context with the performance of similar and related devices that have been reported by other researchers. The nature of the parasitic conduction that was measured will also be discussed. Some initial analysis will also be presented and discussed.

There are two main reasons why the performance of this set of prototype transistors is somewhat limited. One is that at 440 nm, the ZnO layer is too thin; the other is that the ZnO layer was not intentionally doped. These effects are somewhat related, in that one accentuates the effect of the other.

The Schottky contact has a built-in voltage, due to the work function difference between the ZnO and the Schottky contact. In the present set of devices, the depletion region that results from this built-in voltage extends fully across the full depth of the ZnO layer, even when no gate voltage is applied. It is therefore necessary to apply a positive gate voltage to counteract the built-in voltage, and allow the channel to conduct. The range of positive voltage is limited by the onset of conduction of the Schottky diode, and so the usable gate voltage range is extremely limited.

The lack of doping of the ZnO is arguably the major limitation on these devices. Doping (if correctly done) would increase the carrier concentration. This would in turn reduce the depletion region depth, which would mitigate the lack of film thickness. It would also reduce the increase in depletion depth for a given increase in gate voltage. This would increase the usable voltage range. If the ZnO was doped, it would also have a lower resistivity, and therefore a lower series resistance in the material that connects the channel to the metal pads. Heavy doping would, however, also make it more difficult to

make a reliable Schottky contact. It would be necessary to ensure that good Ag_xO Schottky contacts can still be made to ZnO layers doped to the desired level.

To put the device performance into perspective, it is pertinent to compare to devices produced by other groups. At present, there are only a few similar devices to which they can be compared. As mentioned in Chapter 1, there are many publications describing ZnO TFTs, however a comparison with a TFT would probably be unproductive, as the polycrystalline channel material is typically considerably lower quality. More useful comparisons would be with devices fabricated on epitaxially grown material.

The high quality Schottky diode technology that has enabled these devices to be fabricated is relatively recent, so ZnO MESFETs are still relatively rare. Nonetheless, some useful comparisons can be made with other similar devices such as MOSFETs and HEMTs. Although the transistor characteristics are quite different, measures such as channel mobility allow direct comparison of the quality of the channel material.

The most closely related devices are those made by a group at Universität Leipzig, who grow ZnO films using pulsed laser deposition. They have made MESFET devices using the same Schottky material as these devices, and have also used more traditional metals as well. In [48] they used Ag_xO gates, and obtained channel mobilities of 11.3 and 19.1 cm^2/Vs, and transconductances of 30.3 and 10.2 S/cm for ZnO films. In a later paper [19] using metallic gate materials, they achieved similar results, with channel mobilities of 6.3-24 cm^2/Vs, and somewhat better transconductances of 37.5 to 61.3 S/cm.

Earlier work by Kao et al. at the University of Florida [17] also utilised PLD and metallic Schottky contacts to make MESFET transistors. They also made MOSFETs using a similar process, and compared the devices. They did not mention channel mobilities for epitaxially grown devices, but did report a channel mobility of 5.3 cm^2/Vs for polycrystalline material grown on ITO covered glass substrates. Their MESFET had a transconductance of 1 mS/mm (10 mS/cm), which was considerably lower than the MOSFET, at 33 mS/mm (330 mS/cm)

The HEMTs grown by Kano et al. [13] using PAMBE show extremely high channel mobilities. They measured a channel mobility of 140 cm^2/Vs. This is easily comparable to high quality bulk material. Their measured transconductance was 0.7 mS/mm (7 mS/cm) – however this was a rather long device.

5.2 Parasitic conductance

The nature and location of the parasitic conduction between the source and drain are arguably the biggest questions arising from this study. As discussed, there are a few possible explanations, however narrowing down which one it is has proven difficult. Part of that has been the difficulty of finding useful diagnostic techniques that would conclusively determine the nature and physical location of the conduction.

One thing that the experimental data has conclusively shown is that the conduction is a 'layer' effect. It is largely proportional to the width of the channel, and inversely proportional to the length of the channel. This effectively rules out external conduction paths, such as along the edges of the channel, or 'around the outside' of the device, as a completely external path would be independent of channel geometry, and an edge conduction would not be proportional to the channel width. It is therefore necessary to look at the ZnO layer itself. The most simple and likely mechanisms for the conduction would be at the extremities of the ZnO layer – i.e. at the external interfaces. These would be between the substrate and the ZnO, or at the interface between the ZnO and the Ag_xO. 'Simple' in this case refers to a conceptually simple mechanism. There are also reasonable physical reasons why conduction may occur at these locations.

The growth of ZnO on sapphire involves an initial low temperature deposition of a buffer layer. The buffer layer acts as a transition layer between the two different crystal materials. Part of that buffer action is stress relief. This buffer layer would by nature have a high density of defects, and therefore could well be degenerate, and conducting [49,50]. The interface between the ZnO and the Ag_xO is another possible conduction path. As indicated in Chapter 4, there have been reports of conducting layers at the surface of ZnO [46,47]. It is possible that similar layers could exist at the Schottky

interface. They could also be a consequence of the reactive oxygen plasma that is used to grow the Ag_xO film.

One of the diagnostic techniques that should be able to provide some information about the location of conducting layers in a semiconductor is capacitance-voltage (CV) profiling. In this technique, a DC voltage is applied to the gate. Superimposed on this voltage is a small AC voltage. As the reverse voltage is increased, the depletion region under the gate increases. The AC current that flows in response to the applied AC voltage is proportional to the capacitance of the depletion region. This measured capacitance can then be used to infer the thickness of the depletion region, based on the area of the gate, and the dielectric constant of the semiconductor.

The rate at which the capacitance increases as the voltage rises is related to the density of carriers in the semiconductor material. When the depletion region reaches the non-conducting substrate, the conducting material that acts as the other plate of the capacitor should effectively disappear – at which point the capacitance should drop to a very low value, which would represent the fringing capacitance around the periphery. If there were a conducting layer at the substrate, this should remain as a semi-permanent capacitor plate. If this were the case, the capacitance should fall to a fixed value, and remain at that value.

In the ZnO film used in this work, the positive threshold voltage again causes measurement problems. Because the ZnO is already fully depleted at a zero applied bias, it is necessary to apply a positive voltage to explore the region where the channel is depleting. Again – only a limited range of voltages can be applied before the positive DC voltage results in a DC current which swamps the results, and makes them difficult to interpret. Another problem is that the gate and diode sizes are quite small, so the capacitances measured are comparable to parasitic capacitances in the measurements. These capacitances act as offsets to the capacitance that is intended to be measured, and can distort the interpretation of the data.

Figure 5.1 shows the result of a CV measurement of a 100 μm square diode. The measurement was done with a Keithley 590 CV meter using 1 MHz AC. There are several points to note: The maximum

capacitance is 1.4 pF – which is around that which would be expected for a 100 μm square, 400 nm thick, fully depleted ZnO layer. The maximum also appears at around +0.2 V, which corresponds with the threshold voltage measured for the transistors. However – at voltages above this voltage, where one would expect that the depletion layer is getting thinner, and therefore that the capacitance would increase, it in fact decreases.

The traditional method of analysing the CV characteristics of a depletion region is to plot $1/C^2$ against V. This is clearly inappropriate here. Not only is the capacitance changing in the 'wrong' direction, but also, the fact that the capacitance is approaching a zero value, $1/C^2$ is therefore increasing asymptotically.

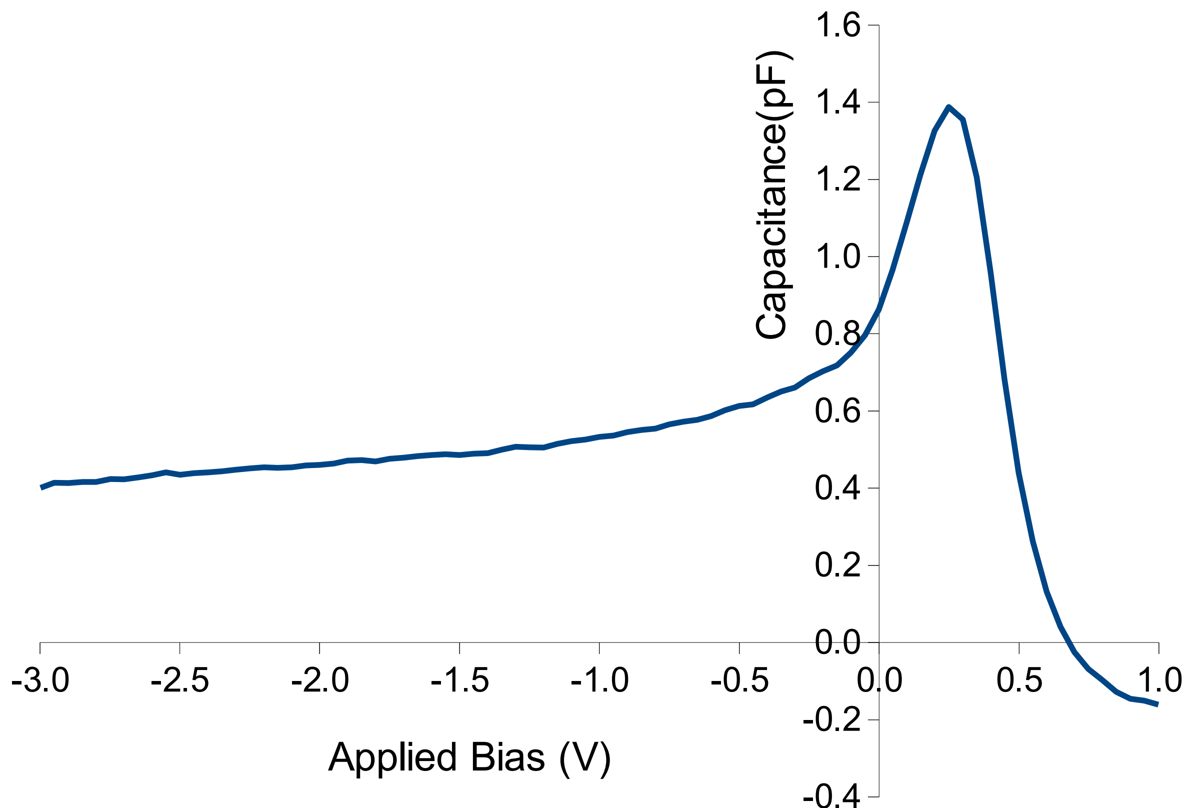

Figure 5.1: Capacitance-voltage plot of 100 μm square diode.

The behaviour at higher reverse voltages appears to be more predictable. At high reverse voltages the capacitance falls slowly, and is also quite small. This would correspond with the model of a fully

depleted ZnO layer, where the capacitance is purely due to peripheral fringing capacitance. As the reverse voltage increases, the lateral depletion would increase, and the capacitance would slowly fall.

At more moderate voltages (+0.2 V to -0.5 V) – the behaviour is less clear. The capacitance certainly does not fall quickly, as one might expect when the ZnO is fully depleted. It is possible that due to resistive effects, the depletion happens radially, which would explain the gradual fall. However, the 0.7 V range over which this happens does seem rather large.

However, going back to the transistor, there is considerable parasitic conduction in the full reverse voltage regime, such as gate voltages of -1 V. The CV measurements indicate a low capacitance in this regime. If there were a degenerate conducting layer just above the substrate, this layer should act as a capacitive counter-plate; producing a 100 µm square, 440 nm thick capacitor. Such a capacitor should have a capacitance of around 1.8 pF. This is clearly not the case. This appears to show that in fact there is no conductive layer near the substrate, and would suggest that the parasitic conduction is not in fact through degenerate buffer layer material. In summary, it is unclear why the capacitance falls over the +0.2 V to +0.7 V range. It is unclear why the capacitance falls slowly over the -0.5 V to +0.2 V range. The behaviour in the voltage range below -0.5 seems reasonable. All these measurements, however, were conducted at 'high' frequency AC. It would be useful to re-do these at a considerably lower frequency, to compare the results. CV at lower frequencies can give very different information, as the carriers may not be able to respond to high frequency fields, but can to lower frequencies.

Chapter 6 - Summary, Conclusion, and Directions for Further Work

6.1 Summary and Conclusions

A large amount of work in semiconductor research over the turn of the millennium has focussed on wide-bandgap compound materials. These materials are of particular interest due to their transparency in the visible spectrum and the potential for integration of both optical and electronic components. Zinc oxide (ZnO) is of particular interest due to being relatively non-toxic, thermally stable, and made from inexpensive raw materials (at least in impure form).

The development of electronic devices made from ZnO has been hindered by the difficulty of making p-type doped material. There has also been a lack of high quality Schottky contacts. The recent development of excellent non-stoichiometric silver oxide (Ag_xO) Schottky contacts at Canterbury University has facilitated the development of electronic devices such as MESFET transistors, which use a Schottky diode and mesa isolation rather than p-n junctions.

In this work, MESFET transistors have been successfully fabricated from ZnO films grown by plasma assisted molecular beam epitaxy on single crystal sapphire substrates. The Schottky contact material was Ag_xO, with a metallic platinum capping layer which was also used as the Ohmic contact. The fabrication used mainly standard planar semiconductor fabrication techniques. It was necessary to develop a technique for mesa etching the ZnO with minimal undercut.

A series of Schottky diodes and transistors were tested, and both generally showed the expected characteristics typical of that device. The performance of the diodes was not as good as similar diodes

fabricated on hydrothermally grown ZnO, but the quality was adequate for this application. The transistors showed typical transistor characteristics, but this was superimposed on a parasitic conduction. The nature of this conduction was quantified and investigated. The physical location and mechanism of the conduction has not been determined.

The transistor performance was not ideal. This was mainly due to the non-optimised characteristics of the ZnO film used. Equipment problems have prevented the subsequent growth of more optimal films, that would hopefully allow considerably better transistors to be fabricated. Measurements on these transistors have however provided information that would allow those optimisations to be subsequently made.

6.2 Directions for future work

The greatest limitation of the MESFET transistors was the fact that the threshold voltage was positive, as it seriously limited the usable gate voltage range of the transistors. Reducing the threshold voltage should allow transistors to be made that more accurately represent the potential performance of these devices. Growing more ZnO films with different growth parameters would enable this to be done.

The simplest option to make better transistors using the existing growth parameters, would be to grow the film thicker. This would mean that the depletion region due to the built-in voltage of the Schottky diode no longer extended fully across the film. The downside to this approach would be the considerably longer time that it would take to grow the film. The films used in this work already took 3 hours to grow. Considerably longer growth times make the logistics of growing a film during a working day more onerous to the operator, and could mean that there is a higher likelihood of a catastrophic failure during growth. Also there may be gradual changes in growth conditions over the longer time of the growth, making the resultant films inhomogeneous.

An alternative scheme would be to deliberately dope the material to increase the number of carriers. This would have the effect of reducing the depletion width, and therefore the threshold voltage. It would also reduce the series resistance of the device. The downside to this method is that adding a

dopant material could mean considerable work in re-characterising the growth parameters, if adding the dopant affected the growth kinetics. It would also however reduce the barrier height of the Schottky contact as well. It would almost certainly be necessary to perform multiple test growths to determine the amount of dopant material necessary to achieve the desired carrier density, and also fabricate Schottky contacts to ensure that the resulting junctions would be of high enough quality to make devices from. It would also possibly require some testing as to whether it is necessary to anneal the material after growth to activate the dopant, and also to quantify the thermal stability of the resultant material, if higher temperature operation of the resultant transistors is desired.

Growing more films would allow further study of the lateral parasitic conduction layer. Altering the growth conditions of the buffer layer may change the conduction of that layer, if that layer is in fact where the conduction is. Since the lateral parasitic conduction is easy to quantify using a transistor structure, growing transistors would be one way to study the effect of mitigation techniques. Those techniques might include such things as post-growth annealing steps, anneals after the gate material deposition, or gate material deposition temperature.

The transistor and diode results presented show that there is a considerable resistance in series with the diode or transistor. This is probably partly due to the resistance of the ZnO layer, and partly due to the resistance of the Ohmic contact. As has been mentioned previously, the Ohmic contact was not been optimised for low resistance, and the specific contact resistance has not been measured. A 'known good' ZnO Ohmic contact was used, to maximise the likelihood of making working devices on the extremely limited amount of pre-grown ZnO film that was available.

There are many reports in the literature of Ohmic contact materials that could be used as alternative contacts. Many of these are reviewed in [31]. There are also well known techniques such as the 'transfer length method' (TLM) [51] for quantifying the resistance that is due to the contact, and separating that resistance from that of the underlying film itself. A TLM test structure would be extremely useful to add to subsequent devices, both to quantify the specific contact resistance of the platinum contact, and also to compare this to that of any alternatives used. Using alternative Ohmic

contact schemes would probably considerably improve the performance of the transistors, and should be relatively easy to quantify, if sufficient high-quality films were available for use for making transistors.

Recent work on high quality ZnO Schottky contacts at the University of Canterbury has shown that using iridium as an alternative to silver in the non-stoichiometric oxide contact produces even better Schottky diodes [52]. The iridium oxide material also has considerably better thermal stability than that of the silver variety. Diodes have been successfully tested at high temperatures.

Making transistors with iridium contacts would be a very interesting exercise. The use of iridium could reduce the leakage current of the gate, and possibly extend the usable range of gate voltages. More importantly, the high thermal stability of the gate material may enable transistors to be made with extremely high operating temperatures. These may have considerable interest in certain niche application areas such as space electronics, nuclear reactor applications, geothermal monitoring, and engine control and monitoring [53]. Being a high-bandgap material, ZnO will be inherently useful at high temperatures, due to lower reverse leakage current than lower-bandgap materials.

The pulsed IV measurements that were performed in order to see whether self-heating was causing a droop in the drain-source current revealed some curious behaviour. There is some indication that the measurements may in fact be time-dependent. More experiments would be useful in investigate this behaviour further. Measurements of the AC performance of the transistors may be enlightening, particularly if the threshold voltage could be changed.

The HEMT/HFET as described in Chapter 4 would appear to also be an interesting exercise to fabricate. Several groups have already made ZnO HEMT transistors. However, one should keep in mind the reason why HEMTs were developed, and why they work well. In high mobility materials, a FET which has its channel just below a metal-oxide interface, or a Schottky junction can suffer from reduced effective channel mobility. This can be due to the effect of interface traps, or the wave function of the carriers extending into the imperfect oxide or Schottky material. In a high mobility

material, this can substantially affect the device performance. In a HEMT, the channel is moved 'down' into the bulk of the semiconductor material, away from where these dissipative effects occur.

ZnO on the other hand, has a quite low mobility. This low mobility may seriously limit the usefulness of any devices made from ZnO. ZnO devices would therefore probably be developed for application areas where the benefits of other properties of ZnO considerably outweigh the limitation of the low mobility. The small additional improvement in channel mobility that might be gained from moving the channel away from interfaces, would therefore be relatively inconsequential.

One of the properties of ZnO that is frequently mentioned in publications is its radiation resistance [31]. It would appear, however, that all these publications reference one specific study [54]. If a suitable test facility were available, it would be extremely interesting to test both the performance and durability of both the Schottky diodes, and also ZnO MESFET devices to irradiation. This would have considerable bearing on several of the previously mentioned potential high-temperature application areas – e.g. nuclear control and monitoring, and particularly space electronics. Irradiation would also provide useful information as to how well ZnO detectors would survive in high-energy electron or x-ray environments.

Any further development of this technology should be done while keeping in mind any potential application areas. As mentioned previously, the low mobility of ZnO seriously limits its potential application as a 'mainstream' transistor. These potential niche application areas should therefore be focussed around the specific beneficial properties of ZnO. Some possible thermal and radiation resistance markets have already been suggested. The other obvious properties are the optical ones – transparency and the high exciton binding energy.

Although the current gate deposition uses a non-transparent metal capping layer, it may be feasible to make the entire transistor transparent. The AgO is moderately transparent, and adequate control of the deposition process may be able to make it fully so. If a transparent conducting overlayer such as indium-tin oxide (ITO) could be used instead of the current metal, the entire device could be made an example of 'transparent electronics'.

MBE grown ZnO could never compete economically in the consumer display market, due to the cost of both the equipment and also the necessary substrate materials. There are however many high value potential niche application areas where using devices such as MESFETs made from ZnO could substantially improve upon the capabilities of currently available parts. Examples that utilise the potential high temperature or radiation resistance properties have been discussed. If progress is made on developing optoelectronic devices based on ZnO, the potential for integrating these devices with on-chip electronics would significantly extend the potential market.

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