Analysis and design of class-B dual fed distributed power amplifiers

K.W. Eccleston and O. Kyaw

Abstract: The analysis of, and derivation of design equations for, a class-B balanced single-ended dual-fed distributed amplifier is presented. This approach allows efficient combining of FET output power without multi-way power combiners, has a good port match, and is easy to design as the gate and drain transmission lines are uniform. The design method ensures that all FETs are optimally used and the efficiency is comparable to that of a conventional single-transistor class-B power amplifier using the same FET type. The design method was applied to a class-B four-FET balanced single-ended dual-fed distributed amplifier designed to operate at 1.8 GHz. Large-signal measurements revealed 8% downward shift of the centre frequency. The measured output power and drain efficiency was consistent with the simulations. The efficiency of the amplifier was comparable to a conventional single-transistor class-B power amplifier using the same type of FET.

1 Introduction

Owing to the limited output power of microwave transistors, it is necessary to combine several transistors to obtain higher output powers. Parallel power combining is often used because of its robustness and relative ease of implementation [1]. FET power amplifiers often use corporate N-way power dividers assembled from two-way dividers, since two-way dividers are easy to analyse and design [1], and are amenable to planar circuit technology. However, the length (and hence losses) increases with each tier of two-way dividers added to the structure (to increase N). For on-chip combining of FETs, N is typically limited to around four.

The distributed amplification approach allows one to combine FET output power without using N-way power combiners. However, up to half of the FET output power in a conventional distributed amplifier (DA) is wasted in idle terminations [2], resulting in a low efficiency (typically less than 20%). Furthermore, interference between the forward and reverse travelling waves on the drain line results in uneven, and hence under-utilised, FETs [2, 3]. Tapering of the drain (output) line can be used to improve efficiency [4] by minimising the reverse waves. Optimisation [5] and non-identical amplifier sections [6] have been proposed to optimally use the transistors, but the efficiency is still limited to around 20%. The resulting DA structures [4–6] are also non-uniform. Furthermore, the conventional DA topology is not directly amenable to class-B operation.

The dual-fed distributed amplifier (DFDA) approach [7, 8] uses a hybrid to feed both ends of the gate line, and another hybrid to combine the waves appearing at the ends of the drain line, thereby increasing the gain. Use of 180° hybrids results in the highest gain [9]. The FET drain voltages and currents are equal when the FETs are spaced 180° at the centre frequency, for the case of 180° hybrids and an even number of FETs [10]. When the drain voltages and currents are equal, the FETs have an equal output power [2] and identical loadlines [10]. When all the FETs operate into identical loadlines, all the FETs can be used to their fullest and optimum extent for the given operating mode [10]. It has been shown that dual-feeding also partially compensates for losses on the gate and drain lines [2].

The DFDA, however, has severely mismatched input and output ports. Under the optimal operating conditions [9, 10], the midpoints of the gate and drain lines of the DFDA may be earthed without disturbing FET operation at the centre frequency [11]. The resulting pair of amplifiers are called single-ended dual-fed distributed amplifiers (SE-DFDA) [12]. A balanced amplifier, with its inherently good port match, can be formed using a pair of identical

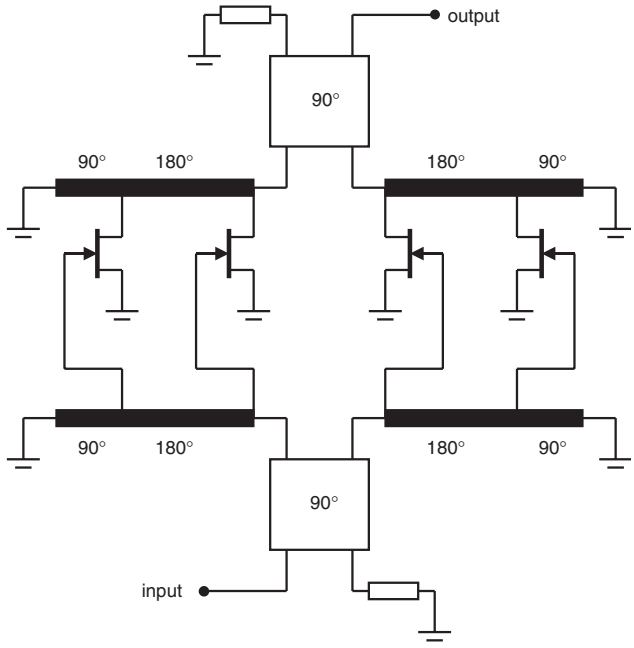

Fig. 1 *A four-FET balanced SE-DFDA*

IEE Proceedings online no. 20040174

doi:10.1049/ip-map:20040174

Paper first received 20th May 2003 and in revised form 18th November 2003. Online publishing date: 20 February 2004

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SE-DFDAs and 90° hybrids [11, 12]. Figure 1 shows a balanced amplifier comprised of two two-FET SE-DFDAs; its uniform topology is evident. The FET bias voltages can easily be fed via the gate and drain line short-circuit terminations [11].

In a previous work [13], we have demonstrated a class-A balanced SE-DFDA with an efficiency similar to a conventional single-transistor class-A amplifier using the same FET type. Simulations have shown that a class-A SE-DFDA can be operated under class-B conditions, thereby improving the efficiency [14]. We now present a detailed analysis of a SE-DFDA operated under class-B conditions including the development of design equations; and demonstrate by experiment, the validity of the design method and simulations. The centre frequency of 1.8 GHz was chosen since it is of interest for application in mobile communications, but can be otherwise arbitrary subject to the assumptions applied in the design method.

2 Theory

2.1 Assumptions and Nomenclature

Fig. 2 shows the circuit diagram of an N-FET SE-DFDA. The short-circuit terminations of both the gate and drain lines give rise to dual-feeding. The gate and drain line characteristic impedances are Z_{oG} and Z_{oD} respectively, and their phase constants are β_G and β_D respectively. Both Z_{oG} and Z_{oD} are pure real since the transmission lines are assumed to be lossless. The physical lengths of each gate and drain line section are indicated beside each section and are related to lengths l_g and l_d respectively. The input generator voltage is E and its Thevenin impedance is Z_{oG} and the load impedance is Z_{oD}.

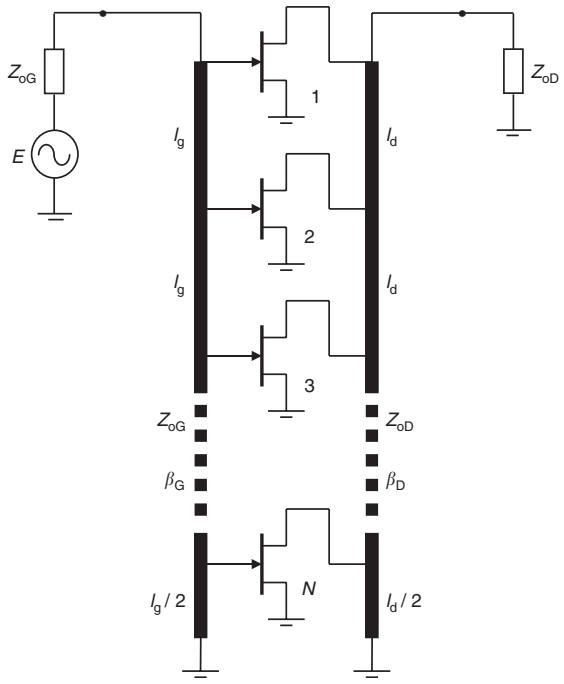

Fig. 2 *SE-DFDA with short-circuit gate and drain line terminations*

Figure 3 shows the idealised drain I/V characteristic and shows the important features to be considered during design:

(i) V_{Dmin} which is the minimum saturation region voltage;
(ii) V_{Dmax} which is the maximum drain voltage;

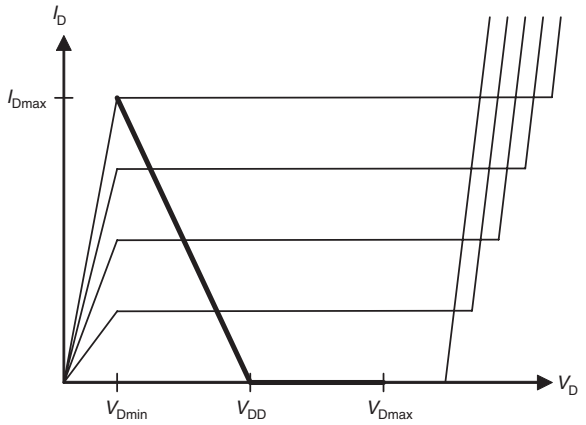

Fig. 3 *Ideal FET output I/V characteristic with optimum class-B (thick line) load trajectory*

(iii) I_{Dmax} which is the maximum drain current;
(iv) the Optimum class-B load trajectory;
(v) the drain bias voltage V_{DD}.

In the interest of reliability, and to maintain an adequate safety margin, V_{Dmax} needs to be lower than that sufficient to cause gate-drain breakdown.

The transfer characteristic of a well designed microwave power FET is nearly linear in the forward saturation region. Hence, we may assume that the drain current is described by:

$$I_D = \begin{cases} 0 & ; \quad V_G < V_T \\ G_m(V_G - V_T) & ; \quad V_T \le V_G \le V_{G\max} \end{cases} \tag{1}$$

where G_m is the large-signal transconductance, V_T is the pinch-off voltage (which is negative for GaAs FETs), and V_{Gmax} is the maximum gate voltage that can be applied before gate conduction. Based on (1), I_{Dmax} is given by:

$$I_{D\max} = G_m(V_{G\max} - V_T) \tag{2}$$

For the sake of argument, we will assume that the FET input and output capacitances are zero (or at least negligible) or alternatively absorbed into the gate and drain lines. In the latter case, the gate and drain lines are therefore artificial transmission lines assembled from microstriplines periodically loaded with shunt capacitances [15].

We will assume that the electrical spacing between each gate is equal to the electrical spacing between each drain and we define a complex variable z, such that:

$$z = \exp(-j\beta_G l_g) = \exp(-j\beta_D l_d) \tag{3}$$

Equation (3) is a basic assumption for all distributed amplifiers.

2.2 Wave Analysis

The analysis is similar to that used for the DFDA [10] and will only consider the AC components of voltages and currents. The AC components of the gate and drain voltages, and drain current will be distinguished by the use of lower case subscripts (V_g, V_d and I_d respectively). The drain current of the kth FET is given by:

$$I_{d_k} = G_m V_{g_k} \tag{4}$$

The gate voltage of the kth FET consists of two component waves, one direct from the generator, and another reflected from the gate line short-circuit termination:

$$V_{g_k} = \frac{E}{2}(1 - z^{2(N-k)+1})z^{k-1} \tag{5}$$

Hence, the drain current of the kth FET will be:

$$I_{d_k} = \frac{EG_m}{2}\left(1 - z^{2(N-k)+1}\right)z^{k-1} \quad (6)$$

The current from each drain current source splits equally causing two voltage waves, one of which travels directly towards the load, whereas the other travels to the load via the short-circuit termination. The kth drain voltage is not solely due to the kth FET drain current, but has contributions from all the FET drain currents and also from reflections from the drain line short-circuit termination:

$$V_{d_k} = -\frac{Z_{oD}}{2}(\cdots + zI_{d_k} + I_{d_k} + zI_{d_{k-1}} + \cdots) + \frac{Z_{oD}}{2}(\cdots + zI_{d_{k-1}} + I_{d_k} + z^{-1}I_{d_{k+1}}\cdots)z^{2(N-k)+1} \quad (7)$$

For odd integer multiples of 180° electrical spacing between the FETs, $z = -1$, and for even integer multiples, $z = 1$. We find V_{g_k} equals E and zero for $z = -1$ and 1 respectively, hence, we only need to consider the case of $z = -1$. $I_{d_k}(z = -1)$ equals G_mE for k odd, and $-G_mE$ for k even, and $V_{d_k}(z = -1)$ equals $-NG_mEZ_{oD}$ for k odd, and NG_mEZ_{oD} for k even. Importantly, for $z = -1$, all FET drain voltage and drain current magnitudes are identical, and hence they all operate into equal loadline resistances of NZ_{oD}. i.e.:

$$V_{d_k}(z = -1) = -NZ_{oD}I_{d_k}(z = -1) \quad (8)$$

2.3 Class-B Operation

For class-B operation, the gate bias voltage is set to V_T so that the FET conducts for half a cycle, and hence the drain current is a half-wave rectified waveform that essentially contains DC, fundamental and even harmonic components. The drain needs to be terminated so that the drain voltage only contains DC and fundamental components, and requires short-circuiting of drain current harmonics. The SE-DFDA topology of Fig. 1, ensures that this is the case for all FETs, without the need for additional resonators [14]. Although the odd harmonics are not short-circuited, they are relatively low for microwave power FETs under class-B operation.

When the input signal level is set so that the peak drain current of each FET is I_{Dmax}, the DC and fundamental components of each FET drain current are I_{Dmax}/π and $I_{Dmax}/2$ respectively. The total power supply current under this condition is therefore NI_{Dmax}/π. From (8), the fundamental component of the drain voltage of each FET is therefore constrained by:

$$|V_{d_k}(z = -1)| = NZ_{oD}\frac{I_{D\,max}}{2} \quad (9)$$

To make full use of the FETs, each drain voltage should vary sinusoidally between the V_{Dmin} and V_{Dmax}. To achieve this, the drain supply voltage V_{DD} is set halfway between V_{Dmin} and V_{Dmax} :

$$V_{DD} = \frac{V_{D\,min} + V_{D\,max}}{2} \quad (10)$$

and the maximum fundamental component of the drain voltage of each FET is:

$$|V_{d_k}(z = -1)| = \frac{V_{D\,max} - V_{D\,min}}{2} \quad (11)$$

Equating (11) and (9) leads to the optimum load impedance, and hence the optimum drain line characteristic impedance:

$$Z_{oD_{opt}} = \frac{V_{D\,max} - V_{D\,min}}{I_{D\,max}N} \quad (12)$$

This is in fact the same optimum drain line characteristic impedance as for class-A operation [11].

From Fig. 2 the load voltage is $V_{d_1}(z = -1)$, which has a maximum value given by (11), and by use of (12), the load power is:

$$P_L = \frac{N}{8}I_{D\,max}(V_{D\,max} - V_{D\,min}) \quad (13)$$

It is easy to show that the sum of the FET output powers is equal to P_L given by (13), and means a 100% combining efficiency at the centre frequency.

Using (10) and noting that the total supply current is NI_{Dmax}/π, the power drawn from the supply is:

$$P_{DC} = \frac{N}{2\pi}I_{D\,max} + (V_{D\,min} + V_{D\,max}) \quad (14)$$

From (13) and (14), the drain DC conversion efficiency is:

$$\eta_{DC} = \frac{\pi}{4}\left(\frac{1 - (V_{D\,min}/V_{D\,max})}{1 + (V_{D\,min}/V_{d\,max})}\right) \quad (15)$$

From (15), we see that the drain efficiency is equal to that of a conventional class-B power amplifier using the same transistors. Clearly, if V_{Dmax} is significantly higher than V_{Dmin}, then the efficiency will approach that of the ideal class-B amplifier value of $\pi/4$. It can be shown that in the case of class-A amplification, a factor of 0.5 would replace the factor of $\pi/4$ in (15).

3 Simulation and Experiment

A balanced amplifier, employing two two-FET SE-DFDAs, with a centre frequency of 1.8 GHz, that uses Fujitsu FLK012WF packaged power GaAs FETs, was considered. Based on the data sheets [16], V_{Gmax}, V_{Dmin}, V_T and I_{Dmax} were found to be 0, 1 and −2 V and 60 mA respectively, whereas V_{Dmax} was conservatively chosen to be 10 V [13]. For circuit simulation, a Statz-Raytheon large-signal FET model was fitted to data sheet S-parameters and I/V characteristics [16].

Using (12), the optimum value of Z_{oD} is 75 Ω and from (10) the optimum drain bias voltage is 5.5 V. The value of Z_{oG} was chosen to be 30 Ω and the coupling of the SE-DFDAs to the hybrids (branch-line couplers) is described in [13]. Thus, the class-B balanced SE-DFDA is identical to the class-A version [13] apart from a change in the gate bias voltage.

Extensive large-signal harmonic-balance simulations at 1.8 GHz have shown that the efficiency is as good as a single-transistor class-B microwave amplifier (using the same transistor type) and clearly much better than a conventional DA [14]. Simulations have also shown that the load trajectories for all FETs are identical at 1.8 GHz and remain nearly identical over a bandwidth of more than 200 MHz [14]. Figure 4 shows the simulated voltage and current waveforms at the internal drain current source of each FET at 1.8 GHz, when the amplifier is driven at its 1 dB gain compression point (GCP). Figure 4 demonstrates that all FETs operate identically and consistent with class-B operation under full drive. The distortion observed in Fig. 4 arises as the amplifier is operated at its 1 dB GCP, but the output voltage (Fig. 5) is relatively free of distortion.

The amplifier was fabricated on a 31 mil Duroid™ substrate ($\varepsilon_r = 2.2$) which was originally designed for class-A operation [13]. The small-signal frequency responses for the gain and the input and output reflection coefficients

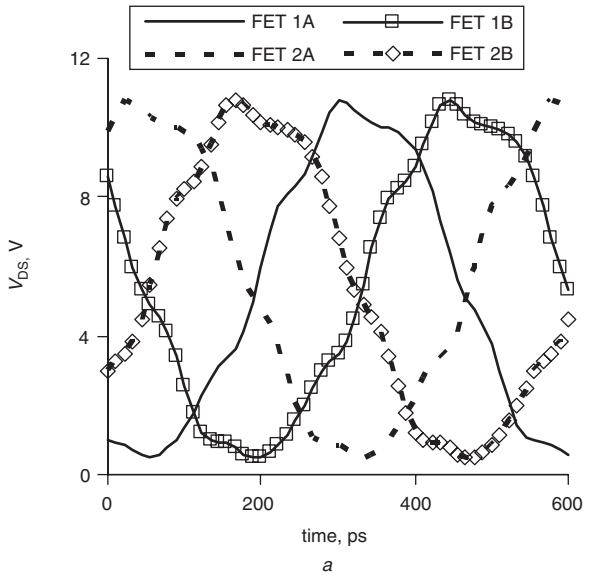

Fig. 4 *Simulated waveforms at 1.8 GHz at the 1 dB GCP*
a FET internal drain-source voltages
b FET internal drain-source currents

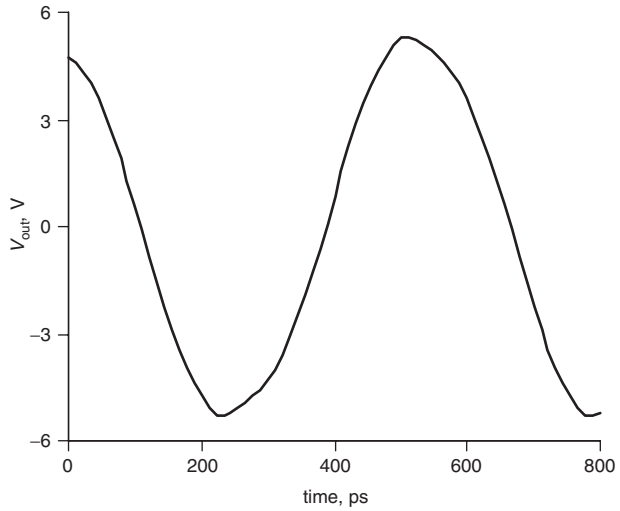

Fig. 5 *Simulated output voltage waveform at 1.8 GHz at the 1 dB GCP*

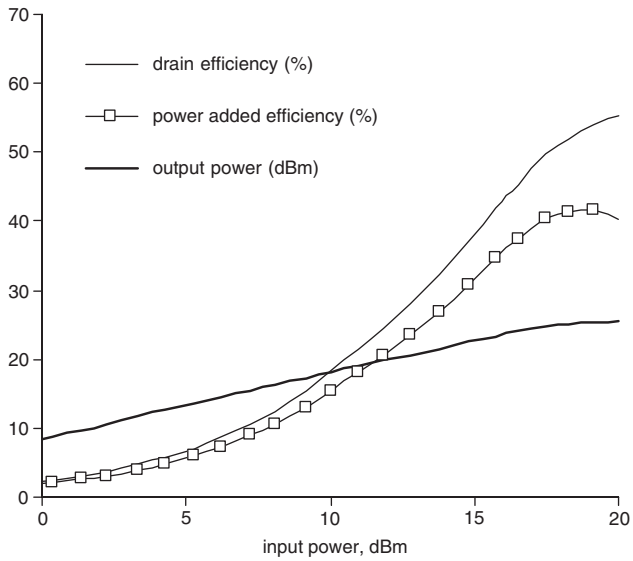

Fig. 6 *Measured output power and efficiency at 1.65 GHz*

were measured under class-A conditions, as the FET is cut-off under class-B bias. The small-signal gain response shows a 6% downward shift of the centre frequency, but otherwise good input and output match over a broad range of frequencies [13]. The output power and efficiency were measured at a number of frequencies under class-B operating conditions, and the performance was found to reach its optimum at 1.65 GHz (as was the case under class-A conditions [13]). Figure 6 shows the measured output power and efficiency as a function of the input power at 1.65 GHz, which compares well with the simulations at 1.8 GHz [14].

Table 1 summarises the amplifier large-signal performance at the 1 dB gain compression point at the centre

Table 1: Large-signal performance at the 1 dB gain compression point

	Class-B			Class-A [13]
	Theoretical* at 1.8 GHz	Simulated at 1.8 GHz	Measured at 1.65 GHz	Measured at 1.65 GHz
Output power, dBm	24.3	24.8	24.7	24.8
Drain efficiency, %	64	61	50	37
Power added efficiency, %	–	50	40	32
Operating power gain, dB	–	7.3	7.3	9.3

*Under full class-B drive.

frequency, and compares it with the measured performance under class-A conditions. Clearly the amplifier operates as expected (aside from the shift in the centre frequency) within the limitations of modelling and experimental errors, and it operates more efficiently than the same amplifier under class-A operating conditions. The ratio of the measured class-B to class-A efficiencies is 1.35 which is consistent with the theoretical ratio of $\pi/2$.

Both simulations and measurements were able to establish that a good output power and efficiency performance is possible over a frequency range of at least 100 MHz, which is sufficient for mobile communications applications.

4 Discussion

We have demonstrated the viability of the proposed class-B SE-DFDA approach for combining the output power of several transistors.

Further investigations were performed to establish the cause of the downward shift of the centre frequency. Circuit simulations suggest that an extra 0.3 pF shunt capacitance is present at each port of each FET. This level of capacitance is too large to be explained by FET modelling error alone, and therefore indicates that the behaviour of the microstripline-FET junction would require 3-D field simulations to account for the interaction of the FET package with the fields at the microstripline-FET junction (which were 'V' shaped).

The circuit simulator used in this work uses a constant series RC network in parallel with the nonlinear drain current source to model the dispersive drain-source behaviour [17]. Although this model is suitable for class-A amplifier simulation, it leads to significant under-estimation of efficiency and load power in class-B and class-C amplifiers [18]. Therefore, during the simulations we did not use the dispersion model. A more accurate dispersion model valid for both conducting and non-conducting halves of the cycle may lead to improved accuracy of efficiency prediction.

It is clear that long transmission lines are required. Artificial transmission lines can be used to replace the microstriplines resulting in a more compact circuit [19]. Further preliminary investigations by the authors for high power microwave FETs have shown the advantages of using artificial transmission lines constructed from microstriplines and shunt capacitances in this type of amplifier [15]. Apart from the compactness, FET input and output capacitances were able to be absorbed into the gate and drain lines, thereby improving the bandwidth of the amplifier [15].

5 Conclusions

The analysis of, and derivation of design equations for, a class-B balanced SE-DFDA has been presented. This approach allows the efficient combining of FET output power without multi-way power combiners, has a good port match, and is easy to design as the gate and drain transmission lines are uniform. The design method ensures that all FETs are optimally used. The validity of the design method was demonstrated by experimental results obtained on a prototype designed for operation at 1.8 GHz. The measured centre frequency was 1.65 GHz and this shift is due to parasitic reactances not accounted for in the circuit simulations. The efficiency is comparable to a conventional single-transistor class-B power amplifier using the same type of transistors and it is better than the same amplifier operated under class-A conditions, and is clearly better than a conventional distributed amplifier.

6 Acknowledgments

The authors gratefully thank Abdul Jalil bin Din, S.C. Lee, H.K. Seah, C.H. Sing, and T.C. Teo for their assistance during the fabrication and testing of the amplifier.

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