

even though the design is formally ECL, the schematic diagram in Fig. 1 clearly shows double emitter followers in the feedback path. Using double emitter followers in a -3.6 V design became possible only due to the unusual nature of the dynamic design, where signals generated by the upper differential pair (they could be called 'data') are fed back into a lower differential pair (where 'clock' is normally applied).

Conclusion: We have designed and tested a 100 GHz dynamic frequency divider in a 207 GHz $f_T/285$ GHz f_{MAX} 0.12 μm SiGe bipolar technology. To our knowledge, this is the highest number ever reported for any transistor-based divider. We also report a 62 GHz, -3.8 V static ECL divider, designed in the same 0.12 μm SiGe bipolar technology. Compared to the previous generation 120 GHz $f_T/100$ GHz f_{MAX} 0.18 μm SiGe BiCMOS technology, this device shows approximately a $2\times$ increase in performance. Comparing static divider data for both technologies we expect that 0.12 μm SiGe static divider performance will benefit significantly from using a double emitter follower E^2CL circuit topology.

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References

- 1 TSUNASHIMA, S., NAKAJIMA, H., SANO, E., IDA, M., KURISHIMA, K., WATANABE, N., ENOKI, T., and SUGAHARA, H.: '90 GHz operation of a novel dynamic frequency divider using InP/InGaAs HBTs'. Indium Phosphide and Related Materials Conf., 2002, pp. 43–46
- 2 WASHIO, K., OHUE, E., ODA, K., HAYAMI, R., TANABE, M., SHIMAMOTO, H., HARADA, T., and KONDO, M.: '82 GHz dynamic frequency divider in 5.5 ps ECL SiGe HBTs', *ISSCC Dig. Tech. Pap.-IEEE Int. Solid-State Circuits Conf.*, 2000, pp. 210–211
- 3 MATHEW, T., KIM, H., JAGANNATHAN, S., SCOTT, D., KRISHNAN, S., WEI, Y., URTEAGA, M., LONG, S., and RODWELL, M.: '75 GHz ECL static frequency divider using InAlAs/InGaAs HBTs', *Electron. Lett.*, 2001, **37**, pp. 667–668
- 4 WURZER, M., BOCK, J., KNAPP, H., AUFINGER, K., and MEISTER, T.: '71.8 GHz static frequency divider in a SiGe bipolar technology'. Proc. IEEE Bipolar/BiCMOS Circuits and Technology Mtg., Monterey, CA, USA, 2002, pp. 216–219
- 5 JAGANNATHAN, B., KHATER, M., PAGETTE, F., RIEH, J.-S., ANGELL, D., CHEN, H., FLORKEY, J., GOLAN, F., GREENBERG, D.R., GROVES, R., JENG, S., JOHNSON, J., MENGISTU, E., SCHONENBERG, K., SCHNABEL, C., SMITH, P., STRICKER, A., AHLGREN, D., and FREEMAN, G.: 'Self-aligned site NPN transistors with 285 GHz f_{sub} MAX/ and 207 GHz f_{sub} T/ in a manufacturable technology', *IEEE Electron Device Lett.*, 2002, **23**, pp. 258–260
- 6 KNAPP, H., MEISTER, T.F., WURZER, M., ZOSCHG, D., AUFINGER, K., and TREITLINGER, L.: 'A 79 GHz dynamic frequency divider in SiGe bipolar technology', *Dig. Tech. Pap.-IEEE Int. Solid-State Circuits Conf.*, 2000, pp. 208–209

Class-F dual-fed distributed amplifier

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The single-ended dual-fed distributed amplifier allows efficient combining of the output power of several FETs without multi-way power combiners. It is shown that this configuration can be operated under class-F operating conditions, thereby allowing high efficiencies.

Introduction: The conventional distributed amplifier offers broad bandwidth but has low efficiency since half of the FET output power is wasted in an idle termination, and only one of the FETs is fully utilised. Further, such amplifiers are normally operated in the class-A mode which has an inherently low efficiency. The single-ended dual-fed distributed amplifier (SE-DFDA) [1] allows all the FET output power to be utilised. The work of Moazzam and Aitchison [1] only considered single-FET SE-DFDAs. The SE-DFDA concept can be extended to N FETs, and if the FETs are spaced 180° , all FETs have identical loadlines, which can be chosen optimally [2]. The SE-DFDA therefore allows efficient power combining of FET output power without using bulky multi-way power combiners [2]. In the previous work on the power SE-DFDA, class-A [2] and class-B [3] operation was demonstrated. A class-F amplifier [4] can offer both high output power and high efficiency (up to 100% for ideal transistors). To date, the developments reported in the literature pertaining to class-F amplifiers have essentially only considered single transistor amplifiers. In this Letter we propose a class-F single-ended dual-fed distributed amplifier (SE-DFDA) configuration that combines several FETs. This proposal therefore partners the SE-DFDA power combining approach with the high efficiency of class-F operation.

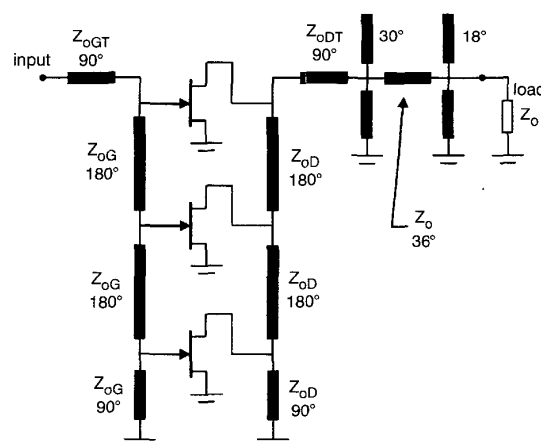


Fig. 1 Circuit diagram of 3-FET class-F single-ended dual-fed distributed amplifier (electrical lengths specified at fundamental frequency)

Class-F dual-fed distributed amplifier: In class-F operation, the input drive is established so that the drain current is a half-sinusoid waveform similar to that in class-B operation, and the drain voltage is a square waveform. High efficiency results as the drain voltage is low when the drain is conducting and vice-versa. To achieve a square drain voltage waveform, the load presented to the drain is resistive for the fundamental, short-circuit for the even harmonics and open-circuit for the odd harmonics. This can be achieved by coupling a parallel resonant load to the FET drain with a quarter-wave transformer. The resonator also suppresses harmonics at the output. For a square waveform to exist, odd harmonics must be present in the drain current and is achieved by appropriate choice of the FET gate bias voltage and input power so that the drain current waveform is not a pure half-sinusoid [4].

Fig. 1 shows the circuit topology of the proposed class-F single-ended dual-fed distributed amplifier and is based on the single-ended dual-fed distributed amplifier [2, 3]. Critical impedances and electrical lengths are indicated in Fig. 1. The dual-feeding of both the gate and drain lines is achieved by the short circuit terminations at the ends of the gate and drain lines farthest from the input and output ports, respectively. These short-circuit terminations allow DC bias voltages to be fed to the FETs and short-circuit the FET drains at even harmonics. The load for the SE-DFDA drain line consists of a quarter-wave transformer that is terminated by the external resistive load (Z_o) and a series of stubs, where Z_o is typically $50\ \Omega$. The open-circuit stubs short-circuit the load at the third and fifth harmonics and the adjacent short-circuit stubs parallel resonate the open-circuit stubs at the fundamental frequency. Therefore, the quarter-wave transformer is

terminated with Z_o at the fundamental, and short-circuited at the third and fifth harmonics. More stub resonators can be added to handle higher-order odd harmonics but the FET typically suppresses these.

For maximum output power and efficiency, we establish drain current and voltage waveforms so that the FET saturation region is fully utilised and means that the drain current varies between 0 and I_{Dmax} , and the drain voltage varies between V_{Dmin} and V_{Dmax} . I_{Dmax} , V_{Dmin} and V_{Dmax} are defined by the FET saturation region and maximum allowable limits (and perhaps the power supply). The drain DC bias is therefore $(V_{Dmin} + V_{Dmax})/2$. Fourier series analysis of the drain current and voltage waveforms for class-F operation indicates that the amplitudes of the fundamental components of drain voltage and current are $2(V_{Dmax} - V_{Dmin})/\pi$ and $I_{Dmax}/2$, respectively, and hence the optimum fundamental load resistance for a FET is equal to $4(V_{Dmax} - V_{Dmin})/(\pi I_{Dmax})$. The quarter-wave transformer characteristic impedance (Z_{oDT}) is chosen so that the resistive termination presented to the drain line is equal to the characteristic impedance of the drain line (Z_{oD}), and hence Z_{oDT} is $\sqrt{Z_{oD}Z_o}$. By considering both forward and reverse travelling waves on the drain line, it can be shown that the resistive load that each FET sees at the fundamental is NZ_{oD} where N is the number of FETs [2]. Thus the optimum value of drain line characteristic impedance is:

$$Z_{oD-opt} = \frac{4}{\pi} \left(\frac{V_{Dmax} - V_{Dmin}}{NI_{Dmax}} \right) \quad (1)$$

Design and simulation: To demonstrate the proposed amplifier and design method, a 2-FET class-F SE-DFDA was designed for operation at 1.8 GHz. The FET considered was a Fujitsu FLK012XP GaAs FET chip. Based on the FET i/v characteristics and recommended safety limits, V_{Dmin} , V_{Dmax} and I_{Dmax} are 1 V, 10 V and 60 mA, respectively. Using (1), the optimum drain line characteristic impedance is 95 Ω , and hence for a 50 Ω load, Z_{oDT} is 69 Ω . The optimum drain bias voltage is 5.5 V and the gate bias voltage was set to -1.7 V so that the drain current waveform is essentially a half-sinusoid with some odd harmonic content. The gate line characteristic impedance (Z_{oG}) was 30 Ω so that the effects of FET input loading are minimal at 1.8 GHz and yet the gate line width is reasonable. The input quarter-wave transformer characteristic impedance (Z_{oGT}) was 39 Ω to couple the 50 Ω generator to the gate line.

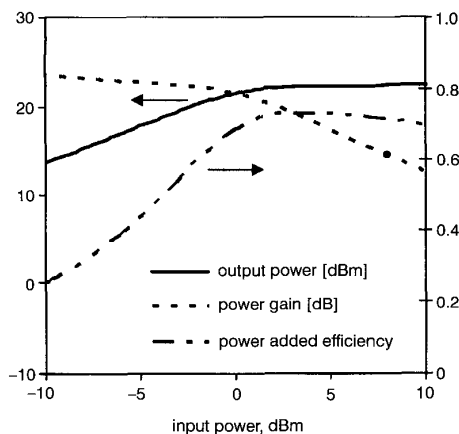


Fig. 2 Simulated output power, gain and efficiency at 1.8 GHz of 2-FET class-F SE-DFDA

Under the condition of an input excitation to fully utilise the FETs according to the above mentioned limits, and the amplitudes of the fundamental components of drain voltage and current are 5.73 V and 0.03 mA, and the DC drain current is 19 mA. Therefore the output power and drain DC efficiency under this condition are 22.4 dBm and 82%, respectively.

A harmonic balance simulation (with eight harmonics) was performed, with the FETs represented by a Statz-Ratheon large-signal model. Fig. 2 shows the simulated large-signal transfer function, power gain and power added efficiency at 1.8 GHz. With an input frequency and power of 1.8 GHz and 0 dBm, respectively, the simulated drain voltage

and current waveforms are consistent with the waveforms assumed in the design calculations, and the FET load lines are identical. Under this condition, the simulations reveal that the output power is 21.5 dBm and the drain DC efficiency is 69%. The output spectrum shows that the harmonics are suppressed by the output stub resonators. The simulation results are therefore consistent with theoretical expectations.

Conclusion: We have demonstrated the viability of a class-F single-ended dual-fed distributed amplifier. The single-ended dual-fed distributed amplifier configuration allows the output powers of several FETs to be combined without multi-way power combiners and dividers. Class-F operation offers both maximum output power from the FETs as well as high efficiency. Combining two class-F SE-DFDAs with hybrids, to form a balanced amplifier, will result in good port match. Artificial transmission lines or photonic-bandgap structures can be used to reduce the physical lengths of the transmission lines used in this amplifier.

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References

- MOAZZAM, M.R., and AITCHISON, C.S.: 'A high gain dual-fed single stage distributed amplifier', *IEEE MTT-S Int. Microw. Symp. Dig.*, 1994, pp. 1409-1412
- ECCLESTON, K.W., and KYAW, O.: 'FET power combining using the balanced single-ended dual-fed distributed amplifier approach', *Microw. Opt. Technol. Lett.*, 2002, **35**, (1), pp. 42-45
- KYAW, O., and ECCLESTON, K.W.: 'Class-B balanced single-ended dual-fed distributed power amplifier'. 3rd Int. Conf. Microwave and Millimeter Wave Technology (ICMMT2002), Beijing, People's Republic of China, August 2002, pp. 919-922
- COLANTONIO, P., GIANNINI, F., LEUZZI, G., and LIMITI, E.: 'On the class-F power amplifier design', *Int. J. RF Microw. Comput. Aided Eng.*, 1999, **9**, (2), pp. 129-149

Analysis of scaling soft information on low density parity check code

Jun Heo

Density evolution is used to analyse the scaling of soft information in the iterative decoding of low density parity check codes. Based on the min-sum algorithm and Gaussian approximation, the thresholds are evaluated with various scaling factors. The optimal scaling factor is found by density evolution and the expected scaling gain matches well with the achievable scaling gain from simulation results.

Introduction: Recently developed density evolution has achieved the analytic capacity of low density parity check (LDPC) codes. In [1], the density evolution technique was recursively used to track the density of extrinsic message between the variable nodes and check nodes of LDPC codes. A simplified version of density evolution was introduced with a Gaussian approximation in [2]. The Gaussian approximation was based on the fact that the extrinsic information can be well approximated as a Gaussian random variable as the number of iterations increases. While [1] and [2] were based on the sum-product algorithm, the density evolution technique based on the min-sum algorithm was derived in [3, 4].

In the literature, it was experimentally shown that the scaling of soft information results in better performance, which was viewed as either slowing down the convergence of iterative decoding or reducing the overestimation error when the sum-product algorithm is replaced with the min-sum algorithm [5]. For both approaches, however, it is not clear when scaling results in a significant performance gain and it is quite heuristic to determine the optimal scaling factor.