Implementation of a Microstrip Square Planar N-Way Metamaterial Power Divider

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***Abstract*—This paper describes a compact square-shaped 20-way metamaterial power divider implemented in microstrip technology and lumped capacitors and inductors. The divider comprises 12 square tiles exhibiting left-handed behavior and 13 square tiles exhibiting right-handed behavior arranged in a checkerboard tessellation (or mosaic). The divider relies upon the infinite wavelength phenomena in two dimensions and this requires the left-handed tiles have an insertion phase between any two of its sides equal to, but with opposite sign, of that of the right-handed tiles. To achieve tessellation, both tile types must be the same size. The design method is based upon an analytic formulation, and was applied to the realization of a 20-way power divider operating at 1 GHz that uses surface-mount lumped components. The resulting divider was 50 mm by 50 mm. Over a 10% bandwidth, the measured insertion loss was less than 1.3 dB, the measured couplings track within ± 1 dB and $\pm 6^\circ$, and the measured input port return loss and isolation was greater than 20 dB. This level of isolation was achieved without isolation resistors. Equal in-phase power division to output ports on the square-shaped periphery allows compact integration with other planar circuit modules in a combined amplifier. The design method can be extended to N-way power division where N is an odd integer multiple of 4.**

***Index Terms*—Infinite wavelength, left-handed materials, metamaterials, microstrip, microwave circuits, negative refractive index, power combining, power dividers.**

I. Introduction

THE N-way power divider is an important component in an parallel combined microwave power amplifier [1]. Two such dividers are required: one to evenly distribute the input signal to N identical power amplifier modules, and another to combine the N amplified output signals. To ensure maximum combining efficiency using a symmetric power divider, the N signals to be combined should have equal magnitude and phase [2].

Microstrip power dividers are cheap to manufacture and permit integration with amplifier modules. However, many microstrip power dividers are either fork, circular or sector shaped [1], and means in-phase output ports are located on a curved (arc or circular) periphery. This requires that the amplifier modules are either located on a circle [3], or if located in a straight line, requires equal length, but nonuniformly meandered interconnecting transmission lines [4], or similar to using waveguide radial combiners [5], a separate printed circuit board (PCB) or microwave integrated circuit is required for each amplifier.

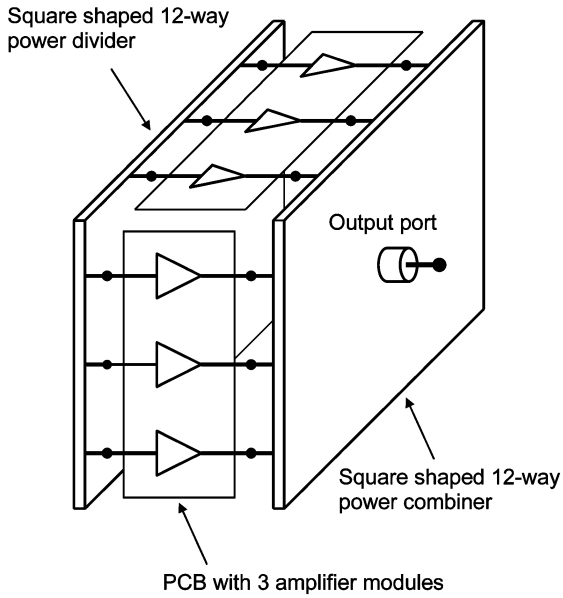

Fig. 1. Application of square-shaped 12-way power dividers in a parallel combined power amplifier.

Typical amplifier modules are rectangular shaped. To achieve compact integration with a uniform layout, it is desirable that the divider output ports are either located on straight line [6] or in groups of straight lines [7]. A square-shaped power divider has four groups of output ports. With a square-shaped divider, amplifier modules can be grouped on four PCBs that can be conveniently interconnected to the dividers as shown in Fig. 1. A square-shaped power divider is expected to result in minimal PCB material wastage compared with a radial power divider where about 21% of material is wasted when cut from a square sheet of PCB material.

The advent of practical microwave metamaterials has given rise to interesting wave phenomena and new options for circuit realization [8]. One phenomenon that can be obtained from metamaterials is propagation with infinite wavelength, where the waves travel across a compact finite sized structure with zero phase shift [9]. Infinite wavelength in 1-D has been demonstrated by others [9]–[11], and exploited in compact 0° phase shifters [10] and 1-D power dividers [9], [11]. Initial investigations by the first author have shown that the infinite wavelength phenomenon can be obtained in 2-D [12]. It is the infinite wavelength phenomenon in 2-D that permits a square-shaped power divider [7].

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The previous investigations by the first author [7], [12] proposed a planar metamaterial structure and its application, but did not consider physical realization other than to suggest applying the transmission line approach [13]–[15] to realize left-handed metamaterials. It is, therefore, the purpose of this study to develop a design method for realising square-shaped N-way power dividers [7] that can be fabricated in microstrip. The square-shaped divider structure is based upon a checkerboard tessellation (or mosaic) of both right- and left-handed square-shaped four-port units cells. Thus, not only do the unit cells need to display a certain electrical behavior, they need to be the same physical size to permit tessellation.

Section II describes the important principles of the tessellated metamaterial structure and compares its response to square-shaped planar structures employing only conventional materials. Section III describes the design procedure to design geometrically and electrically compatible left- and right-handed unit cells for the tessellated metamaterial structure. Section IV describes the application of the design method to a 20-way power divider operating at 1 GHz. Section V shows the simulation and measurement results for the realized divider. Finally, Section VI gives the conclusions. Throughout this study, circuit simulations were performed using Applied Wave Research (AWR) Microwave Office.[1]

II. Tessellated Metamaterial Structure

A complete treatment of left-handed metamaterials can be obtained elsewhere [8]. In this study, we will confine ourselves to left-handed metamaterials realized using the transmission line approach [13]–[15], as this has been shown to yield useful devices in microstrip and offers wide bandwidth [8]. Suffice to say, we will define a right-handed transmission line as one whose insertion phase is negative (or phase lag), and a left-handed transmission line as one whose insertion phase is positive (phase lead) [8]. Right-handed transmission lines are simply conventional transmission lines (such as microstrip) that use conventional dielectrics. Left-handed transmission lines, on the other hand, must be artificially realized [13]–[15]. Consistent with material concepts, the size of metamaterial constituent elements should be small compared to wavelength.

Fig. 2 shows a diagram of a 5 by 5 version of the structure exhibiting infinite wavelength phenomena in 2-D [12]. The power divider comprises 12 square left-handed and 13 square right-handed tiles, denoted L and R, respectively, arranged in a checkerboard tessellation (or mosaic). There are 21 ports: with port 0, the divider input port, connected to a central point within the central tile; and ports 1–20, the divider output ports, along the periphery.

All tiles have one port located on each side. The central tile has a fifth port connected to a central point within it. Each tile is constructed so that they all have the same characteristic impedance [14] of Z_o, and the insertion phase between any pair of side ports is 2φ in the case of the L tiles, and -2φ in the case of the R tiles, where φ is positive valued. For the central tile, the insertion phase between its fifth port and any of its side ports is $-\varphi$. A small value of φ ensures that the tiles are small and wide bandwidth is achieved. The divider output ports (ports 1–20) are matched terminated with an impedance of Z_o [12]. By symmetry, $S_{1,0}$, $S_{5,0}$, $S_{6,0}$, $S_{10,0}$, $S_{11,0}$, $S_{15,0}$, $S_{16,0}$, and $S_{20,0}$ are all equal; $S_{2,0}$, $S_{4,0}$, $S_{7,0}$, $S_{9,0}$, $S_{12,0}$, $S_{14,0}$, $S_{17,0}$, and $S_{19,0}$ are all equal; and $S_{3,0}$, $S_{8,0}$, $S_{13,0}$, and $S_{18,0}$ are all equal. Therefore, there are only three unique divider couplings: $S_{1,0}$, $S_{2,0}$, or $S_{3,0}$.

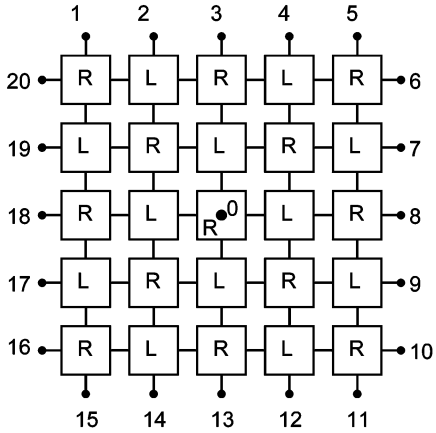

Fig. 2. 5 by 5 tessellated metamaterial power divider.

At the center frequency, the phases of $S_{1,0}$ and $S_{3,0}$ are equal to $-\varphi$, and the phase of $S_{2,0}$ is φ [12]. When the input port is excited, the central node voltages of each tile are equal in both amplitude and phase and this means that the amplitude of waves emanating from the output ports will have equal magnitude, and that the input impedance of the input port (port 0) will be $Z_o/20$ [12]. This operational behavior means that the isolation between the output ports is equal to 26 dB at the center frequency. The above concepts can be generalized for an N-way divider, with N being an odd integer multiples of 4: the input impedance of the input port (port 0) will be Z_o/N [12], and the isolation will be $20 \log N$ dB.

Although equal amplitude power division occurs, the phase at each port alternates between $-\varphi$ and φ. To equalize phase, short lines whose characteristic impedance is Z_o can be added at the output ports. If the electrical length of the lines connected to ports 1, 3, 5, 6, 8, 10, 11, 13, 15, 16, 18, and 20 is Θ_1, and Θ_2 for the lines connected to ports 2, 4, 7, 9, 12, 14, 17, and 19, then $\Theta_2 - \Theta_1 = 2\phi$ will achieve phase equalization. It will be shown in Section IV that the lines with electrical length Θ_2 can be meandered so all divider output ports are on a square boundary.

The transmission line realizations for the R and L tiles are shown in Figs. 3 and 4, respectively. The L tiles are implemented as a composite left-handed right-handed structure [13]–[15].

It can be shown [12] that $\varphi = 5.63°$ at 1 GHz and $Z_o = 100\,\Omega$ if: 1) the L tiles have $L_o = 43.7$ nH, $C_o = 4.37$ pF, and its conventional transmission line elements have a characteristic impedance of 100 Ω and an electrical length of 4.8° at 1 GHz and 2) the transmission line elements of the R tiles have a characteristic impedance of 100 Ω, and an electrical length of 5.65° at 1 GHz. The input impedance of the tessellated metamaterial divider at port 0 is equal to 5 Ω when the output ports are terminated with 100 Ω [7].

[1]Microwave Office, version 7.5, Appl. Wave Res., El Segundo, CA. [Online]. Available: http:\\web.awrcorp.com

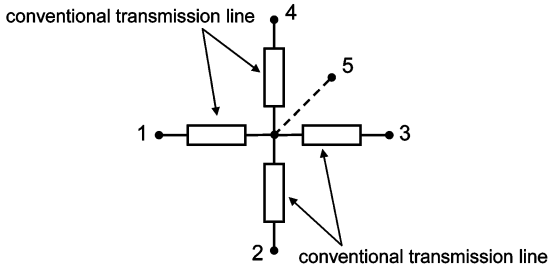

Fig. 3. 2-D circuit to implement the R tiles. Port 5 only exists for the central tile.

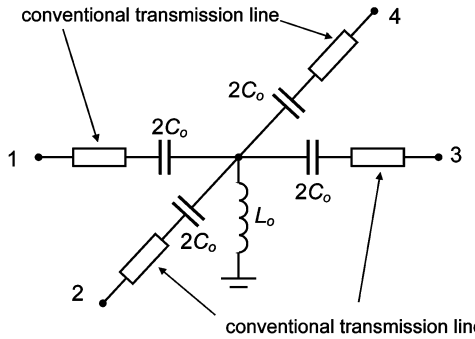

Fig. 4. 2-D composite left-handed right-handed transmission line to implement the L tiles.

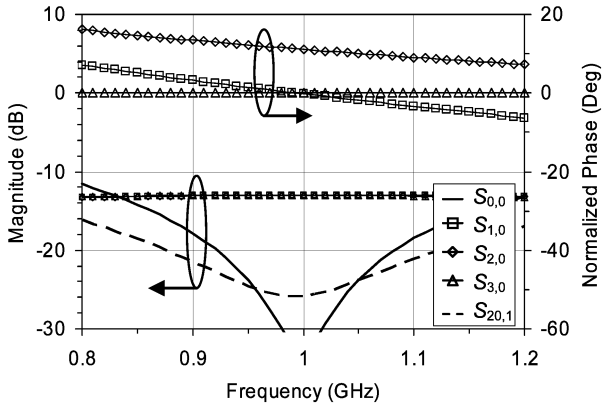

Fig. 5. S-parameters of 5 by 5 tessellated metamaterial structure.

Fig. 5 shows the simulated frequency response of the input reflection coefficient $(S_{0,0})$, couplings ($S_{1,0}$, $S_{2,0}$ or $S_{3,0}$), and one output port coupling $(S_{20,1})$. The S-parameter reference impedance is $5 + j0.95\ \Omega$ for port 0, and $100\ \Omega$ for ports 1–20. The nonzero imaginary part of the port 0 reference impedance stems from residual mismatch between left- and right-handed tiles. The coupling phases are normalized to the phase of $S_{3,0}$. The output ports isolations were all found to be 26 dB at 1 GHz, but $S_{20,1}$ (being equal to $S_{5,6}$, $S_{10,11}$, and $S_{15,16}$) was found to deteriorate the fastest away from the center frequency. At 1 GHz, the divider operates as expected: coupling of -13.1 dB being consistent with a 20-way divider, and phase of $S_{1,0}$ being equal to $S_{3,0}$, but differing from $S_{2,0}$ by 11.3° and an isolation of 26 dB. Over the range of 0.8–1.2 GHz, the coupling magnitudes are nearly identical and flat, and the coupling phase differences are less than 16°. The input return loss, and the isolation exceed 20 dB over a bandwidth of 160 and 240 MHz, respectively.

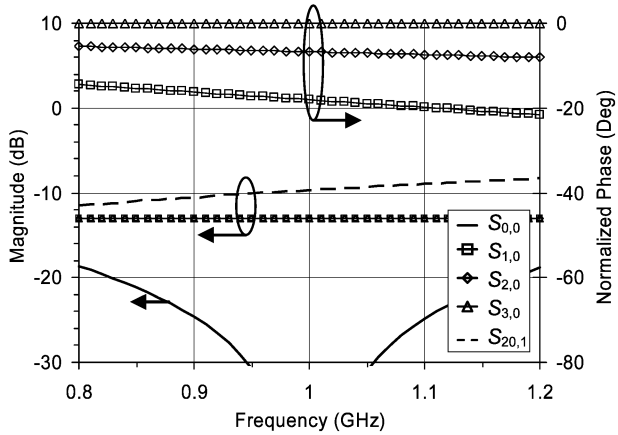

Fig. 6. S-parameters of 5 by 5 array of 11.3° right-handed tiles.

When the extra lines are used to equalize the coupling phases at 1 GHz, it can be shown that the phases will differ by less than 6° over that range of 0.8–1.2 GHz. An *LC* impedance transformer comprising a series capacitor (11.3 pF) and a shunt inductance (2.66 nH) can match the divider input to a 50-Ω generator. Other simulations show that such a matching circuit has minimal impact on the coupling and isolation bandwidth, but the input port return-loss 20-dB bandwidth reduces to 50 MHz.

As the right-handed tile sizes are small, one may ask whether one could achieve acceptable performance from a square-shaped divider constructed entirely from the right-handed tiles. Fig. 6 shows the simulated frequency response of such a divider whose R tiles have $\varphi = 5.65°$ at 1 GHz. The port 0 reference impedance was $5.5 - j6.1\ \Omega$. Although the input is matched over a wide bandwidth and the coupling magnitudes are identical at -13 dB, the coupling phases differ by 18° at 1 GHz, and up to 22° at 1.2 GHz, and the isolation is only 10 dB at 1 GHz. Although phase equalization lines can be added, the resulting output ports would be more or less on a circular boundary. This comes as no surprise, as this case can be likened to a probe-fed parallel-plate waveguide with right-handed media where cylindrical waves emanate from the probe [12], and also explains the relatively large imaginary part of the input port reference impedance [16].

It is interesting to consider a divider that uses only R tiles with $\varphi = 180°$ making each tile one wavelength at 1 GHz. Although such a divider has good performance at 1 GHz, but the bandwidth is very narrow and the size is now 5λ by 5λ, which is far greater than the proposed tessellated metamaterial structure whose size is only 0.16λ by 0.16λ.

The metamaterial power divider uses lumped components however, and it is important to consider the level of stress they endure. Simulations have shown that all the tile central node voltages are identical [12]. It can be shown that for a given input power P_{in}, the voltage across each inductor is $\sqrt{2P_{\text{in}}Z_o/N}$. The stress on the capacitors varies with position within the structure, but the four capacitors closest to the central tile each carry the highest current being one quarter of the input port current (which is $\sqrt{2P_{\text{in}}N/Z_o}$). With knowledge of the component values, the inductor current and maximum capacitor voltage can be computed.

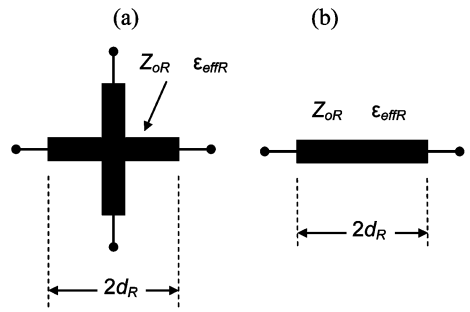

Fig. 7. Microstrip R tile realization. (a) Layout. (b) 1-D equivalent unit cell.

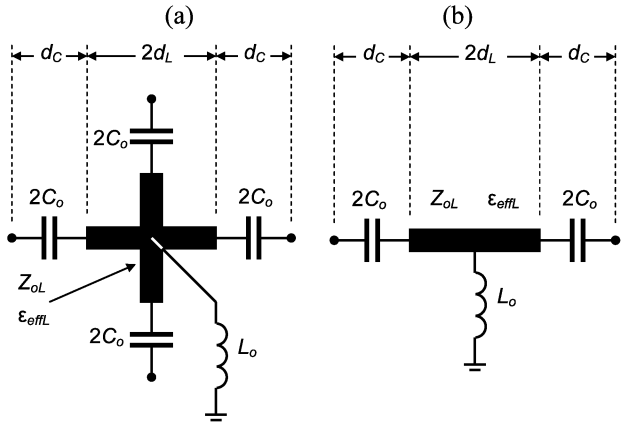

Fig. 8. Microstrip L tile realization. (a) Layout. (b) 1-D equivalent unit cell.

III. Design of the Tessellated Metamaterial

The essential tasks of a design method are to ensure that: 1) each tile has the same physical size; 2) that the L tile has an equal, but opposite insertion phase shift compared to the R tile; and 3) each tile is matched to the same characteristic impedance.

Figs. 7(a) and 8(a) show the physical layout of the R and L tiles, respectively, in microstrip, where it is assumed that both tiles are isotropic and means that their width and height are equal. A notable difference between the layout of Fig. 8(a) and the schematic of Fig. 4 is the capacitors and transmission lines have been transposed. This change permits physical realization in microstrip but has an insignificant effect provided d_L is much smaller than one guide wavelength. The microstrip characteristic impedances and effective dielectric constants of the R and L tiles are denoted Z_{oR}, $\varepsilon_{\mathrm{eff}R}$, Z_{oL}, and $\varepsilon_{\mathrm{eff}L}$, respectively, and are dependent on microstrip width and substrate [17].

The length of the L tile capacitors d_C will contribute to the L tile size. Thus, to achieve identical tile size,

$$d_R = d_C + d_L. \tag{1}$$

A tessellation comprised entirely of either the R tiles [see Fig. 7(a)] or L tiles [see Fig. 8(a)] can be treated as 2-D periodic structures. Similar to [14], one can use 1-D periodic structure analysis [17] to analyze the 2-D structure. If the tessellation of Fig. 2 has a large size, then each L tile is only connected to an R tile and vice versa, and the results of other simulations [12] indicate that the equivalent 1-D unit cells are as depicted in Figs. 7(b) and 8(b). The design method will ignore the parasitic effects of the lumped component and the microstrip cross.

With reference to Fig. 7(b), the insertion phase of the R tiles is

$$\angle S_{21R} = -\frac{2\omega d_R \sqrt{\varepsilon_{\mathrm{eff}R}}}{3\times 10^8} \tag{2}$$

where the reference impedance is Z_{oR}. The $ABCD$ parameters of the L tile equivalent 1-D unit cell [see Fig. 8(b)] are

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 1 & \frac{1}{j2\omega C_o} \\ 0 & 1 \end{bmatrix} \begin{bmatrix} \cos\theta & jZ_{oL}\sin\theta \\ j\frac{\sin\theta}{Z_{oL}} & \cos\theta \end{bmatrix} \begin{bmatrix} 1 & 0 \\ \frac{1}{j\omega L_o} & 1 \end{bmatrix} \times \begin{bmatrix} \cos\theta & jZ_{oL}\sin\theta \\ j\frac{\sin\theta}{Z_{oL}} & \cos\theta \end{bmatrix} \begin{bmatrix} 1 & \frac{1}{j2\omega C_o} \\ 0 & 1 \end{bmatrix} \tag{3}$$

where

$$\theta = \frac{\omega d_L \sqrt{\varepsilon_{\mathrm{eff}L}}}{3\times 10^8}. \tag{4}$$

As the network is reciprocal and symmetrical so the Bloch impedance is [17]

$$Z_{\mathrm{Bloch}} = \sqrt{\frac{B}{C}} \tag{5}$$

and expressions for the S-parameters, S_{11} and S_{21} of the two-port depicted in Fig. 8(b) [17] are as follows:

$$S_{11L} = \frac{\frac{B}{Z_o} - CZ_o}{2A + \frac{B}{Z_o} + CZ_o} \tag{6}$$

$$S_{21L} = \frac{2}{2A + \frac{B}{Z_o} + CZ_o} \tag{7}$$

where Z_o is the port reference impedance.

Clearly from (5) and (6), S_{11} is zero if

$$Z_o = Z_{\mathrm{Bloch}} \tag{8}$$

and the R and L tiles are matched if

$$Z_{oR} = Z_{\mathrm{Bloch}}. \tag{9}$$

In general, the Bloch impedance will be dependent on d_L, and the phase of S_{21} of will be nonlinearly related to d_L. However, if

$$Z_{oL} = \sqrt{\frac{L_o}{C_o}\left(1 - \frac{1}{4\omega^2 L_o C_o}\right)} \tag{10}$$

we find that the sensitivity of the Bloch impedance with respect to d_L is considerably reduced and the phase of S_{21L} is approximately linearly related to d_L. Clearly, the operating frequency needs to be greater than $1/4\pi\sqrt{L_oC_o}$. Using (1) and (2),

$$\angle S_{21R} = -\frac{2\omega\left(d_L + d_C\right)\sqrt{\varepsilon_{\mathrm{eff}R}}}{3\times 10^8}. \tag{11}$$

Having made a choice for L_o and C_o, the design begins by calculating Z_{oL} using (10). As a starting point, it is assumed that $\varepsilon_{\mathrm{eff}R}$ is equal to $\varepsilon_{\mathrm{eff}L}$, which is reasonable in practice assuming Z_{oL} and Z_{oR} are similar. The insertion phases $\angle S_{21L}$, and $-\angle S_{21R}$ can be numerically calculated using (7) and (11),

respectively, and plotted as a function of d_L with the intersection giving d_L. Finally, Z_{oR} is calculated using (9) and d_R using (1).

IV. Realization of a 1-GHz Power Divider

The aim was to develop a 20-way power divider operating at 1 GHz with similar electrical properties to that discussed in Section II and in [7] and [12]. A substrate whose height is 1.575 mm (62 mil) and dielectric constant is 2.22 was chosen so that the width of 100-Ω microstrips would be around 1.4 mm, thereby minimizing conductor losses. American Technical Ceramics (ATC)[2] surface-mount capacitors (600S series) and inductors (0603 series) with a 0603 case style and a 5% tolerance were used. The capacitors have a parasitic series inductance of 0.15 nH and the inductors have a parasitic shunt capacitance of 0.15 pF. The allowance for the capacitor size, d_C, was 1 mm. The inductor of the L tiles is realized by placing the surface-mount inductor upright in a hole drilled through the substrate. This method has been successfully used by others in the low gigahertz frequency range [14].

Several combinations of values of L_o and $2C_o$ were tried from a range of 10, 22, and 43 nH and 4.7 and 10 pF, respectively, and finally $L_o = 43$ nH and $2C_o = 10$ pF were chosen as it yielded a divider that was compact, but could be manufactured. This combination is also similar to that used in previously discussed dividers [7], [12]. At 1 GHz, the Q of the inductors is 49 and the Q of the capacitors is 200.

Microstrip design formulas [17] were used to relate characteristic impedance and effective dielectric constant to the microstrip width and substrate parameters. Using (10), $Z_{oL} = 91.4\ \Omega$, and evaluating (7) and (11) numerically, $\angle S_{21L}$, and $-\angle S_{21R}$ were plotted yielding $d_L = 2.55$ mm, and the insertion phases of the L and R tiles are 11.4° and −11.4°, and hence, $\varphi = 5.7°$ at 1 GHz. From (1), d_R is 3.55 mm, meaning each tile has a size 7.1 mm by 7.1 mm. Using (5), the Bloch impedance is 93.5 Ω at 1 GHz, and hence, from (9), $Z_{oR} = 93.5\ \Omega$.

To achieve in-phase couplings, the extra phase equalizing lines were added with Θ_1 and Θ_2 set to 11.1° and 22.4°, respectively, corresponding to physical lengths of 7 and 14.1 mm, respectively. The later line lengths can easily be meandered to space its ends 7 mm apart. The resulting power divider size is 50 mm × 50 mm. The output port spacing is 7.1 mm, and this would be sufficient to accommodate monolithic microwave integrated circuit (MMIC) power amplifiers, either bonded to a PCB or mounted in surface-mount packaging, when the divider is used in a parallel combined power amplifier (Fig. 1).

Calculations show that microstrip technology rather than the ratings of the lumped components that will limit power handling.

The power divider was manually assembled and Fig. 9(a) shows a close-up view of the fabricated actual metamaterial power divider structure. The input port is probe fed from the center conductor (1.27-mm diameter) of an SMA connector attached to the bottom of the PCB mounting plate.

Fig. 9(b) shows a photograph of the test fixture used to measure the divider performance. Since the divider was measured in a 50-Ω test system, quarter-wave transformers are used to transform the 50-Ω terminations to 93.5 Ω to terminate the divider output ports at 1 GHz. This means that divider output ports are only match terminated at 1 GHz; however, the measurements are not unduly compromised by this due to the high output port isolation.

[2]ATC. [Online]: Available http://www.atceramics.com/

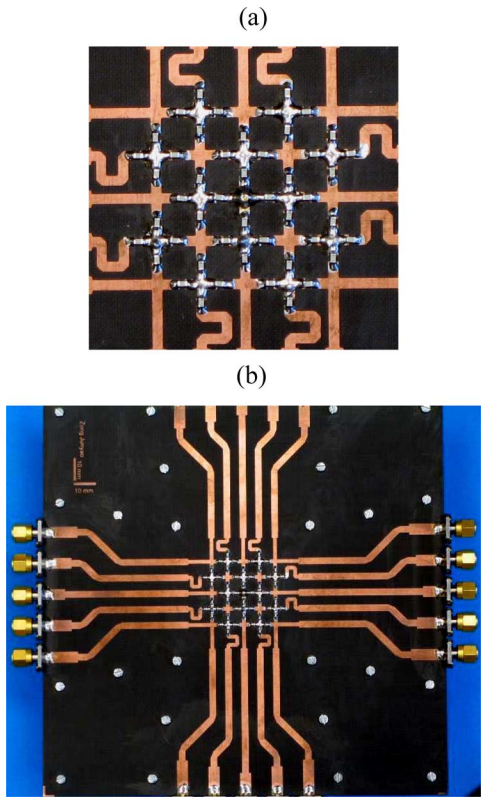

Fig. 9. Fabricated 20-way power divider. (a) Close-up of square-shaped metamaterial power divider. (b) Power divider test fixture. The input port is probe-fed from underneath.

V. Simulation and Measurements

Using Microwave Office, simulations were conducted in a manner to replicate the text fixture measurement environment [see Fig. 9(b)]. The simulations include the effect of surface-mount component parasitics though losses had an insignificant effect. Electromagnetic simulation of a via-port feeding a microstrip cross was used to account input port probe feed inductance.

An Agilent E8362B 20-GHz two-port network analyzer was used to obtain measurements. Two port deembedding was applied to the raw two-port data to remove the effects of the SMA-to-microstrip transitions, 50-Ω feed lines, quarter-wave transformers, and the input SMA connector. Signal flow graph theory [17] was used to correct the raw isolation measurement data for the input port termination mismatch. In addition to random measurement error, other sources of random error in the measurements are due to surface-mount component tolerance (5%), and residual mismatch of 50-Ω SMA terminations.

Fig. 10 shows the simulation and deembedded measurement results for the 20-way power divider with Fig. 10(a) showing magnitudes of key S-parameters and Fig. 10(b) showing coupling phases normalized to an average phase. In the case of simulation, only $S_{0,0}$, $S_{1,0}$, $S_{2,0}$, $S_{3,0}$, and $S_{20,1}$ are shown. All

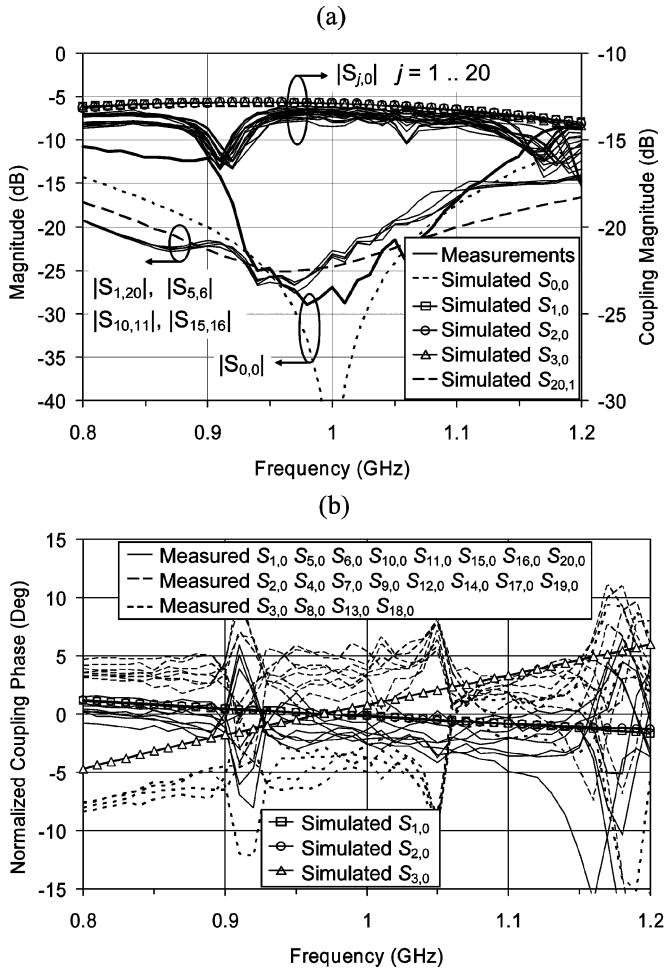

Fig. 10. Simulation and measurement results of the fabricated 20-way power divider. (a) Magnitudes. (b) Coupling phases.

the measured divider couplings $S_{j,0}$, where $j = 1, \ldots, 20$ are shown, but no attempt has been made to identify each trace, as the purpose here is to demonstrate the extent to which equal in-phase power division was obtained. As the structure is mechanically symmetrical, in Fig. 10(b), measured $S_{1,0}$, $S_{5,0}$, $S_{6,0}$, $S_{10,0}$, $S_{11,0}$, $S_{15,0}$, $S_{16,0}$, and $S_{20,0}$ are grouped to compare with the simulated $S_{1,0}$; measured $S_{2,0}$, $S_{4,0}$, $S_{7,0}$, $S_{9,0}$, $S_{12,0}$, $S_{14,0}$, $S_{17,0}$, and $S_{19,0}$ are grouped to compare with the simulated $S_{2,0}$; and measured $S_{3,0}$, $S_{8,0}$, $S_{13,0}$, and $S_{18,0}$ are grouped to compare with simulated $S_{3,0}$.

The measured isolations were all found to be around 26 dB around 1 GHz. The measured $S_{20,1}$, $S_{5,6}$, $S_{10,11}$, and $S_{15,16}$ were similar and had the narrowest bandwidth so their measured magnitudes are plotted in Fig. 10(a). There are 20 two-port S-parameter data sets each giving a measurement of $S_{0,0}$. As these $S_{0,0}$ measurements were nearly all identical, Fig. 10(a) shows the average measured $|S_{0,0}|$ response.

For both simulations and measurements, the output port reference impedance is 93.5 Ω. The input port reference impedance is $4.7 - j1.5\,\Omega$ for the simulations, whereas it is $4.7 - j2.9\,\Omega$ for the measurements. The complex value accounts for the probe feed inductance. The difference between the reactance for measurements (2.9 Ω) and simulations (1.5 Ω) is due to a combination of modeling error and input port deembedding error.

The simulated responses of $S_{1,0}$ and $S_{2,0}$ and $S_{3,0}$ show that equal amplitude in-phase power division occurs at 0.97 GHz. The deviation from 1 GHz is due to surface-mount component parasitic reactances. Over a 10% bandwidth (0.92–1.02 GHz), the couplings track within $\pm 1.3^\circ$ and there is no discernable difference for the magnitudes. Both input return-loss and the isolation are better than 20 dB from 0.92 to 1.02 GHz. At 0.97 GHz, all output port isolations were found to be 26 dB with $S_{20,1}$ having the narrowest bandwidth. It should be emphasized that this level of isolation was achieved without the use of isolation resistors.

The measured center frequency is 0.98 GHz. The input return loss and the isolation are better than 20 dB from 0.93 to 1.03 GHz. From 0.93 to 1.03 GHz, the measured couplings track within ± 1 dB and $\pm 6^\circ$. The measured insertion loss is less than 1.3 dB from 0.95 to 1.05 GHz.

Monte Carlo simulations indicate that the observed coupling spread is expected for a 5% surface-mount component tolerance. Tighter component tolerance and automated assembly would reduce this spread. The measured coupling magnitudes show a slight dip at 1.06 GHz and a more deeper one at 0.92 GHz. Simulations indicated that microstrip cross discontinuity parasitics cause the dip at 1.05 GHz. The input reflection coefficient and the couplings at 0.92 GHz indicate significant radiation loss occurs at 0.92 GHz. This suggests that the microstrip grid and ground plane supports parallel-plate propagation modes that are excited by the probe and subsequently radiate. Therefore, more attention is needed to design a probe feed to prevent this.

Other simulations have shown that the input port can be matched to 50 Ω using an *LC* impedance transformer comprising a series capacitor of 8.9 pF and a shunt inductance of 2.57 nH with minimal impact on the isolation and coupling bandwidth but the input return-loss 20-dB bandwidth reduces to 48 MHz.

VI. Conclusion

We have presented the design of a compact square-shaped N-way power divider based upon a metamaterial structure. The design method is based upon a numerical solution of an analytic model. A 20-way divider operating at 1 GHz was implemented in microstrip and surface-mount lumped components. The divider size was 50 mm by 50 mm. Over a 10% bandwidth, the measured insertion loss was less than 1.3 dB, the measured couplings track within ± 1 dB and $\pm 6^\circ$, and the measured input port return loss and isolation was greater than 20 dB. This level of isolation was achieved without isolation resistors. At higher frequencies, the "mushroom" structure [15] could be used to realize the left-handed behavior and this would also eliminate variations due to component tolerances. It is also important to design an input probe feed to prevent coupling to higher order modes.

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