Compact Dual-Fed Distributed Power Amplifier

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Abstract—The dual-fed distributed amplifier (DFDA) allows efficient combining of field-effect transistors (FETs) at the device level without using n-way power combiners. However, the FETs must be spaced 180°, resulting in physically large circuits. In this paper, meandered artificial transmission lines (TLs) comprised of microstrip lines periodically loaded with short open-circuit stubs can be used in place of TLs to reduce the size. The approach incorporates FET input and output capacitances with the artificial TLs, thereby eliminating their detrimental effects on bandwidth and performance. Both simulation and experimental results of a class-A three-FET single-ended DFDA designed to operate at 1.8 GHz demonstrate the feasibility of this approach and the validity of the design method. The size reduction is approximately one-third compared to realization using microstrip lines only, and the maximum efficiency is greater than 35% over a bandwidth of 15%.

Index Terms—Distributed amplifiers, microstrip circuits, microwave field-effect transistor (FET) amplifiers, microwave power FET amplifiers.

Fig. 1. Generic schematic of optimum single-ended dual-fed distributed power amplifier.

I. INTRODUCTION

TO OBTAIN high microwave powers using solid-state devices, it is necessary to combine the output power of several transistors. Parallel power combining is a popular method and is performed: 1) at the system level, involving separate design of amplifier modules and n-way combiners [1] or 2) at the device level, involving combiners that integrate both combining and impedance matching [2]. However, inter-connecting transmission lines (TLs) between amplifier modules and combiners add to the size and have nonzero insertion loss in the case of the former, while the necessity of using wide microstrip lines limits the performance of the latter [3]. Distributed amplification [4] is a method where power combining is performed directly at the device level without the need for n-way combiners. The conventional distributed amplifier (CDA) offers ultra-wide bandwidth, but has low efficiency and some of the transistors are under utilized—particularly at microwave frequencies [5].

The dual-fed distributed amplifier (DFDA) [6] comprises a pair of TLs that are periodically coupled by transistors, a hybrid to drive both ends of the gate (input) line, and another hybrid to combine waves appearing at the ends of the drain (output) line. There is no idle gate and drain line terminations in the DFDA, which are the bane of gain and efficiency of the CDA. Early investigations of the DFDA have demonstrated its gain [6] and efficiency [7], [8] advantages over the CDA.

The gain of the DFDA is maximized when 180° hybrids are used [9]. For the case of an even number of field-effect transistors (FETs) and use of 180° hybrids, 180° electrical spacing between the FETs results in all FETs contributing equal output power [10] and operating into identical load trajectories [11]. These identical load trajectories can be made optimum, thereby ensuring efficient operation and full utilization of all FETs [11]. Under this condition, the combining efficiency is 100% [10].

However, despite the above advantages, the DFDA has severe input and output match. The single-ended dual-fed distributed amplifier (SE DFDA) is a half-circuit equivalent of the DFDA [12]. Two SE DFDAs can be combined using 90° hybrids to form a balanced amplifier with its inherently good port match [12], [13]. Similar to the DFDA, the SE DFDA operates efficiently when ideal FETs are electrically spaced 180° [13]. The number of FETs in this optimum SE DFDA is, in principle, arbitrary. The SE DFDA has been demonstrated in practice to be a viable and efficient method of combining FET output power without using n-way combiners for both class-A operating conditions [14] and class-B operating conditions [15].

The optimum SE DFDA, however, requires 180° electrical spacing between the FETs [13], and means that the circuit is physically large at low microwave frequencies. Meandering of the TLs can be used to achieve compactness [16]. The use of artificial transmission lines (ATLs) in place of TLs can be used to reduce the length [17]–[19]. Photonic-bandgap structures that can be implemented in a microstrip line allow reduction of length [20], but explicit design formulas are as yet unavailable. Another approach is to replace a long length of TL with a shorter length of TL with shunt capacitances at each end [21], [22]. In this paper, we demonstrate that meandered ATLs result in significant reduction of circuit size. The proposed

TABLE I
EFFECT OF FET INPUT AND OUTPUT CAPACITANCE ON THREE-FET SE DFDA PERFORMANCE

Case	FET input and output capacitance	Φ at 1.8 GHz	Small-signal center frequency (f_o)	Small-signal bandwidth	Comparison of FET load trajectories around f_o
1	0 pF	180°	1.8 GHz	400 MHz	Identical
2	0.5 pF	180°	1.57 GHz	280 MHz	Nearly identical
3	0.5 pF	154°	1.8 GHz	280 MHz	Nearly identical
4	1.6 pF	120°	1.8 GHz	110 MHz	Differ significantly

method incorporates FET input and output capacitances into the ATLs, thereby eliminating the detrimental effects of these capacitances upon bandwidth and performance.

II. EFFECT OF FET INPUT AND OUTPUT CAPACITANCE ON THE SE DFDA

Fig. 1 shows a schematic of an n-FET SE DFDA. It is important to note that there are no idle resistive gate and drain line terminations, as is the case in the CDA. The short-circuit terminations of both the gain and drain lines emulate the dual feeding of the gate and drain lines [15]. Other pure reactive terminations can be used instead of short circuits [23], [24], though short-circuit terminations, as shown in Fig. 1, allow convenient application dc-bias voltages to the FETs [13].

In the case of the circuit of Fig. 1, the generator Thevenin impedance is equal to the gate line characteristic impedance Z_{oG}, and the load impedance is equal to the drain line characteristic impedance Z_{oD}. The electrical length of each TL section is indicated in Fig. 1. Namely, the electrical spacing between FET gates and FET drains is Φ, and the short-circuit terminations of the gate and drain lines are located $\Phi/2$ from the nth FET. We assume that the FETs are identical.

If we now assume that FET input and output capacitances are zero (at least at the center frequency), then with Φ equal to 180°: 1) the FET drain current magnitudes are equal; 2) the FET drain voltage magnitudes are equal; and 3) for each FET, the drain voltage is antiphase with respect to the drain current [11], [13]. In other words, the FET load trajectories are identical when Φ is equal to 180° [11], [13]. It has been shown [10] that the dual-feeding mechanism partially compensates for line loss, resulting in similar load trajectories in the presence of line loss.

For efficient operation and full utilization of the FET, we want the drain current to swing between zero and its maximum allowable value ($I_{D\max}$), and the drain voltage to swing between the knee voltage ($V_{D\min}$) and the maximum allowable voltage ($V_{D\max}$). Hence, for class-A operation of the SE DFDA, the FET load trajectories are optimum when [13]

$$Z_{oD} = \frac{V_{D\max} - V_{D\min}}{nI_{D\max}}. \qquad (1)$$

The above principles and design method assume that the FET input and output capacitances are zero. In practice, the input and output capacitances of microwave FETs are nonzero, but their effects are minimal at low microwave frequencies, especially if the characteristic impedance of the gate and drain lines is sufficiently low [14]. The gate characteristic impedance can be

made arbitrarily low, but the drain line characteristic impedance is constrained by (1). Fortunately, the output capacitance is less than the input capacitance. Alternatively, the input and output of each FET can be parallel resonated by shunt inductances to eliminate the effects of FET input and output capacitances at the center frequency [11], [13]. However, the inclusion of parallel resonant circuits into the SE DFDA limits the bandwidth.

Simulations of a three-FET SE DFDA were performed to investigate the effect of FET input and output capacitance on the circuit of Fig. 1, and to investigate the feasibility of reducing the size of the SE DFDA using capacitive loading [21], [22] at the FET ports. To eliminate other artifacts such as nonlinearity, parasitic inductances, etc., the FETs were represented by a simple linear model comprising a transconductance and input and output capacitances. Z_{oG} and Z_{oD} were both equal to 50 Ω. The following four cases were considered:

Case 1) Zero FET capacitances.
Case 2) 0.5-pF FET input and output capacitance and Φ equal to 180°.
Case 3) 0.5-pF FET input and output capacitance and Φ adjusted to compensate for these capacitances.
Case 4) Shunt capacitances at FET ports adjusted so that a one-third circuit size reduction is achieved.

The results of these simulations are summarized in Table I. In all cases, the load trajectories are essentially resistive about the small-signal center frequency (f_o). The right-most column of Table I gives a qualitative comparison of the FET load trajectories. Identical load trajectories mean that all FETs are equally utilized and, hence, all FETs can be made to operate optimally and be fully utilized. When the load trajectories differ significantly, at most, only one FET can operate optimally.

As expected, Case 1—being the ideal case—allows for optimum operation and has the largest small-signal bandwidth. Cases 2 and 3 represent the cases of capacitance of a typical medium power microwave FET. The effect of the capacitance is a noticeable reduction in small-signal bandwidth. Case 4 demonstrates that considerable circuit size reduction can be achieved, but is at the expense of bandwidth and the load trajectories are unsatisfactory.

The conclusion of this investigation is that the effects of the FET input and output capacitances need to be eliminated for maximum bandwidth and optimum performance. Further, the use of shunt capacitive loading at the FET ports is unfeasible for reducing the size of the SE DFDA. This is quite different from the CDA, where FET input and output capacitances are normally absorbed into the gate and drain line, since the electrical separation between FETs is small [25].
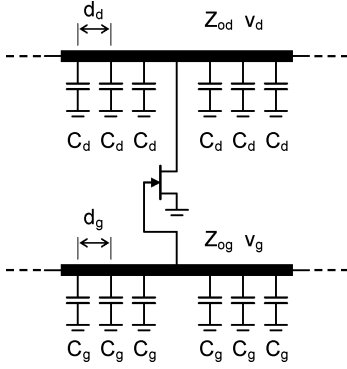
Fig. 2. Application of ATLs in the SE DFDA. Only one FET section is shown. In this case, m is 7 for both input and output ATLs.

III. SE DFDA USING ATLs

Meandering of the TLs is a commonly used method to reduce the area occupied by the circuit (e.g., [16]), but meandering alone has limited scope since: 1) the gate line has to be wide to mitigate the effect of FET input capacitance [14] and 2) a minimum separation between parallel sections of a meandered line is necessary to minimize the effects of spurious coupling [26].

ATLs are periodic structures that can be employed in place of TLs, resulting in size reduction. Earlier work on the application of ATLs in branch-line and rat-race couplers have demonstrated realization methods in microstrip line that makes optimum use of circuit area [19]. The proposal is to replace the gate and drain line TLs with ATLs.

Fig. 2 shows the method to apply ATLs to one FET (180°) section of the SE DFDA. The spacing between shunt capacitances (including FET input and output capacitances) is identical. The shunt capacitances on the middle ATL sections of Fig. 2 are provided by the FET input and output capacitances. The number of ATL unit cells for a 180° section is m and, hence, m is 7 for both input and output ATLs in Fig. 2. The characteristic impedances and phase velocities of the input and output TL elements are Z_{og} and Z_{od} and v_g and v_d, respectively.

If the input and output capacitances of the FET are C_{in} and C_{out}, respectively, then C_g and C_d should be equal to C_{in} and C_{out}, respectively, to ensure that the periodic structures behave as electrically smooth TLs (i.e., ATLs) [27]. The effective characteristic impedances of the input and output ATLs are Z_{oG} and Z_{oD}, respectively, and are smaller than Z_{og} and Z_{od}, respectively [19], [28]. The effective phase velocities of the ATLs are also smaller than v_g and v_d [19], [28]. It is possible to have C_d greater than C_{out} and C_g greater than C_{in}, in which case, capacitances of C_d–C_{out} and C_g–C_{in} must be placed in shunt with the gate and drain terminals of the FET, respectively.

It can be shown using the theory for periodic structures [27] that the values of C_g, Z_{og}, v_g, and d_g are constrained so that the desired value of Z_{oG} is obtained as follows:

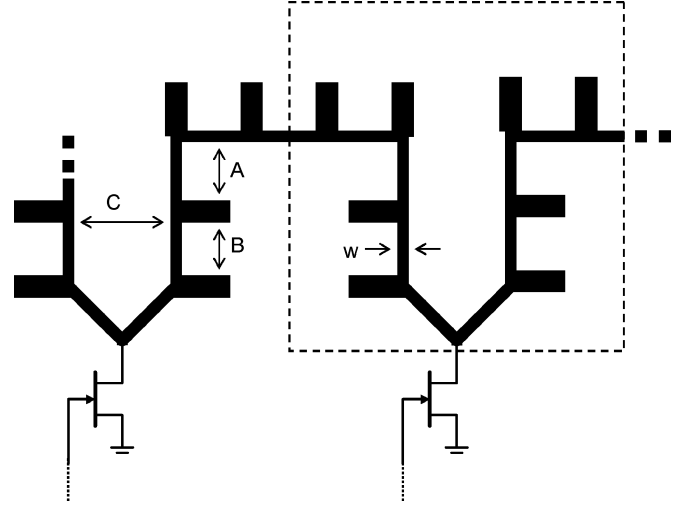$$Z_{oG} = \sqrt{\frac{d_g Z_{og}^2}{d_g + C_g v_g Z_{og}}} \qquad (2)$$

Fig. 3. Physical realization of the ATL. Only the output line is shown and, in this case, m is 9. Dashed box indicates portion of ATL simulated.

and m ATL sections have an electrical length of 180° as follows:

$$m \frac{\omega d_g}{v_g} \sqrt{1 + \frac{Z_{og} v_g C_g}{d_g}} = \pi \qquad (3)$$

where ω is the center angular frequency of the amplifier. Similar constraints apply for the drain ATL.

The microstrip characteristic impedance Z_{og} and phase velocity v_g are dependent on its width w, as well as substrate height and permittivity, and conductor thickness [26]. Equations (2) and (3) can be solved to eliminate d_g resulting in Z_{oG} in terms of C_g, Z_{og}, and v_g. Hence, a relation between Z_{oG} and w can be established, which can be used to obtain a suitable value of w that gives the desired value of Z_{oG} (e.g., 50 Ω). Finally, (2) can be solved for d_g.

In previous research, we have realized compact ATLs entirely from microstrip-line elements to implement compact hybrids [19]. Fig. 3 shows the proposal for application in the SE DFDA and involves meandering for both compactness and layout compatibility with the FETs, i.e., the "Y"-shaped three-way junctions minimizes interaction between the FET package and ATL. In the case of Fig. 3, m is 9. The shunt capacitances are realized with stubs. When realizing the ATLs, it is important that dimensions A, B (space between stubs), and C, shown in Fig. 3, are at least three times the substrate height so that coupling between elements is minimized [26]. The dimensions d_g and d_d and stub lengths need to be less than one-tenth the guide wavelength [19], [27].

IV. AMPLIFIER DESIGN

We now consider the design of a three-FET SE DFDA that operates at 1.8 GHz, uses the Fujitsu FLK012WF packaged GaAs FET [29], and has a substrate with 31-mil height and dielectric constant of 2.22.

As is the case in all power-amplifier design, it is necessary to have a large-signal model of the FETs. In this study, ADS[1]

[1]Advanced Design System 2002 (ADS), Agilent Technol., Palo Alto, CA, 2002. [Online]. Available: http://www.agilent.com

was used to simulate the amplifier and, hence, the standard ADS GaAs FET large-signal model was used with the following options invoked:

1) Statz drain current model [30];
2) junction capacitance model for both C_{GS} and C_{GD};
3) diode junctions to model breakdown and gate forward conduction.

The model also included linear parasitic elements and a constant series RC network in parallel with the drain current source to account for drain current dispersion [31]. The parameters for the model were obtained from information provided in the data sheets [29] and the model was fitted to the data sheet dc I/V characteristic and S-parameters. The optimized model gave good representation of the dc I/V characteristics and the S-parameters up to 10 GHz (though S_{12} prediction became less accurate above 6 GHz).

From the FET model (and data sheet [29]), design parameters were extracted, i.e., $V_{D\,\max} = 10$ V, $V_{D\,\min} = 1$ V, and $I_{D\,\max} = 60$ mA, and the pinchoff voltage is -2 V. Application of (1) results in Z_{oD} equal to 50 Ω, and the gate and drain bias voltages should be -1 and 5.5 V, respectively, for class-A operation [14]. Under this condition, the FET model reveals that C_{in} is 0.47 pF and C_{out} is 0.34 pF. The theoretical load power when the FETs are driven to their maximum undistorted class-A extent is 23.1 dBm, and the corresponding dc efficiency (ratio of load power to dc power drawn from the power supply) is 41%. It is easy to show that the dc efficiency of a single FET operated under exactly the same conditions would have a dc efficiency of 41%.

As both C_{in} and C_{out} are similar, the approach taken in this study was to design identical input and output ATLs, and an FET loading capacitance of 0.41 pF (being the average of 0.47 and 0.34 pF) was assumed. That is both ATLs were designed to have an effective characteristic impedance of 50 Ω. With 50-Ω ATLs, coupling to a 50-Ω generator and load is simplified.

The width of the stubs was set to 2 mm, and a length of 5.02 mm gives an input admittance equal to that of a 0.41-pF capacitance at 1.8 GHz. In the layout, the actual stub length was shortened by $w/2$ and no additional shortening of the stub was required to compensate for end-effect fringing. With m equal to 7, w equal to 1.3 mm results in Z_{oG} equal to 50 Ω, and d_g equal to 6.1 mm.

An electromagnetic (EM) simulation was performed of a 180° section of the planar ATL structure using Sonnet.[2] The outcome of the simulation was three-port S-parameters representing the geometry enclosed in the dashed box of Fig. 3 over a range of frequencies. To ensure that the simulation boundaries used by Sonnet do not affect the results, the sidewalls were placed at least 3 mm away from the structure. Sonnet can be setup to remove the effects of microstrip lines used to connect the structure to the simulation ports on the sidewalls.

To confirm that the simulated geometry and the FET input (or output capacitance) behaves as a 50-Ω 180° TL, the simulated results were embedded with a lumped capacitance of 0.41 pF to represent the FET input or output capacitance, as

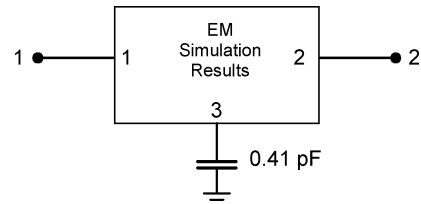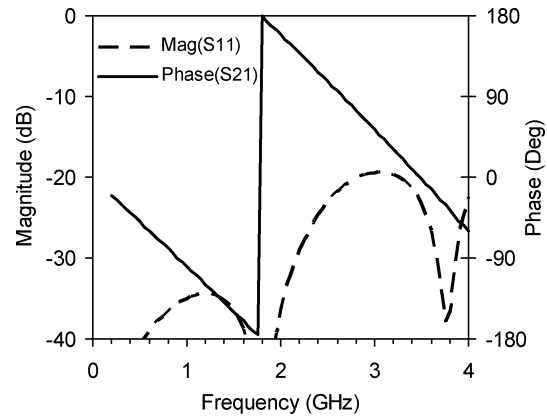Fig. 4.   Embedding circuit to confirm response of ATL geometry.

Fig. 5.   Embedded simulated s-parameters of the 50-Ω/180° ATL.

shown in Fig. 4. The result of this embedding is two-port S-parameters. For the initial design, it was found that the effective characteristic impedance was satisfactory, but the electrical length was only 162° at 1.8 GHz. Thus, d_g and stub length were both lengthened by 11%, and, hence, the final optimized values of d_g and stub length are equal to 6.8 and 5.6 mm, respectively. The structure was resimulated and the embedded results are shown in Fig. 5. Fig. 5 shows that the ATL return loss is greater than 30 dB below 2.2 GHz.

As a comparison, if microstrip TLs had been used, their length would have been around 63 mm to achieve an electrical length of 180° at 1.8 GHz. On the other hand, the 180° ATL is 48 mm in length and has been meandered.

The three-port data for the ATL section was exported to ADS for harmonic-balance and small-signal S-parameter simulations. The three-port data represented the ATLs up to a frequency of 18 GHz in steps of 0.2 GHz, which is sufficient for harmonic-balance simulation with up to eight harmonics. Chip capacitors of 10-pF capacitors were used for both dc blocking and to short-circuit terminate the gate and drain ATLs at RF frequencies. The chip capacitors have a series inductance of 300 pH, and this effect was included in the simulations. The gate and drain power supplies were fed to the end of the ATLs. A 50-Ω chip resistor was included in series with the gate bias power supply to ensure stability of the circuit at low frequencies. For convergence of the harmonic-balance simulations, eight harmonics was found to be sufficient. The simulations confirmed that the amplifier would work in accordance with theoretical expectations, and is stable.

The amplifier was fabricated, and Fig. 6 shows a photograph of the amplifier. The size of the amplifier is about the same as a two-FET SE DFDA [14] with the same operating frequency, but uses 180° microstrip TLs between each FET. Thus, the size of an amplifier section had been reduced by about one-third.
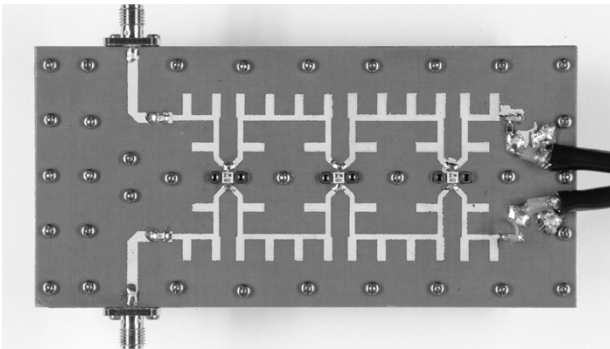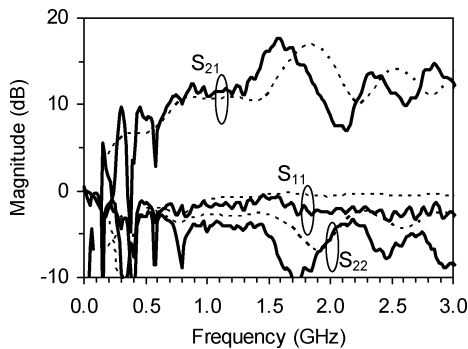
Fig. 6.   Prototype three-FET SE DFDA.

Fig. 7.   Measured and simulated small-signal S-parameters of the amplifier. Heavy lines are measurements, thin dashed lines are simulations.

Fig. 8.   Measured and simulated load power and PAE versus input generator available power at 1.8 GHz.

Fig. 9.   Measured load power versus frequency.

V. EXPERIMENT

Due to manufacturing variations, the actual FETs will have characteristics that differ from published data [29]. DC measurements of the amplifier were first performed and established that the optimum gate bias voltage for class-A operation to be −1.1 V when the drain bias voltage is 5.5 V.

Small-signal S-parameter measurements were made under class-A operating conditions using a vector network analyzer. Fig. 7 shows the measured and simulated values of S_{11}, S_{22}, and S_{21}. The measured small-signal gain (S_{21}) has a peak of 17 dB and is consistent with the peak simulated small-signal gain. Aside from a shift in center frequency, the measurements are consistent with the simulations. The shift in center frequency is due to uncertainties such as the interaction between the body of the FET packages and the ATL (that was not considered in the simulations) [15], circuit etching tolerance, tolerance of FET location, and FET model uncertainty. The bandwidth is, however, 350 MHz and is close to the bandwidth obtained for the ideal case (Case 1) investigated in Section II.

The mismatch at both the input and output ports (Fig. 7) is normal for SE DFDAs, which are inherently mismatched. In practice, one would use two identical SE DFDAs in a balanced amplifier whose ports would be matched [12], [14].

Scalar large-signal measurements of the amplifier were obtained using a computer-controlled system comprising a spectrum analyzer, signal generator, and multiplexed multimeter. The spectrum analyzer was calibrated against a power meter. The software managed the calibration and accounted fo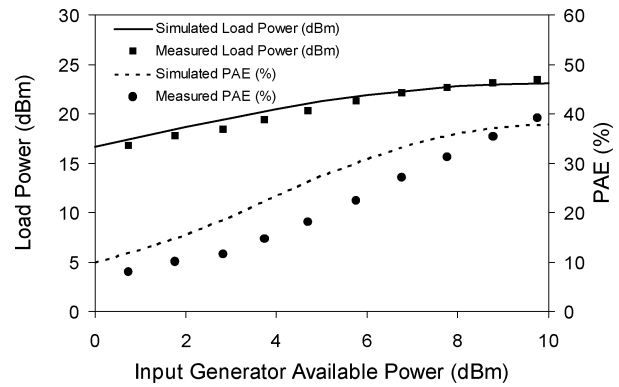r cable insertion loss. The measurement system permitted measurement of the input generator available power, load power, and the power drawn from the power supply.

The facilities we had did not permit accurate measurement of the amplifier input power. Instead, the input power was taken as the input generator available power and this is justified since, in practice, the SE DFDA would be used in a balanced amplifier that has matched ports [12], [14]. Due to the mismatched port of the SE DFDA, the actual input power will be considerably smaller than the generator available power and, therefore, the measured power-added efficiency (PAE) will be smaller than the true PAE; but is a true reflection of the PAE that would be encountered in practice when used in a balanced amplifier [12], [14], [15].

Fig. 8 shows the measured and harmonic-balance simulation results of the load power and PAE at 1.8 GHz. Fig. 8 shows good correspondence between simulation and measurements, as well as consistency with theoretical predictions.

Figs. 9 and 10 show, respectively, the measured load power and PAE as a function of frequency for various input generator power levels. The measurements show that the optimum large-signal performance is centered at 1.7 GHz. It is clear that the amplifier saturates at around 23 dBm over a bandwidth of 200 MHz. The maximum efficiency is greater than 35% over a bandwidth of 250 MHz (or 15%). The efficiency of the experimental three-FET SE DFDA is as good as a conventional single-FET power amplifier that uses the same FET.
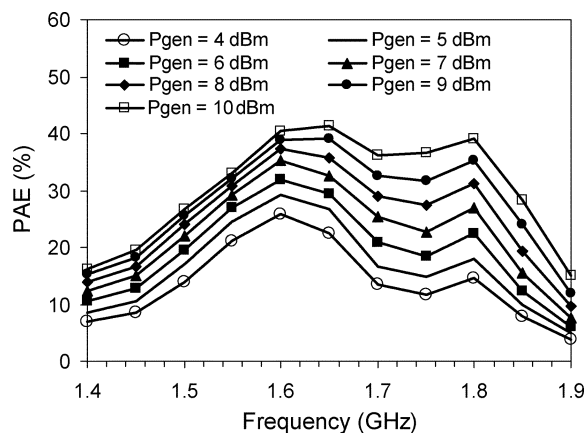
Fig. 10.   Measured PAE versus frequency.

VI. CONCLUSION

In this paper, we have demonstrated a distributed combined power amplifier with an efficiency similar to a conventional single-FET power amplifier employing the same FET. The amplification principle is based upon the DFDA approach to efficiently combine FET output power. Meandered ATLs assembled from microstrip-line elements used in place of TLs results in compactness, and also incorporates FET input and output capacitances, thereby eliminating their detrimental effect on bandwidth and performance. The experimental results of a class-A three-FET SE DFDA designed to operate at 1.8 GHz demonstrated the feasibility of the proposed method and the validity of the design method. The level of size reduction is one-third per amplifier section, and maximum efficiency was greater than 35% over a bandwidth of 15%.

The experimental amplifier was realized using a soft substrate, but the principles of the method could be applied to other realization technologies. The proposed method allows the realization of an SE DFDA on a monolithic microwave integrated circuit (MMIC) where 180° microstrip lines would otherwise be unfeasible. In this case, the shunt capacitances could be realized with metal–insulator–metal (MIM) capacitors available in standard MMIC processes [26]. This would be necessary for high-power FETs due to their significant input and output capacitances [28]. The application of ATLs in active MMICs has been demonstrated by others [17].

The proposed method assumed that FET parasitic gate and drain inductances have a negligible effect. This assumption is valid at 1.8 GHz for the FETs used in the prototype (operating at 1.8 GHz). This assumption becomes increasingly invalid with increasing frequency. The author is currently investigating methods to design the SE DFDA that consider FET parasitic inductances, as well as input and output capacitances, and would enable the SE DFDA to be applied at higher frequencies.

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