DESIGN CONSIDERATIONS FOR THE DUAL-FED DISTRIBUTED POWER AMPLIFIER.

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The dual-fed distributed amplifier is a variation of the conventional single-fed distributed amplifier whereby the input signal is fed to both ends of the input line using a hybrid, and signals appearing at both ends of the output line are combined using another hybrid. Such a configuration allows utilisation of output power in the backward as well as forward waves. Much of the previous work in the literature only considered small-signal analysis and small electrical spacing between FETs, and did not lend insight into the operational behaviour. This paper therefore considers the development of a design method for the dual-fed distributed power amplifier with large electrical spacing. The simulations demonstrate optimum loadlines are achieved for all FETs and that all FET output power is utilised.

1 Introduction

The conventional distributed amplifier has proven highly successful for small-signal broadband applications. However, its success in power applications has been limited for a number of fundamental reasons such as: uneven output power distribution among the FETs [1], and output power wastage in the back-ward waves [2]. The first problem results in under utilisation of some of the FETs, whilst the second problem results in lowered efficiency due to wasted output power. Typically at microwave frequencies, the FETs nearest the output terminal contributes the most power whilst the FETs farthest away contributes minimal. Over some frequency ranges, some of the FETs sink rather than source power [1]. Methods such as output line tapering [2] may be used to minimise power in the backward waves and circuit optimisation [3] may be used to improve the output power distribution among the FETs. However, their success is limited as the problems they aim to cure are fundamental in nature.

A variation to the distributed amplifier topology, the dual-fed distributed amplifier, has been proposed as a means to utilise output power in both the backward and forward waves [4]. The circuit diagram of the modified distributed amplifier is shown in Figure 1 and essentially involves a dual-feed at both the input and output lines using hybrids. Despite the promise that such feeding should provide, the previous work [4][5][6] only considered a small-signal analysis and small electrical spacing between FETs, and did not lend insight into the operational behaviour. Recent work by this author [7], which considered large electrical spacing between the FETs, determined the conditions whereby power equalisation among all the FETs can be achieved. With power equalisation it is possible to have all FETs operating into an optimum lineline. It is therefore the purpose of this work to develop design guidelines for power amplification using the dual-fed distributed amplifier based on the conclusion of the previous investigation [7].

2 Theory

For the purposes of developing design equations, the circuit shown in Figure 1 may be represented by a simplified circuit depicted in Figure 2 [7]. It has been assumed that FET input and output capacitances have been absorbed into the respective transmission lines [7] or effects neutralised by a resonant circuit. The input hybrid may be replaced by a pair of Thevenin sources representing the signals appearing at the output of the input divider. The output hybrid may be replaced by the loads seen by the output transmission line. For argument sake, we will further assume that the input and

output transmission line sections are lossless, have equal length, both have effective characteristic impedance Z_o and phase constant **b**. It will be assumed that the couplers are both matched to Z_o at the frequencies of interest. Let the complex variable z ("delay variable") equal e$xp(- jl$**b**$)$. The voltages and currents in Figure 2 are peak values and refer to signals and do not include dc bias. If the FETs are operated in class-A mode, and have high linearity then the drain current of the kth FET is approximately given by:

$$I_{d_k} = G_m V_{g_k} \qquad \qquad ...1$$

where G_m is the large-signal transconductance. We will assume, as many other such analyses assume, that feedback may be neglected.
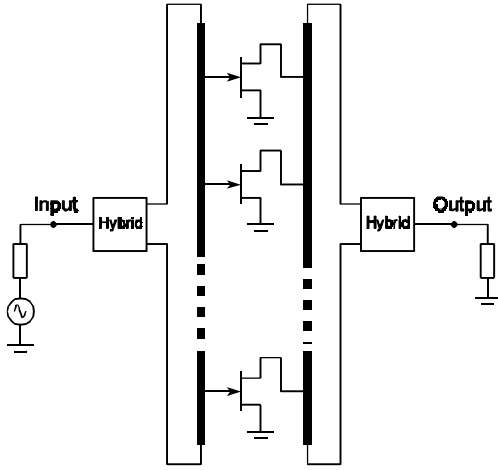

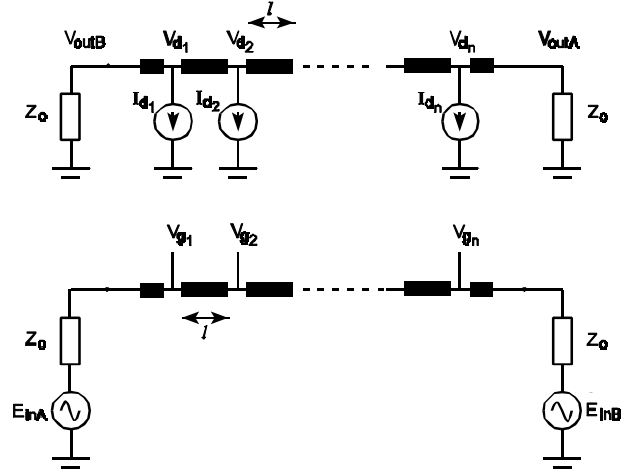Figure 1   Dual-fed distributed amplifier

Figure 2 Equivalent circuit of dual-fed
distributed amplifier.

Let E_{inA} is equal to E, and E_{inB} equal to $E\,exp(j$**f**$)$.   The gate voltage of the kth FET will consist of two components, one due to E_{inA}, and the other due to E_{inB} :

$$V_{g_k} = \frac{E\sqrt{z}}{2}\left(z^{k-1} + z^{n-k}\,e^{jf}\right) \qquad \qquad ...2$$

and hence the drain current of the kth FET will be:

$$I_{d_k} = \frac{G_m E\sqrt{z}}{2}\left(z^{k-1} + z^{n-k}\,e^{jf}\right) \qquad \qquad ...3$$

All drain current sources drive into a load impedance of $Z_o/2$ and expressions for the drain voltages can however be written in terms of the drain current sources:

$$V_{d_k} = \frac{Z_o}{2}\left(... + z^2 I_{d_{k-2}} + z I_{d_{k-1}} + I_{d_k} + z I_{d_{k+1}} + z^2 I_{d+2} + ...\right) \qquad ...4$$

The point to realise is that the kth drain voltage is not solely due to the kth FET drain current but has contributions from all FET drain currents.

The previous work [7] determined that z equal to –1 (spacing of 180 °) results in output power equalisation among the FETs. For n equal to 4 and setting z equal to –1 gives:

$$V_{d_1}(-1) = V_{d_3}(-1) = -V_{d_2}(-1) = -V_{d_4}(-1) = -jG_m E Z_o\left(1-e^{jf}\right) \qquad ...5a$$

$$I_{d_1}(-1) = I_{d_3}(-1) = -I_{d_2}(-1) = -I_{d_4}(-1) = \frac{jG_m E}{2}\left(1 - e^{jf}\right) \qquad ...5b$$

We see that the two output voltages will be 180° out of phase, the drain voltage and current for each FET are 180° out of phase and the magnitude of their ratio is $2Z_o$. In other words the effective

loadline resistance of each FET under this condition is 4 times the actual load resistance $Z_o/2$. One could conclude that for (at least) even n, the loadline resistance is n times $Z_o/2$.

Figure 3 shows idealised drain i/v characteristics with an optimum class-A load trajectory overlaid. The optimum loadline resistance is given by the reciprocal of the slope of the load trajectory and equating to $nZ_o/2$ we obtain the optimum characteristic impedance of the output transmission line for n even:

$$Z_{o_{opt}} \quad = \quad 2\left(\frac{V_{D\max} - V_{D\min}}{I_{D\max}\, n}\right) \qquad\qquad ...6$$

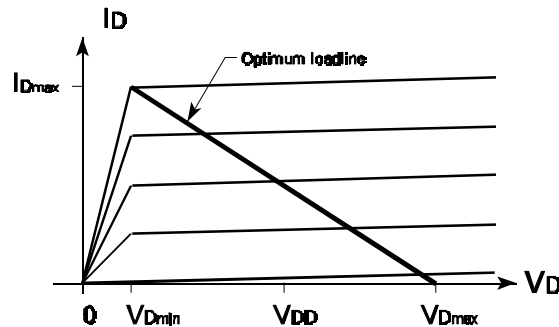Figure 3 FET drain dc i/v characteristics

3   Design Example

We consider the design of a dual-fed distributed amplifier with a centre frequency of 10 GHz employing four FETs ($n = 4$), rat-race hybrids at both the input and output (hence f is 180°). The FETs have a minimum and maximum drain voltage of 1 V and 10 V respectively, and a maximum drain current of 60 mA. The FETs were each spaced by 180° at 10 GHz so as to achieve power equalisation at 10 GHz [7]. Using (6) the optimum value of the output line characteristic impedance was found to be 75 Ω which was coupled to the 50 Ω rat-race hybrid by quarter-wave transformers. The dc gate and drain bias voltages were set to –1 V and 5.5 V respectively. The input line characteristic impedance was set to 50 Ω. The input and output of each FET was resonated using parallel resonators with Q chosen to trade-off distortion and bandwidth. The gate and drain bias voltages were fed to the FETs using the resonator inductances. Further calculations revealed that the output power of each FET would be 68 mW (18.3 dBm), and hence the total output power should be 272 mW (24.3 dBm), and the drain efficiency to be 41 %.

Table I   FET Parameters

Parameter	Value	Parameter	Value	Parameter	Value
β	0.205 AV^{-2}	R_G	0.6 Ω	C_{RF}	1 µF
b	6 AV^{-1}	R_S	1.7 Ω	R_C	500 Ω
V_{TO}	-2 V	R_D	2.0 Ω	V_{BR}	15 V
α	2 V^{-1}	L_G	0.17 nH		
V_{bi}	0.85 V	L_S	0.054 nH		
C_{GS0}	0.41 pF	L_D	0.12 nH		
C_{GD}	0.027 pF	C_{DS}	0.14 pF		

Simulations using HP MDS^{TM} were used to check the validity of the calculations and their corresponding assumptions. The FETs were modelled using the well known Statz-Raytheon model of which the parameters are given in Table I. At 10 GHz with an input level of 12 dBm: the load

trajectories (as seen by the drain current source) were essentially optimum and identical for all FETs. Each FET sourced 18.1 dBm, and the total output power was 24.2 dBm meaning all power in the forward and backward waves was recovered. The simulation therefore confirmed the design procedure. The drain efficiency was found to be 39 %, whilst the power added efficiency was 37 %. Figure 4 shows the output voltage waveform (across 50 Ω load) whilst Figure 5 shows the small-signal transducer gain frequency response.
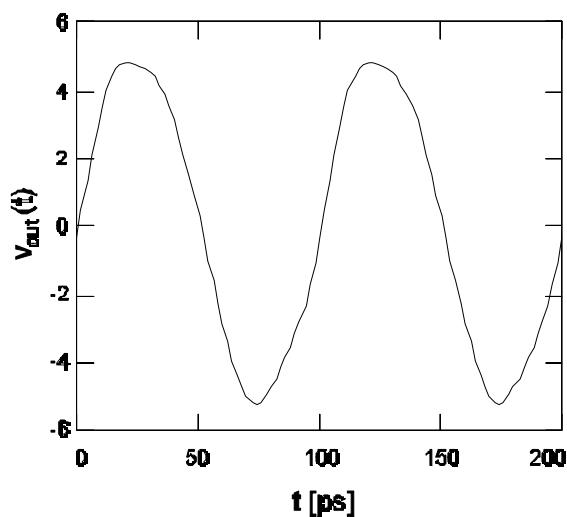

Figure 4. Output voltage waveform with input power level of 12 dBm.
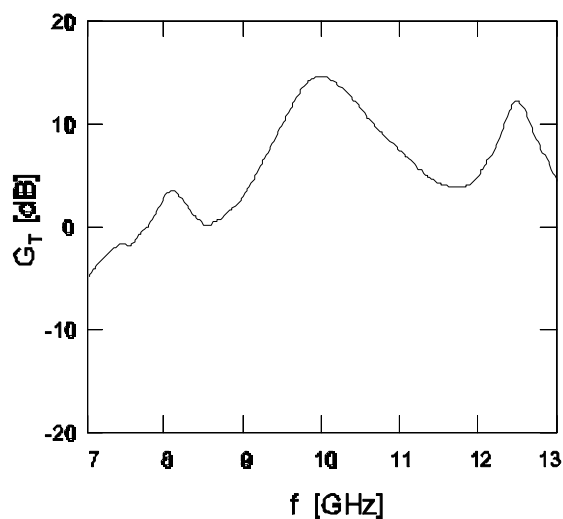

Figure 5. Small-signal transducer gain.

4   Conclusion

In this paper we have shown the development of a design method for the dual-fed distributed power amplifier that achieves power equalisation and optimum loadline trajectory for all FETs. For power equalisation, the spacing between the FETs must 180° at the centre frequency, and for an optimum loadline, the characteristic impedance of the output line must be $2/n$ times the optimum loadline resistance for the case of an even number of FETs. Simulations have demonstrated the validity of this approach. Work is continuing to improve the bandwidth and to apply the design concepts developed in this paper for MMIC realisation.

References

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