Multiband Power Amplifier for Multiband Wireless Applications

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Abstract:
RF sub-systems in multimode / multiband wireless communication systems need to operate on different bands that are typically narrow but sparsely separated. We show that a single-ended dual-fed distributed amplifier can operate efficiently over several sparsely separated bands. This approach therefore alleviates the need for separate amplifiers for each band.

1. Introduction
To facilitate roaming across mobile telephone networks, the handset must be able to operate in several different modes and bands. For example a dual-band GSM handset operates at both 900 MHz and 1800 MHz to implement GSM900 and GSM1800 respectively. Third generation mobile systems will need to operate over several more bands ([1][2], and may receive GPS as well as being able to connect to wireless LANs [1]. The bands are typically narrow but are sparsely separated ([2][3]. It is difficult to design an efficient power amplifier that operates efficiently over a wide bandwidth. Hence the usual approach for multiband systems is to have separate narrowband power amplifiers for each band that are combined using duplexers [4].

It has been shown that the dual-fed distributed amplifier (DFDA), which uses hybrids to feed both ends of the gate and drain lines, can utilise all FET output power [5], and with suitable circuit design, can utilise FETs to their fullest extent [6]. The efficiency of a DFDA is therefore significantly better than a conventional distributed amplifier. Theoretical investigations of the DFDA [7] have revealed the periodic frequency response of the FET output power and amplifier output power. It is this periodic frequency response that can be exploited for multiband application. A variant of the DFDA - the single-ended dual-fed distributed amplifier (SE-DFDA) - allows realisation of balanced amplifiers, with their inherently good port match, but with the additional benefits of the DFDA [8].

For a DFDA that uses 180° hybrids and an even number of identical FETs, the FET output powers are equal, and the amplifier output power maximum, when the spacing between the FETs is integer multiples of 180° [7]. Under this condition, of equal FET output power, the loadlines can be made identical and optimum [6].

It has been shown that for 180° FET spacing, the FETs in a single-ended dual-fed distributed amplifier (SE-DFDA) - shown in Figure 1 - can operate optimally as though they were in a DFDA using 180° hybrids and twice as many FETs with 180° spacing [9]. The SE-DFDA will only work under this optimum condition at odd integer multiples of 180° FET spacing. The short-circuit gate and drain line terminations of the SE-DFDA (Figure 1) short-circuit the FET ports at even multiples of 180° FET spacing. Therefore the SE-DFDA of Figure 1 would not be a suitable candidate for a dual-band system whose band centres are even multiples (eg. GSM900 / GSM1800). At the odd multiples of 180° FET spacing, the short-circuit terminations are transformed to open-circuits at the terminals of the FETs. This suggests that the short-circuit terminations be removed, leaving open-circuit terminations for the gate and drain lines as depicted in Figure 2. The two variants of the SE-DFDA will therefore be distinguished by the gate and drain line terminations: short-circuit terminated SE-DFDA (SC-SE-DFDA) and open-circuit terminated SE-DFDA (OC-SE-DFDA).

2. Theoretical Analysis
Assumptions made and nomenclature used in this theoretical analysis of the circuits in Figures 1 and 2 will be similar that used in references [6][7]. We will assume that the FETs in Figures 1 and 2 are ideal with zero input and output parasitics, and can be described by a large-signal transconductance Gm. For well designed power FETs, Gm may be assumed constant under class-A operating conditions. For argument sake, we will further assume that the gate and drain line transmission line sections have equal length, have effective characteristic impedance Z0 and phase constant β. Let the complex
variable \( z \) ("delay variable") equal \( \exp(j\beta l) \) where \( l \) is the physical spacing between the FETs. We will consider only the signal voltages and currents and ignore dc bias, and number the FETs beginning from the port ends of the gate and drain lines.

The drain current of the \( k \)th FET is approximately given by:

\[
I_{d_k} = G_m V_{g_k} \quad \ldots 1
\]

The gate voltage of the \( k \)th FET will consist of two components, one due to the incident voltage and another due to the voltage wave reflected from the gate line termination:

\[
V_{g_k} = \frac{E}{2} \left( z^{k-1} + z^{2(n-k)} \Gamma \right) \quad \ldots 2
\]

where \( \Gamma \) is equal to -1 for the SC-SE-DFDA (Figure 1) or equal to 1 for the OC-SE-DFDA (Figure 2). Hence the drain current of the \( k \)th FET will be:

\[
I_{d_k} = \frac{EG_m}{2} \left( z^{k-1} + z^{2(n-k)} \Gamma \right) \quad \ldots 3
\]

All drain current sources drive into a load impedance of \( Z_0/2 \). The \( k \)th drain voltage is not solely due to the \( k \)th FET drain current, but has contributions from all FET drain currents and reflections from the drain line termination:

\[
V_{d_k} = -\frac{Z_0}{2} \left( \ldots + z I_{d_{k-1}} + I_{d_k} + z I_{d_{k+1}} + \ldots \right) \quad \ldots 4
\]

\[
= \frac{Z_0 \Gamma}{2} \left( \ldots + z I_{d_{k-1}} + z^{2(n-k)} I_{d_k} + z^{2(n-k)} I_{d_{k+1}} + \ldots \right)
\]

For odd integer multiples of \( 180^\circ \), \( z \) is equal to -1, and for even integer multiples, \( z \) is equal to 1. For both the SC-SE-DFDA and the OC-SE-DFDA, we find \( I_{d_k}(-1) \) is equal to \( G_m E \) for \( k \) odd, and \( -G_m E \) for \( k \) even, and \( V_{d_k}(-1) \) is equal to \( -nG_m E Z_0 \) for \( k \) odd, and \( nG_m E Z_0 \) for \( k \) even. The SC-SE-DFDA gate and drain voltages are equal to zero when \( z \) is equal to 1. For the OC-SE-DFDA we find \( I_{d_k}(1) \) is equal to \( G_m E \) for all \( k \), and \( V_{d_k}(1) \) is equal to \( -nG_m E Z_0 \) for all \( k \). One concludes that the FET loadline resistance is \( nZ_0 \) for the SC-SE-DFDA (\( z = -1 \)) and OC-SE-DFDA (\( z = 1 \)).

Figure 3 shows idealised drain i/v characteristics with an optimum class-A load trajectory overlaid. \( V_{D_{\text{max}}} \) is the boundary between the triode and saturation regions, \( V_{D_{\text{max}}} \) is the maximum voltage determined by drain breakdown, whilst \( I_{D_{\text{max}}} \) is the maximum drain saturation current. The optimum loadline resistance is given by the reciprocal of the slope of the load trajectory, and equating to \( nZ_0 \) we obtain the optimum characteristic impedance of the drain transmission line:

\[
Z_{0_{\text{opt}}} = \frac{V_{D_{\text{max}}} - V_{D_{\text{min}}}}{I_{D_{\text{max}}}} \quad \ldots 5
\]
4. Discussion

The above simulations have demonstrated the ability of the OC-SE-DFDA to amplify in several narrow but sparsely separated bands. Although the FET spacing is large, slow-wave structures, such as artificial transmission lines, can be used in place of conventional transmission lines to interconnect the FETs. The SE-DFDA has severe mismatch but this can be overcome by combining two SE-DFDAs using 90° hybrids to form a balanced amplifier [8][9]. Clearly for multiband application, the hybrids need to at least have a multiband frequency response. The conventional branchline hybrid works for line lengths equal to odd multiples of 90° and hence is suitable for the SC-SE-DFDA. Clearly broadband hybrids (eg. [10]) are required for the OC-SE-DFDA to cover, for example, the first two passbands.

5. Conclusion

We have demonstrated that the SE-DFDA offers a multiband response that can be used in multiband/multimode wireless communications where the bands are narrow but sparsely separated. This approach alleviates the need to multiple amplifier modules for each band and associated diplexers. The SE-DFDA offers better efficiency compared to a conventional distributed amplifier. Work is continuing to design suitable compact hybrids for combining two SE-DFDAs, as well as design artificial transmission lines that have shorter physical length compared to conventional transmission lines.

References:


Figure 4: Small-signal transducer gain.

Figure 5: Output power and efficiency at 900 MHz.

Figure 6: Output power and efficiency at 1800 MHz.

Figure 7: FET loadlines at 1700 GHz with 7 dBm input source power.

Figure 8: FET loadlines at 1900 GHz with 7 dBm input source power.