Four-transistor interleaved Doherty amplifier

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A Doherty amplifier that combines four transistors is proposed. Two transistors are operated in class-B and are interleaved with another two operated in class-C. The interleaved transistors are driven by a travelling-wave feed and their output currents are combined using a single distributed power combiner.

Introduction: A conventional RF or microwave power amplifier achieves high DC-to-RF conversion efficiency when operating at maximum output power. When amplifying signals that modulate the amplitude (eg. QAM or OFDM), a low average efficiency is obtained. The Doherty amplifier [1] couples a class-B main amplifier and a class-C peaking amplifier so that high DC-to-RF conversion efficiency is achieved over a wide dynamic range. The main amplifier operates over the entire range of input levels and the peaking amplifier only operates over the upper end of the dynamic range.

The Doherty amplifier is designed so that the peaking amplifier turns on when the main amplifier reaches maximum output power. The peaking amplifier along with an impedance inverter coupling the amplifiers, causes the main amplifier load impedance to decrease (called load modulation) thereby allowing it to operate at maximum output power and efficiency over the upper end of the dynamic range without saturating.

Additional peaking amplifiers can be combined either to extend the upper end of the dynamic range [2, 3]. Distributed power combiners can be used to yield separate multi-transistor power-combined main and peaking amplifiers, which are coupled to form a conventional Doherty amplifier [4]. In this Letter, a Doherty amplifier is described that comprises multiples of class-B and class-C operated transistors that are combined with a single combiner, hence reducing circuit size.

Proposed circuit: Fig. 1 shows a circuit that interleaves two class-B operated transistors (M1 and M2) with two class-C operated transistors (P1 and P2). Without loss of generality, FETs are shown in Fig. 1, but bipolar junction transistors could be used, and the approach could be extended to combine more than four transistors. The bias circuits are not shown, but decoupling is required on the input feedline between FET gates as they necessarily have different bias voltages to achieve alternating class-B and class-C operation. The parallel resonators connected in shunt with each FET drain are tuned to the amplifier centre frequency and have sufficient Q to shunt harmonic currents generated by the FETs to ground.

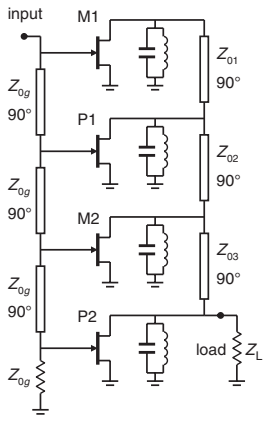

Fig. 1 *Interleaved four-FET Doherty amplifier*

The input signal is fed to the FET gates using a travelling-wave distributed feed so that all FETs are driven with the same amplitude but with: M1 180° out of phase with M2, P1 180° out of phase with P2, M1 90° out of phase with P1, and M2 90° out of phase with P2. At the load, all FETs combine in phase.

The two class-B operated FETs (M1 and M2) are combined as though they were in a dual-fed distributed amplifier [5], and similarly for the two class-C operated FETs (P1 and P2). However, unlike previous work [4], the main and peaking transistors are interleaved so only the input feeding network and one combiner are used to achieve dual-fed distributed combining of M1 and M2, and dual-fed distributed combining of P1 and P2. By eliminating a power combiner and input feed network, the circuit size is reduced by 50%.

Similar to the original Doherty amplifier [1], the class-C and class-B transistors interact to achieve load modulation of the class-B transistors. Theoretical calculations have shown that the characteristic impedances (Z_{01}, Z_{02} and Z_{03}) of the transmission line elements coupling the FET drains, and the load impedance Z_L, determine the nature and level of the load modulation.

Simulation: To show that the circuit efficiently combines the transistors and achieves load modulation of the class-B transistors (M1 and M2), simulations were conducted using a harmonic balance microwave circuit simulator. The amplifier was designed to operate at 1 GHz. The FETs were assumed to have zero input and output capacitance, and zero parasitics, and a drain current, I_D, being a function of the gate-source voltage, V_{GS}, and drain-source voltage, V_{DS}:

$$I_D = \begin{cases} I_{DSS}(1 - V_{GS}/V_T)\text{TANH}(\alpha V_{DS}); & V_{GS} > V_T \\ 0 \quad ; & V_{GS} \le V_T \end{cases} \tag{1}$$

where V_T, I_{DSS} and α are model parameters, and TANH(x) is a polynomial approximation to the hyperbolic tangent function. In this work $\alpha = 2.5\ \text{V}^{-1}$ and $V_T = -2$ V with the former parameter value yielding a knee voltage of approximately 1 V.

A gate bias voltage of −2 V was used for M1 and M2 to achieve class-B operation, and a gate bias voltage of −3 V was used for P1 and P2 so they are active when the amplifier RF input voltage exceeds 1 V. M1 and M2 had an $I_{DSS} = 100$ mA, and P1 and P2 had an $I_{DSS} = 250$ mA, and this meant all four FETs ideally achieve a maximum fundamental component of drain current of 50 mA when the RF input voltage is 2 V.

The drain bias voltage for all FETs was set to 5 V. The impedances Z_{01}, Z_{02}, Z_{03} and Z_L were chosen to be 40, 31, 40 and 30 Ω, respectively. These values of impedance ensure that useful load modulation occurs and that the drain i/v characteristics of M1 and M2 are effectively utilised over the upper 6 dB of the dynamic range to maximise efficiency. Z_{0g} was chosen to be 50 Ω, which means that the amplifier input is matched to 50 Ω.

Fig. 2 shows the simulated results for the fundamental components of drain voltage of M1 and M2. The fundamental component of the drain voltage of P2 is also the amplifier output voltage, and is also shown in Fig. 2. For input voltages below 1 V, the drain voltages of M1 and M2 are directly proportional to the input voltage demonstrating constant loads. As the input voltage rises above 1 V, the drain voltages of M1 and M2 are confined to ranges of 3.6–4.2 V and 3–4.3 V, respectively. Loadlines plotted on i/v characteristics confirmed that this was an artefact of load modulation of M1 and M2, rather than the saturation. Indeed, as the drain voltage of P2 in Fig. 2 shows, the amplifier remains linear for input voltages above 1 V.

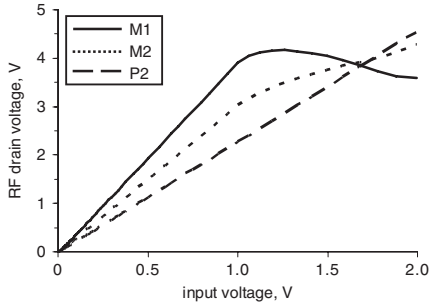

Fig. 2 *Fundamental component of drain voltage of M1, M2 and P2*

Fig. 3 shows the DC-to-RF conversion efficiency for the proposed interleaved Doherty amplifier, and a class-B amplifier employing a FET with $\alpha = 2.5\ \text{V}^{-1}$, $V_T = -2$ V and $I_{DSS} = 100$ mA, a load of 80 Ω and a drain bias voltage of 5 V. It is clear that the interleaved Doherty amplifier achieves high efficiency over the upper 6 dB of its dynamic range and, over a considerable dynamic range, significantly outperforms the class-B amplifier. The power gain of the amplifier was found to be 9.3 dB, only varying by 0.3 dB over a 16 dB range of input power.

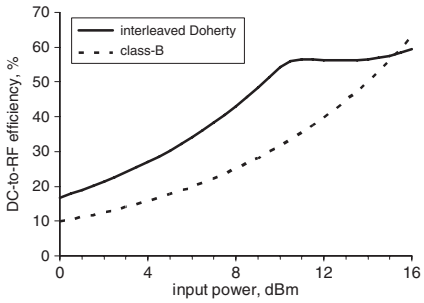

Fig. 3 *DC-to-RF conversion efficiency against input power*

Conclusions: A linear power amplifier interleaving class-B operated transistors with class-C operated transistors that achieves power combining with a single power combiner and input feed has been demonstrated to achieve high DC-to-RF efficiency over a wide dynamic range. The presence of load modulation of the class-B operated transistors demonstrates Doherty amplifier behaviour. Further investigations are required to quantify load modulation behaviour to permit optimum circuit design.

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References

1 Doherty, W.H.: 'A new high efficiency power amplifier for modulated waves', *Proc. IRE*, 1936, **24**, (9), pp. 1163–1182
2 Yang, Y., Cha, J., Shin, B., and Kim, B.: 'A fully matched N-way Doherty amplifier with optimised linearity', *IEEE Trans. Microw. Theory Tech.*, 2003, **51**, (3), pp. 986–993
3 Srirattana, N., Raghavan, A., Heo, D., Allen, P.E., and Laskar, J.: 'Analysis and design of a high-efficiency multistage Doherty power amplifier for wireless communications', *IEEE Trans. Microw. Theory Tech.*, 2005, **53**, (3), pp. 852–860
4 Cho, K.J., Kim, W.J., Stapleton, S.P., Kim, J.H., Lee, B., Choi, J.J., Kim, J.Y., and Lee, J.C.: 'Design of *N*-way distributed Doherty amplifier for WCDMA and OFDM applications', *Electron. Lett.*, 2007, **43**, (10), pp. 577–579
5 Eccleston, K.W., and Kyaw, O.: 'Analysis and design of Class-B dual-fed distributed power amplifiers', *IEE Proc., Microw. Antennas Propag.*, 2004, **151**, (2), pp. 104–108