AN ULTRA-CHEAP GRID CONNECTED INVERTER FOR SMALL SCALE GRID CONNECTION

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ABSTRACT

This paper reports on the development of a cheap and simple grid connected inverters. It is intended for an integration of a small power photo-voltaic or wind turbine to a grid at low cost. The proposed inverter uses the single cycle control technique, which reduces switching complexity and forces the current waveform to match the voltage waveform. The control circuit operation for unity power factor output is explained. The method is simulated on PSCAD program for single phase system. The simulation output exhibits excellent performance with few components. The paper only considers the current wave-shaping control of the inverters and does not discuss other aspects of control such as maximum power point tracking. The simulations are compared with the prototype waveforms.

INTRODUCTION

The purpose of a grid connected inverter (GCI) is to transfer energy to the utility. Various single stage and multi-stage GCI are used. The single stage inverter offers simple structure and low cost but suffers from limited input voltage range, while the multi stage inverters are complex, expensive and less efficient (Xue et al. 2004). The GCI mostly utilizes complex circuitry to improve the power quality. Often it requires a DSP or FPGA for the control system and synchronization with the utility (Shaffer et al. 2003). Continuous research and development on GCIs have already established efficient and rugged inverters in the market. When the power level goes down to a couple of hundred Watts, the cost of the inverter becomes the dominant factor. In case of the grid connected photo voltaic (PV) systems the GCI system carries the significant percentage of cost for its investment (Khaouzam, 1997). It is challenging to make a cheap GCI with unity power factor, high efficiency, high reliability and simple circuitry etc.

For developing countries like Nepal, large scale power generation requires huge investment and the transmission cost is very expensive due to its mountainous topography. The alternative is to accommodate smaller grid systems in rural areas, powered with freely available renewable sources. Nepal has tremendous potential for small hydro, solar and wind generation at most of the remote places. The average solar

insolation is around 4.5KWh/m^2/day, almost evenly distributed in Nepal (Adhikari, 1998). Cheaply available GCIs will increase the utilization of resources in such places. But this GCI is more suitable for a strong grid where the voltage waveform is generally good quality and the source impedance is small.

This paper explains the development of a cheap directly coupled GCI for low power level using a single cycle control technique (SCC). The shape of the output current is controlled by controlling the converter's switching pulse duration such that its average value is proportional to the current reference in each switching cycle (Smedley, 1991). A prototype inverter has been built in the laboratory. Detailed design considerations and simulated results are presented. The inverter operates in buck mode during unity power factor operation, which requires the DC side voltage to be greater than the peak of the AC voltage. The converter current magnitude can be varied by changing the signal at the input of the integrator. The maximum power point tracking, control and protection of requirements for grid connected application are not included in this paper. Finally the scaled experimental results for unity power factor output are presented to verify the simulation.

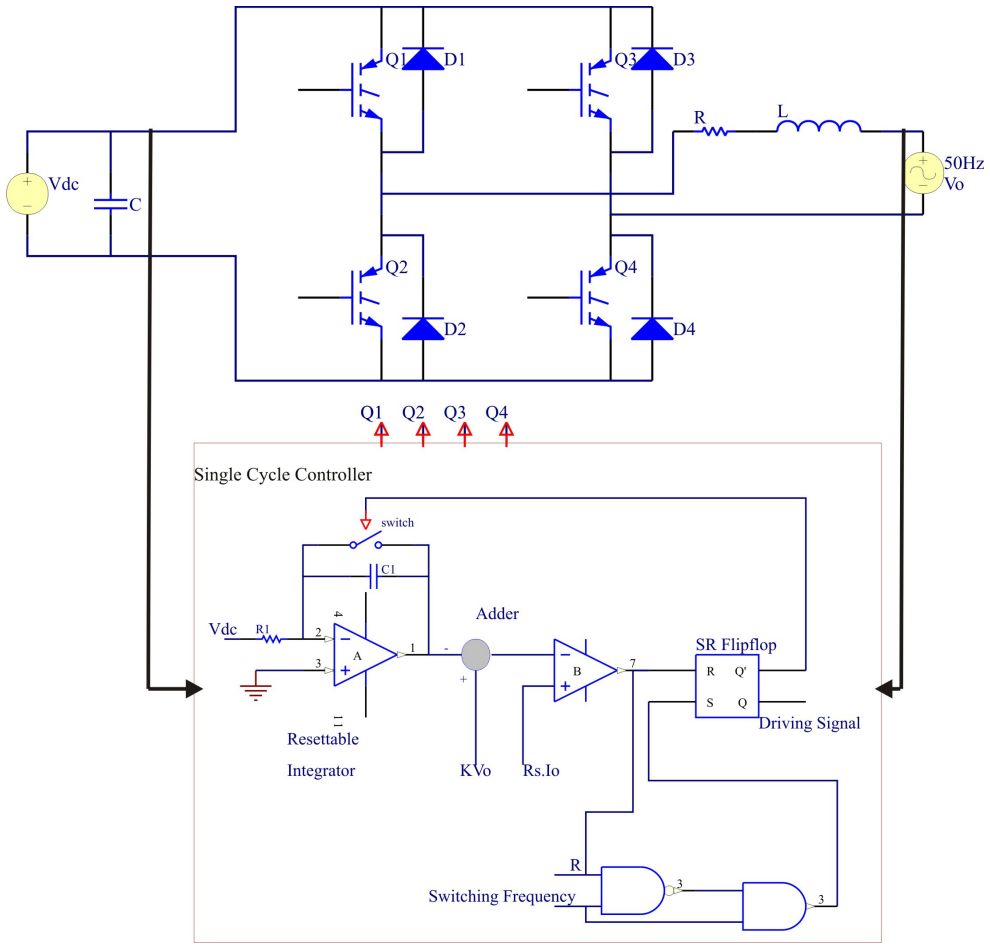

Fig. 1: GCI block diagram

DESCRIPTION

The GCI can be divided into three functional blocks; the controller, power-bridge and the filter. The GCI block circuit diagram is shown in Fig. 1.

Controller

The single cycle controller (SCC) is used to control the power switches. The controller is very effective for grid connection applications. It forces the output current to match the voltage waveform, hence fulfils the most desirable characteristic of unity power factor. The controller comprises a constant frequency oscillator, resettable integrator, voltage adder, comparator and a flip-flop switch. The flip-flop sets the constant switching frequency for the converter. The duty cycle depends on the integrator voltage slope and the output current flowing through the inductor at the given power level.

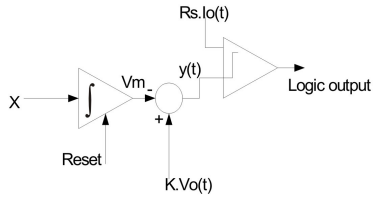

Fig. 2: SCC signal flow block

As shown in Fig. 2, X is the steady signal applied at the input of the resettable integrator. This defines the rms current level being injected into the AC system. The integrator output falls with a negative voltage, the slope depends upon the magnitude of X. The switching frequency is much higher than the utility frequency. The output is added to K.Vo(t) which is the reference voltage waveform taken from the utility to shape the output current. The result y(t) is compared with the inductor current Io(t) with multiplying factor current sensing resistance Rs. The logic output drives the flip flop. The converter current rises while y(t) is greater than the Rs.Io(t), and when they are equal the integrator is reset and the converter current falls. Equation (1) describes the switching condition for a switching period Ts.

$$K.Vo(t) - X.DTs = Rs.Io(t) \quad (1)$$

The single cycle controller governing equation (2) is developed by (Smedley et al., 2003). Vo is the utility voltage and Io is the inverter current.

$$Rs.Io = K.Vo - Vm \quad (2)$$

Where K is a constant and Vm is the voltage fall before the integrator is reset. This is implemented as shown in Fig. 2. As shown in Fig. 3, Vmax is the maximum voltage that can fall during each cycle. Hence Vm from equation (2) is described by equation 3.

$$Vm = -V\max.D \text{ for } t \le DTs \quad (3)$$

$$Vm = 0 \text{ for } t \ge DTs$$

The converter current magnitude can be controlled by controlling the signal X at the input of the integrator. By increasing the signal X the integrator output falls more quickly, increasing the slope and eventually decreasing the average output current. Depending upon the type of source, X can be controlled for maximum power point tracking operation.

Power bridge

A simple H-bridge type inverter as shown in Fig. 1 is implemented in the circuit which allows for four quadrant (4Q) operations. Reversible active and reactive power control is achievable in the 4Q operation. The SCC compares the falling edge of the integrator voltage with the rising edge of the inductor current to terminate the switching signals. The hybrid pulse width modulation (HPWM) switching strategy is used. It is named HPWM because only two of the four switches are operate at high frequency and the other two are operate at the line frequency (Lai & Ngo, 1994).

The HPWM strategy has an identical inverter output voltage shape to the conventional unipolar pulse width modulation (UPWM), though it loses the frequency doubling effect.

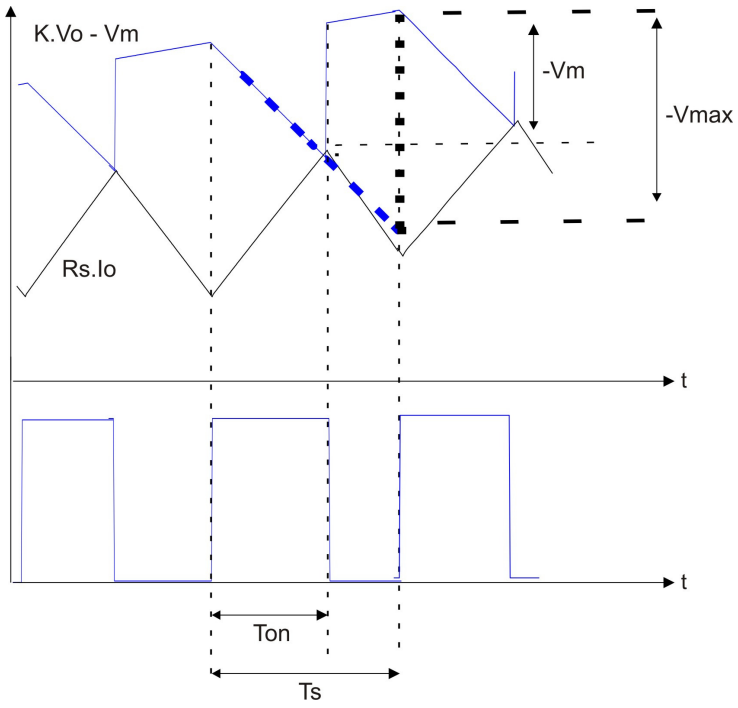

Fig. 3: Controller operation waveform

The prospective inverter output voltages for HPWM switching strategy are tabulated in Tab. 1.

Tab. 1: Inverter voltage for HPWM switching strategy

High Side Switches		Low Side Switches		Converter Voltage
Q1	Q3	Q2	Q4	
ON	OFF	OFF	ON	+Vdc
OFF	OFF	ON	ON	0
OFF	ON	ON	OFF	-Vdc

ON	ON	OFF	OFF	0

The HPWM offers low switching losses and switching strategies for two quadrant and four quadrant operation of the H-bridge inverter. For least current distortion during zero-crossings the following switching strategy is chosen.

In the inverter as shown in Fig. 4,

1. During Positive half cycle:

   The switch Q1 operates at PWM switching frequency, Q4 ON and Q3 and Q2 are OFF.

2. During Negative half cycle:

   The switch Q3 operates at PWM switching frequency, Q2 ON and Q1 and Q4 are OFF.

When the switches Q1 and Q4 are ON rising current flows through the switch Q1, inductor and Q4 until the current meets the adder output voltage y(t) as shown in Fig 2. When the switch Q1 goes OFF the inductor current reduces through the switch Q4 and the diode D2 until next switching cycle starts. Similarly switches Q2, Q3 and the diode D4 will activate during negative half cycle.

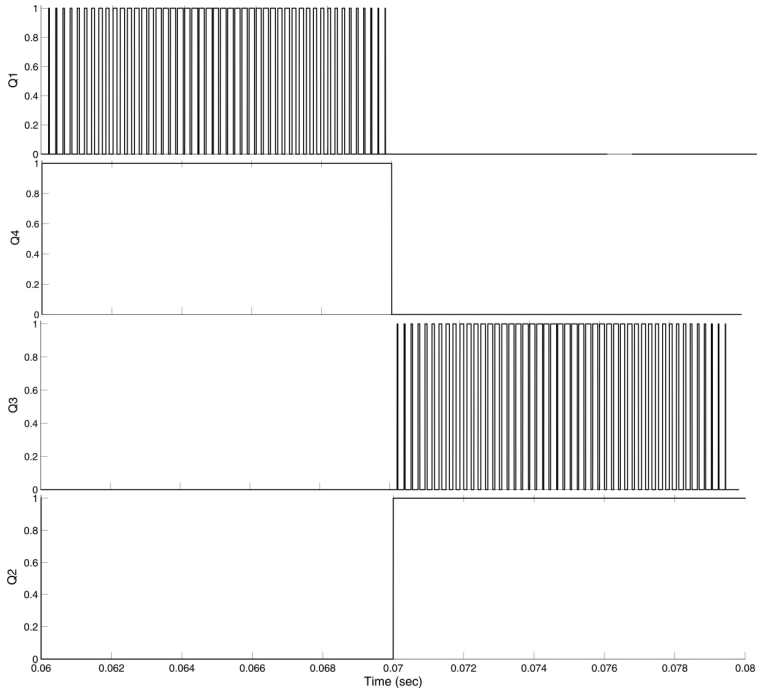

Fig. 4: Switching logic for Q1, Q2, Q3 and Q4

Filter

The purpose of filter is to reduce the high frequency harmonic content of the line current due to the switching operation of the inverter. The series inductor is used as a filter. The inverter is directly coupled to the mains through the filter. The SCC compares the inductor current with the integrated voltage at each switching cycle. The converter operates in continuous conduction at 5KHz. The fixed frequency oscillator ensures the integrator starts integrating at the right time. The inductor is such that the current ripple is small. The integrator time constant is shorter than the time of one switching cycle to ensure that the integration is completed within one switching period and the controller resets it to zero to prepare for the next cycle.

The current shape should match the voltage waveform to get unity power factor, but the current rise and fall through the inductor has a limitation during zero crossing periods. The current rise $\frac{dIon,rise}{dt}$ is fast because the inductor voltage is high during ON period around zero crossings and the current fall $\frac{dIoff,fall}{dt}$ is slow. The slow falling of current creates a distortion around the AC voltage zero crossings as shown in Fig. 5. The RS flip-flip gets a high signal at both R and S input pins at this stage which gives an unknown output due to undefined state of the flip-flop. It may reset the integrator or turn ON/OFF a IGBT at the wrong time and violate the SCC control principle which would give distorted current waveform. In order to minimise this waveform distortion, an additional logic circuit as shown in Fig. 6 is added in the controller to avoid the undefined states. The truth table after modification is given in Tab.2, where R and SW1 are applied at the reset and set pins of the flip-flop, and SW1 and SW2 are intermediate stages of the logic circuit as shown in Fig. 6.

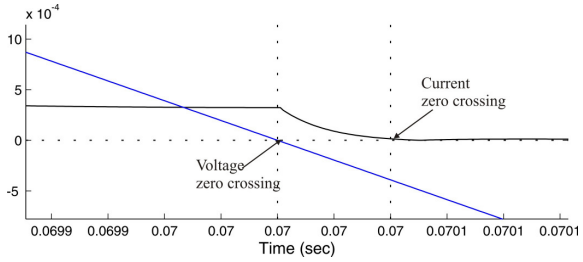

Fig. 5: Output Current and AC voltage near zero crossing

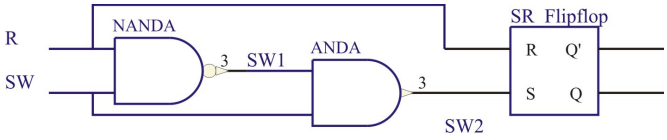

Fig. 6 Additional logic to avoid RS flip flop in unknown states

Tab. 2: Truth table for modified logic circuit

R	SW	SW1	SW2
0	0	1	0
0	1	1	1
1	0	1	0
1	1	0	0

SIMULATION RESULTS

PSCAD software is used to simulate the GCI. The absolute value of y(t) and Io(t) are compared as shown in Fig. 7(1). At the zero crossing it is noticed that the current signal is higher than the voltage. The reset pin of flip flop as shown in Fig 7(2) is high during that period after the addition of logic circuit as shown in Fig. 6. As mentioned in power bridge section, the switch Q4 ON for whole positive half cycle, hence current keeps flowing through Q4, diode D2 and inductor until the next cycle starts. The prospective inverter output voltage during that period is zero as shown in fig. 7 (3).

A single phase 230VAC, 50Hz line is considered as a grid. The input DC voltage is at 400V. A single phase full bridge inverter is used and power switches are IGBT switches. The switching frequency is at 5KHz. The inverter output is directly coupled to the utility using a 40mH Inductor and a 0.01 Ohm series resistor. The reference voltage and current comparison, integrator reset signal, inverter output voltage and output current and the line voltage are shown in Fig. 7 for 500W single phase system.

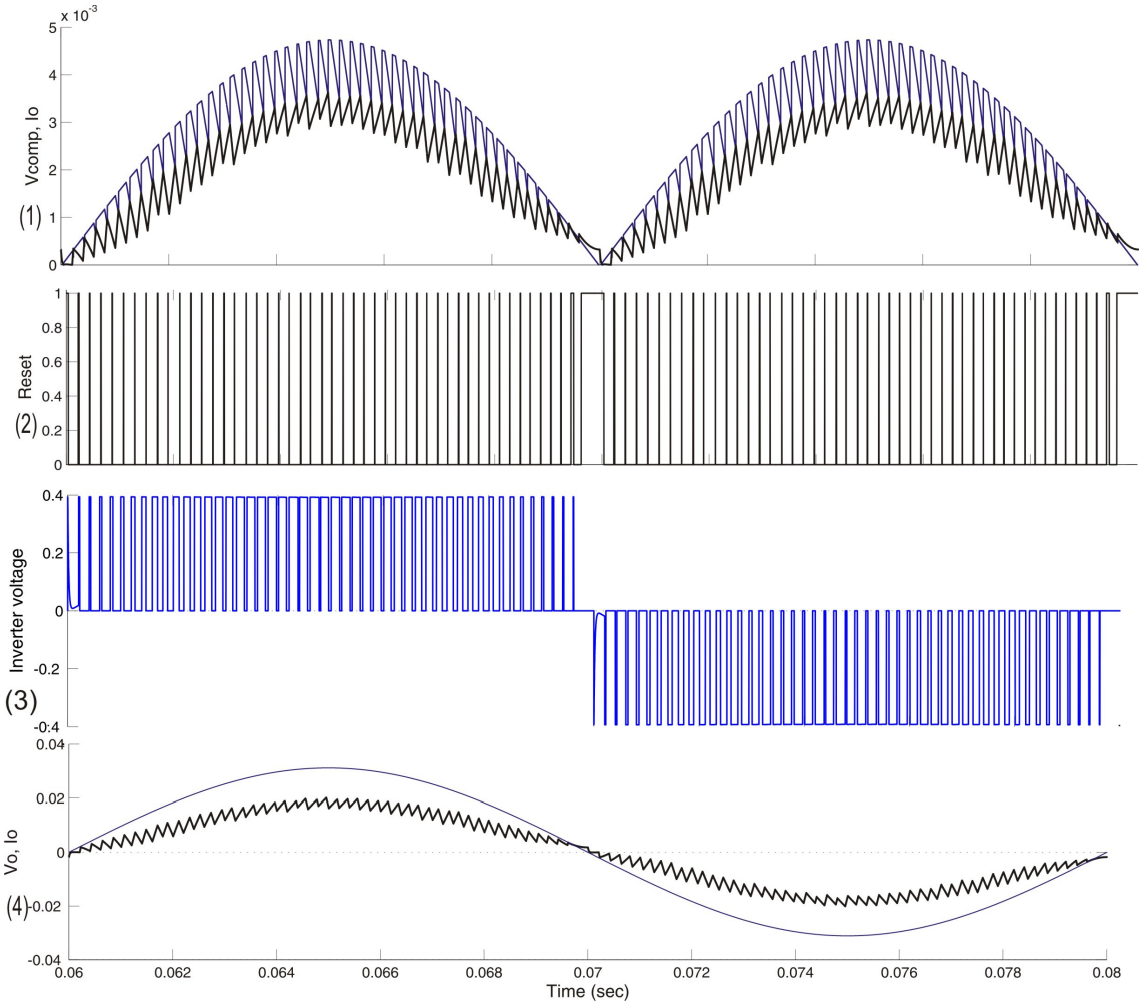

Fig. 7: Simulated results for (1). Integrated Voltage and current comparison (2). Integrator reset (3). Inverter output voltage (4). Output voltage and current waveform

EXPERIMENTAL RESULTS

A prototype inverter is built at the laboratory. The peak power rating for the inverter is 1KW. A HCPL 788j is used for the current sensing. A simple 555 timer is used as an oscillator to generate the fixed switching frequency. A combination of CMOS logic gates are used to operate the bridge in the HPWM switching mode. The IGBT Hi and Low side driver IR2112 is used to drive the IGBT in the power bridge. The experimental measurements of output current and line voltage reference are shown in Figure 8 at 1:10 scaled utility and DC side voltage level.

The controller forces the output current to be the same shape and phase angle as the line voltage, as shown in the experimental results Fig. 8. The DC side voltage of the inverter contains 100Hz ripple during experimental measurement which distorted the integrator output voltage in each cycle. The experimental output current waveform is distorted during zero crossings as found in simulation as shown in Fig. 7(4). The output current has high frequency ripple as observed in the simulation. The experimental results verify the simulation results for unity power factor operation. The significantly more distorted waveform is likely to be due to noise on the measured waveforms affecting the control strategy.

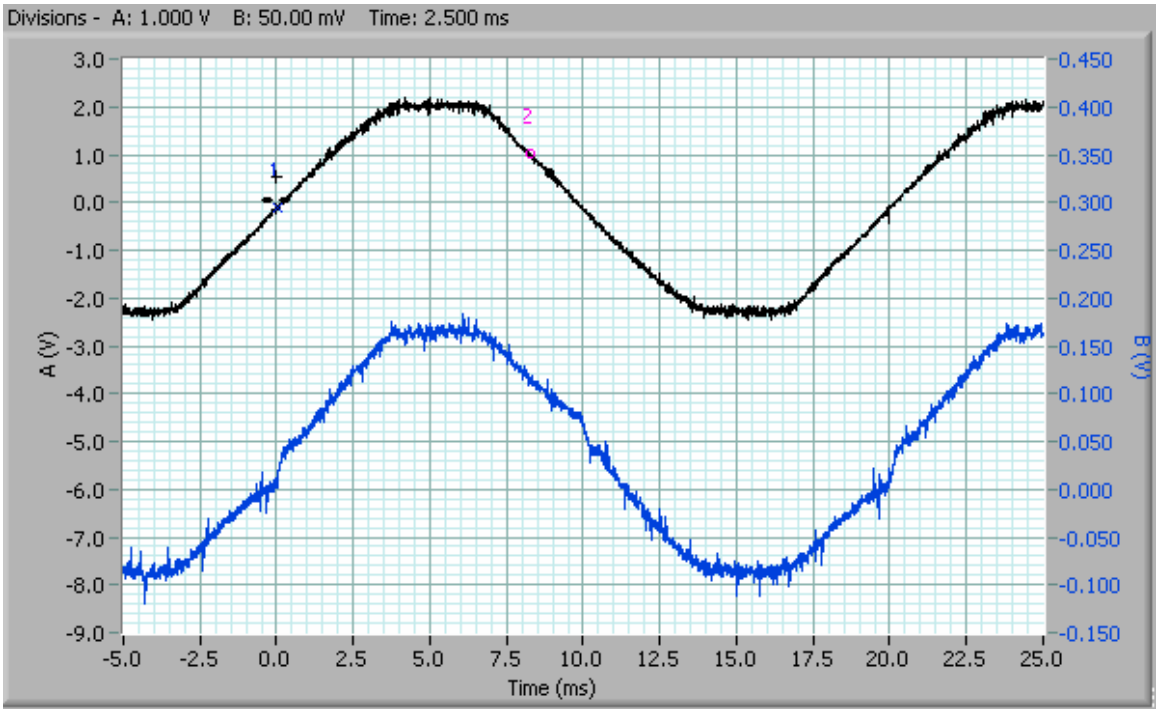

Fig. 8: Scaled Line voltage taken as a reference waveform (upper), Output current (lower)

Voltage scale 1:1,1V/div, Current scale 100mV/A, 50mV/div

(Experimental results for GCI at unity power factor)

FUTURE DEVELOPMENT

The ability to connect small scale generation to weak grids is especially important. The SCC control technique as presented cannot provide reactive power, so is less flexible for grid support than more complex controllers. Further to this, as the current is controlled to follow the voltage wave shape, existing voltage distortion will not be reduced.

Each of these can be addressed by generating a suitable voltage reference waveform that can efficiently allow a different current phase angle and/ or wave shape to flow. To allow this, the switching strategy also must be extended. A cheap implementation of this is currently being investigated.

CONCLUSION

This paper reports on the development of cheap single stage directly coupled grid connected inverter for low power generator. The SCC control technique reduces its complexity and makes it cheap with a unity power factor output. The HPWM switching strategy is used which offers low switching losses across the power switches. The simulations results are verified by experiment and the work is in progress for the performance improvement of the simple GCI.

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BRIEF BIOGRAPHY OF PRESENTER

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