Fast Ethernet Readout for Medipix Arrays with MARS-CT

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The MARS readout is a gigabit ethernet camera readout for Medipix 2 and Medipix 3 devices. Medipix is a family of highly integrated photon counting/timing pixel processors developed by CERN. The pixels are $55 \times 55\,\mu$m in a 256×256 array, so the chip is 14×14 mm. Medipix 2 has 2^{16} independent 14-bit counters, one per pixel. Medipix 3 has the same number of 24-bit counters, with several optional counter configurations including 2 counters per pixel.

Medipix 2 can count energy or time events that occur within two programmable thresholds. Medipix 3 can do the same, but it can instead bin events into 2 contiguous bins per pixel or 8 per 2×2 super-pixel. For example, while Medipix 2 can count photons that fall inside a single range of energies, Medipix 3 can classify photons into 8 energies in one exposure. This feature allows for innovative spectral analysis of radiation such as x-rays.

The MARS-CT is a compact x-ray CT scanner that uses Medipix chips as photon counters. It takes advantage both of the high detector efficiency and of the ability to classify individual photons by energy. It thus produces "color x-rays" being spectral x-ray images, and allowing new types of materials analysis.

The MARS-CT 3 scanner accepts objects up to 100 mm in diameter, 300 mm in length, resolves voxels to $30\,\mu$m resolution, and measures up to 24 energy bands. Six Medipix chips butted in an array are operated at a frame rate of up to 100 Hz. With Medipix 2 chips this generates a sustained bit rate of 5.5×10^8 bits/s. The Medipix 3 generates 9.5×10^8 bits/s.

After considering the NIKHEF Muros 2 and the IEAP-CTU USB readouts, we decided to implement a new design that is compact, has high bandwidth, and can easily be operated from standard workstations over a network. The MARS readout uses UDP over IP, which is a common protocol on networkable PC's.

The MARS readout is small and light enough to mount on the MARS-CT gantry. It implements the features required to operate 6 Medipix chips simultaneously:

- supply and monitor high voltage bias (either polarity), and low voltage analog and digital rails

- write the pixel configuration matrix at high speed

- read the pixel counters at a rate of up to 100 Hz from 6 Medipix chips

- set and trigger the shutter time with sub-millisecond resolution up to tens of seconds

- generate pixel test voltages and pulses (or pulse trains)

- perform self-test and reset

The MARS readout is implemented in an Altera^{TM} field programmable gate array (FPGA) in a hybrid of hardware and software. "Hybrid", because the FPGA uses a small proportion of its gates (5%) to act as a "soft CPU" with 32-bit memory. The FPGA also implements controllers for external flash and DDR RAM memory. A third-party software product is used to implement the UDP/IP stack. Third party FPGA code implements the gigabit ethernet MAC (data link) layer.

FPGA logic gates implement time-critical functions such as shift registers and pulse generators. On the other hand, software is used to implement the network protocols and to provide the application programming interface (API) for the external workstation that will eventually receive, store and process the Medipix images. The API includes functions to load Medipix configurations, select shutter times, trigger image acquisition, and stream binary readouts. These functions control 1 to 6 Medipix chips during the CT scanning process. There are also functions to test the Medipix chips, and to measure supply voltages and currents.