INTERFACING SOLAR PANELS WITH A HIGH VOLTAGE ELECTRIC VEHICLE BATTERY BUS

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**TERMS AND ABBREVIATIONS**

*Alphabetic Listing*

**AC** - refers to the components of a current or voltage measurement which have non-zero frequency (see also **DC**)

**Battery** - see **Battery Bus**

**Battery Bus** - i) the expected form of the EEE-EV battery bus is 20 12V batteries in series, with a nominal voltage of 240V. This system is expected to have an internal resistance of under 10Ω. ii) an electronic imitation of the lead-acid form, made for the purposes of this project

**Boost Converter** - a type of DC-DC converter which has a higher DC voltage at the output than at the input (see also **DC-DC converter**)

**Crisp** - refers to a variable that is not fuzzy, but uniquely defined. Crisp variables have Boolean membership of the subset of variables over which they are defined (see "fuzzy").

**DC** - refers to the average value of measurement of a current or voltage. Unless otherwise stated, non zero AC components of the measurement are unwanted or ignored (see **AC**)

**DC-DC converter** - an electronic power device which uses the switching of current through an inductor or transformer to alter the voltage (see also **Boost Converter**)

**Deep Cycle battery** - a battery, usually lead-acid, which is able to be repeatedly fully discharged/charged without degradation (see also **Lead-acid battery** and **SLI battery**)

δ - delta, the duty cycle of a boost converter switch

**EEE-EV** - the Austin Farina-based Electric Vehicle belonging to the Electrical and Electronic Engineering Department of Canterbury University

**EMI** - electro-magnetic interference - radiated or conducted noise that can affect the performance of the device(s) that produced the noise or other devices.
First stage - refers to one or all of the three DC-DC converters which take their input from one solar panel and output to a common intermediate point (see also Second stage, DC-DC converter and Intermediate point)

Fuzzy - refers to a parameter that has a variable degree of membership of a subset - opposite of "crisp".

Intermediate point - the part of the Panels to Battery Bus Interface formed by the common connection of the first stage outputs and the second stage input (see First stage, Second stage, Panels, Battery Bus and Interface)

Interface - the hardware and software which allowed the electrical energy from the Panels to be taken up by the Battery Bus. Includes the first and second stage boost converters, their interconnections and power maximising control system (see First stage, Second stage, Panels, Battery Bus, and Power Maximisation)

Irradiance - measure of incident photon energy density (S); has SI units of W.m\(^{-2}\)

I/V characteristic - current-voltage characteristic, particularly that of a solar panel

I(V(S,T)) - PV panel current as a function of PV panel voltage (see V(S,T))

I(V(S,T))\(_{\text{max}}\) - the PV panel current when the PV panel voltage is such that the PV panel output power is maximised (see V(S,T)\(_{\text{max}}\))

Lead-acid battery - an electrical battery made up of lead/lead sulphate cells, each with a nominal voltage of 2V. A common form has 6 cells in series, hence the term "12V battery" (see also SLI battery)

NZDST -- New Zealand Daylight Saving Time

Panels - refers to the group of three PV panels used for this project - 2 by 63W modules and 1 by 45W module (see PV panel)

Polycrystalline - a form of extremely pure silicon which exists as groups of large crystals. Widely used in high performance PV panels. (see PV panel)

PV panel - photovoltaic panel also known as solar panel

R\(_L\) - the series resistance in a component designed to be an inductor

R\(_{\text{on}}\) - i) the on-resistance of a MOSFET switch ii) the on-resistance of the paralleled MOSFETs of the boost converters used in this project, approximately
equal to the resistance of a single MOSFET divided by the number of near-identical MOSFETs in parallel.

S - symbol for irradiance (see Irradiance)

Second stage - the DC-DC converter which has as its input the Intermediate point. Its output is connected to the Battery Bus. (see First stage, DC-DC converter, Intermediate point, and Battery Bus)

SLI battery - Starting, Lighting and Ignition battery - a type of 12V lead-acid battery which is specialised for short bursts of high current drain. Commonly used in automotive applications (see also Lead-acid battery and Deep Cycle battery)

T - temperature, in units of Centigrade (°C)

V(S,T) - PV panel voltage as a function of irradiance and temperature (see Irradiance and T)

V(S,T)_{max} - the PV panel voltage for a particular irradiance and temperature at which the PV panel output power is maximised (see also I(V(S,T))_{max})
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Introduction

Sunlight irradiates the surface of the Earth with a maximum intensity of about 1000W.m\(^{-2}\). Use of this renewable energy source can reduce the demand on other renewable and non-renewable energy sources. This project is concerned primarily with using solar power to supplement the power supply of the Austin Farina-based electric vehicle in the Department of Electrical and Electronic Engineering of Canterbury University (EEE-EV) [Williams 1993]. However, the project has far more general application. Solar power is useful in situations where other forms of energy supply are expensive, distant or unreliable - such as remote sensing stations - and in situations where sunlight is the most appropriate power source [Dunn 1986].

Photovoltaic (PV) Panels

PV panels presently provide the most direct means of converting sunlight into electrical power. Common photovoltaic cells (the building block of PV panels) are composed of alloys of bilayer silicon with variable levels of doping by semiconductors and/or metallic elements. They operate as reverse biased diodes, that is diodes in which minority carriers formed by the photoelectric effect are driven across the pn-junction by the junction field, producing a photocurrent [Zweibel 1990]. The typical maximum efficiency of these common devices (based on available energy as a fraction of the photon energy incident on the active surface of the panel) is about 14%. This definition of energy efficiency gives an overestimate of the efficiency of multi-cell panels, which require passive electrical and structural components to be part of the total area, and when reading PV panel datasheets it is important to check the practical panel efficiency. Other forms of PV panels with higher efficiencies and lower costs per peak watt output are currently the subject of research activity [Zweibel 1990]. Single junction silicon cells with band gaps between 0.9 and 1.8eV are limited to (active area) efficiencies of less than 30%, but multilayer cells that allow absorption of photon energy from a wider spectral range are theoretically capable of up to 70% active area efficiency, and may eventually be technologically feasible. Boeing Aerospace have already developed a 34% active area efficient cell [Zweibel 1990]. Techniques such as silicon wafering, thin film panels and incorporation of frameless panel units into building structures are a feature of German PV research. The German researchers also favour manufacturing methods with few steps, and are attempting to produce panels in a way which causes less stress to the environment [Bundesverband Solarenergie 1992]. Until new cheap and efficient designs are developed economics may dictate that simpler cell designs remain prominent, as panel costs remain the barrier to the widespread introduction of PV technology to the marketplace [Zweibel 1990]. As
devices that convert sunlight energy directly to electrical energy become cheaper to manufacture (costs per peak watt output), their usage will increase [Zweibel 1990]. The most recent development in solar-electric devices is a novel form of polarising films [Haber 1993]. Speculative initial research has found photon to electric energy efficiency of up to 80%, with relatively low projected production costs, but this has so far been restricted to microwave frequencies, which contain a very small proportion of the energy in sunlight. Other long-term research goals are more modest, but surer to be of benefit. Plans for decentralisation of electricity generation systems, including the installation of large scale photovoltaic arrays, integration of building techniques with PV panel technology and concerted research effort over the full range of PV technology from cells through to batteries are features of German research [Bundesverband Solarenergie 1992].

A PV panel has an I/V characteristic which is dependent upon irradiance and temperature. The characteristics are such that there is a unique voltage $V(S,T)_{\text{max}}$, where $S$ is irradiance ($\text{W.m}^{-2}$), $T$ is temperature (K) at which $V(S,T)^*I(V(S,T))$, the DC power, is maximised. This voltage is defined to be the "maximum power voltage". In order to get the maximum available panel output power, the panel must be forced to operate at the maximum power DC voltage by the use of additional components. In a general case, where multiple non-identical panels are placed such that they are subject to different irradiation and temperatures, $V(S,T)_{\text{max}}$ can vary between panels. As we seek the maximum power output from all panel groups, irrespective of their irradiance, direct parallel electrical connection of the panels' output is not possible, even if the panels are identical in composition.

**The placement of PV panels on the EEE-EV**

The approach taken in this project was to split the total available panel area into separate units, where the panels may be in different light intensity zones, but individual panels are evenly irradiated. This allows the panels to be placed according to the available area on the car (for example, see fig 1.1), as well as orientation to incident sunlight. This approach will be useful in other applications where the placement of panels in series electrical, spatially parallel groups is not possible.

**The EEE-EV battery and interface to the PV panels**

The EEE-EV has a lead-acid battery energy storage system with a nominal voltage of 240V. This provides a means of storing sunlight energy, which is variable in supply, but forces the design to be aimed at transforming photon energy into electrochemical storage, at a voltage dictated by the battery charge and its loading.
The high battery voltage is advantageous in that conduction losses for a given load or charge current are reduced. However, converting from the low-voltage and high current power output of solar panels requires a voltage-boosting interface. This project attempts to generalise the form of the interface so that the boosting is done in more than one stage (see fig 1.2). The reasons for choosing this type of interface for boosting to 250V are given in §1.3.

Fig 1.1 Placement of PV panels on the EEE-EV

Plan View of the Austin Farina

Bonnet

LA321K45 PV Panel (aka LA-45) 45W rating
445mm

Windscreen

LA441K63 aka LA-63 PV Panel - 63W rating
880mm

Roof

LA-63 PV Panel
All the panels must be able to withstand hail
445mm

1195mm

Side View of the Austin Farina

The PV Panels cannot easily be secured in a spatially parallel arrangement, but similar inclination allows the vehicle to be parked such that all the PV Panels are facing the sun

The two LA-63 panels may be skewed slightly to allow best fit to the curvature of the roof. Some form of moulding, perhaps by fibreglass, will be necessary to maintain vehicle aerodynamics and secure the panels to the bodywork

The basic requirements are:
i) one “first-stage” booster per panel (group of cells), which each regulate their separate input (panel) voltages. All the first stage boosters output to a common point.

ii) If the first-stage units are not capable of boosting to the battery bus voltage efficiently, further booster unit(s) in series are required. Booster units beyond stage 1 are referred to as “second stage” units.
In this project, two identical solar panels, and third smaller panel, were used (shown in fig 1.1 - see also App. A). They all had $V(S,T)_{max} < 20V$ in normal sunlight conditions. Therefore three first-stage units and a second stage unit to boost the common first-stage output to the battery bus were used. Extension to a system where there are more panel units (requiring additional first stage units) and a higher battery bus voltage (requiring further second stage units in series) follows readily. It is important to note that the interface is designed to maximise the uptake of solar power, whatever the irradiance, and efficiently convert it to electrochemical energy in a battery. If the irradiance was constant at its maximum level, the interface could be simplified to cope only with this circumstance. This project aims to make use of the available solar power in situations where the irradiance is low and/or variable. The design must therefore be aimed at efficient performance at low irradiance, without sacrifice of high irradiance performance, with an ability to respond to changes in irradiance.
CHAPTER 1. PRINCIPLES

§1.1 Aim of the Project

The project aim is to make an interface between photovoltaic (PV) panels and a battery bus. The interface must allow the maximum conversion of available photovoltaic energy into electrochemical energy, by forcing the panels to convert light energy into electrical energy efficiently and simultaneously efficiently delivering that energy to the EEE-EV battery bus.

§1.2 Solar Panels and Batteries

Photovoltaic panels are based on arrays of semiconductor photodiodes which are in series and/or parallel connection. The interconnection of the discrete photodiodes means that the power output of the array is limited by the least irradiated series unit. We can choose a panel size and placement such that all the active surface of the panel is evenly irradiated, but this limits the maximum size of the panels and is not always possible, especially on a fast moving vehicle. For a panel of \( N_s \) identical cells in series and \( N_p \) identical cells in parallel (see fig 1.3), the panel voltage, current and power can be analytically derived:

\[
V_s = \frac{AKT}{q} \ln\left[\frac{(KS - \beta I_s - I_0)}{I_0}\right] - I_s R_s \quad \text{eq 1.1 and}
\]

\[
I_{pv} = I_s N_p
\]

\[
V_{pv} = V_s N_s \quad V_{ext} = V_{pv} - I_{pv} R_{ext}
\]

where \( V_s \) and \( I_s \) are cell voltage/current, \( R_s \) is the cell internal resistance, \( k \) is Boltzman's constant, \( T \) is the absolute temperature, \( q \) is the charge of an electron, \( S \) is the irradiance (W.cm\(^{-2}\)) \( K = 0.56A.W^{-1}.cm^2 \), \( A \) is a scalar between 1 and 3, \( I_0 \) is the reverse saturation current and \( \beta \) is a constant (Hilloowala 1992, Rauschenbach 1980).

The available power (\( P_{ext} = V_{ext} I_{pv} \)) is diminished by losses in external resistances, lumped as \( R_{ext} \) in fig 1.2. This becomes important when \( R_{ext} \) is large, and/or is significant before the point where the panel voltage is monitored (eg cables to the rest of the interface). See §2.1.2.8 for details.
In the figures on pages 9-14 we can see I/V and P/V characteristics for the Kyocera photovoltaic modules that were used for the purposes of this project; one of model LA-45 (45W output rating) and two of model LA-63 (63W output rating). These panels are composed of polycrystalline silicon cells in series. The ambient temperature at the time of measurement was 25°C, but the temperature of the panel active surfaces was estimated to be 35°C due to the intensity of the sunlight at the time. The light intensity was estimated by a phototransistor-meter, previously calibrated according to readings from the lightmeter in the Geography Department. (see fig 1.4 and App. A)

A major source of error for the calibrated and calibrating meters was differing spectral content in the sunlight. The meters underestimated the energy available to the panels under cloudy to overcast conditions due to the low meter sensitivity to wavelengths shorter than 500nm and overestimated available sunlight energy when the sun was far from the zenith, due to lower photovoltaic efficiency in predominantly longer wavelength light (see App. A). Thus, calibration and measurement were done in similar, sunny conditions, between 1130 and 1300hrs (NZDST), with only small light level and spectral content variance during the time of the measurements. The meter was placed so that it measured the component of irradiance perpendicular to the panel surface. Since the purpose of the measurement was to determine the shape of the characteristics, rather than get a family of curves for different light levels, the panels were oriented so that a moderate effective irradiance of between 750-850W.m⁻² was applied to them.
Fig 1.4 calibration for irradiance meter, based on work using the Geography Dept. meter as a standard (see App. C for details)

Solar Irradiance
vs. Meter Illuminance Reading

\[ y = 14.502x + 66.418, \quad r^2 = .988 \]

The panel characteristics in figs 1.7a/b/c and 1.8a/b/c show relevant features of solar panels. The first figure (fig1.5) shows the manufacturer's data for the LA-45 and LA-63 models. The I/V characteristics in fig 1.5 are parameterised by irradiance and temperature. See App. A for details of the manufacturer's data sheets.
Fig 1.5  Electrical characteristics of the LA-45 and LA-63 panels, supplied by Kyocera. N.B. 100mW/cm² = 1000W.m⁻².

I-V characteristic of solar module LA441K63 at various cell temperature and irradiance levels.

I-V characteristic of solar module LA321K45 at various cell temperature and irradiance levels.

Fig 1.6  Example panel characteristics parameterised by irradiance

Figs 1.7a, 1.7b and 1.7c show the I/V characteristics from data collected by the author. The measured open circuit voltages for the two LA-63 panels are near identical at 25V and the smaller (less series units) panel has an open circuit voltage of 17V. The panel voltage drops with decreased load resistance, but the panel
current is limited by the increased temperature of the active units. Note that the testing was consistently done by reducing load resistance/increasing panel current thereby consistently giving higher temperature panels toward the end of each trial. Figs 1.8a, 1.8b, 1.8c show reduced scale versions of the I/V characteristics and full-scale P/V characteristics. The curve-fit to the P/V traces consistently underestimate the maximum power voltage. The peak of the P/V characteristic is almost symmetrical about the maximum power voltage, with a slightly steeper slope on the high voltage side. This indicates that a control system based on altering the panel voltage by discrete steps can be simplified by symmetry. Furthermore, the sharp (with respect to voltage) peaks of the P/V characteristic and the narrow (with respect to voltage) maximum power locus (fig 1.6) mean that the panel voltage need only be altered through a narrow range For example, the changes will be in steps of no more than 1V for response to 50% changes in irradiance.

A control system used for maximum power tracking was developed by Hilloowala and Sharaf [Hilloowala and Sharaf 1992]. Their system compares the power output of a panel with an estimate of the maximum available power as a quadratic function of the irradiance. This gives the control system a reference power to seek, but the reference does not take account of the variance of maximum power voltage with temperature. Also, the interface to the battery will have an efficiency which is a function of panel voltages that is not easy to analyse. This project aims to develop a control system that does not refer to assumed maximum values of panel power output, but seeks to maximise power delivery to the battery bus. This type of control system is quickly adaptable to different panels and interface forms.
Fig 1.7a  I/V characteristic developed from data collected 11 December 1992 for the LA-63 panel which was eventually connected to Stage 1a.

Characteristic of Panel with zero Stripes

Irradiance = (770 +/- 30) W/m²
(lower for lower voltage results)

$$y = -1.13 + .551x - .023x^2$$

Panel Current (amps)
Fig 1.7b  I/V characteristic developed from data collected 11/92 for the LA-63 panel which was eventually connected to Stage1b.

Panel Characteristic for the single stripe panel (LA63)
Irradiance = (790 ± 20) W/m²

Panel Current (A)
Panel Voltage (V)
Fig 1.7c  I/V characteristic developed from data collected 11/92 for the LA-45 panel which was eventually connected to Stage1c.

Panel characteristic for the small panel (LA45)
Irradiance was 790W/m² at first
and rise to 834W/m² for the lower voltage measurements

O Panel Current (A)

Panel Voltage (V)

\[ y = 6.49 + 0.433x - 0.01x^2 + 0.001x^3 \]
Fig 1.8a  P/V and I/V characteristics developed from data collected 11/92 for the LA-63 panel which was eventually connected to Stage1a.

Power and Current Vs. Voltage for the Panel with Zero Stripes (LA63)

Irradiance = 770W/m²

- □ Panel Power (W)
- △ Panel Current (I)

Panel Voltage

Panel Power
Fig 1.8b  P/V and I/V characteristics developed from data collected 11/92 for the LA-63 panel which was eventually connected to Stage1b.

Panel Characteristic for the single stripe panel (LA63)
Irradiance = 790 +/- 20 W/m²

- ○ Panel Current (A)
- □ Panel Power (W)
Fig 1.8c  P/V and I/V characteristics developed from data collected 11/92 for the LA-45 panel which was eventually connected to Stage1c.
The battery bus of the EEE-EV is composed of 20 series-connected nominal 12V lead-acid SLI batteries (hereafter known as the battery). As these were not purchased during the time of the project, some estimation of their properties follows. If the unit electrochemical cells are in good health, the battery will have a full-charge open circuit (or nil net current) voltage of $20 \times 6 \times 2 = 240$V. The internal resistance of the battery is a non-constant function of the charge/discharge current and state of charge and this results in a V/I characteristic for a near-full charge battery as shown in fig 1.9. The largest internal resistance that could be expected in a better than decrepit battery was estimated to be about 10Ω.

Fig 1.9 The Battery Voltage at near full charge as a function of net charge/discharge

The actual voltage of the bus varies according to loading and state of charge from 180V at minimum recoverable charge to over 350V during regenerative braking [Williams 1993]. The spectrum of battery voltage variation covers the range of less than 10V.hr$^{-1}$ for normal charge and discharge rates to 50V.s$^{-1}$ (up to 100V total change) during regenerative braking or sharp changes in acceleration. Furthermore, there is noise on the bus, with a MHz power spectrum and uncertain amplitude, due to power switching of the EEE-EV motor. This voltage variation places a strain on the stability of the interface between the PV panels and the battery bus.
The total nominal power from the PV panels is (63+63+45)W=171W. At 240V this amounts to less than 0.71A of charging current, a value that is insignificant compared to battery current flows due to the EEE-EV motor power supply. Thus the battery voltage will not be immediately significantly altered by changes in the power output from the solar panel interface. If standard SLI units are employed, the capacity of the battery will be 8000Whrs, equivalent to 33A.hrs at 240V. The solar powered charger will take 47 hours to fully charge such a battery in ideal conditions, which means 4 days of 12 hours of sunshine at best. More realistically, allowance for clouds and other forms of shade, imperfect panel orientation, and interface inefficiency reduce the likely daily captured solar energy to 500Whrs per day. In other words, it would take about 16 days to fully charge the battery from low charge if no other form of charging was used. It appears that the solar charging system is not appropriate as a primary charging source for this particular vehicle in a Canterbury climate. However, more suitable vehicles (lighter, with more efficient motor(s)) or devices rated <500Whrs in areas far from national grid connection that have reliable sunshine would be able to be economically powered by the solar charger. An all-terrain EV produced by Heron Industries for Electricorp NZ has been bequeathed to EEE for testing and this is a more useful product for application of this project.

§1.3 Selected Method - Boost Conversion

This project assumes that the means of capturing sunlight energy will be photovoltaic panels, rather than means such as water heating or other forms of photochemistry. The interface therefore has a DC input and output, within the limits described in §1.2. The known means of interfacing two different DC voltages are numerous [Rashid], but in this case we are restricted to finding an efficient means of changing from a low voltage/high current to high voltage/low current - boosting. A simple hardswitched boost DC-DC converter [Rashid] was considered. Boost converters can operate in two distinct modes: continuous inductor current, or discontinuous inductor current. Continuous current mode was selected for this project, for reasons given in §2.1.2.3 and §2.4. If power output maximisation is required the input (panel) voltages must be regulated by the converter using some form of feed-forward control. This is so that the panel maximum power voltage can be tracked by appropriate variation of the input voltage set-point.

Fig 1.10 shows such a converter which can act as the interface between a solar panel group and the battery bus. Diode $d_{\text{out}}$ is essential in this configuration as the voltage at its anode is close to ground when the switch is closed. Diode $d_{\text{in}}$ is not
essential in a boost configuration, but protects the panel from possible faults where the battery, or some other high voltage source would otherwise destructively reverse the panel current.

![Diagram of a boost configuration](image)

A simple boost configuration. $V_{d_{out}}$ and $V_{d_{in}}$ are forward bias diode conduction voltages. Three of these units output to a fourth (without solar panel) which has its output connected to the Battery.

Given that $\delta$ is the duty cycle of the switch, we can derive the DC (average) relation:

$$V_{out} = \frac{(V_{in} - V_{d_{in}})}{(1-\delta)} - V_{d_{out}} \quad \text{eq.1.2}$$

This neglects switching losses, which arise from the finite switching time of real semiconductor switches. A design compromise for switching frequency is necessary because the switching losses are proportional to switching frequency ($f_{s}$) and required inductor size decreases with approximately the square root of the switching frequency [Billings]. Conduction losses from the inductor resistance ($R_{L}$) and switch on-resistance ($R_{on}$) also decrease the output power. Since we wish to boost from $<20V$ to about $250V$, the duty cycle of a single stage booster will be about $0.92$. If the turn-off time of the switch is large enough to be comparable to $0.08f_{s}$ the switching losses will be prohibitive.

A single-stage boost converter will be too lossy to be useful, at least for currently available semiconductor switches, or too large and expensive to be economical.

Hardswitched boost converters can be cascaded. As described in the thesis introduction, one first stage converter per panel is required, so that independent panel voltage regulation can occur, but all of the "first-stage" converters can output to the input of a single "second stage" unit, which regulates the output voltage of all
of the first stages simultaneously. In this case there are 3 panels, so a total of 4 converters will suffice (see fig 1.11).

In the system shown in fig 1.11 the aim is still maximisation of the charging power. The factors relevant to this criterion are: the power output from each panel, the efficiency of the first stage converters and the efficiency of the second stage converter. Converter efficiency decreases with the boost ratio and input current, so in the most efficient state, each panel voltage will be above that which would give maximum panel output power. The voltage of the first stage outputs (input of the second stage), which is designated as the intermediate voltage \( V_{int} \), is critical to the balance of first and second stage efficiency. If it is too low, the improved first stage efficiency will be negated by the stress on the second stage; too high and the second stage is underutilised, causing the first stages to boost too far to be efficient.

Formalising these concepts gives the following relation:

\[
P_{out} = \eta_2 (P_a \eta_{1a} + P_b \eta_{1b} + P_c \eta_{1c}) \quad \text{eq 1.3}
\]

where \( P_{out} \) is the battery charging power, \( P_{a/b/c} \) are the respective panel output powers, \( \eta_{1a/b/c} \) are the respective first stage efficiencies and \( \eta_2 \) is the second stage efficiency. Note that the RHS variables are interdependent, for example:

\[
\eta_2 = \eta_2 (\delta_2, \ I_{int}) \quad \text{eq 1.4}
\]

where \( I_{int} \) is also a multidependent function:

\[
I_{int} = I_{int} (P_{a/b/c}, \delta_{1a/b/c}, \eta_{1a/b/c}) \quad \text{eq 1.5}
\]
It is therefore very difficult to form an analytical solution to the form of a control algorithm that maximises power output to the battery for this system.

A method not considered during the early stages of the project was to use a transformer, rather than inductor based voltage booster. The system does not require the isolation of a transformer.

§1.4 Possible Control Strategies

The aim of the interface is to maximise power transfer from the PV panels to the batteries, in spite of varying light levels and temperature. This aim requires a control system that determines the duty cycles of the boost converter switches.

The switch duty cycles are determined by the output levels of the respective SG-3526 error amplifiers (see App. B). Thus, the configuration of inputs to the error amplifiers are central to any control system. Analogue positive feed-forward (+FF) of the input voltage to the error amplifiers allows the input voltage of each converter to be regulated, so long as the output voltage is fixed. The error amplifier gain (see fig 1.12) is set by the feedback ratio:-

where \( V_{\text{in/t}} \) is the converter input voltage (either a panel voltage \( V_{a/b/c} \) or the intermediate voltage \( I_{\text{int}} \)) and \( V_{\text{EAout}} \) is the error amplifier output voltage.

\[
V_{\text{EAout}} = V_{\text{in/t}} (1 + \frac{Z_2}{Z_1}) \quad \text{eq 1.6}
\]

Fig 1.12 Left: the schematic of the +FF for a converter; right: the error amplifier general configuration
Refer to fig 1.12 for the following discussion. The shunt capacitance $C_s$ is used to stabilise the output of the error amplifier which is of the transconductance type (see App. B). The inverting input is connected to a stable reference voltage - either ground or a voltage derived from the on-chip 5V reference - via $Z_1$. If the gain is set high then the inverting and non-inverting inputs must be similar values. This can be arranged by coarse adjustment of the divider to the non-inverting input or by changing $V_{ref}$, by voltage division if necessary. High gain in the error amplifier increases susceptibility to EMI, which causes the error amplifier output to become unstable. See §2.4 for the result of analogue positive feed-forward implementation and error amplifier instability.

If the analogue positive feed-forward is replaced with a 0-5V microprocessor ($\mu$P) output (see fig 1.13), the error amplifier can be operated as a unity gain buffer, with the reference voltage set to 0V. A leakage path to ground from a point close to the error amplifier input reduces the noise that would otherwise appear on the high error amplifier input impedance. Chapter 3 discusses the implementation and results of $\mu$P control.

Fig 1.13 on the left is the schematic of the $\mu$P control of a converter, and on the right is the error amplifier configuration for a $\mu$P controlled Interface
CHAPTER 2  HARDWARE

§2.1 Choice and Design of Components

§2.1.1 Introduction

Having decided to build four separate converters, three to interface to the solar panels and one to interface with the battery bus, the challenge was to realise the panel/battery bus interface in reliable hardware. The basic circuit diagram is shown in fig 2.1.

Fig 2.1. The 2-stage boost configuration complex. $V_{d_{out}}$ and $V_{d_{in}}$ are forward bias diode conduction voltages. See also figs 1.2, 1.10 and 1.11.
§2.1.2 Component Specification

This section lists the circuit components, their required specifications and the specifications of the component actually used. Refer to fig 2.1 and App. B:

§2.1.2.1 Input diode $D_{in}$ for panel protection

This must have a very low forward-bias voltage at currents of up to 3A to minimise power loss, be rated at well above 3A for cases of panel short circuit, and have a high reverse breakdown voltage for panel protection. An MBR10-100 Schottky diode (TO-220 package) rated at 10A/100V with a 3A forward current voltage of $<$0.6V at $T_j = 25^\circ C$ was used for all three panels, soldered in place at the weather proof junction box attached to each panel. Note that this component is not required for the second stage.

§2.1.2.2 $C_{in}$, the input capacitance for each converter and $C_{out}$, the output capacitance of each stage

If the difference between the actual panel voltage and the maximum power voltage is less than 100mV then the loss in power is less than 10% (see PV characteristics figs 1.7a/b/c and 1.8a/b/c). Taking $f_s$ as the switching frequency (Hz), $\Delta V_{in}$ as the voltage ripple on the capacitor (which will be closely followed on the panel, or common output of the first stages for $C_{in2}$) and $I_{in}$ as the input current to a converter then the general equation $C = \frac{\Delta I_{in}}{I_{in}}$ can be adapted to a worst case situation where the duty cycle is close to one and the converter operation borders on discontinuous inductor current ($\Delta I_{in} = I_{in}$).

$$\Delta V_{in} = \frac{I_{in}}{C_{in} f_s} \quad \text{eq 2.1}$$

If, for a high input current of 3A and a low switching frequency of 20kHz a panel voltage ripple of $<$ 50mV about the max-power voltage is required, a capacitance of at least 3000$\mu$F is necessary. If the switching frequency is increased to $>$30kHz and the ripple conditions for the panels are relaxed to 100mV, then $C_{in} = 1000$,$\mu$F with a high $R_p$ (see fig 2.2) is the best choice. A low-loss input capacitor (see fig 2.2) would have a small $R_s$ so that the losses due to ripple currents are minimal, small $L_s$ so that the self-resonant frequency is high and a large $R_p$ so that leakage losses are low. The capacitors must have a breakdown voltage much greater than 25V (for the first stages) or 250V for the second stage. This is because:

a) the solar panels have maximum open-circuit voltages of $<$25V.

b) the intermediate voltage will not usually climb above 100V, but there can be large
amplitude voltage spikes due to the power switching of both the first and second stages. A possible fault condition, where the intermediate voltage rises to meet the battery bus, requires that the capacitors be rated to the battery bus voltage. No allowance for voltage spikes should be necessary, as the relevant fault condition is likely to coincide with low power transfer.

![Fig 2.2 Lossy high frequency model of a capacitor](image)

It is possible for the real capacitor to self-resonate at: \( \omega_r = \frac{1}{\sqrt{L C}} \) and other resonances may exist when the real capacitor interacts with the reactive components, particularly the boost inductor, in the circuit. Self resonance can cause instability of input voltage regulation and is to be avoided.

The capacitors selected for the first stage inputs (1a and 1b) from the LA-63 panels were 2x 1000\( \mu \)F/35V SXE electrolytic capacitors, the LA-45 1c converter required only one SXE type. These have a low series resistance and were preferred to high \( R_p \) tantalums due to their much greater capacitance density and tolerance of high frequency ripple. Finding suitable capacitors for the intermediate point was more challenging, due to the increased voltage rating. Maximum ripple at the intermediate voltage is limited only by its effect on the stability of the converter operation, so less capacitance is required than at the input of the first stages. The method used to determine the least lossy capacitor bank was to add discrete capacitors until stable operation was achieved, then add a few surplus units to lower the effective \( R_s \) of the bank. Note that the input capacitance of the second stage is in parallel with the output capacitance of the first stages.

The capacitors were arranged as follows:
2x 33\( \mu \)F/250V Rubycon units on the output of each first stage, 1x 68\( \mu \)F/250V Philips unit on second stage board and a vero board group of 2x 22\( \mu \)F/385V Philips and 2x 33\( \mu \)F/250V Rubycon units attached by 0.15m leads to the output of the stage 1c converter.
The output capacitors for the interface were chosen mainly on the basis of voltage rating, and paralleled to reduce $R_g$. Two Philips 385V/47μF were used for voltage ripple reduction. The problem of back-feeding of bus noise was dealt with by adding an additional 140pF/8kV ceramic disc capacitor in parallel to the bypass units. Higher voltage rated bypass units would be more reliable, but their size would be a problem. The high frequency and/or amplitude spikes on the bus are absorbed preferentially by the 8kV ceramic, lowering stress on the bypass units.

### §2.1.2.3 The Boost Inductance

There is a design compromise. Lowering the input voltage ripple can be achieved by increasing either the input capacitance or the boost inductance. It is easier and cheaper to use a large capacitance and the input capacitances were designed to cope with the maximum possible current ripple in a maximum current situation. However, if the input current is too low, the current through the inductor will become discontinuous unless the inductance is overrated. Discontinuous current mode (DCM) is more likely to occur for a given inductance if the switching frequency is low. DCM is a problem because of the resonance in the switch voltage, which is lossy and has a destabilising effect on the converter(s) concerned. See §2.4 for details. For now, it is assumed that if the panel output is so low that $<0.5\text{A} (<10\text{W} \text{at an estimate of the relevant max power voltage})$ is delivered to any first stage or $<0.25\text{A} (<20\text{W} \text{at an intermediate voltage of 80V})$ to the second stage, then it is possible to ignore occasional DCM as the resultant loss in output to the battery will be low anyway. This forms the lower limit to this project's attempt to utilise low irradiance sunlight. Thus, the current ripple must be limited to 1A for the first stage boost inductors and 0.5A for the second stage inductor. Taking $V_{in}$ as the input voltage, $V_o$ as the output voltage, $f_s$ as the switching frequency and $\Delta I_{in}$ as the acceptable ripple we can derive an equation for the minimum boost inductance:

\[
L \geq \frac{V_{in}(V_o - V_{in})}{f_s \Delta I_{in} V_o} = \frac{\delta V_{in}}{f_s \Delta I_{in}} \quad \text{eq 2.2}
\]

If $f_s = 30\text{kHz}$, and for the first stages the input/output voltages are 15V/60V ($\delta = 0.75$) then a boost inductance of at least 375μH is required for the first stage inductors, and some excess would be useful for the lower current stage attached to the LA-45 panel. For the second stage the input/output voltages were estimated to be 60V/250V ($\delta = 0.76$) and the minimum second stage inductance is 3040μH. Upper limits to the inductance are the size/cost of the device, the resistance of the coil, and flux saturation of the inductor core. If cores as small as ETD-39 for all the
stages, then the second stage inductance has to be decreased to avoid core saturation. If the current ripple limits are to be maintained, the switching frequency of the second stage must be increased to 40kHz and the required inductance drops to 2280\(\mu\)H.

The inductors were made from ETD-39 formers with Siemens N-27 ferrite cores [Siemens Ferrites and Accessories databook 1990/91]. An important design criterion was low resistance, at frequencies from DC up to 100kHz which will cover the fundamental of the switching frequency (~30kHz) and its lower harmonics, when the skin effect becomes significant. The skin-depth can be determined for copper wire using a rule of thumb [Laird 1992]:-

\[
\text{Skin depth (mm)} = \frac{66.1}{\sqrt{f_s}} \quad \text{eq 2.3}
\]

at 100kHz the skin depth (SD)=0.21mm

Thus there is little point in using copper wire with a diameter of >0.42mm. The current carrying cross-sectional area \((A_c)\) will still increase with \(r = \text{wire radius}\):

\[
A_c = \pi \text{SD}(2r - \text{SD})
\]

but the wasted area of copper beneath the skin depth increases with wire radius as:

\[
A_{\text{wc}} = \pi (r - \text{SD})^2
\]

so that the ratio of useful to wasted copper decreases with \(r\):

\[
\frac{A_c}{A_{\text{wc}}} = \frac{\text{SD}(2r - \text{SD})}{(r - \text{SD})^2} \quad \text{eq 2.4}
\]

In order to meet the dual requirements of low series resistance and small former size multistranded wire of diameter <0.42mm was used. The theory detailed above applies to a single strand not in close contact with any others. The effective skin depth for multistranded cable is lower than for the single stranded case, by an amount dependent upon the geometry [Billings].

For an inductance \(L\) and a peak current \(I_p\) (which is the peak current through the inductor) the maximum magnetic energy stored in an inductor is \(\frac{1}{2}LI_p^2\). In order for a core to remain unsaturated, the number of turns must be restricted and/or a low-permeability gap must be introduced to the flux path. If it is assumed that the flux
gap has a permeability much lower than that of the ferrite core - valid if the gap is composed of air or plastic - then the total gap length \( d_g \) can be related to the maximum magnetic energy \( (L_0^2) \) by the following formula:

\[
d_g = \frac{0.4\pi}{A_c B_m^2} L_0^2
\]

\[\text{eq 2.5 [Siemens Ferrite databook 1991]}\]

where for an ETD-39 core and N27 ferrite, the coil area \( (A_c) \) is at least \( 125 \times 10^{-6} \) m\(^2\) and the saturation field for the ferrite core \( (B_m) \) is 0.35T.

The value of the inductance \( (L) \), which has already been determined from the current ripple requirements, can be related to the required number of coil turns \( (L) \) by the formula:

\[
N = \sqrt[2]{\frac{L}{A_L}}
\]

\[\text{eq 2.6 [Siemens Ferrite databook 1991]}\]

Where \( A_L \) is unit inductance ie the single turn inductance, a decreasing function of the gap length and core material/geometry. For example, in the ETD-39/N27 combination if \( d_g = 0.5 \text{mm} \) then \( A_L = 0.325\mu\text{H} \), \( I_o = 3\text{A} \) (an overestimate since the average output current from a converter is unlikely to exceed 1A and the current ripple is aimed at being less than 1A) and if \( d_g = 1 \text{mm} \) then \( A_L = 0.195\mu\text{H} \). Using eq 2.5 with the required inductance we can determine a minimum gap needed to avoid saturation and then use eq 2.6 to determine the required number of turns.

5-stranded 0.45mm diameter enamel-coated wire was used for winding onto the inductor formers. The 5 strands were loosely twisted together and wound as a unit onto the formers. One former was wound with 55 turns, which gave a measured (Philips PM6303 meter) inductance of 848\mu\text{H} with no gap. Two formers were wound with 51 turns, giving 752/730\mu\text{H}, again ungapped. The fourth former was intended for use in the second stage and the maximum number of turns that could be fitted on the former were wound - 92 in all, giving an ungapped inductance of 2410\mu\text{H}.

The ungapped values represent the upper limit of the inductance available from the window area (see fig 2.3).

Gapping was applied to reduce the inductance to the minimum required values, so as to maximise the possible saturation current. This gives a margin for reduction of the gapping if ripple reduction of lower than expected average currents is required, rather than saturation avoidance at higher than expected average currents.
The gapping was achieved by insertion of 2 equally thick plastic strips between the outer limbs of the E-cores. Note that for a strip of thickness d, the total gap length \(d_g = 2d\) (see fig 2.3b).

With retrospective knowledge of the low output from the LA-45, it would have been more sensible to install inductor #1 on stage1c, but the current ripple through the inductor on stage1c can be reduced by increasing the switching frequency, or decreasing the gapping. This problem was exacerbated by the fact that the intermediate voltage between the 2 stages stabilised at about 90V, increasing the first stage \(v_s\) (at 30kHz) to 0.83 from 0.75. Use of eq 2.2) implies that inductance required to keep the ripple below 1A is 417\(\mu F\). The second stage duty cycle drops to 0.64 (at 40kHz), but the input voltage increases to ~90V. This changes the required \(<1A\) ripple inductance to 2830\(\mu F\).

It can be concluded that the ETD-39 package is too small for the second stage inductor. Since the inductor was not easy to remake using larger cores (eg ETD-44) a compromise is necessary. DCM loss that restricts the usefulness of the interface
at low irradiances can be accepted, or the second stage switching frequency can be increased to avoid DCM but incur greater switching losses, or the gapping on the second stage inductor can be decreased, reducing the safety margin for flux saturation. The result of making changes to the gapping and switching frequencies is explored in §2.4. In chapter three, it is shown that the intermediate voltage tends to climb above 100V, in which case the second stage inductor can be adequately formed by an ETD-39 core.

When it was noticed that switching noise was being broadcast/received by the inductor coils, a brass shield was wrapped around each coil. The overlapping edges were taped to prevent the formation of a shorted secondary path. A direct connection from the shield to the ground plane of the PCB under the inductor was soldered into place, so that the shield would assist in noise suppression.

§2.1.2.4 The Boost Switch

Requirements:

a) a low on-resistance
b) a high off-resistance
c) high-speed of switching between the on and off states, so that switching at up to 40kHz does not cause gross switching losses.
d) low power consumption in the control signal
e) an easy means of attachment to a PCB and heatsink
f) voltage and current ratings appropriate to each stage of the converter. For the first stages this means a 200V rating so that voltage spikes do not destroy the device. The peak current through the switch depends upon the panel output current and the current ripple. The properties of the panels/inductors indicate that 5A is a gross overestimate of the possible peak currents, which allows for some safety margin. The second stage switch is subjected to much harsher conditions, having to switch at up to 300V and cope with spikes from the EEE-EV motor, since it is separated from the battery bus by a single diode. Ratings of 500V and 5A would not be excessive.

A MOSFET in a TO-220 package would generally fulfil all the requirements but a) MOSFETs with the combination of very high voltage rating and very low on-resistance are very expensive. Fortunately, a consequence of low-on-resistance is high-current carrying capacity, so MOSFETs that meet the voltage rating and low-resistance requirements are suitable. The IRF-640/TO-220 at 200V/18A/0.18Ω for the first stage and IRF450/IRFP-450 ISOWATT218 (P for non-International Rectifier
origin) at 500V/13A/0.4Ω for the second stage seemed to be the best options for a reasonable price. It is easy to damage MOSFETs by static discharge when they are out of a circuit (during installation) and paralleling devices avoids the risk of having a single handling error disable a solitary MOSFET. For a given total on-resistance, it was cheaper to purchase several MOSFETs with moderate on-resistance and put them in parallel than risk converter operation on the failure of an expensive, very low on-resistance type. Insulated Gate Bipolar Transistors (IGBTs) can also be used if the switching frequency is below 25kHz. ION50 devices are 500V rated and are therefore appropriate for the second stage.

Up to 4 paralleled IRF-640s were used for each of the first stages, giving an on-resistance of down to 45mΩ. Relative to switching losses this effectively eliminates conduction losses from the first stage switch. This means that the losses will be determined by the turn-on/turn-off times of the devices, which are limited by the gating signals. The second stage was built to accommodate 2 IRFP-450s in parallel, and the 0.2Ω on-resistance of the two devices is barely significant compared to the switching losses. However, these MOSFETs proved unreliable in conditions where DCM occurred, as they overheated and failed, and they were replaced with 2x ION50 IGBTs. This necessitated switching at a lower frequency (<25kHz), which made the second stage more prone to DCM mode. Since the IGBTs had no reverse diode on the collector/emitter path, DCM mode was characterised by a resonant voltage on the top side of the switch, which could go significantly negative (see §2.4).

§2.1.2.5 The positive feed-forward control system

The positive feed-forward control system is critical to the stable and efficient operation of the converters. As described in §1.4, the input voltage of each converter is regulated by some form of positive effect on the duty cycle of the relevant converter's switch. §2.3 covers the issue of closed loop control in more detail, including stability and Chapter Three describes use of a microprocessor to replace the direct +FF.

The Motorola SG-3526 PWM (see App. B) controller chip is able to accept an (internal) error amplifier output signal in the range of 2-5V and drive MOSFETs directly from its totem-pole outputs.

In fig 2.4 the critical inputs and outputs of the 18 pin DIP SG-3526 package are shown. The user has access to the error amplifier via pins 1,2 and 3. The error amplifier is of a transconductance type so gain/stability can be adjusted by choice of
$Z_1$, $Z_2$ and $C_s$, the shunt capacitance. If the error amplifier is to operate at high gain, the voltage on the non-inverting input must be close to the reference voltage, which may be 0V or derived from the on-chip 5V reference. As the input voltage of all the stages can be much larger than 5V, a voltage divider on $V_{in}$ is essential.

![Schematic diagram of a closed loop +FF Control system, showing MOSFET output driver, with the MOSFET gate represented by a capacitance, $C_g$. N.B. $V_{cc} > 8V$.](image)

The error amplifier output is compared to an oscillator signal that has an externally programmed frequency and dead-time (the downward going part of the saw-tooth), which is available at pin 10. The fraction of time during which the error amp output exceeds the oscillator signal's rising phase gives the output duty cycle, $\delta$. However the output is delivered in two complementary halves, and if $\delta$<0.5 is required, two outputs must be interchanged to the MOSFET gate by diodes.

The output drivers of the SG-3526 have a current rating sufficient to cope with switching a capacitance, such as $C_g$, but when driving several MOSFET gates in parallel, a pull-down resistance, $R_{pd}$, is required to lower the switching losses incurred by a slow turn on/off. This limits the number of MOSFETs that can be efficiently paralleled and driven by a SG-3526 device. If the effective $C_g < 10nF$ for IRF-640 and IRFP-450 MOSFETs, and $R_g = 3.9\Omega << R_{pd}$ we can determine that...
the rise/falltime for four paralleled IRF-640s is about $40\,R_{pd}$ ns and for two parallel IRFP-450s is $20\,R_{pd}$ ns. If the MOSFETs are to be switched at up to 50kHz, an acceptable rise time for the gate signal would be 200ns, 1% of the cycle. This suggests $R_{pd}$ values of no more than 50Ω for the first stages and 100Ω for the second stage. Power dissipation in the pull-down resistors gives a lower limit to the values of $R_{pd}$:

$$P_{pd} = \frac{V_c^2 \delta}{R_{pd}} \quad \text{eq 2.7}$$

For $V_{cc} = 12\,V$, $\delta = 0.9$ and $R_{pd} = 100\,\Omega$ the current through $R_{pd}$ when the gating signal is high will be 120mA. Since this is actually drawn through the 10Ω resistor to $V_c$ (which prevents current surges at the instant when both output drivers short to ground in the cycle) the actual gating voltage may be 10.8V and $P_{pd} + P_{10\Omega}$ is about 1W. This is inversely proportional to $R_{pd}$ so the reduction in switching losses must be balanced against increased $P_{pd}$. Finding the value of $R_{pd}$ which minimises the total losses for a particular converter is essential for maximising the usefulness of the interface. However, the energy consumed by the controller chip and its gate drive is a fixed cost, and will be less significant if larger panels are attached to the interface (see §4.1 and §4.2).

§2.1.2.6 The output diodes

These are required to be fast switching, have a voltage rating appropriate to converter in which they are installed, be able to deal with currents of up to $(1\,A + \text{the expected ripple and current spikes})$ and have a low forward bias voltage at maximum expected currents. To avoid generation of high frequency noise, the reverse-recovery must be soft. Philips BY229-800 diodes in the TO-220 package are rated at 800V and 4A average forward current at $\delta = 0.5$, with a reverse recovery time of 150ns without snap-off. Lower voltage-rated diodes do not offer significant advantages, except perhaps cost, so BY229-800 diodes were installed on all the converters.

§2.1.2.7 The Battery Bus

The battery bus is a variable DC voltage source with a low series impedance. Fig 2.5 shows how the solar charger interfaces with the battery bus. The EEE-EV has a battery bus formed by 20 12V lead-acid batteries in series. However, these batteries were not available for use in the initial stages of this project. Instead, a simulated
battery bus, based on the circuit shown in fig 2.6, was used. This system had to have an easily and rapidly changeable "bus" voltage which is nearly independent of solar current sinking of up to 1A. Any dependence of the "bus" voltage on current sinking should mimic that which would occur for a real battery system.

![Fig 2.5 How the Panels interface with the Battery Bus](image)

![Fig 2.6 circuit for simulated battery bus](image)

The isolated variac provides a variable AC source of up to mains amplitude which is converted to a variable DC source (0-300+V) using a bridge rectifier. Ripple suppression is done by a 22000μF 400V capacitor. The IGBT acts a regulator of the bus voltage $V_{bus}$ in the face of varying $I_{solar}$ by holding $I_{load}$ constant and controlling "$I_{batt}"$ to match. $R_{load}$ must be chosen such that $(I_{solar}.R_{load})_{max} < V_{bus}$. Given that $(I_{solar})_{max} << 1A$ for $V_{bus} > 200V$, $R_{load} < 300\Omega$ is appropriate. The smaller $R_{load}$ is, the larger "$I_{batt}"$ will be, forcing greater power dissipation on $R_{load}$, but this reduces the relative change in "$I_{batt}"$ in response to $I_{solar}$ changes, improving the voltage regulation.

The voltage across the IGBT is $<5V$ and, more importantly, has only a very slight positive dependence on "$I_{batt}"$. Note that increasing $I_{solar}$ decreases "$I_{batt}"$ and will therefore increase $V_{bus}$ slightly. In the real battery bus, a similar relation holds for no-load conditions, when solar charging would increase the bus voltage (see fig 1.5). When the bus is loaded, increased $I_{solar}$ would also tend to increase $V_{bus}$ by
reducing the loss in the internal resistance of the battery. Thus, the rectifier/IGBT "battery bus" is a good substitute, in terms of regulation, for the real thing.

A difference from ideal mimicry of a real battery is that the rectifier supplies pulsatile current at twice line-frequency. Thus $I_{\text{batt}}$ and $I_{\text{solar}}$ will have non-DC components (peaks and dips respectively), with a fundamental at 100Hz. This can be minimised by extra filtering on the output from the rectifier, but since the second stage converter had enough output capacitance to maintain stability the issue was considered unimportant (see §2.4 and §2.5).

§2.1.2.8 Interconnection cables

Connecting cables, from the panels to the converters, between the converter stages, and between the converters and "battery bus" have to be of low resistance to reduce losses. The cables used for converter interconnection and converter to "battery bus" connection were short heavy gauge fine-braided types, with a low resistance, even at 100kHz. However, a 20m extension cord was used for the panel to converter connection, with a 40m 50A rated ABCAL cable for panel earth return. Each panel to stage1 converter resistance was still less than 1Ω, and the earth return resistance was less than 0.3Ω. The effect of this resistance was to increase the maximum power voltage of the panels. For example if the LA-63 panel was operating in a 1000W.m⁻² irradiance then the expected max-power voltage is 20V, giving, say, 3A/60W (allows for loss in panel protection diodes). If a 1.3Ω total resistance is in series with the panel current, the available power is 48.3W at a panel voltage of 20V. Assuming that the panel current is 2.9A at a panel voltage of 21V, the available power is 48.608W (see figs 1.7a/b and 1.8a/b for confirmation of feasibility). This voltage raising effect is dependent upon the function $I_p = I_p(V_p)$ for the panels, and the size of the series resistance ($R_s$). The available power rises with rising panel voltage until the rate of decrease of panel power output per unit volt exceeds that of the rate of decrease of power loss in the series resistance per unit volt. At the optimum voltage, the rate of change of available power is zero:-

$$\frac{dP_a}{dV_p} = \frac{dP_p}{dV_p} \frac{dI_p}{dV_p} = 0 \text{ at max available power panel voltage } V_p = V_{P(\text{max/a})} \text{ eq 2.8}$$

also $V_{P(\text{max/a})} = 2R_sI_{P(\text{max/a})} - \left(\frac{I_p}{dV_p}\right)_{\text{max/a}}$ and $V_{a(\text{max/a})} = V_{P(\text{max/a})} - R_sI_{P(\text{max/a})}$

where $P_a$ is the available power, $P_p$ is the panel output power, $V_p$ is the panel voltage, $I_p$ is the panel current, $P_L$ is the power loss in the series resistance and (max/a) refers to the value of the subscripted variable at maximum available power.
Note that the available voltage at maximum available power ($V_{a(max/a)}$) is lower than the panel voltage.

§2.2 Design of PCBs for Boost Circuit

The hardswitched boost converters used in this project had to be efficient and stable. Input currents of up to 3A @ 20V from the LA-63 panels are possible (max-power voltage of 20V in 1kWm$^{-2}$ sunlight) and the current may go higher if the panel voltage is below the max-power voltage - though this condition should be transient in a well controlled system.

The high currents paths in the boost circuit must, therefore, have a low resistance. Control signals on the PCB must be protected from high frequency switching noise. This can be achieved by careful planning of the PCB topology and geometry. Maximising the physical separation of power and signal lines while minimising the area enclosed by high current loops reduces the possibility of contamination of the low-voltage control signals. The high-current paths were made of short-as-possible 50 to 100mil width track, and copious solder was added to these tracks to increase their conductance. Gentle curves and avoidance of sharp corners lowered EMI radiation due to acceleration (changing of direction of motion) of charges [White 1971-75].

Signal paths in the PCB layout were protected from high-level noise by keeping them away from power circuits and by placement of tongues of ground-plane on either side of them.

The 4-way converter system is a substantial package of components, and the eventual aim would be to reduce the required PCBs to minimal size. If all the converters could be located on one PCB it would remove the replicated ground-plane, input and output links, and increase the reliability by reducing the non-PCB connections. It might be expected that the size reduction would also reduce the radiation area of the PCB. However, placing the converters on a single board caused interference between the converters, if only because of their proximity. When the error amplifiers were operated at a high gain, as in closed loop control (see §2.3), the single board layout could not be operated stably. However, the single board system was untested by μP control, where the error amplifiers are operated at unity gain (see chapter 3), and it may give good results in that case. App. B has details of the PCB schemata and layouts.
§2.3 Closed Loop Control

In §2.1.2.5, the concept of a +FF system based on the SG-3526 PWM controller chip was introduced. Fig 2.7 shows the realisation of such a system.

For a DC input, the error amplifier shown in fig 2.7 has a gain of $1+R_2/R_1$, where $R_2$ and $R_1$ are the resistances of the lumped components $Z_2$ and $Z_1$. The accuracy of the input voltage regulation is proportional to the gain. However, the gain and/or phase margins for stable operation at frequencies comparable to the switching frequency ($f_s$) must be maintained. In practice, this limited the DC gain to values less than 100, and a 1μF monopac in parallel with the 100kΩ feedback resistor gave a stable response for $f_s=20-50$kHz. The error amplifiers were not required to respond to disturbances in the input voltages faster than that caused by the passing of clouds, which occur with time constants comparable to 1 second. The shunt capacitance ($C_s$) used was up to 1000μF, which filtered amplified noise in the transconductance error amplifier, without increasing the response time of the error amplifier to greater than 1 second.
§2.4 Preliminary Results

Figures 2.8 - 2.14 show voltage and current waveforms for the first and second stage boost converters of the interface. Figure 2.8 shows the effect of discontinuous current mode (DCM) due to low switching frequency/small boost inductance. Figs 2.9 - 2.12 show the effect of DCM, during startup of the interface. Figs 2.13 - 2.14 show operation in continuous current mode.

Figure 2.15 shows the effect of power switching on a SG-3526 error amplifier.

Fig 2.8  DCM mode in a MOSFET switched stage1 converter. Note that the MOSFET gate signal is low during the time of DCM excursion.
Fig 2.9  DCM during startup in the second stage of a converter switched by an IGBT. DCM mode is indicated by the collapse of the collector voltage into a damped sinusoid, and occurs when the inductor current falls to zero before the next high gate signal.

Fig 2.10  DCM at a later stage in startup than shown in fig 2.9 in the 2nd stage converter switched by an IGBT. Note that the collector voltage and inductor current may go negative (see also figs 2.11/12)
Fig 2.11  the final phase of startup in an IGBT switched second stage. The period in which the inductor current oscillates about zero reduces to zero as the negative duty cycle of the switch approaches 0.8.

Fig 2.12  Startup in the second stage, showing the collector voltage and current output to the battery bus
Fig 2.13  second stage MOSFET drain voltage and inductor current in normal operation.

Fig 2.14  second stage MOSFET drain voltage and inductor current in normal operation, showing switching transitions.
Fig 2.15  error amplifier output and oscillator waveform for a single stage1 converter operating in closed loop mode with an error amplifier gain of 100. Note the large spikes at the times of power switching (turn off of MOSFET switches)

§2.5 Current Measuring Devices

In §1.5 control strategies based on maximisation of output currents are described. These depend on inputs from some sort of current sensors, which, for the purposes of this project, are required to have a measurement resolution no less than that of an 8-bit A/D for sensed currents in the range of 0-5A. They must be able to interface with the 0-5V rails of the 80C451 microprocessor system and the intermediate/ output voltages (around 100V and 240V respectively). The sensors must have
minimal power consumption. Otherwise the usefulness of the control system is negated.

The LEM Module LA 25-NP, made by LEM of Switzerland was determined to be the most suitable current sensing device for this project. Based on a flux balancing current transformer, the compact module can be configured to accurately measure currents in the 0-5A range by connecting all 5 primary coils in series, maximising the current sensitivity. It completely isolates of the current input from the output (>1500MΩ at 500V input/25°C), has an accuracy an order of magnitude greater than that of an 8-bit A/D (see fig 2.17/18) and a bandwidth of greater than 100kHz.

Fig 2.16 LEM sensors (see also App. B)

The LEM sensors operate on a ±15V (±5%) power supply and draw 15*(0.01+ι₂) watts each (ι₂ is the secondary current which travels through the measurement resistor - .025A at ι_p = 5A). A worst case scenario has 1A exiting each converter, including the secondary, giving a total ι₂ of 25mA*4/5=20mA through 100Ω loads which implies maximum output voltages from the LEMs of 0.5V. Thus the maximum
total (all four LEMs) power consumption in this case is expected to be less than 3.6W. The power supply requirements of the LEM sensors can be justified, but we are unable to make full use of the 0-5V range for the A/D especially during periods of lower output currents, such as during overcast conditions, when accurate control would have the most relative benefit.

A simple solution is to amplify the voltage signal from the LEMs using low-power op-amps by a factor of about 10. The gain of the op-amps can be adjusted for individual converters - to 15 for the LEM sensing current on the first stage converter fed by the smaller LA-45 panel and down to 7 for the first stages fed by the larger LA-63 panels. Simply increasing the load resistance on the LEMs is another option, but this places a strain on the compliance of the current-source output of the LEMs. If the LEM output current is less than 5mA (ie primary current of 1A, the maximum current expected), load resistances of 680Ω give output voltages appropriate to the usage (3.4V for 5mA LEM output). In poor sunlight conditions the LEM output current will be no more than 0.68V (200mA primary current). This is rather low for a 0-5V µP system with 8-bit (20mV) resolution but allows a safety margin in the limiting of the LEM output to below 5V.

Fig 2.17 shows the LEM output voltages with a 100Ω load in the 0-5A and 0-1A range. Note that linearity of the LEM output voltage is retained for primary (sensed) currents of up to 1.5A and that a 1V output corresponds to a LEM output current of 10mA. Fig 2.18 shows LEM outputs for higher load resistances.

LEM load resistances of about 680Ω were used for the purposes of this project.
The LEM output is sampled by an 8-bit μP A/D and the first step to accurate control is accurate measurement of the mean output current from each converter. The high bandwidth of the LEMs is in fact a hindrance, especially in the second stage unit, which has significant ripple due to the form of the artificial "battery bus". Since the A/D samples at essentially random intervals (every 6 seconds) with respect to the output current ripple, the measured current is not a stable representation of the mean current. The simplest solution is to add extra filtering to the second stage LEM output. A 1000μF/10V Rubycon unit, parallel to the 10nF greencap units on all the LEMs, reduced the 100Hz ripple to negligible levels. There remained a noise fluctuation of 80mV_{pp} (-10dB referenced to a typical signal -four 5V 8-bit units) on the LEM outputs which, though not desirable, did give the fuzzy control system something to be tested against.
Fig 2.19 LEM output voltage to a 100Ω load, with/without filter capacitor. Note the 100Hz ripple, which was a consequence of disturbance in the mains voltage (and thereby the battery bus) by a large motor operating nearby

**Tek**

<table>
<thead>
<tr>
<th>ch1 w/1mF cap</th>
<th>400mV</th>
<th>w/1mF cap</th>
<th>10ms</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ch2 no 1mF</td>
<td></td>
<td>no 1mF</td>
<td></td>
</tr>
<tr>
<td>mean 594.4mV</td>
<td></td>
<td>mean 382mV</td>
<td></td>
</tr>
<tr>
<td>pk-pk 80mV</td>
<td></td>
<td>pk-pk 504mV</td>
<td></td>
</tr>
</tbody>
</table>

LEM sensing a primary current of ~0.1A for no cap and ~0.15A w/cap

Channel 2 frequency 98.1635Hz
Unstable histogram

The LEMs were implemented in the interface as shown in fig 2.20
Fig 2.20 implementation schematic for the LEMs (see also figs 1.2, 1.10 and 1.11)
CHAPTER 3 MICROPROCESSOR CONTROL

Introduction

The analogue closed loop feed-forward control discussed in §1.4 allows accurate regulation of the converter input voltages and rapid adjustment to system perturbation. However, the set-point of the regulation must be adjusted manually, and the control system does not necessarily maximise battery charging power. Automated regulation of input voltage as a means of power output maximisation makes the interface useful, as it needs to operate in variable light conditions for long hours, possibly in remote areas. The cost of implementing a microprocessor controller is small compared to the cost of PV panels, so the benefits of output power maximisation are economically justifiable [Enslin 1990].

A microprocessor system (μP) on a 5V supply is ideally suited to controlling the output of the SG-3526 PWM-controller error amplifier (see §2.1.2.5). The challenges of operating such a control system include:

i) establishing a complete set of inputs to the control system and the use of appropriate sensors.

ii) configuring A/D - D/A functions and interfacing the required hardware with the μP and converters.

iii) developing software which realises the aim of output power maximisation.

The control systems developed for this project are based on previous work which attempted to maximise photovoltaic power uptake. Harashima et. al. used a simple tracking algorithm with no reliance on an irradiance measurement [Harashima et. al. 1987]. Hoshino et. al. used a fuzzy logic expert system that attempted to seek an irradiance-based estimate of the maximum available power [Hoshino et. al. 1988].

For this project, not having to rely on irradiance measurements was considered desirable (see §3.2). Both simple trackers and fuzzy logic expert systems were developed. Repeatable test conditions were established and the effectiveness of the different control systems was tested (see §3.4). The strengths and weaknesses of the different control systems are discussed in §4.2 and §4.3.
§3.1 The 80C451 Development Board

Industrial Research Limited (Christchurch) have produced a convenient development board for the 80C451 µP. A specialised on-board BASIC and I²C bus interface to an on-board 4-channel A/D, single channel D/A (PCF8591 chip) and serial port interface to a PC made this development board particularly useful. Add-ons of up to 7 more 4-channel A/D, single channel D/A's are possible. The Interface required 4 µP outputs - one for each converter, and the 4 PCF8591 chips this requires allow 16 different analogue inputs from the interface to be processed. 4 converter output currents, 4 converter input voltages, the battery bus voltage and the measured irradiance could be digitised with 6 channels to spare, so a total of 4 PCF8591 chips were used. Fig 3.1 shows the block layout of the development board and its connection to the rest of the Interface.

Fig 3.1  The IRL 80C451 development board schema. EA= SG-3526 error amplifier (see §2.1.2.5)

§3.2 A Simple Tracker

Refer to fig 3.2 for illustration of the following discussion. Since the aim of the controller is to maximise the output power to the Battery - the DC product $I_{out} \times V_{out}$ - and $V_{out}$ is only weakly dependent upon the power output of the solar charger, the control system should aim to maximise $I_{out}$ irrespective of the value of $V_{out}$ (within
safe operating limits). $I_{out}$ is multidependent on previous steps in the interface and panels:

$$I_{out} = \eta_2 (1 - \delta_2) (I_{Ia} + I_{Ib} + I_{Ic}) = \eta_2 (1 - \delta_2) I_{int} \quad \text{eq.3.1}$$

Similarly, the current output of each of the first stage units is multidependent:

$$I_{Ix} = \frac{\eta_{Ix}}{\delta_{Ix}} I_x \quad \text{eq.3.2}$$

$$V_{int} = V_{out} (1 - \delta_2) \quad \text{eq.3.3}$$

Maximising the $I_x$ values (the panel output currents) will not maximise the output power of the interface, since this implies a short-circuit panel condition. If eq 3.3 holds, and therefore $V_{int}$ is constant with respect to $I_{int}$, then a control strategy based on seeking the maximum current output from each converter is possible. However, losses in the second stage converter are proportional to the power input to it. This means that $V_{int}$ has a positive dependence upon $I_{int}$. If this dependence
interferes with the lower voltages in the boost chain the tracking control will be unstable. The uncertainty can be removed by seeking maximum power output from each converter. This requires that the voltages \( V_{\text{in}} \) and \( V_{\text{out}} \) be known, in addition to the 4 currents \( I_{\text{a}}, I_{\text{b}}, I_{\text{c}}, \) and \( I_{\text{out}} \). A comparison of the performance of these two methods of simple tracking is presented in §3.4.

The simple tracking system software was programmed in BASIC. The required algorithm for each converter is represented in fig 3.3:

![Simple tracker algorithm diagram](image)

In order to get the maximum tracking resolution from the 8-bit \( \mu \)P, the default change in \( \mu \)P error amplifier control voltage (\( \mu \)PCV) is one 8-bit unit = +/-19.6mV. This algorithm requires that the current/power measurements have an uncertainty much lower than the current/power change induced by the alteration in output to the error amplifiers in one iteration. Figs 1.7a/b/c and 1.8a/b/c show that if the panel voltages are below 12V (LA-63) or 9V (LA-45) the change in current/power per volt is <10%. The aim of the tracker is to reach the absolute maximal stationary point, about which the changes in current/power with respect to voltage are minimal (see fig 3.4). This forces the current/power measurements to be extremely accurate.
Unless the measured output current/power has a noise amplitude much smaller than the range between maxima and local minima, there is the risk that the tracker will be temporarily held by a local minimum, though this condition is unstable. Since the current/power output of any particular converter depends on the duty cycle as well as the panel voltage and its irradiance, there may be multiple local maxima/minima in the functions of current/power output with respect to the μP error amplifier control voltage (see fig 3.4).

Fig 3.4  A possible form of the output current/power from a particular first stage converter, with respect to the μP error amplifier control voltage (μPCV) (see §2.1.2.5 for error amplifier (EA) configuration).

In order to avoid the trap of local minima or local maxima (as opposed to the absolute maximum), the change in μPCV per iteration can be increased such that the converter moves out of local minima and into the vicinity of the absolute
maximum. However, this makes the control coarser, and accurate tracking of the absolute maximum is impossible. A more complicated system that uses large $\mu$PCV changes per iteration when the changes in current/power output are high and small $\mu$PCVs changes when the changes in output are small can still be captured by local minima. If the $\mu$PCV is too high or low for a particular situation, the tracker may be trapped in a situation where the output is low due to the related panel being either open or short-circuited. For example, this occurs if the initial $\mu$PCV is too low to start a converter in high irradiance conditions (open circuit), or if the irradiance on a panel drops suddenly, leading to a near-short-circuit. The tracker may also be trapped by local maxima. It is essential that the time spent in these relatively low output conditions is minimised, so fast-acting safeguards must be used.

If the input voltages of all of the converters are known, these can be compared to previously established limits of input voltages (the upper voltage limit - UVL - and lower voltage limit - LVL - see tables 3.5/3.6) that give a significant power output and enclose only one maximum - the absolute maximum (see fig 3.4). Furthermore, useful limits on $\mu$PCV can be established, i.e. $5 > \mu\text{PCV} > 0.3$V to ensure that the error amplifier output will be in the range of the saw-tooth voltage with which it is compared (see §2.1.2.5). If the input voltage or $\mu$PCV limits are exceeded, an override can be applied to the simple tracking algorithm. The input voltage override consists of a 2x8-bit unit/39.2mV $\mu$PCV change which is activated until the system gets back into an acceptable operating region.

Table 3.5 The useful voltage limits for the panels. Note that these limits are higher than would be expected for the panels used, because of the non-zero panel to converter cable resistance (see §2.1.2.8).

<table>
<thead>
<tr>
<th>Conditions at which the out-of-range voltage overrides are activated</th>
<th>Upper Voltage Limit (UVL) at measured Irradiance=500W.m$^{-2}$</th>
<th>Lower Voltage Limit (LVL) at measured Irradiance=500W.m$^{-2}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Converters 1a and 1b</td>
<td>18V</td>
<td>15V</td>
</tr>
<tr>
<td>Converter 1c</td>
<td>15V</td>
<td>9V</td>
</tr>
<tr>
<td>Converter 2</td>
<td>100V (independent of irradiance)</td>
<td>40V (independent of irradiance)</td>
</tr>
</tbody>
</table>

Measurement of the irradiance is useful, for analysis of the trackers' responses and setting of the voltage override limits (VOL). It was decided not to use the irradiance
measurement as a direct determinant of the controller output in the simple tracker, as the μPCV for maximum current/power output is not a simple function of irradiance, and the measured irradiance is based on a different spectral response to that of the panels (see App A). Furthermore, a single point measurement is only useful if the phototransistor sensor is in the same light environment as the entire panel surface. The panels may be in mixed shade but multiple sensors could not be used without enormous complication. The sensor voltage was scaled by a voltage divider and software so that the irradiance in W.m\(^{-2}\) could be displayed and stored. The panel voltage limits were scaled by a convenient function of the measured irradiance, which ideally has the form of the inverse function of maximum power voltage with respect to irradiance. eq 3.4 shows a function which was made by a simple curve fit to the gathered data of maximum power voltage with respect to irradiance (see figs 1.7/1.8):

\[
\text{VOL} = (\text{VOL at } 500\text{W.m}^{-2} \times \frac{\text{Measured Irradiance (W.m}^{-2})}{500\text{ W.m}^{-2}})^{\frac{1}{2}}
\]

eq 3.4

Table 3.6 Out of range voltage overrides for different values of measured irradiance

<table>
<thead>
<tr>
<th>Out-of range voltage limits</th>
<th>UVL at 1000 W.m(^{-2})</th>
<th>LVL at 1000 W.m(^{-2})</th>
<th>UVL at 500 W.m(^{-2})</th>
<th>LVL at 500 W.m(^{-2})</th>
<th>UVL at 200 W.m(^{-2})</th>
<th>LVL at 200 W.m(^{-2})</th>
</tr>
</thead>
<tbody>
<tr>
<td>Converter 1a and 1b</td>
<td>21.4V</td>
<td>17.8V</td>
<td>18V</td>
<td>15V</td>
<td>14.3V</td>
<td>11.9V</td>
</tr>
<tr>
<td>Converter 1c</td>
<td>17.8V</td>
<td>10.7V</td>
<td>15V</td>
<td>9V</td>
<td>11.9V</td>
<td>7.15V</td>
</tr>
<tr>
<td>Converter 2</td>
<td>100V</td>
<td>40V</td>
<td>100V</td>
<td>40V</td>
<td>100V</td>
<td>40V</td>
</tr>
</tbody>
</table>

The override μPCV change may be scaled to match the amount by which the input voltages exceed their limits, thus giving a more rapid return to useful operation. However, this complication was used only in the fuzzy controller, which is discussed in §3.3.
In conclusion, the simple tracker was designed as a minimalist control system, with the aim of maximising of the output current or power from each converter independently. An override procedure ensured that the converters forced the interface out of non-useful input voltage zones quickly.

§3.3 Principles and Application of Fuzzy Logic Expert Systems

§3.3.1 Introduction

The simple tracker forms described in §3.2 have a limited range of control inputs and outputs. They take no concerted account of the interaction between converters, acting only to maximise the output power or current from each individual converter. In circumstances where a concerted response would be sensible, such as a marked, even change in irradiance, a more complicated control system is required.

Conventional PID control is inappropriate for this application, as the control functions cannot be easily put into analytic form. The continuous, as opposed to discrete form of the panel VI characteristics suggests that a Fuzzy Logic Expert System would be appropriate for the Control Task [Aptronix pid-fuz.txt]. Fuzzy Logic allows for a smooth, continuous response to control inputs and enables the user to program the controller to weight its response to different input variables, such as output current changes, power output changes and irradiance fluctuations. This contrasts with the simple tracker's fixed decision-making process, which resolves changes in controller input as positive or negative only.

§3.3.2 Principles of a Fuzzy Logic Expert System

The basis for fuzzy logic is a generalisation of Boolean Logic, a system in which the validity of all statements are restricted to the set {True, False}. This binary system is not the natural human language of description of variables, which ascribes a variable degree of aptness to a statement of quantity.

For example, if a binary system was deciding if a variable called "Irradiance" was high, it might compare a (continuously variable) measurement to an arbitrary border value (500 W.m$^{-2}$, say). If the measurement was greater than or equal to 500 W.m$^{-2}$ the outcome of the measurement would be := "high" is True. Otherwise the outcome would be : "high" is False. A human would be inclined to use the term "high" with a qualifier. Measurements of less than 250 W.m$^{-2}$ could be described as "not high", values between 250 and 750 W.m$^{-2}$ could be described as "fairly high" and values
above 750 W.m\(^{-2}\) could be described as "very high". Moreover, there are no sharp borders for deciding the appropriateness of the qualifier to the group "high". In fact, the number of available qualifiers is infinite, spanning the range between absolutely False to absolutely True. Translating this into a numerical, computer-oriented system, multiple *degrees* of truth between 0 and 1 can be ascribed to a statement, which contrasts with the stark choice of 0 or 1 in Boolean Logic.

Thus, for the superset of non-negative real numbers which contain all possible values of the variable "irradiance" - the universe of discourse, and division into subsets is possible. Fig 3.7 below shows possible ways of defining a subset "high irradiance". The process of converting a variable into a degree of truth of membership of a fuzzy subset is called "fuzzification". Before fuzzification, the variable is "crisp".

**Fig 3.7** comparison of possible Boolean and fuzzy subsets "high irradiance" on the universe of discourse "irradiance"

**Boolean:**

- High Irradiance = { 0 if 0<Irradiance<500
- { 1 if Irradiance ≥ 500

**Fuzzy:**

- High Irradiance = { 0 if 0<Irradiance<250
- { (Irradiance-250)/500 if 250<Irradiance<750
- { 1 if Irradiance>750
Fuzzy membership functions are not necessarily probability density functions, but probability density functions are all fuzzy sets. Fuzzy membership functions defy the Boolean concept of "the law of the excluded middle", by their continuous filling of the gap between absolute truth and falsehood of a statement. Crisp values can have non-zero membership of more than one fuzzy set. Typical guidelines for membership function definitions are shown below:

i) For any value of the variable undergoing fuzzification the pointwise sum of the membership functions is one. An example of this is shown in fig 3.8 by the membership functions for subsets \( F \) = "high irradiance" and \( G \) = "low irradiance". This is not essential, but it can help to keep a normalised scale of fuzzy memberships. The membership sum could be variable or constant, not necessarily equal to one; eg the fuzzy set "fairly high irradiance" shown in fig 3.8 is introduced, the sum of the fuzzy memberships is 1.5 for a crisp input of 500W.m\(^{-2}\). Membership functions are defined so that there is a smooth complementary transition in values about the operating point [Brubaker brub8.txt].

ii) Values of the variable undergoing fuzzification which have maximal membership in a fuzzy subset also have minimal membership of a fuzzy subset that aims to cover opposing values of the variable. This is shown in fig 3.8, and follows from the definition of \( G \) as the fuzzy negation of \( F \). A strength of fuzzy logic is its ability to accurately cover the middle ground between variable extremes, but this merit must not be negated by giving a single crisp value a high degree of membership in two opposing categories. The amount of overlap of adjacent fuzzy sets is called aliasing and it can make up for an incomplete rulebase [Lotfi 1993].

iii) The same shape of translated membership function is used for all values of the variable to be fuzzified, and the same membership functions are used for all variables. This amounts to a simplification for ease of implementation, and is neither necessary or justifiable in terms of benefit to the fuzzy logic system.

There are multiple possible values of truth in answers to the question "is the Irradiance a member of the fuzzy subset 'high irradiance'?". This type of multivalued logic (MVL) forms the basis of a fuzzy expert system. It was pioneered by Lotfi Zadeh in the 1960s [Zadeh 1965], and has been extensively developed for use in computers by Zadeh and others since then [Zadeh 1984]. Fig 3.8 shows how the familiar logical terms NOT, AND and OR are interpreted in MVL.
Fig 3.8  Fuzzy Logic definitions

In general, for fuzzy subsets/membership functions F, G ad infinitum, the truth/degree of membership for the basic logical operators is given below and illustrated by example for the subsets \( F = \text{"high irradiance"} \) and \( G = \text{"NOT high irradiance"} = \text{"low irradiance"} \).

\[
\text{Truth}(\text{NOT}(F)) = 1 - \text{Truth}(F) \quad (\text{in this case} \, G = \land(F))
\]

\[
\text{Truth}([F] \land [G]) = \text{minimum}([\text{Truth}(F), \text{Truth}(G))] = \text{Truth}([F] \land [G])
\]

(in this case \( \text{Truth}([F] \land [G]) = \text{"fairly high irradiance"} \))

\[
\text{Truth}([F] \lor [G]) = \text{maximum}([\text{Truth}(F), \text{Truth}(G)]) = \text{Truth}([F] \lor [G])
\]

A fuzzy expert system uses fuzzy membership functions and applies fuzzy logic to the rules which determine the form of the expert system. The rules (generally more than one) are collectively known as the rulebase, or knowledge base. A rulebase is complete if all possible combinations of the input fuzzy sets are considered. For example, a system with two input variables that are both fuzzified into three fuzzy subsets can have 9 rules that are based on duplex OR combinations of the two input variables, plus another 9 for duplex AND combinations. Combinations of different fuzzy subsets of the same variable are possible (even "F AND not F" can have a non-zero truth in fuzzy logic), and the only restriction on the number of fuzzy
subsets that may be logically combined in rules is the total number available (in this case, 6). Thus, the strictly complete rulebase for this example has about $10^2$ rules. An important part of forming a simplified fuzzy expert system is determination of which rules from the complete rulebase can be eliminated. Rules which have an AND combination of non-intersecting sets will always have zero truth, and are an example of rules that can be ignored.

It is not essential to include all rules with a possibility of non-zero truth if there is sufficient overlap, or aliasing of the fuzzy input sets. The aim of aliasing is to ensure that at least one rule in the (incomplete) rulebase fires (has a non-zero degree of truth) [Lotfi 1993]. Using the membership functions from fig 3.7, a possible rule is shown below:-

Example Rule 1  IF "fairly high irradiance" THEN [control value] is MEDIUM

`---------`  `---------`
premise/antecedent conclusion/consequent

If the measured irradiance is such that its memberships of \( F \) and \( G \) are both non-zero, then the above rule will fire. The degree of firing is not absolute, but a fuzzy membership of the output set, MEDIUM, which in this case (AND) is equal to the minimum of memberships of \( F \) and \( G \).

Using the rulebase and membership functions, a process of inferencing is used to determine the output variables. Inferencing is composed of the following sub-processes:-

1) Fuzzification - as already mentioned, this is the determination of the degree of membership of fuzzy subsets for a crisp variable.

2) Inference - the application of the rulebase to the fuzzy input membership values. If a rule fires, the fuzzy output membership function that is the rule’s consequent must be weighted according to the degree of firing. There are two common methods of output membership inference: MIN and PRODUCT (see fig 3.9). MIN Inference is equivalent to a fuzzy AND between the degree of firing and the output membership function and can be graphically interpreted as clipping the output membership function at the height of the degree of firing of the rule premise. Product inference works by scaling the output membership function by the degree of firing of the rule premise. If the output membership functions are discrete (zero area), MIN and PRODUCT inference are identical.
Fig 3.9 If the measured irradiance is 500W.m⁻² then Example Rule 1 fires with a degree of 0.5. The effect of MIN and Product inference on arbitrarily defined membership functions are shown below.

3) Composition is the aggregation of all the output membership functions inferred by the firing of rules into a single fuzzy output set for each output variable. If the rulebase is expanded and the required output membership functions are defined, then different forms of composition can be shown by example.

Example Rule 2  IF F THEN [control value] is LOW
Example Rule 3  IF G THEN [control value] is HIGH

Fig 3.10 shows the application of two possible composition methods to the processing of a crisp input of 500W.m⁻². Maximum composition takes the pointwise maximum of all the output fuzzy sets that are pointed to by firing rules. Sum composition pointwise adds the contribution of all the inferred fuzzy output sets, which can result in functions that exceed the maximum values of the fuzzy output sets. This requires a defuzzification method that can accept these large composition function values.
4) Defuzzification is optional, as the composed fuzzy output sets are full of control information. However, most applications require a single crisp output and the composed output set must be defuzzified. Therefore, the aim of defuzzification is to reduce a fuzzy output set to a crisp value by a means which gives a value representative of the fuzzy output set. There are at least 30 defuzzification methods [Fuzzy Logic Primer - primer.ps] which vary in their calculation complexity and response to different fuzzy output set forms. Two groupings are: a) centre of gravity, where the centroid of the output membership function is computed, and b) maximum methods, which include mean and median of maxima. Both of these methods can cope with sum composition, but method b) usually involves less
computation. If possible the composition and defuzzification processes should be linked to lower the total computation effort.

In the case of fig 3.10, symmetries make the choice of crisp output clear. A crisp input of 500W.m\(^{-2}\) gives a crisp output of 1.5.

§3.3.3 Application of a Fuzzy Logic Expert System to Control of the Interface

The Fuzzy Logic Expert System (FLES) aims to maximise the output power of the Interface. It fuzzifies a set of inputs, which specify the change in performance of the Interface since the previous iteration of the fuzzy program in the 80C451 \(\mu\)P. It then processes this information with respect to the discrete changes in \(\mu\)PCV by inferencing, and composes discrete output functions, which are defuzzified to their centre of gravity. The crisp changes to \(\mu\)PCV are added to the respective channel's previous value of \(\mu\)PCV and new \(\mu\)PCV values are delivered to the appropriate channel's D/A, as in the simple tracker (see fig 3.11).

In order to allow the FLES to give a concerted response to input changes, it is necessary to have an inference system that allows global interface information to affect the \(\mu\)PCV output to any converter. The rulebase contains rules which have premises based on information from more than one converter, usually but not necessarily including the converter that corresponds to the consequent output membership function.

![Fig 3.11](image)

The hardware scheme for the FLES. Compare with figs 3.2, 1.2

The fuzzy tracker can use any combination of the output current/power changes and previous changes in \(\mu\)PCV from any converter, as well as irradiance changes to determine the new change to control value \(\mu\)PCV.
Fuzzy input membership functions were defined for the converter output current changes since the previous iteration, battery bus voltage change and interface output power change. The final version of the FLES also used a crisp measurement of the irradiance change as part of the inferencing. Crisp measurements of the battery bus voltage and converter input voltages were used for comparison with out-of-range voltage override conditions (see tables 3.5/3.6). The output current changes were fuzzified into 5 categories: Large Negative (LN), Negative (N), Zero (Z), Positive (P) and Big Positive (BP) (see fig 3.12). The shape of these membership functions was based on the principles discussed in the guidelines i), ii) and iii) in §3.3.2. For any crisp input, the memberships summed to 1 and the aliasing about the ideal operating point (the centre of set Z) was set at 50%. The battery bus voltage change was fuzzified into three subsets: Negative (N), Zero (Z) and Positive (P) with 50% aliasing about the centre of set Z (see fig 3.12).

**Fig 3.12** Fuzzy membership functions. 3.12 i) converter output current changes 3.12 ii) and 3.12 iii) Battery bus voltage and irradiance changes 3.12 iv) $P_{out}$ changes, for the case of 3.12 i)a).

The horizontal scales in fig 3.12 are arbitrarily defined. The ideal inputs to the output current change fuzzifier would cover the range [-10,10] fully in the course of
operation, neither regularly exceeding the bounds or only covering a small section at the centre of the Z subset in cases of extreme input variable changes. An important part of the fuzzification was prescaling of the crisp current changes, as measured by the change in LEM output voltage (see §2.5), according to the inverse of the measured irradiance. The variable SCALE was defined thus:

\[ \text{SCALE} = \frac{500 \text{W.m}^{-2}}{\text{Measured Irradiance W.m}^{-2}} \quad \text{eq 3.5} \]

The crisp current changes were also normalised to the absolute value of the respective converter output current. In general:

\[ \text{CCC}_p = X_c \cdot \text{SCALE} \cdot \frac{\Delta I_o}{(I_o + 1)} \quad \text{eq 3.6} \]

where \( \text{CCC}_p \) = preprocessed crisp converter output current change (to be fuzzified), SCALE is as defined above, \( \Delta I_o \) = change in digitised LEM output, \( I_o \) = digitised LEM output. The added 1 is to avoid divide by zero errors at startup, and is usually less than 5% of \( I_o \). The factor \( X_c \) is a user defined scaler, converter-specific, which can be used to force the \( \text{CCC}_p \) values into the range \([-10,10]\). The same process of scaling and normalising the output current change inputs can be adapted to the changes in battery bus voltage and output power.

The rulebase is the most critical part of this FLES - the rules must be based on a sound understanding of the panels, interface, and battery bus. The rulebase for this FLES was made by considering the system characteristics and the degree of linkage between all the input variables. For example, if all the output currents from the stage1 converters increase unilaterally then there is a stronger case for taking action as if the irradiance had increased than if the changes are mixed. One of the means of realising this variable importance of input variable combinations was by weighting of the rule firing. The lowest weight used was 1 and the highest was 12. This means that the firing of a heavily weighted rule can override the firing of other less relevant rules. In a sense, any unused rules from the complete rulebase can be said to have a weighting of zero.

The rules all pointed to (had consequents of) crisp changes in \( \mu \text{PCV} \) for one or more converters, which were restricted to the values \([-2,-1,0,1,2]\). This offers an improvement on the simple trackers by allowing \( \pm 2 \) (for drastic action) and 0 (if at the maximum) as part of the within-voltage-limits operation. The rule antecedents
generally contained at least one crisp μPCV from the previous iteration with fuzzy-
logical operations on the changes in converter output currents/powers and the 
battery bus voltage change. Rules with strong linkages were given a higher 
weighting so that composition would be biased toward them.

From fig 3.12 it is apparent that the lack of aliasing for the crisp values converter 
output current changes between ±3 and ±7 will require that the rulebase must 
include a rule that points to an output membership function for any converter that 
has an output current change with non-zero membership of set P or N. Otherwise, 
there is a possibility that no rule for a particular converter will fire, leaving the new 
μPCV for that converter indeterminate.

In other cases the rulebase for this FLES was incomplete. Rules taking individual 
stage1 converter output current changes as a premise and pointing to another 
stage1 converter as conclusion were considered irrelevant. Rules which took 
combinations of stage1 variable changes and pointed to stage2 changes were 
considered important predictors of changes that would otherwise need to be made 
at the next iteration, but the combinations used were not exhaustive. The rulebases 
are in the inference sections of the .BAS files on disk in App. D.

Since the consequents of the inference were crisp, the result of inference was a set 
of scaled crisp output sets for each converter. Centroid composition also defuzzified 
the results, which were adjusted to the nearest whole value and set as the new 
μPCVs. Centroid composition allowed the firing of rules which pointed to opposing 
and/or concerted outputs to be averaged, making the FLES more resistant to noise 
in its inputs.

App. D (on disk) gives program listings for three BASIC programs which varied in 
only the fuzzification and inference sections.

FY.BAS used changes in output currents from all the converters and changes in 
output power (fig 3.12 i)a and iv)), changes in output voltage (fig 3.12 ii) and 
previous changes in μPCV to determine the new changes in μPCV. The rulebase 
for FY.BAS was the largest of the three programs, as the fuzzy conclusions from 
output current changes were corroborated with other variables.

FPC.BAS used the change in output power from each converter, with the fuzzy 
memberships shown in fig 3.12 i)b), the change in output voltage and change 
irradiance (fig 3.12 ii)(iii) . The rulebase for FPC.BAS was minimised. Twenty rules 
covered the most likely combinations of inputs from the set \[\text{previous } μPCV = (0,±1), \]
change in output power = (Z,N,P)] (see fig 3.12 i) . Twenty-one rules were assigned
to point to stage1 μPCV change =±2 and stage2 μPCV change = ±1 in the cases
where large changes in the measured variables gave input fuzzy memberships
which indicated large changes in irradiance or some other gross disturbance. A
further twenty-four rules had stage1 μPCV change =±2 as a premise, and directed
the new change in μPCV to ±1, depending upon whether or not the previous μPCV
change =±2 gave an improved result.

FIB.BAS was based on FPC.BAS, but had an additional nine heavily weighted rules
which used changes in the irradiance to force changes in μPCV = ±1 as
appropriate. Presuming that the irradiance had stabilised, the next iteration of the
program would then use the first forty-one rules to either continue, halt, or reverse
the change in μPCV. As discussed in §3.2 , the use of a single measured irradiance
is contrary to the assumption of independence of the irradiance on the three PV
panels and the possibility of uneven irradiance on the active surface of the PV
panels. The purpose of FIB.BAS was to compare the function of a FLES which had
no direct measure of the converter output powers with one which did (FPC.BAS), in
conditions of even irradiance.

Due to the slow execution of uncompiled BASIC code, the fuzzy tracking programs
had a minimum iteration period of six seconds. The simple trackers could be run at
down to two seconds, but for test purposes were limited to six second iterations. Six
second iterations are sufficiently frequent to cope with most conditions other than
fast moving patchy cloud cover.
§3.4 Comparison of Performance of the Different Control Strategies

§3.4.1 The Test Conditions

The PV panels were fixed in a parallel array for testing. Fig 3.13 shows the arrangement of the panels in a steel frame with a steel easel support.

In order to compare the different control strategies, definitive and repeatable tests had to be used. Two distinct test situations can be arranged:

1. Panel irradiance altered in step changes, either an individual panel or in groups.

   This requires a steady light source of measurable irradiance equivalent to sunlight. If the light source is solar (a sunny day) then the panel irradiance can only be altered by partial shading. A beige cotton sheet was used to cover either all the panels or just panel A (LA-63) by quickly spreading a smooth single layer of fabric over the appropriate panel surface(s). The lightmeter sensor could also be covered, ideally at the same time as the panels, to give a measure of the shaded irradiance. For measured unshaded solar irradiances above 300Wm⁻², a single layer of fabric decreased the measured irradiance by 40-60%, usually very close to 50%. Perhaps due to the greater blocking of UV and blue light, as opposed to longer wavelengths, this gave a poorer power output than a spectrally even filter would have done. However, the simplicity of the sheet system, and its ability to be rapidly applied or removed outweighed its spectral transmittance characteristics. Artificial lighting of an equivalent average irradiance and spectral content to sunlight, with a spatially even
irradiance over the area of the panel array (2m\(^2\)), was considered both prohibitively expensive and difficult to implement, and was not used.

2. Panel irradiance altered gradually, either an individual panel or in groups
Given that the only available suitable light source was solar, the most realistic test of the interface control systems was to test them in conditions where the weather, particularly irradiance and temperature, varied with time. Since the weather does not occur in reproducible patterns, the only sure way to compare the effectiveness of different interface control systems would be to have multiple units of the panel/interface/battery system and run them simultaneously in the same environment. This approach was not considered for this project, but some testing under moving and variable cloud cover was carried out. This allowed crude evaluation of the real-life capabilities of different control systems.

Extensive preliminary testing was carried out prior to final comparison of the different \(\mu P\) control systems. Cloudless days were particularly useful, both for checking and debugging the software without the complication of erratic irradiance, and also for testing the hardware in high stress conditions. By running the system during both sunny and cloudy weather conditions it was possible to modify the rule weighting and scaling of the crisp changes in converter output currents/powers for the fuzzy controllers so that better performance was achieved. Performance was evaluated on the basis of rapidity of stabilisation after startup or a change in irradiance, and the power output to the battery bus after stabilisation.

In order to have an accurate record of the performance of the interface, file logging under a facility in the communications package, ProCom Plus, was used. The controller software was enlarged with formatted print statements covering all the controller inputs and measured circuit parameters plus irradiance. During each iteration of the controller software, the data echoed to the PC screen was also added to a text file, FILENAME.LOG. Selected data from the log files could then be extracted and examined as a discrete function of time. Data of particular interest were the output power to the battery bus, which was recorded in a form calibrated to \(\pm 20\%\) by the Tektronix TDS-520 oscilloscope and co-requisite current probe, the absolute values/changes in \(\mu PCV\) and the irradiance. Other variables directly affecting the control systems were also selectively extracted:- the fuzzy memberships of change in converter output current/power, the absolute values and changes in output current/power from the first stages, and the panel voltages. Graphs of these variables vs. time show how the systems performed. In conjunction
with oscilloscope printouts made during the generation of .LOG files, a comparison of the different controllers could be made.

On July 20 1993, the atmospheric conditions were as good as could be expected in a Christchurch Winter (see App. C for details). A NE breeze cleared the air of smog and no clouds were visible in the sky during the time of the trials (11:30 am to 3:15pm). The air temperature was 10-13°C during this time. Step changes in irradiance of the panels could be arranged with the full level measured irradiance known to be stable at about 600Wm⁻². Application of the sheet reduced the measured irradiance of the covered area to about 300Wm⁻². In order to ensure that a fair comparison could be made, the fuzzy controller which had previously shown the best performance in informal trials (using FPC.BAS) was trialed first, in the most intense and bluest light of midday and again last, in the fading and reddening light at 3pm. The other controller versions were trialed in between, and their performance compared with the early and late performance of the FPC.BAS-based controller.

A critical test was to compare the power output to the battery for different control systems, after stabilisation in response to a covering of all the panels, when the system had previously been in a stable state with all the panels fully irradiated. "stabilisation" was determined to be a state where the average first stage µPCV was zero, and each first stage converter's µPCV was restricted to 0 and ±1, with a time average of about zero also. The controllers tended to overshoot their target µPCV, so impending stabilisation was indicated by a change in sign of the µPCVs which had previously been adjusting monotonically. The time taken to reach stabilisation was also noted, as an important parameter of performance for conditions where the irradiance is unstable. The control system must be able to react to and track the changes in irradiance in a shorter time than the period of irradiance fluctuations, otherwise it will be continually seeking a target which is changing too fast to be tracked. Factors which affected the performance of each controller version were considered, either as strengths/flaws in the controller strategy, or strengths/flaws in the realisation of that strategy. The implications of the results are discussed in §4.2.

§3.4.2 Test Results

Figures 3.14-20 show the results of step changes in irradiance on 20 July 1993 for controller software FPC.BAS (from A20793.LOG), FIB.BAS (from B20793.LOG) and simple tracker program PA6S.BAS (from F20793.LOG). The results for FY.BAS were neglected because they were indicative of software inferior to that of FPC/FIB.BAS (see §4.2 for discussion). Results for PA2S.BAS (2 second iteration period version of PA6S.BAS) could not be directly compared with that of the 6
second iteration period software. Figure pair 3.15-16 shows results for FPC.BAS, fig. pair 3.17-18 shows results for FIB.BAS, and fig. pair 3.19-20 shows results for PA6S.BAS.

Fig 3.14 shows composite TDS-520 oscilloscope output power traces. The mean output powers were calculated by the TDS-520 DSP. The upper graph compares the steady state interface output powers for three different control systems. The top trace is for FPC.BAS at midday, which acts as a reference. The next highest trace shows the steady state power output under FPC.BAS when the panels were covered by the sheet. This can be compared with the two lower traces for FIB.BAS and PA6S.BAS, which were obtained from 1-2:30pm. The lower graph uses the 3pm full sun steady state output under FPC.BAS as a reference (top trace). The next highest trace shows the shaded FPC.BAS performance at 3pm and the two lower traces are identical to those in the upper graph. The shaded performances are comparable, with FPC.BAS showing slightly higher output powers. These results do not conclusively determine which is the best controller.

The first figure of each pair (figs 3.15/17/19) presents irradiance, voltage and $\Delta \mu$PCV data. The second figure of the pair (figs 3.16/18/20) presents irradiance and power output data. In all the graphs, breaks in the data lines cover times when the interface and controller were considered to be in a steady state. The data for the undisplayed "steady state" sections can be seen in the appropriate .LOG files (App. E).

Fig 3.15 (top graph) shows that the battery bus voltage ($V_{out}$) was steady at about 250V. However, the intermediate voltage ($V_{int}$) tended to climb above its set limit of 100V (a voltage that was determined for the protection of the 200V rated MOSFETs of the first stage), after an initial dip at startup. This poor regulation of intermediate voltage was a common feature of all the control systems. The loss of regulation was characterised by high $\mu$PCV values for the second stage, typically close to the 5V maximum set by the $\mu$P power supply, which would be expected to cause the intermediate voltage to be low, due to the high second stage duty cycle (greater than 0.8). The second stage was unable to keep the intermediate voltage below 100V, particularly when the power input to the second stage was high. A sure explanation of this problem was not found, but the problem can be interpreted as a high minimum input impedance for the second stage. Further investigation of the insensitivity of the intermediate voltage and second stage duty cycle to $\mu$PCV may find a solution. The middle and bottom graphs of fig 3.15 show the regulation of the panel voltages by FPC.BAS. The panel voltages dip at startup, but move into the
region of their respective maximum panel powers after about 20 controller iterations. The voltage override limits are exceeded at the time of the changes in irradiance, which caused the non-fuzzy section of the controller to lower the panel voltages when the irradiance was lowered and raise them again when the sheet was removed. The fuzzy control is barely used in this test, because although the changes in converter output powers at the time of changes in irradiance were sufficient to give high fuzzy memberships of LN/BP sets (App. E - refer to A20793.LOG), the irradiance based panel voltage overrides dictate the response. Fig 3.16 shows that tracking for maximum output power is poor, based upon good performance by stage1b and erratic tracking in stages1a/1c.

Figs 3.17/18 show results for FIB.BAS which expose the reasons for the poor performance of stages1a/1c. When, during the trial recorded in B20793.LOG, the sheet was placed to cover the panels, an extra fold of material covered the light sensor, giving a falsely low irradiance measurement. The subsequent excessive depression of the panel voltages caused the stage1 output powers to collapse. The restoration of accurate irradiance measurements in the shaded condition led to strong recovery by stage1b power output, but smaller improvements in stage1a/1c. The output power of the interface was barely altered, which may indicate a poor second stage efficiency that curtails marginal improvements. Removal of the sheet gave an immediate improvement in all output converter powers, but the stage1a power output decreased after this due to continual breach of the irradiance based upper voltage limit (UVL) and subsequent over-depression of VinA. Without any μPCV changes for stages1b/1c their power outputs increased. This was because the increasing intermediate voltage lifted VinB/VinC closer to their respective maximum power voltages. The lack of activity by the fuzzy controller when there was an apparent potential for greater power output indicates that the sensitivity of the fuzzy inference system to changes in output currents needs to be increased. When the stage1 μPCV was lowered to 20 by the repeated activation of the VinA UVL control, the μPCV over-override was invoked, raising the stage1A μPCV to 105. This resulted in a huge increase in stage1A power out, but the increase in power output to the battery bus was moderated by decreases in stage1b/1c output powers. The stage1B/1C decrease can be explained by a drop in the intermediate voltage which gave a flow-on decrease in VinB/VinC. The behaviour of stage1A can be explained by an error discovered in the voltage calibration. This caused VinA to be underestimated by a factor of 1.75, leading the control system to try to increase VinA to a voltage well above optimum. VinC was also underestimated, by a factor of 1.9 but the lower voltage limits for VinC were set lower than for VinA/VinB (see fig 3.6) and the power output from stage1c was not so badly affected. VinB was
accurately calibrated and the continued good performance of stage1b in spite of the faults in VinA/VinC calibration was a plus for the FPC.BAS/FIB.BAS-based control systems. Figure 4.3 (see §4.2 for discussion) shows the errors and easily applicable corrections for the panel voltage measurements that would greatly improve the performance of controllers based on FPC.BAS/FIB.BAS.

Figures 3.19/20 show results for PA6S.BAS, a simple tracker, from F20793.LOG. PA6S.BAS demonstrates the most effective tracking control in response to the step change in irradiance test. The UVL and LVL are exercised at the time of the changes in irradiance, excessively for stage1a/1c, but subsequent ±1 changes in μPCV lift the power output of the interface. The strength of the PA6S.BAS based controller is its sensitivity. While within the UVL/LVL criteria, it responds to the sign of converter power output changes, no matter how small. This allows it to extract the marginal benefits of very small changes in panel voltages. However, the limited size of ΔμPCV makes the startup slow (30 iterations compared with the 20 typical of FPC.BAS/FIB.BAS).
Fig 3.14  Power output waveforms for the different control systems. Top: FPC.BAS tested at noon. Bottom: FPC.BAS tested at 3pm
Fig 3.15 FPC.BAS operating conditions and tracking control during step changes in measured irradiance. The time domains for all three graphs are the same.
Fig 3.16 FPC.BAS Top: converter output power during step changes in irradiance.
Bottom: interface output power during step changes in irradiance.
Fig 3.17  FIB.BAS operating conditions and tracking control during step changes in measured irradiance. The time domains for all three graphs are the same.
Fig 3.18  FIB.BAS: Top: converter output power during step changes in irradiance.  Bottom: interface output power during step changes in irradiance.
Fig 3.19 PA6S.BAS operating conditions and tracking control during step changes in measured irradiance. The time domains for all three graphs are the same.
Fig 3.20  PA6S.BAS performance during step changes in irradiance

PA6S.BAS Power tracking performance

PA6S.BAS : Power and irradiance
CHAPTER 4 DISCUSSION AND CONCLUSIONS

The strengths and weaknesses of the interface will be discussed in this chapter, and suggestions for improvements will be made. §4.1 briefly covers the energy efficiency of the interface hardware, and examines the value of a panel voltage tracking system. Suggested methods for self-powering of the interface are included. §4.2 discusses the relative merits of the control systems that were described in §3.4 and contains suggestions for future modifications. §4.3 summarises the research covered by this thesis.

§4.1 Energy Efficiency - tracing losses from the Panels to the Batteries

The energy efficiency of the interface has to be considered in global terms, which means that the start of the energy transfer scheme is the photon energy input and the end is the electrical energy delivered to the battery bus. This concept is illustrated in fig 4.1

![Diagram](image)

Fig 4.1 global efficiency

\[ E_{\text{in}} = \text{photon energy incident on panel area} \]

\[ E_{\text{out}} = \text{electrical energy delivered to the battery bus} \]

\[ \eta_{\text{global}} = \frac{E_{\text{out}}}{E_{\text{in}}} \]

The panel area available in this project was about 2m². Note that this refers to the area of the frame, which includes inactive portions (see the thesis introduction). This allows an expected maximum rate of incident photon energy of 2000W. The maximum rate of energy output for a 1000Wm⁻² panel irradiance according to the
manufacturer's data (see App. A) is 171W, so the expected energy efficiency of the panels is 8.6%. This is the major loss between the incident photon energy and the batteries. Until panel costs per peak watt can be reduced significantly, a more efficient means of transforming photon energy is developed, or the panel irradiance can be increased by passive intensifiers, photovoltaic panels will remain a marginal energy source [Zweibel 1990].

The following discussion of energy losses assumes that panel protection diodes are not used. This is because they are not essential for the function of the first stage boost converters and can be replaced by non-lossy protection devices such as metal oxide varistors (MOVs). The conduction losses in the cables between the panels and the rest of the interface hardware were significant. Up to 1.3Ω was in series with each panel. Given that both the LA-63 and the LA-45 panels output 3A, this represents a potential peak loss of 11.7W. Thus the energy efficiency up to the first stage converters is 8%, and of the energy available at the panel terminals, 7% can be lost in the cables. An easy way to improve efficiency would be to shorten the cables. The best principle to follow is: increase the voltage/decrease the current at the start of power transfer chain so that conduction losses are minimised. The final form of the interface would best be placed close to the panel structure.

The first stage converters had an efficiency of approximately 75%. This varied greatly with the total power transfer in each of the first stages, decreasing with power transfer. A near-fixed loss was set by the self-powering of the converters. A separate 12V power supply was a part of each stage one converter. This was derived from a 7812 linear regulator which was powered by the panel to which the converter was connected. The power supply had to supply the requirements of the SG3526 and its MOSFET gate driver (see §2.1.2.5 and eq 2.7). The panel with the highest voltage also had to power the second stage. An estimate of the power drawn by each converter is 3W. Thus a further 12W may be taken as a fixed loss in the power supplies for the converters. The final loss in the power transfer chain was in the second stage converter. Second stage efficiency was estimated to be 65%. It was certainly lower than in the first stage converters, as the current inputs were near equal but the voltages were much higher in the second stage, leading to greater switching losses in the (higher voltage rating) MOSFETs/IGBTs. The second stage inductor also had a higher resistance.

The estimated maximum power that could be delivered to the battery is 72W. Including fixed losses, this is equivalent to a 42% interface efficiency and 3.6% global efficiency ($\eta_{\text{global}}$). The interface efficiency can be improved by the use of
advanced converter technologies, such as resonant switching topologies [Mohan], but it is clear that the photovoltaic conversion efficiency is the limit to performance. An interface which is relatively inefficient at converting the energy it receives can be effective if it is able to maximise the energy it receives by forcing the panels to be at their maximum power voltage (see the thesis introduction).

A hypothetical situation can be used to evaluate the worth of panel voltage tracking. If the panel output powers are (2 by LA-63 and 1 by LA-45 respectively) 60W (at 20V), 60W (at 20V) and 40W (at 16V) in high irradiance conditions, the cable to converter losses and the control power requirements are insignificant, the first stage efficiencies are 70% and the second stage efficiency is 60%, the output power to the battery is 67.2W. If the irradiance drops by 5% and the panel voltages are held constant by a closed loop controller, the panel output powers will drop to, say, 50W (at 20V), 50W (at 20V) and 30W (at 16V). The first stage efficiency might rise to 75% and the second stage efficiency might rise to 65%, and the output power is 63.375W. If a tracking controller lowers the panel voltages so that they are at the new maximum power voltages, the panel output powers may be 55W (at 19.5V), 55W (at 19.5V) and 35W (at 15.5V). The first/second stage converter efficiencies may drop to 72%/62% but the power output is an improved 64.728W.

In practice, a closed loop controller will not be able to regulate the panel voltages precisely. The panel voltages will sag when the irradiance drops and vice-versa. This may allow a closed loop controller to track the panel maximum power voltage, but the precision of tracking is likely to be limited to a small range of irradiance variation. For small scale photovoltaic installations, closed loop control with an optimised error in regulation will be preferable to systems with fixed losses in the tracking controller.

The interface developed for this project used photovoltaic power to activate the converter controller chips via 12V linear regulators. Each first stage controller was powered by the connected panel, and the second stage converter was powered by the panel with the highest voltage. This means only the converters that are converting significant power are activated. The converters continue to operate until their power supply voltage drops below 8V (see App. B). Thus, in all but dark conditions the panel voltages will not drop below 8V. Panel voltages below 8V are a good criterion for operation of an automatic shutdown system. The μP 5V and PC power supplies were derived from the mains. It was intended that the LEMs would be powered photovoltaically via a specialised power supply that can form a ±15V supply from a (single sided) +5V supply (see MAX742/743 specifications in App. B).
However, the +5V rail was derived from the mains because the small scale of the photovoltaic system was insufficient for extended self-powering. The self-powering system should activate the interface whenever the potential net power output is positive, and should be efficient so that maximum time is spent in the active condition. An improved scheme for self-powering is shown in fig 4.2. Because the LEMs consume a large fraction of the total control power requirements, a split supply generator which is able to accept a single sided input greater than 5V should be considered so that the LEM supply is taken from a node closer to the primary input than shown in fig 4.2 (see App. B). It is assumed that future versions of the interface will operate without a PC. The µP will require a ROM that contains the controller algorithm, and be able to go into low-power "sleep" mode at times when the net power output to the battery bus in active mode is negative.

Fig 4.2 proposed self powering system

For this project, a 2-stage boost conversion system was selected. This system is simpler to build than a 2-stage resonant-mode booster [Mohan]. A transformer based converter would have required three units rather than four (no need for second stage units, as the first stage converters could efficiently boost directly to the battery bus), but making high-frequency transformers is more difficult than making inductors. The critical design feature of the magnetic components of a boost converter is the maximum allowable flux density, which must be high to avoid saturation at DC currents of up to 3A. See §2.2 for details on inductor design.
§4.2 The effectiveness of Fuzzy Logic control

In §3.4, several different forms of control system were described, and the results of a repeatable test were presented. This test examined the response of the control systems to step changes in irradiance, both upward and downward. This test was not able to distinguish the different strengths of the control systems, which are apparent in conditions where the irradiance varies only slowly, rather than sharply, as in the test. This was because the voltage override limits were invoked by the collapse/overshoot of the panel voltages and the changes in the voltage override limits at the time of the irradiance changes (see fig 3.6). Though the voltage override limits could be useful in changing the panel voltages such that the maximum available power output of the interface is regained quickly, the reliance on measurement of the a irradiance of a single spot was shown to be unwise by the results shown in figs 3.17/18. The errors in calibration of panel A and panel C voltages caused stage1a, and to a lesser extent, stage1c to be forced away from their maximum power output operation points. A common feature of the $\Delta \mu$PCV values for stages1a/c was repeated operation of the under-voltage override limits until the measured panel voltages were within the set limits and then a few iterations in which the basic controllers (correctly) lowered the panel voltages until the overrides began to operate again (see figs 3.15-20 and the .LOG files in App. E). Fig 4.3 shows how the calibration may be corrected, according to the scaling of the digitised input voltages in the software listed on disk in App. D.

Fig 4.3 Correction of wrongly calibrated panel voltages. Vina needs to be multiplied by 1.75, Vinb multiplied by 1.06 and offset by Vinb(0) = 1.51V, and Vinc needs to be multiplied by 1.9.
Given that the calibration is corrected, the suggested aim for future work is reduction of reliance on irradiance measurements and usage of trackers based on maximisation of converter output power. This can be accomplished on two fronts:-

i) widening of the voltage override limits, and/or accurate determination of the analytic form of the ideal panel voltage as a function of irradiance. Note that the "ideal" panel voltages (such that the power output to the battery is maximised) are dependent upon many more variables than just irradiance, and the emphasis should be placed on widening the limits so that the basic controllers can operate freely to find the truly ideal operating points.

ii) increasing the resolution of output power changes in the basic controllers so that the hill-climbing algorithm can successfully keep the interface at the point of absolute maximum output power.

Based on ii), some specific suggestions about how to realise the potential of the fuzzy controllers can be made. First, the fuzzy memberships for the groups representing a small change in output power should be made to rise more sharply from the origin, as shown in fig 4.4 (see also fig 3.12i).

![Fig 4.4 suggested fuzzy memberships for converter power output changes](image)

The purpose of the narrowing of the Z group and concurrent squeezing of the P/N groups shown in fig 4.4 is to emulate the sensitivity of the simple tracker to changes in power, but retain the noise reduction afforded by the fuzzy blending of the border between perceived small change and nil change. The noise level in the measured converter power output changes will be comparable to of the width of the Z group. Because of normalisation of the changes, the actual width of the Z group will have to be a compromise value that represents twice the relative noise amplitude at a moderate level of absolute output. Flow-on effects include:- a need for new fuzzy groups to cover the region between small and large changes, since the groups P/N would otherwise be spanning a wide range of values; and an increase in weighting
of rules relating Z group membership with no change in $\mu$PCV, since the narrower Z grouping allows a more certain conclusion that the power output change is very close to zero.

The fuzzy sets representing large changes in converter power output (BP/LN) will become more useful as the voltage override limits are widened. The fuzzy memberships of these groups was high at the times of step changes in irradiance (see .LOG files in App. E), but the firing of rules which had membership of sets BP/LN was ineffective due to the activity of the voltage overrides at the same time.

The optimisation of fuzzy set memberships is a topic of current research throughout the world, and the analytical improvement of the fuzzy control system will rely on developments in this field [Lotfi 1993].

The fuzzy rulebase for FPC.BAS (see App. D) is considered to be appropriate for the interface. The aliasing of the input fuzzy membership functions was large enough, so that a small number of rules could cover all possible input states. This meant that the interface was never in a state of indeterminate control, as at least one rule per converter was sure to fire.

A better rulebase for the interface could be made by further investigation of the most effective input/output function of the controller. The different weighting of rules should be emphasised, so input patterns which more strongly indicate that a particular output should be made are dominant in the rulebase (see §3.3.3).

To take advantage of the improved resolution of the fuzzy software, corresponding reduction in the minimum value of $\Delta \mu$PCV is required. A 16-bit microprocessor would have a greater resolution, but at a cost. A cheaper method, using only two extra op-amps is shown in fig 4.5. If the gain of the first stage for $\mu$PCV is $y$, where $y$ domain is $-1<y<0$, the error amplifier output voltage resolution is improved.

![Fig 4.5 increasing the error amplifier resolution (compare with fig 2.7)](image)
The first stage also sums \(\mu_{PCV}\) and the reference voltage \(V_{\text{ref}}\), which is equal to the minimum required value of \(\mu_{PCV}\) (depends on the minimum required duty cycle of a particular converter). This gives the relation between the error amplifier output \(V_{E\text{Aout}}\) and input to the first stage op-amp shown in eq 4.1.

\[
V_{E\text{Aout}} = V_{\text{ref}} - y(\mu_{PCV} - V_{\text{ref}}) \quad \text{(without an input pot)} \quad \text{eq 4.1}
\]

if \(y = -0.5\) then \(V_{E\text{Aout}} = -(-0.5V_{\text{in}} - 0.5V_{\text{ref}})\)

The response for \(y = -0.5\) shown in eq 4.1 is correct and the error amplifier output is always greater than \(V_{\text{ref}}\), but has a resolution of \(5/(255*0.5)\text{mV} = 9.8\text{mV}\). If \(y > -0.5\) then either the gain for \(V_{\text{ref}}\) must be increased, or the input potentiometer must be set to reduce the sensitivity to \(\mu_{PCV}\). If \(y > -0.5\) (which gives greater resolution than \(y < -0.5\)) then the first stage gain for \(V_{\text{ref}}\) must be reduced by the factor of \(-y/(1+y)\).

### §4.3 Summary

The solar powered battery charger interface designed and built for this project was found to operate successfully. Interface control systems were developed using an 80451C microprocessor, and these attempted to maximise the battery charging power. Regulation of the intermediate voltage by \(\mu\)P control is the only remaining challenge to the working of the interface in principle. Faults in the calibration of panel voltage measurements prevented the control systems from operating to their potential. Solutions for these faults, as well as suggestions for increasing the potential performance are given in §4.2. Further improvement could be made by using a software language and or \(\mu\)P which makes more frequent tracking iterations possible. Six second iteration periods were the limit of the execution speed of the uncompiled BASIC code. The suggested maximum iteration period is 1 second, so that irradiance changes due to fast moving clouds can be tracked.

This project has demonstrated the potential worth of fuzzy logic in maximising solar powered charging of a high voltage battery bus. Fuzzy logic is suitable for this application, since the ideal controller output is a complex function of irradiance, PV panel temperature, and interface losses. The separation of the power input into three separate panel units that can interact in the interface further complicates the system under control. This means that it is difficult to arrange an analytic control function. A fuzzy logic expert system can allow good control with minimal understanding of the control function for the interface. The costs of microprocessor control are not dependent upon the software used (after the initial development) and it is worth the effort of tuning the fuzzy input membership functions and rules so that the power maximising tracking control is very accurate.
The costs associated with building an interface that can maximise solar powered charging of a battery are small in comparison with the cost of PV panels [Enslin 1990] and the costs become proportionally smaller as the size of the array becomes larger. The first application of this project will be the EEE-EV and this will provide publicity for the concept of solar power. It is hoped that an interface controlled by fuzzy logic for larger PV panel arrays will also be built.
CHAPTER 5 REFERENCES

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fuzzy-server@til.com, the email server for Togai InfraLogic. Send email to fuzzy-server@til.com and put <help> in the body of the mail or try info@til.com

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APPENDIX A  PV PANEL SPECIFICATIONS

LA321K45
HIGH EFFICIENCY MULTICRYSTAL PHOTOVOLTAIC MODULE
TYPICAL OUTPUT 45.2 Watts
SELF REGULATING TYPE

HIGHLIGHTS OF KYOCERA PHOTOVOLTAIC MODULES

Kyocera's advanced cell processing technology and automated production facilities have produced a highly efficient multicrystal solar modules.
The conversion efficiency of the Kyocera solar cell is over 14%.
These cells are encapsulated between a tempered glass cover and an EVA potant with PVF and aluminum foil back sheet to provide maximum protection from the severest environmental conditions.
The entire laminate is installed in an anodized aluminum frame to provide structural strength and ease of installation.

APPLICATIONS

- Microwave/Radio repeater stations
- Electricity to villages in remote areas
- Medical facilities in rural areas
- Power source for summer vacation homes
- Emergency communication systems
- Water quality and environmental data monitoring systems
- Navigation lighthouses, and ocean buoys
- Pumping systems for irrigation, rural water supplies and livestock watering
- Aviation obstruction lights
- Cathodic protection systems
- Desalination systems
- Recreational vehicles
- Railroad signals
- Sailboat charging systems

SPECIFICATIONS

<table>
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<th>Electrical Specifications</th>
<th>Physical Specifications</th>
</tr>
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<tr>
<td><strong>MODEL</strong></td>
<td><strong>LA321K45</strong></td>
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<tr>
<td>Output</td>
<td>45.2 Watts</td>
</tr>
<tr>
<td>Open-circuit Voltage</td>
<td>18.9 Volts</td>
</tr>
<tr>
<td>Short-circuit Current</td>
<td>3.23 Amperes</td>
</tr>
<tr>
<td>Length</td>
<td>800 mm (31.5 in.)</td>
</tr>
<tr>
<td>Width</td>
<td>445 mm (17.5 in.)</td>
</tr>
<tr>
<td>Depth</td>
<td>36 mm (1.4 in.)</td>
</tr>
<tr>
<td>Weight</td>
<td>3.2 kg (7.1 lbs.)</td>
</tr>
</tbody>
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Notes:
The above specifications are under test conditions at maximum of 1.5 suns illuminations of 1000 milliwatts per square meter.
Kyocera reserves the right to modify these specifications without notice.
Custom made terminations and modules are also available upon request.
QUALITY ASSURANCE
Kyocera multicrystal photovoltaic modules exceed government specifications for the following tests:
- Thermal cycling test
- Thermal shock test
- Thermal-Freezing and high humidity cycling test
- Electrical isolation test
- Hail impact test

- Mechanical, wind and twist loading test
- Salt mist test
- Light and water-exposure test
- Field exposure test

Please contact our office to obtain quotes without hesitation.
These cells are encapsulated between a tempered glass cover and an EVA material and aluminum foil back sheet to provide maximum protection from the severest environmental conditions. The entire laminate is installed in an anodized aluminum frame to provide structural strength and ease of installation.

**APPLICATIONS**

- Microwave/Radio repeater stations
- Electrification of villages in remote areas
- Medical facilities in rural areas
- Power source for summer vacation homes
- Emergency communication systems
- Water quality and environmental data monitoring systems
- Navigation lighthouses, and ocean buoys
- Pumping systems for irrigation, rural water supplies and livestock watering
- Aviation obstruction lights
- Cathodic protection systems
- Desalinization systems
- Recreational vehicles
- Railroad signals
- Sailboat charging systems

**SPECIFICATIONS**

<table>
<thead>
<tr>
<th><strong>Electrical Specifications</strong></th>
<th><strong>Physical Specifications</strong></th>
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<td><strong>MODEL</strong></td>
<td><strong>Size</strong></td>
</tr>
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<td>445 x 90 x 35 mm</td>
</tr>
<tr>
<td>Output</td>
<td>62.7 Watts</td>
</tr>
<tr>
<td>Optimum Voltage</td>
<td>20.7 Volts</td>
</tr>
<tr>
<td>Optimum Current</td>
<td>3.03 Amps</td>
</tr>
<tr>
<td>Open Circuit Voltage</td>
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<tr>
<td>Short-Circuit Current</td>
<td>5.25 Amps</td>
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<td>Length</td>
<td>1955 mm (77.0 in.)</td>
</tr>
<tr>
<td>Width</td>
<td>445 mm (17.5 in.)</td>
</tr>
<tr>
<td>Depth</td>
<td>35 mm (1.4 in.)</td>
</tr>
<tr>
<td>Weight</td>
<td>7.3 kg (16 lbs.)</td>
</tr>
</tbody>
</table>

*Note: The physical specifications are approximate and may vary depending on the manufacturer's specifications and conditions.*
Electrical Characteristic

I-V characteristic of solar module LA441K63 at various cell temperature and irradiance levels.

Environmental Conditions

<table>
<thead>
<tr>
<th>Operating temperature</th>
<th>-40 ~ +90°C</th>
</tr>
</thead>
<tbody>
<tr>
<td>Storage temperature</td>
<td>-40 ~ +90°C</td>
</tr>
</tbody>
</table>

QUALITY ASSURANCE

- Thermal cycling test
- Thermal shock test
- Thermal/Freezing and high humidity cycling test
- Electrical isolation test
- Hail impact test
- Mechanical, wind and twist loading test
- Salt mist test
- Light and water-exposure test
- Field exposure test

Please contact our office to obtain details without hesitation.

PHOTOCOMM, INC.
Solar Electric Systems

PH: 916-477-5121
FAX: 916-477-5751
TELEX: 82366

930 Idaho Maryland Rd.
Grass Valley, CA 95945

The contents of this catalog are subject to change without prior notice for further improvement.
Appendix B  PCBs and Schematics

PCF8591 A/D-D/A, as used in the 80C451 kit supplied by Industrial Research Ltd., Christchurch

Fig. 2 Pinning diagram.

FUNCTIONAL DESCRIPTION

Addressing

Each PCF8591 device in an I²C bus system is activated by sending a valid address to the device. The address consists of a fixed part and a programmable part. The programmable part must be set according to the address pins A0, A1 and A2. The address always has to be sent in the first byte after the start condition in the I²C bus protocol. The last byte of the address byte is the read/write bit which sets the direction of the following data transfer (see Figs 2 and 10).

Data transfer

The second byte sent to a PCF8591 device will be stored in its control register and is required to control the device function.

The upper nibble of the control register is used for enabling the analog output, and for programming the analog inputs as single-ended or differential inputs. The lower nibble selects one of the analog input channels defined by the upper nibble (see Fig. 8). If the analog channel flag is set the channel number is incremented automatically after each A/D conversion.

The selection of a new existing input channel results in the highest available channel number being adjusted. Therefore, if the next available channel will be always channel 0. The most significant bit of both nibbles are reserved for future functions and have to be set to 0.

After a power-on reset condition all bits of the control register are reset to 0. The D/A converter and the oscillator are disabled for power saving. The analogue output is switched to a high impedance state.
Fig B.1 the final PCB versions used for the project.
### Electrical Characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Characteristic</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>I_CBO</td>
<td>Collector Dark Current</td>
<td>0.25</td>
<td>25</td>
<td></td>
<td>nA</td>
<td>$V_{CE} = 10$ V. $T_J = 85^\circ$ C (Note 5)</td>
</tr>
<tr>
<td>I_CBO</td>
<td>Collector Dark Current</td>
<td>0.025</td>
<td>0.5</td>
<td></td>
<td>µA</td>
<td>$V_{CE} = 10$ V. $T_J = 85^\circ$ C (Note 5)</td>
</tr>
<tr>
<td>I_CEO</td>
<td>Collector Dark Current</td>
<td>2.0</td>
<td>100</td>
<td></td>
<td>nA</td>
<td>$V_{CE} = 5.0$ V.</td>
</tr>
<tr>
<td>R_CB</td>
<td>Responsivity (Tungsten)</td>
<td>0.8</td>
<td>1.6</td>
<td></td>
<td>µA/mW</td>
<td>$V_{CE} = 10$ V. $H = 5.0$ mW/cm² (Notes 3 and 6)</td>
</tr>
<tr>
<td>R_CB</td>
<td>Responsivity (GaAs)</td>
<td>0.8</td>
<td>1.0</td>
<td></td>
<td>µA/mW</td>
<td>$V_{CE} = 10$ V. $H = 5.0$ mW/cm² (Notes 3 and 6)</td>
</tr>
<tr>
<td>I_CEO()</td>
<td>Photo Current (Tungsten)</td>
<td>1.8</td>
<td>4.8</td>
<td></td>
<td>µA/mW</td>
<td>$V_{CE} = 10$ V. $H = 5.0$ mW/cm² (Notes 3 and 6)</td>
</tr>
<tr>
<td></td>
<td>FPT100/A/B</td>
<td>1.6</td>
<td>3.0</td>
<td></td>
<td>µA/mW</td>
<td>$V_{CE} = 10$ V. $H = 5.0$ mW/cm² (Notes 3 and 6)</td>
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<td>I_CEOH</td>
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<td>mA</td>
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<td></td>
<td>FPT100/A/B</td>
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<td>0.88</td>
<td></td>
<td>mA</td>
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<td>I_CE(H)</td>
<td>Photo Current (GaAs)</td>
<td>0.6</td>
<td>4.2</td>
<td></td>
<td>mA</td>
<td>$V_{CE} = 5.0$ V. $H = 5.0$ mW/cm² (Note 7)</td>
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<tr>
<td></td>
<td>FPT100/A/B</td>
<td>0.6</td>
<td>2.7</td>
<td></td>
<td>mA</td>
<td>$V_{CE} = 5.0$ V. $H = 5.0$ mW/cm² (Note 7)</td>
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<tr>
<td>t_L</td>
<td>Light Current Rise Time</td>
<td>2.8</td>
<td></td>
<td></td>
<td>µs</td>
<td></td>
</tr>
<tr>
<td>t_D</td>
<td>Light Current Fall Time</td>
<td>2.8</td>
<td></td>
<td></td>
<td>µs</td>
<td></td>
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<tr>
<td>V_CE(0)</td>
<td>Collector-to-Emitter Saturation</td>
<td>0.18</td>
<td>0.3</td>
<td></td>
<td>V</td>
<td>$I_C = 500$ µA. $H = 20$ mW/cm² (Note 5)</td>
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<tr>
<td></td>
<td>Voltage FPT100/A/B</td>
<td>0.18</td>
<td>0.33</td>
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<td>V</td>
<td>$I_C = 500$ µA. $H = 20$ mW/cm² (Note 5)</td>
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<td>B_CE</td>
<td>Collector-to-Base Breakdown Voltage</td>
<td>50</td>
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<td></td>
<td>V</td>
<td></td>
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<tr>
<td>V_CE(0)</td>
<td>Collector-to-Emitter Sustaining</td>
<td>30</td>
<td>50</td>
<td></td>
<td>V</td>
<td></td>
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<tr>
<td></td>
<td>Voltage FPT100/A/B</td>
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<td>50</td>
<td></td>
<td>V</td>
<td></td>
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<tr>
<td>E_CE</td>
<td>Emitter-to-Collector Breakdown</td>
<td>7.0</td>
<td></td>
<td></td>
<td>V</td>
<td></td>
</tr>
</tbody>
</table>

**Notes:**
1. These are guaranteed limits.
2. These ratings give a maximum junction temperature of $85^\circ$ C and a junction-to-case thermal resistance of 30°C/W (dissipation factor of 10.5 mW/°C).
3. Measured at a rated current as emitted from a tungsten filament lamp at a color temperature of 2564°K. The effective photoresponsive area is typically 211.25 mm² (FPT100/A/B) and 0.76 mm² (FPT110/A/B).
4. These are values obtained in rated conditions as emitted from a GaAs source at 900 nm.
5. Measured with radiative flux intensity of less than 0.1 µW/cm² over the spectrum from 100 to 1500 nm.
6. These are the times required for $I_C$ to rise from 10% to 90% of peak value. This time is defined as the time required for $I_{CE}$ to decrease from 90% to 10% of peak value. Test conditions are: $I_{CE} = 4.0$ mA, $V_{CE} = 5.0$ V, $R_L = 100$ Ω, GaAs source.
7. No electrical connection to base lead.

### Angular Response

**Collector Dark Current vs Temperature**

<table>
<thead>
<tr>
<th>$T_J$ (°C)</th>
<th>$I_C$ (mA)</th>
</tr>
</thead>
<tbody>
<tr>
<td>25</td>
<td>1.0</td>
</tr>
<tr>
<td>50</td>
<td>1.5</td>
</tr>
<tr>
<td>75</td>
<td>2.0</td>
</tr>
<tr>
<td>100</td>
<td>2.5</td>
</tr>
</tbody>
</table>

**Collector Base Characteristics**

### Collector Current vs Collector Voltage

**Collector Base Characteristics**

**Collector Current vs Collector Voltage**

<table>
<thead>
<tr>
<th>$V_{CE}$ (V)</th>
<th>$I_C$ (mA)</th>
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</thead>
<tbody>
<tr>
<td>1.0</td>
<td>1.0</td>
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<tr>
<td>2.0</td>
<td>1.5</td>
</tr>
<tr>
<td>3.0</td>
<td>2.0</td>
</tr>
<tr>
<td>4.0</td>
<td>2.5</td>
</tr>
</tbody>
</table>

**Collector Dark Current vs Temperature**
General Description
The FPT100 and FPT110 are 3-terminal npn Planar phototransistors with exceptionally stable characteristics and high illumination sensitivity. The availability of the base pin gives wide latitude for flexible circuit design. The case is a special plastic compound with transparent resin encapsulation that exhibits stable characteristics under high humidity conditions. The controlled sensitivities offered in the A and B versions give the circuit designer increased flexibility.

Exceptionally Stable Characteristics
Controlled Sensitivities

Absolute Maximum Ratings
Maximum Temperature and Humidity
Storage Temperature: -55°C to +125°C
Operating Temperature: -55°C to +85°C
Pin Temperature (Soldering, 5 s): 260°C
Relative Humidity at 65°C: 85%

Maximum Power Dissipation (Notes 1 and 2)
Total Dissipation at $T_C = 25°C$: 200 mW
Total Dissipation at $T_A = 25°C$: 100 mW

Maximum Voltages and Current (Note 5)
$V_{CB}$ Collector-to-Base Voltage: 50 V
$V_{CE}$ Collector-to-Emitter Sustaining Voltage (Note 3): 30 V
$I_C$ Collector Current: 25 mA

<table>
<thead>
<tr>
<th>Test Conditions</th>
<th>Units</th>
<th>Max</th>
<th>Min</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_P = 40 mA$</td>
<td>V</td>
<td>1</td>
<td>1.7</td>
</tr>
<tr>
<td>$I_H = 100 \mu A$</td>
<td>mA</td>
<td>0.1</td>
<td>0.2</td>
</tr>
<tr>
<td>$I_F = 40 mA$</td>
<td>mW</td>
<td>25</td>
<td></td>
</tr>
<tr>
<td>$P_{D} = 20 mA$</td>
<td>mW/°C</td>
<td>120</td>
<td></td>
</tr>
<tr>
<td>$I_J = 10 mA$</td>
<td>°C</td>
<td>120</td>
<td></td>
</tr>
</tbody>
</table>

Notes:
All dimensions in inches or millimeters (parentheses).
Tolerance unless specified = ±0.215 (±0.51).

Inches (mm)
HIGH INJECTION N-CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTORS (IGBT)

<table>
<thead>
<tr>
<th>TYPE</th>
<th>V_{DS}</th>
<th>I_D</th>
</tr>
</thead>
<tbody>
<tr>
<td>STH10N50</td>
<td>500 V</td>
<td>10 A</td>
</tr>
<tr>
<td>STH10N50FI</td>
<td>500 V</td>
<td>10 A</td>
</tr>
</tbody>
</table>

* HIGH INPUT IMPEDANCE
* LOW ON-VOLTAGE
* HIGH CURRENT CAPABILITY
* FAST TURN-OFF: t_f < 1.5 μs

APPLICATIONS:
* MOTOR CONTROL

N-channel High Injection POWER MOS transistors (IGBT) which feature a high impedance insulated gate input and a low on-resistance characteristic of bipolar transistors. This low resistance is achieved by conductivity modulation of the drain. These devices are particularly suited to switching motor control applications in consumer equipment such as washing machines and tumble dryers and industrial equipment motor control.

INTERNAL SCHEMATIC DIAGRAM
1. Gate
2. Drain
3. Source

ABSOLUTE MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drain-source voltage</td>
<td>V_{DS}</td>
<td>500 V</td>
</tr>
<tr>
<td>Gate-source voltage</td>
<td>V_{GS}</td>
<td>40 V</td>
</tr>
<tr>
<td>Drain current (contin.) at T_J = 25°C</td>
<td>I_D (C)</td>
<td>30 A</td>
</tr>
<tr>
<td>Drain current (pulsed)</td>
<td>I_D (P)</td>
<td>30 A</td>
</tr>
<tr>
<td>Total dissipation at T_J &lt; 25°C</td>
<td>P_{D}</td>
<td>100 W</td>
</tr>
<tr>
<td>Derating factor</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Storage temperature</td>
<td>T_{STG}</td>
<td>-65 to 150 °C</td>
</tr>
<tr>
<td>Max. operating junction temperature</td>
<td>T_J</td>
<td>150 °C</td>
</tr>
</tbody>
</table>

(*) Pulse width limited by Safe operating area

June 1988
### THERMAL DATA

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{th,j-case}$</td>
<td>Thermal resistance junction-case</td>
<td>max</td>
<td>1.25</td>
<td>3.57</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

### ELECTRICAL CHARACTERISTICS ($T_j = 25^\circ C$ unless otherwise specified)

#### OFF

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DS(OFF)}$</td>
<td>Drain-source breakdown voltage</td>
<td>$I_D = 250 \mu A$</td>
<td>$V_{GS} = 0$</td>
<td>500</td>
<td>V</td>
</tr>
<tr>
<td>$I_{oss}$</td>
<td>Zero gate voltage drain current ($V_{DS} = 0$)</td>
<td>$V_{DS} = \text{Max Rating}$</td>
<td>$V_{DS} = \text{Max Rating} \times 0.8$</td>
<td>$T_j = 125^\circ C$</td>
<td>250</td>
</tr>
<tr>
<td>$I_{GSS}$</td>
<td>Gate-body leakage current ($V_{DS} = 0$)</td>
<td>$V_{GS} = \pm 20 V$</td>
<td></td>
<td></td>
<td>$\pm 100$</td>
</tr>
</tbody>
</table>

#### ON (*)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{GS(HI)}$</td>
<td>Gate threshold voltage</td>
<td>$V_{GS} = V_{GS}$</td>
<td>$I_D = 250 \mu A$</td>
<td>2</td>
<td>4</td>
</tr>
<tr>
<td>$V_{DS(HI)}$</td>
<td>Drain-source voltage</td>
<td>$V_{DS} = 15 V$</td>
<td>$I_D = 10 A$</td>
<td>$T_j = 100^\circ C$</td>
<td>2.7</td>
</tr>
</tbody>
</table>

### DYNAMIC

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$g_m$</td>
<td>Forward transconductance</td>
<td>$V_{GS} = 20 V$</td>
<td>$I_D = 10 A$</td>
<td>2.5</td>
<td>mS</td>
</tr>
<tr>
<td>$C_{iss}$</td>
<td>Input capacitance</td>
<td>$V_{GS} = 25 V$</td>
<td>$f = 1 MHz$</td>
<td>850</td>
<td>pF</td>
</tr>
<tr>
<td>$C_{oss}$</td>
<td>Output capacitance</td>
<td>$V_{GS} = 0$</td>
<td></td>
<td>90</td>
<td>pF</td>
</tr>
<tr>
<td>$C_{rss}$</td>
<td>Reverse transfer capacitance</td>
<td></td>
<td></td>
<td>40</td>
<td>pF</td>
</tr>
</tbody>
</table>

### SWITCHING

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{r}$</td>
<td>Turn-on delay time</td>
<td>$V_{GS} = 400 V$</td>
<td>$I_D = 10 A$</td>
<td>100</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{f}$</td>
<td>Rise time</td>
<td>$V_{GS} = 15 V$</td>
<td>$R_D = 100 \Omega$</td>
<td>700</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{f}$</td>
<td>Turn-off delay time</td>
<td></td>
<td></td>
<td>500</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{f}$</td>
<td>Fall time</td>
<td></td>
<td></td>
<td>800</td>
<td>ns</td>
</tr>
</tbody>
</table>

---

*SGS-THOMSON*
Power Field Effect Transistor
N-Channel Enhancement-Mode
Silicon Gate TMOS

These TMOS Power FETs are designed for low-voltage, high-speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds
- Low RDS(on) to Minimize On-Losses. Specified at Elevated Temperature
- Rugged - SOA is Power Dissipation Limited
- Source to Drain Diode Characterized for Use With Inductive Loads

MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Device</th>
<th>IRF640</th>
<th>IRF641</th>
<th>IRF642</th>
<th>IRF643</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDS (DSS)</td>
<td>200 V</td>
<td>150 V</td>
<td>200 V</td>
<td>150 V</td>
</tr>
<tr>
<td>VGS(th)</td>
<td>200 V</td>
<td>150 V</td>
<td>200 V</td>
<td>150 V</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Source Voltage</th>
<th>VGS</th>
<th>-20 Vdc</th>
</tr>
</thead>
</table>

<table>
<thead>
<tr>
<th>Drain Current</th>
<th>ID</th>
</tr>
</thead>
<tbody>
<tr>
<td>Continuous, TC = 25°C</td>
<td>18 A</td>
</tr>
<tr>
<td>100°C</td>
<td>11 A</td>
</tr>
<tr>
<td>25°C</td>
<td>72 A</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>RDS(on)</th>
<th>0.18 Ohm</th>
</tr>
</thead>
</table>

<table>
<thead>
<tr>
<th>Power Dissipation, TC = 25°C</th>
</tr>
</thead>
<tbody>
<tr>
<td>PD</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Operating and Storage Temperature Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>TJ, TS</td>
</tr>
</tbody>
</table>

TYPICAL CHARACTERISTICS

<table>
<thead>
<tr>
<th>Rg</th>
<th>12.5</th>
<th>1°C/Ohm</th>
</tr>
</thead>
</table>

<table>
<thead>
<tr>
<th>Tj</th>
<th>300°C</th>
</tr>
</thead>
</table>
## ELECTRICAL CHARACTERISTICS (TC = 25°C unless otherwise noted)

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Symbol</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>OFF CHARACTERISTICS</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Drain-Source Breakdown Voltage</td>
<td>V_BR</td>
<td>200</td>
<td></td>
<td>Vdc</td>
</tr>
<tr>
<td>(VDS = 0, ID = 0.25 mA)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>150</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Zero Gate Voltage Drain Current</td>
<td>IDSS</td>
<td>—</td>
<td>0.2</td>
<td>mA</td>
</tr>
<tr>
<td>(VGS = 0, VDS = 0, TJ = 125°C)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>Gate-Body Leakage Current, Forward</td>
<td>IGSSF</td>
<td>—</td>
<td>100</td>
<td>nA</td>
</tr>
<tr>
<td>(VGS = 20 Vdc, VDS = 0)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Gate-Body Leakage Current, Reverse</td>
<td>IGSSR</td>
<td>—</td>
<td>100</td>
<td>nA</td>
</tr>
<tr>
<td>(VGS = 20 Vdc, VDS = 0)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ON CHARACTERISTICS*</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Gate Threshold Voltage</td>
<td>VGS(th)</td>
<td>2</td>
<td>4</td>
<td>Vdc</td>
</tr>
<tr>
<td>(ID = 0.25 mA)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Static Drain-Source On-Resistance</td>
<td>RDS(on)</td>
<td>—</td>
<td>0.18</td>
<td>Ohm</td>
</tr>
<tr>
<td>(VDS = 10 Vdc,</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ID = 10 A)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>0.22</td>
<td></td>
<td></td>
</tr>
<tr>
<td>On-State Drain Current (VGS = 10 V)</td>
<td>IDS</td>
<td>18</td>
<td>—</td>
<td>A</td>
</tr>
<tr>
<td>(VDS = 3.2 Vdc)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>16</td>
<td>—</td>
<td></td>
</tr>
<tr>
<td>Forward Transconductance</td>
<td>SFS</td>
<td>6</td>
<td>—</td>
<td>mhos</td>
</tr>
<tr>
<td>(VDS = 3.2 V, ID = 10 A)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>6</td>
<td>—</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>4</td>
<td>—</td>
<td></td>
</tr>
<tr>
<td>DYNAMIC CHARACTERISTICS</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Capacitance</td>
<td>CIF</td>
<td>—</td>
<td>110</td>
<td>pF</td>
</tr>
<tr>
<td>(VDS = 25 V, f = 1 MHz)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Capacitance</td>
<td>COS</td>
<td>—</td>
<td>70</td>
<td>pF</td>
</tr>
<tr>
<td>Reverse Transfer Capacitance</td>
<td>COSS</td>
<td>—</td>
<td>300</td>
<td>pF</td>
</tr>
</tbody>
</table>

## SWITCHING CHARACTERISTICS* | | | | |
| Turn-On Delay Time | tD(on) | — | 30 | ns |
| (VGG = 75 V, IG = 10 A, | | | | |
| VDS(on) = 4.7 Ohms) | | | | |
| Rise Time | tr | — | 60 | |
| Fall Time | tf | — | 80 | |
| Total Gate Charge | Qg | 38 | — | nC |
| Gate-Source Charge | Qgs | 16 | — | |
| Gate Drain Charge | QGD | 22 | — | |

## SOURCE DRAIN DIODE CHARACTERISTICS* | | | | |
| Forward On-Voltage | VSD | 1.8 | — | Vdc |
| (IG = Rated ID, | | | | |
| VGS = 0) | | | | |
| Forward Turn-On Time | tPD | Limited by stray inductance | | |
| Reverse Recovery Time | tRR | 450 | — | ns |

## INTERNAL PACKAGE INDUCTANCE | | | | |
| Internal Drain Inductance | Ld | 3.5 | — | nH |
| (Measured from the contact screw on tab to center of die) | | | | |
| (Measured from the drain lead 0.25" from package to center of die) | | | | |
| Internal Source Inductance | Ls | 7.5 | — | |
| (Measured from the source lead 0.25" from package to source bond pad) | | | | |

*Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2.5%. (1) Add 0.1 V for IRF640 and IRF643.
Two Stage Boost Converter, showing one of the three first stage converters and the 2nd Stage.
**Dual-Output, Switch-Mode Regulator**

(+5V to ±12V or ±15V)

**General Description**

The MAX742 DC-DC converter is a controller for dual-output power supplies in the 3W to 60W range. Relaying on simple two-terminal inductors rather than transformers, the MAX742 regulates both outputs independently to within ±4% over all conditions of line voltage, temperature, and load current.

The MAX742 has high efficiency (up to 92%) over a wide range of output loading. Two independent PWM current-mode feedback loops provide tight regulation and operation free from subharmonic noise. The MAX742 can operate at 100kHz or 200kHz, so it can be used with small and lightweight external components. Also, ripple and noise are easy to filter. The MAX742 provides a regulated output for inputs ranging from 4.2V to 10V (and higher with additional components).

External power MOSFETs driven directly from the MAX742 are protected by cycle-by-cycle overcurrent sensing. The MAX742 also features undervoltage lockout, thermal shutdown, and programmable soft-start.

Inductors and capacitors to complement the MAX742 can be ordered directly from Maxim in production quantities (see Ordering Information). Refer to the MAXL001 and MAXC001 data sheets for detailed product specifications. If 3W of load power or less is needed, refer to the MAX743 data sheet for a device with internal power MOSFETs.

**Features**

- Spec Guarantee for In-Circuit Performance
- Load Currents to ±2A
- 4.2V to 10V Input-Voltage Range
- Switches From ±15V to ±12V Under Logic Control
- ±±4% Output Tolerance Max Over Temp, Line, and Load
- 90% Typ Efficiency
- Low-Noise, Current-Mode Feedback
- Cycle-by-Cycle Current Limiting
- Undervoltage Lock-Out and Soft-Start
- 100kHz or 200kHz Operation

**Ordering Information**

<table>
<thead>
<tr>
<th>PART</th>
<th>TEMP. RANGE</th>
<th>PIN-PACKAGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>MAX742CPP</td>
<td>0°C to +70°C</td>
<td>20 Plastic DIP</td>
</tr>
<tr>
<td>MAX742CWP</td>
<td>0°C to +70°C</td>
<td>20 Wide SO</td>
</tr>
<tr>
<td>MAX742CJD</td>
<td>0°C to +70°C</td>
<td>Dice</td>
</tr>
<tr>
<td>MAX742EPP</td>
<td>-40°C to +85°C</td>
<td>20 Plastic DIP</td>
</tr>
<tr>
<td>MAX742EWP</td>
<td>-40°C to +85°C</td>
<td>20 Wide SO</td>
</tr>
<tr>
<td>MAX742MJP</td>
<td>-55°C to +125°C</td>
<td>20 CERDIP</td>
</tr>
</tbody>
</table>

Ordering Information continued on page 15.

**Applications**

DC-DC Converter Module Replacement
Distributed Power Systems
Computer Peripherals

**Pin Configuration**

| PB | 1 |
| CC | 2 |
| KMD | 3 |
| AV | 4 |
| 100Ω | 5 |
| 10Ω | 6 |
| VRF | 7 |
| CC | 8 |
| FS | 9 |

**Simplified Block Diagram**

[Diagram of the MAX742 block diagram showing the various components and connections.]
**General Description**

The MAX743 DC-DC converter IC contains all the active circuitry needed to build small, dual-output power supplies. Relying on simple two-terminal inductors rather than transformers, the MAX743 regulates both outputs independently to within ±4% over all conditions of line voltage, temperature, and load current.

The MAX743 typically provides 75% to 82% efficiency over most of the load range. It operates with current-mode feedback at 200kHz, so it can be used with small, lightweight external components. Also, ripple and noise are easy to filter.

The MAX743 is inherently reliable due to its internal power transistors and monolithic construction. Thermal shutdown prevents overheating, and cycle-by-cycle current sensing protects the power-switch transistors. Other features include undervoltage lock-out and programmable soft-start.

Inductors, capacitors, and diodes to complement the MAX743 can be ordered directly from Maxim in production quantities (page 11). An evaluation kit for prototyping (MAX743EVKIT) is also available (page 9).

If higher load currents are needed, refer to the MAX742 data sheet for a device that drives external power MOSFETs.

**Applications**

- DC-DC Converter Module Replacement
- Distributed Power Systems
- Computer Peripherals
- Portable Instruments

**Features**

- Generates ±100mA or ±125mA
- Specs Guaranteed for In-Circuit Performance
- ±4% Output Tolerance Max Over Temp, Line, and Load
- 82% Typ Efficiency
- Low-Noise, Current-Mode Feedback
- On-Board Current Limiting
- Thermal Shutdown Protection
- Undervoltage Lock-Out and Soft-Start
- Switches From ±15V to ±12V Under Logic Control
- Evaluation Kit Available
- Internal Power MOSFETs

**Ordering Information**

<table>
<thead>
<tr>
<th>PART</th>
<th>TEMP. RANGE</th>
<th>PIN-PACKAGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>MAX743CPE</td>
<td>0°C to +70°C</td>
<td>16 Plastic DIP</td>
</tr>
<tr>
<td>MAX743SHE</td>
<td>0°C to +70°C</td>
<td>16 Wide SO</td>
</tr>
<tr>
<td>MAX743CJO</td>
<td>0°C to +70°C</td>
<td>Dice</td>
</tr>
<tr>
<td>MAX743EPE</td>
<td>-40°C to +85°C</td>
<td>16 Plastic DIP</td>
</tr>
<tr>
<td>MAX743EWE</td>
<td>-40°C to +85°C</td>
<td>16 Wide SO</td>
</tr>
<tr>
<td>MAX743MUE</td>
<td>-55°C to +125°C</td>
<td>16 CERDIP</td>
</tr>
</tbody>
</table>

Ordering information continued on page 11.

**Pin Configuration**

**Typical Operating Circuit**

*MAXIM* is a registered trademark of Maxim Integrated Products.
Dual-Output, Switch-Mode Regulator
(+5V to ±15V or ±12V)

Table 1. Component Design Chart

<table>
<thead>
<tr>
<th>DESIGN REQUIREMENT</th>
<th>LOW COST, LOW NOISE</th>
<th>LOWEST COST</th>
<th>WIDE TEMP RANGE</th>
<th>MINIATURE</th>
<th>SURFACE MOUNT</th>
</tr>
</thead>
<tbody>
<tr>
<td>INDUCER</td>
<td>Low Cost, Low Noise</td>
<td>Lowest Cost</td>
<td>Wide Temp Range</td>
<td>Miniature</td>
<td>Surface Mount</td>
</tr>
<tr>
<td>* Iron Powder Toroid ** * Ferrite Beads **</td>
<td>* Low Noise, Low Cost</td>
<td>* Wide Temp Range</td>
<td>* Miniature</td>
<td>* Surface Mount</td>
<td></td>
</tr>
<tr>
<td>MAX001-SO8 by Maxim, G # 51-546</td>
<td>All Inductors</td>
<td>Gowinda Corp. Part #: 51-598</td>
<td>Gowinda Corp. Part #: 51-598</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Printed Circuit Layout

Dual-Output, Switch-Mode Regulator
(+5V to ±15V or ±12V)

Printed Circuit Layout for Radial-Mount Components

Chic, stable operation requires a good layout (Figure 6, Grounding is especially important for low-noise operation. Do not connect the shield analog ground strip on the Pin 1 side of the IC to the ground plane or any other ground. A short connection between this strip and an analog ground minimizes voltage noise coupling to the reference and compensation capacitors. All +5 V power-supply bypass and +5 V SO packages are connected to ±15 V supplies for low thermal resistance. For maximum board shrinkage, solder Pins 4, 5, 12, and 13 directly to a large copper trace. For +12 V operation, cut the trace connected to 10/13 and insert jumper, J1.

Figure 6. PC Layout for Circuit of Figure 4 Using MAX001/MAX002/ MAX743

Printed Circuit Layout for Radial-Mount Components

Printed Circuit Layout for Radial-Mount Components

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Printed Circuit Layout for Radial-Mount Components
### Dual-Output, Switch-Mode Regulator

**(+5V to ±15V or ±12V)**

#### ELECTRICAL CHARACTERISTICS

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output Voltage</td>
<td>100mA ± 100mA to 120mA</td>
<td>14.55</td>
<td>15.45</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>±15V Mode</td>
<td>x = ±25°C</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>±12V Mode</td>
<td>x = ±25°C</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

#### ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, Vcc = ±5V, 10/15 pin = ±6V, 12/10 pin = ±12V, x = Tav = TavX, unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Efficiency</td>
<td>ILLOAD = 150mA</td>
<td>75</td>
<td></td>
<td></td>
<td>%</td>
</tr>
<tr>
<td>Supply Current (Note 2)</td>
<td>20</td>
<td>30</td>
<td>mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Standby Current</td>
<td>VREF = ±5V includes VREF current</td>
<td>2.2</td>
<td>4</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>Line Regulation</td>
<td>Vx = ±5.5V to ±5.5V</td>
<td>0.05</td>
<td></td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>Load Regulation</td>
<td>ILLOAD = ±100mA</td>
<td>1</td>
<td></td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>Reference Voltage</td>
<td>±VREF</td>
<td>1</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Oscillator Frequency</td>
<td></td>
<td></td>
<td></td>
<td>kHz</td>
<td></td>
</tr>
<tr>
<td>Undervoltage Lock-Out</td>
<td>Measured at V+</td>
<td>2.8</td>
<td>4.2</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Thermal Shutdown Threshold</td>
<td>±95°C</td>
<td>-1.0</td>
<td></td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>LX, On Resistance (Note 3)</td>
<td></td>
<td>1.2</td>
<td>3.0</td>
<td>Ω</td>
<td></td>
</tr>
<tr>
<td>LX, Off Resistance (Note 3)</td>
<td></td>
<td>1.0</td>
<td>2.2</td>
<td>Ω</td>
<td></td>
</tr>
<tr>
<td>LX, Leakage Current (Note 4)</td>
<td></td>
<td></td>
<td></td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>Compensation Pin Impedance</td>
<td>CC + CCC</td>
<td>10</td>
<td></td>
<td>kΩ</td>
<td></td>
</tr>
<tr>
<td>Soft Start Source Current</td>
<td>SS + 2mA</td>
<td>3.0</td>
<td>7.0</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>Soft Start Sink Current</td>
<td>SS - 2mA</td>
<td>0.5</td>
<td>2.0</td>
<td>mA</td>
<td></td>
</tr>
</tbody>
</table>

**Note 1:** All devices tested to full load conditions with 500mA pulse load using a constant load equipment. In continuous operation, the maximum allowable output current is determined by package thermal characteristics and passive component ratings.

**Note 2:** Full load current including standby current. The worst case for supply current occurs at low load voltage.

**Note 3:** Guaranteed by design; not 100% tested. Output currents are 100% tested.

**Note 4:** Tested at steady state, not in pulse load test.

---

### ABSOLUTE MAXIMUM RATINGS

**Supply Voltage**

<table>
<thead>
<tr>
<th>Supply Voltage</th>
<th>4V to 36V (±15V Models)</th>
<th>4V to 36V (±12V Models)</th>
<th>4V to 36V (±12V Models)</th>
</tr>
</thead>
<tbody>
<tr>
<td>MAXVCC</td>
<td>0°C to 70°C</td>
<td>0°C to 70°C</td>
<td>0°C to 70°C</td>
</tr>
<tr>
<td>MAXVCC</td>
<td>-40°C to +125°C</td>
<td>-40°C to +125°C</td>
<td>-40°C to +125°C</td>
</tr>
<tr>
<td>Output Switch Voltages (±15V to GND)</td>
<td>±15V, ±5V (±12V Models)</td>
<td>±15V, ±5V (±12V Models)</td>
<td>±15V, ±5V (±12V Models)</td>
</tr>
<tr>
<td>Output Switch Currents</td>
<td>25mA ±5V</td>
<td>25mA ±5V</td>
<td>25mA ±5V</td>
</tr>
<tr>
<td>LX Sink Current (Peak)</td>
<td>10mA ±5V</td>
<td>10mA ±5V</td>
<td>10mA ±5V</td>
</tr>
<tr>
<td>LX Source Current, Peak</td>
<td>10mA ±5V</td>
<td>10mA ±5V</td>
<td>10mA ±5V</td>
</tr>
<tr>
<td>Power Dissipation</td>
<td>See Figure 2</td>
<td>Load Temperture (Soldering, 10 sec.)</td>
<td></td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>-40°C to +125°C</td>
<td>-40°C to +125°C</td>
<td>-40°C to +125°C</td>
</tr>
</tbody>
</table>

**Maximum Ratings**

- DO NOT INSERT DEVICE INTO SOCKET WITH POWER APPLIED.
- BE CERTAIN THAT OUTPUT FILTER CAPACITORS ARE CONNECTED.
- DO NOT SOLDER ON WORK CIRCUIT WHILE POWER IS APPLIED.
- OBSERVE SUPPLY VOLTAGE RATINGS CAREFULLY.

---

**Figure 1:** Basic Application Circuit

**Figure 2:** Maximum Load Current Vs. Temperature

**Notes:**
- LX Inductors: MAX6001 or equivalent.
- GF Filter Capacitors: MAX6001 or 100μF ±10% equivalent.
- C1 by-pass Capacitor: MAX6001 or 22μF ±5%
- C2 by-pass capacitor is optional
- DA Schottky Diode: IN4007 or equivalent.

---

MAX743
Multi-range current transducer
5-6-8-12-25 A

General description

The LEM Module LA 25-NP is a multi-range current transducer. Based on the principle of magnetic compensation, it provides electronic measurement of DC, AC, pulse, and DC/AC currents and their combination with galvanic isolation.

Principle of operation

The magnetic field produced by the primary ampere-turns (current to be measured x number of primary turns) is compensated by a magnetic field produced by the secondary ampere-turns (output current x number of secondary turns). The system incorporates an induction detector connected to an electronic circuit generating the output current.

Thus the fundamental equation applies:

\[ N_p \cdot I_p = N_s \cdot I_s \]

Advantages

- Measurement of all types of currents with galvanic isolation
- 5 current ranges with the same components
- High overload capacity
- Excellent endurance performance and life
- Low power consumption
- Compact dimensions
- Totally encapsulated
- High reliability
- Optical locating mark for automatic assembly

Applications

- Feedback control systems
- Variable speed drives
- Power supplies
- Robotics
- Overcurrent protection

110
<table>
<thead>
<tr>
<th>Number of primary turns</th>
<th>Primary current (nominal) ( I_p ) [mA]</th>
<th>Nominal output current ( I_o ) [mA]</th>
<th>Turn ratio</th>
<th>Primary resistance ( R_p ) [mΩ]</th>
<th>Primary inductance ( L_p ) [nH]</th>
<th>Recommended connections</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>25</td>
<td>30</td>
<td>25</td>
<td>1/1000</td>
<td>0.3</td>
<td>0.023</td>
</tr>
<tr>
<td>2</td>
<td>12</td>
<td>12</td>
<td>24</td>
<td>2/1000</td>
<td>1.1</td>
<td>0.59</td>
</tr>
<tr>
<td>3</td>
<td>8</td>
<td>12</td>
<td>24</td>
<td>3/1000</td>
<td>2.5</td>
<td>0.21</td>
</tr>
<tr>
<td>4</td>
<td>6</td>
<td>9</td>
<td>24</td>
<td>4/1000</td>
<td>6.3</td>
<td>0.58</td>
</tr>
<tr>
<td>5</td>
<td>5</td>
<td>7</td>
<td>25</td>
<td>5/1000</td>
<td>6.3</td>
<td>0.58</td>
</tr>
</tbody>
</table>

**General characteristics**

- **Operating Temperature**: \( 0 \text{°C} \) to \( +70 \text{°C} \)
- **Storage Temperature**: \( -25 \text{°C} \) to \( +85 \text{°C} \)
- **Current Consumption**: \( 10 \text{mA} \) (output current)
- **Secondary Internal Resistance**: \( 120 \text{Ω} \) (at \( +25 \text{°C} \))
- **Primary Internal Resistance**: \( <0.25 \text{Ω} \)
- **Installation Resistance**: \( >1500 \text{Ω (at 500V and } +25 \text{°C)} \)
- **Weight**: 18 g
- **Construction**: potted in insulated self-extinguishing plastic case
- **Current direction**: a positive output current flows from terminals 1, 2, 3, 4 and 5 to terminals 10, 9, 8, 7 and 6.

**Accuracy - Dynamic performance**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>Typical</th>
<th>Maximum</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Offset</td>
<td>( I_{os} )</td>
<td>( I_p = 0A, T = +25 \text{°C} )</td>
<td>( \pm 0.25 )</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>Residual current *</td>
<td>( I_{rs} )</td>
<td>( I_p = 0A, T = +25 \text{°C} )</td>
<td>( \pm 0.5 )</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>Offset current drift with temperature</td>
<td>( d I_{os} )</td>
<td>( I_p = 0A, T = +6 \text{°C} ) to ( +70 \text{°C} )</td>
<td>( \pm 0.2 )</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>Linearity</td>
<td>( I_L )</td>
<td>( I_p = 0mA )</td>
<td>( \pm 0.2 )</td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>Delay time</td>
<td>( t_d )</td>
<td>( I_p = 25A ) (see graph)</td>
<td>1</td>
<td>μs</td>
<td></td>
</tr>
<tr>
<td>Bandwidth</td>
<td>( f )</td>
<td>( I_p = 25A ) at ±1dB</td>
<td>DC to 150 MHz</td>
<td>Hz</td>
<td></td>
</tr>
</tbody>
</table>

* Result of the zero cross-field of the switching circuit.
Application note

Recommendations for the layout of the primary circuit:

- Pad diameter: 2 mm
- Hole diameter: 1.2 mm
- Track width: 2 mm

For completion of the primary windings:

- (a) from pin 5 to pin 3

Track resistance for completion of the primary windings:

- For a single-side PC board at 70°C:
  - 55 microns of copper: 1.6 mΩ/m
  - 70 microns of copper: 0.8 mΩ/m

(*) For an assembly comprising several windings in parallel, the pads are tracked to ensure good current distribution.

For pulsed operation, please consult us.

Load resistance vs. primary current (maximum & minimum values)

Primary and output current (Ig & Is)

Definition of delay time vs. output current

Current derating vs. frequency and ambient temperature

Delay at 90% of In [ms]
FEATURES
- 8V to 35V Operation
- Guaranteed ±1% 5V Reference
- Guaranteed 10mW/1000 Hrs. Long Term Stability
- Guaranteed ±3% Oscillator Temperature Stability
- Undervoltage Lockout
- 100mA Source/Sink Outputs

APPLICATIONS
- Switching Power Supplies
- Motor Speed Control
- Power Converters

DESCRIPTION
The LT1526 is an improved general purpose switching regulator control circuit. Included on the chip are a 1% voltage reference, oscillator, error amplifier, pulse width modulator and low impedance output drivers. Also included are protective features such as a current limit comparator, undervoltage lockout, soft-start circuitry, and adjustable delaytime. This versatile device can be used to implement single-ended or push-pull switching regulators of either polarity, both transformerless and transformer-coupled.

Although pin-for-pin and functionally compatible with industry standard 1526 and 3526 devices, Linear Technology has incorporated several improvements in the design of the LT1526. A subsurface zener has been used to provide excellent reference voltage stability and the reference offers improved line regulation and load regulation. The current limit comparator sense voltage initial accuracy and temperature stability have been greatly improved.

The combination of improved features and advanced linear processing for high reliability make Linear Technology's switching regulators a superior choice.

Reference Line Regulation

\[ V_{ref} \] vs. \[ V_{in} \] Graph

Block Diagram

\[ \text{Diagram of LT1526/3526 Regulating Pulse Width Modulator} \]
ABSOLUTE MAXIMUM RATINGS

(Note 1)

Input Voltage (+Vdd) ...................................... +40V
Collector Supply Voltage (+Vc) .......................... +40V
Logic Inputs ............................................ -0.3V to +5.5V
Analog Inputs ........................................... -0.3V to +Vdd
Source/Sink Load Current (each output) ............... 200mA
Reference Load Current .................................. 50mA
Logic Sink Current ...................................... 15mA
Operating Junction Temperature Range
  LT1526 .......................................... -55°C to +150°C
  LT3526 .......................................... 0°C to +125°C
Storage Temperature Range ............................. -65°C to +150°C
Load Temperature (Soldering, 10sec) .................... +300°C

RECOMMENDED OPERATING CONDITIONS (Note 2)

Input Voltage ........................................... +6V to +35V
Collector Supply Voltage ................................. +4.5V to +35V
Sink/Source Load Current (each output) ............... 0mA to 100mA
Reference Load Current ................................ -5mA to 20mA
Oscillator Frequency Range ............................... 1Hz to 400kHz
Oscillator Timing Resistor ................................. 2kΩ to 15kΩ
Oscillator Timing Capacitor .............................. 1nF to 200nF
Available Deadline Range at 40kHz ................... 3% to 50%

ELECTRICAL CHARACTERISTICS

(+Vdd = 15V, and over operating junction temperature, unless otherwise specified.)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>LT1526</th>
<th>LT3526</th>
</tr>
</thead>
<tbody>
<tr>
<td>REFERENCE SECTION (Note 3)</td>
<td></td>
<td>MIN</td>
<td>TYP</td>
</tr>
<tr>
<td>Output Voltage</td>
<td>+Tj = 25°C</td>
<td>4.05</td>
<td>5.00</td>
</tr>
<tr>
<td>Line Regulation</td>
<td>+Vdd = 9V to 25V</td>
<td>2</td>
<td>10</td>
</tr>
<tr>
<td>Load Regulation</td>
<td>L = -5mA to +20mA</td>
<td>5</td>
<td>10</td>
</tr>
<tr>
<td>Temperature Stability</td>
<td></td>
<td>15</td>
<td>50</td>
</tr>
<tr>
<td>Total Output Voltage Range</td>
<td>Over Recommended Operating Conditions</td>
<td>4.00</td>
<td>5.00</td>
</tr>
<tr>
<td>Short-Circuit Current</td>
<td>Vref = 0V</td>
<td>25</td>
<td>50</td>
</tr>
<tr>
<td>Long Term Stability</td>
<td>Tj = 125°C</td>
<td>2</td>
<td>10</td>
</tr>
<tr>
<td>UNDervoltage LOCKOUT</td>
<td></td>
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APPLICATIONS INFORMATION

FUNCTIONAL DESCRIPTION AND PIN FUNCTION

Voltage Reference

The reference regulator (pin 18) supplies a regulated 5.0V to all internal circuitry, as well as up to 20mA for external circuitry. It is fully active at supply voltages (pin 17) of 8V and greater.

The LT1526 can operate from a 5V supply by connecting +VIN to VINP (pin 18 to pin 17) and maintaining the supply between 4.8V and 5.2V.

Undervoltage Lockout

The undervoltage lockout circuitry protects both the switching regulator and the power devices if controls from inadequate supply voltage, which can result in unstable control circuitry. If +VIN is too low, the circuit turns off the output drivers, holds RESET (pin 5) low and the soft-start capacitor in a discharged state.

Soft-Start

The soft-start circuitry protects the power devices from high surge currents during power supply turn-on by limiting the available PWM duty cycle.

When +VIN reaches a sufficient voltage to allow RESET to go high, a 100μA current source charges the external Cs capacitor (pin 4) linearly to 5V. The ERROR AMPLIFIER output is clamped to 600mV above the Cs voltage, and the available duty cycle of the PWM increases linearly. Maximum duty cycle is available when the Cs voltage reaches about 3V.

Digital Control Ports

The three digital control ports are bidirectional. Each port can drive TTL and 5V CMOS logic directly. They can also be driven by open-collector TTL, open-drain CMOS, and open-collector voltage comparators.

Driving SYNC (pin 12) low causes a discharge cycle in the oscillator. Driving SHUTDOWN (pin 8) low causes the outputs to turn off. Driving RESET (pin 5) low causes the outputs to turn off and discharges the Cs capacitor.

Oscillator

The internal oscillator circuitry sets the frequency of operation for the switching regulator. Frequency is set by \( R_T \) (pin 9), \( C_T \) (pin 10), and \( R_D \) (pin 11). With \( R_D = 0\Omega \), the values for \( R_T \) and \( C_T \) may be chosen from the oscillator period graph. If the desired deadtime is increased, the value of \( R_T \) may need to be decreased to maintain the desired frequency.

The frequency at either output is half that of the oscillator, and the frequency at +VC (pin 14) is equal to the oscillator.

Synchronous Operation

Two or more switching regulators may be synchronized by setting the master to the desired frequency and sharing the oscillator signals with the slave units. Slave C1 pins are tied to the master C1 pin, and slave SYNC pins are tied to the master SYNC pin. Slave R1 and R0 pins are left open.

External logic synchronization can be used by setting the oscillator period to be 10% longer than the external clock period, and connecting the external clock to the SYNC pin. A periodic low of about 0.5μs wide will lock the oscillator to the external frequency.

Error Amplifier

The differential input (pins 1 and 2), single-ended output (pin 3) transconductance amplifier provides about 70dB of gain. The output has an impedance of 2MO, and since all voltage gain occurs at the output, the gain characteristics can be controlled with shunt reactance to ground.

Output Drivers

The totem-pole output drivers can source and sink 100mA continuously and 200mA peak. The outputs are driven 180° out of phase by the flip-flop. Loads can be driven either from the outputs or the +VC pin. Since large transient currents occur within the output stages during switching, a resistor is recommended in series with +VC (pin 14) to limit the peak current. The resistor value should be +VC/200mA.
Appendix C

Weather Data for 20 July 1993

NOAA Satellite Image

(U. S. National Oceanic and Atmospheric Administration)
Sun-synchronous polar orbit, altitude 850 km, pixel resolution ~ 3 km.
Image Type: Thermal infrared; light = cold, dark = warm.

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Time: AM
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- No Filter Paper Error
SILICON PYRANOMETER SP 437

CALIBRATION & INSTRUCTIONS

Calibration

SP 437 number 1.25 delivers 0.436 mW/m²/s across the 1.25 cm internal load resistor.

Installation

Screw down the polycarbonate base onto a level substrate. If you want to monitor the silica gel condition, remember at this time to either make an inspection hole in the substrate, or provide for easy removal of the pyranometer. Remember that the simplest mounting method—gluing down to the substrate with Silastic (silicon rubber based adhesive)—is a very imperfect solution. Pyranometers returned for service with their bases covered in Silastic will be returned after service in the same condition.

If you are mounting the instrument on a metal surface that gets hot, try to insulate, or air-space it from the substrate, to avoid violent temperature cycling of the pyranometer.

Underwater installation for a month or two is acceptable, but watch out for corrosion of the copper terminals if it is installed in the hot brine environment of a 'Solar Pond'. Temperatures over 70 Celsius exceed the rating of the silicon sensors used.

Signal connections

The positive terminal is nearest the serial number stamped on the rim of the polycarbonate disc. For long term reliability, there is no substitute for soldered joints. If the provided cable is joined to a screw terminal block which is kept dry, this is acceptable.

For use out in all weathers, or underwater, the terminals must of course be sealed. The best method is to wipe a blob of outboard motor grease over them, to cover both the pipe in the area and the vinyl insulation at the start of the cable. Normal car grease is nearly as good, and both types, although messy, can be quickly wiped off for inspection of the joint. Again Silastic is used for this purpose, and will work if the pipe is well cleaned before sealing, and the cable is not pulled too hard.

Maintenance

Dirt will accumulate on the top of the pipe diffuser, and the only remedy is to clean it occasionally. Soap, water and a 2.5 cm paintbrush do a good job quickly without damaging the diffuser surface. The sides of the diffuser simply blocks light, and there is no need to clean it.

There should be no need to replace the silica gel, but if necessary, the six base screws may be removed and the gel replaced. Care must be taken to keep the joint surfaces clean on assembly, or it will not seal.
SILICON PYRANOMETER SP 437

CONSTRUCTION

A solid PIPE cosine corrected cylindrical diffuser 8.5 cm in diameter and 3 cm high is mounted on a polycarbonate disc base 10 cm diameter and 1 cm thick.

The silicon cell is located in a cavity at the bottom of the diffuser, and is itself a hermetically sealed unit with a glass window.

Behind the silicon cell, the cavity enlarges to accommodate the load resistor and the output conductors, which are solid copper rods compress-fitted through the PIPE. The enlarged cavity is sealed to the base by a high pressure neoprene 'O' ring, and filled with silica gel to maintain dry conditions. The base is attached to the diffuser by six long stainless steel self-tapping screws. Although one filling of silica gel is intended to last the life of the instrument, the removal of the base, gel replacement and reassembly can all be carried out by a customer able to handle a screwdriver.

The output conductors appear on the side of the PIPE diffuser as solder terminals 1.25 cm apart. The base, being polycarbonate, is transparent so that the condition of the silica gel may be monitored. Three holes are provided to screw it down to a level substrate.

The cosine-correction curve machined into the top of the PIPE diffuser has a drain hole, for discharging water after rain.

A variant is available - the SP 440A - which has no internal load resistor, for use with current-input amplifiers, or for special purposes.

The value of the load resistor will be in the range of 50 to 200 Ohms, depending on the radiation sensitivity of the silicon cells being used. The load resistance will be specified on the calibration sheet supplied with the instrument. Operating a 200 Ohm resistance unit into a 20,000 Ohm amplifier will deliver a reading 15% low. This may be corrected with calculation, or ignored as being well within the 15% calibration tolerance.

PERFORMANCE SPECIFICATIONS

<table>
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<tr>
<th>Spectral Response</th>
<th>Normal 'silicon curve', peaking sharply in the near infra-red.</th>
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<tbody>
<tr>
<td>Time Constant</td>
<td>About 0.6 milliseconds.</td>
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<tr>
<td>Voltage output</td>
<td>Between 0.08 and 0.22 millivolts/milliwatt/minute.</td>
</tr>
<tr>
<td>Linearity</td>
<td>Better than 1%.</td>
</tr>
<tr>
<td>Temperature Coeff.</td>
<td>Less than ±0.1% for 1 degree Celsius rise between 0 and 50 degrees.</td>
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<tr>
<td>Calibration</td>
<td>Within plus or minus ±5% of Grade 1 Pyranometer.</td>
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<tr>
<td>Cosmic Response</td>
<td>Angles to horizontal - Better than ±1°.</td>
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<td>10 degrees plus or minus ±5°</td>
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Tolerance

±15%
APPENDIX D  BASIC SOURCE CODE LISTINGS

N.B. the files are contained on the included diskette as .BAS text files.
APPENDIX E .LOG FILES

N.B. the files are contained on the included diskette as .LOG text files.