A CONTROLLED CURRENT INVERTER

FOR AN ELECTRIC VEHICLE.

A Thesis submitted in partial fulfilment of the requirements for the degree of Master of Engineering (Electrical and Electronic).

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ABSTRACT

The University of 'Canterbury Mark II' electric vehicle has been out of service for several years due to the lack of a suitable inverter to provide a variable frequency AC supply to its traction motors.

This thesis describes the design and construction of such an inverter, using high current bipolar junction transistors as the switching elements, so that the car might be returned to service in the near future. The inverter is based on an existing commercial AC motor speed controller. Modifications to this AC motor speed controller were made to suit the low voltage, high current rating of the traction motors. These modifications are described and it is shown that these modifications permitted the inverter to deliver the required increase in current.

The inverter differs from most conventional AC motor speed controllers in that it acts to shape load current rather than potential, and uses an asynchronous switching technique to do this. The Thesis describes this technique and the control hardware constructed to implement it.

Test results, showing the performance of the combined inverter/motor system are then presented graphically and discussed with reference to standard AC motor theory, giving consideration to the harmonic content of the AC waveforms. Consideration is also given to a suitable closed-loop control system which could be expected to ensure that the inverter's output frequency is controlled in such a manner as to give a safe and predictable response to the brake and accelerator controls.
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AN INTRODUCTION TO THE ELECTRIC VEHICLE

Electric cars are not a recent development. In the early years of the twentieth century they were a predominant force in the world's vehicle fleet. Some 40% [Hamer, 1986] of all cars in existence at the time were electric, with only 20% powered by the internal combustion engine, (the remainder being steam powered).

Driving speeds then were generally very slow and cars had only very low power motors. Consequently the limited energy available from a battery did not pose the disadvantage it does today in modern high powered vehicles. This combined with the reliability and ease of starting afforded by electric vehicles (EVs) assured their popularity.

However within the space of a decade this was to change. Improvements continued to be made to the internal combustion vehicle (ICV), improving its reliability and performance. Drivers began to expect their automobiles to offer both greater speed and range, neither of which could be easily accomplished with battery powered cars. Ironically, the development of the electric starter motor sealed the fate of the EV by overcoming the last advantage it still held, that of easy starting. Electric vehicle production all but ceased after World War One and has remained a negligible portion of global vehicle production ever since.

However, while the production of EVs dwindled, some research and development in electric propulsion continued. The period from 1967 to 1978, coinciding both with an oil crisis and an increased concern for the environment [Kiehne, 1988], saw renewed interest in the USA and Europe toward pollution free battery powered cars which could be run on electricity generated from readily available supplies of domestic coal. Several industrialised nations began researching anew into more effective electric propulsion systems, including most importantly, more lightweight and powerful batteries. Hampered by technical difficulties much of this newly promised battery technology failed to eventuate, and with a subsequent reduction in world crude oil prices in the 1980s interest in alternative propulsion again declined.
Chapter One: An Introduction to Electric Vehicles.

Interest in the EV has recently begun anew, urged by the increasing need to reduce atmospheric pollution, particularly in large cities where it creates ever rising health costs. In the American State of California alone it is estimated that nearly $NZ 20 Million is spent annually on treating illness related to such pollution [Dables, 1992]. As a result, the state has drafted stringent legislation decreeing that by the year 2003, 10% of all passenger cars sold (some 200 000 automobiles) each year must emit absolutely no pollution. At the present time the only economic alternative is the battery electric vehicle [Riezenman, 1992]. Several other American states have expressed their intention to follow this example and the world’s car manufacturers have become engaged in developing successful production cars for this market [Sacks, 1992].

As it always has, the state of the art in battery technology is hampering the development of the EV. Several contenders for a lightweight battery are in existence [Sacks 1992], but no single battery is considered ideal and none are yet economically viable.

Batteries remain a far heavier and more bulky means of storing energy than liquid fuels such as petrol or diesel. Six litres (4.5kg) of petrol [Dables, 1992], even allowing for the low conversion efficiency of an internal combustion engine, contains more energy than is available from modern lead acid battery packs weighing some 400kg. Energy efficiency then, is of paramount importance in the development of a successful vehicle. Recent designs have seen considerable efforts spent on producing cars which offer minimal energy consumption, with an emphasis placed on reducing aerodynamic drag and improving the efficiency of motors and speed control electronics.

In the past virtually all EVs employed standard, mechanically commutated DC motors. At the time these offered the greatest ease of speed control, with a relatively simple and cheap electronic chopper or even a rheostat being used to alter the mean terminal voltage to the machine [Christian, 1980]. Nominal efficiencies for such DC systems are around 70-80%. Cars were often fitted with standard ICV gearboxes [Peyriere, 1989] to further improve the flexibility of this speed control, at the expense of adding extra weight and further reducing efficiency.

Rapid advances made in power electronics technology, coupled with reducing semiconductor prices in the last decade, have made the use of AC induction and permanent magnet brush-less DC motors an attractive alternative [Lipo, 1988]. Such AC machines offer several advantages, particularly those of low maintenance and improved efficiency.
1.1 THE DEVELOPMENT OF THE UNIVERSITY OF CANTERBURY ‘MARK II’ ELECTRIC VEHICLE

Canterbury University began working on its first electric car in 1974, following three years of experimentation with an AC induction motor speed control system [Byers, 1978]. At that time such systems were rarely used in vehicles, and car was thus considered a suitable test-bed by which to demonstrate this technology. This first ‘Mark I’ car ran in 1976 and although having a limited range of 40km (at constant 50km/h) due to very poor aerodynamic characteristics, did serve to show that a roadworthy machine could be built and operated in urban driving conditions.

In an effort to improve the range obtainable from the strictly limited energy reserve held by its batteries, a ‘Mark II’ vehicle based on an Austin A40 Farina body was developed during the period 1976 to 1982. Although heavier than the Mark I, the Mark II exhibited a much improved drag co-efficient over its predecessor and was subsequently capable of travelling in excess of 60km on one charge at a constant 65km/h [Harman, 1992] with cruising speeds of up to 80km/h possible. Both cars utilised conventional three phase induction motors for propulsion, supplied with variable frequency current from a pulse width modulation (PWM) inverter.

Figure 1.1 shows the arrangement of the major components of the Mark II. Three physically separated groups of lead acid batteries (each weighing about 110kg) are interconnected to form a 240V DC supply with an energy capacity of approximately 8kWh (at the one hour rate). Use of a 240V nominal battery voltage permits charging to be done directly from a standard household supply without the need for a transformer [Byers, 1983] and results in a compact and lightweight charger which may be carried on board the car.

Power from the batteries is controlled by the inverter housed in a purpose built enclosure which is located between the drive motors. The motors themselves are star connected and linked in parallel to the inverter. Each drives one rear wheel by way of a single speed chain drive. During braking the motors are run as generators returning energy to the battery bank, obviating the need for conventional rear drum brakes and helping improve the cars range in stop-start driving conditions. For safety and to comply with ministry of transport regulations, conventional unassisted hydraulic brakes operate the front wheels to provide extra braking as required.
Chapter One: An Introduction to the Electric Vehicle.

Figure 1.1 Layout of the Mark II electric car.
Although driving induction motors via an inverter requires a relatively complex controller as compared to a DC chopper, there are definite advantages in using an AC drive system:

- Induction motors are cheap, rugged machines requiring virtually no maintenance, whereas DC machines are expensive and the mechanical commutator/brush assembly must be periodically maintained for reliable operation.

- A variable frequency supply permits an AC induction motor to be operated over a wide speed range, typically from 0 to 5 times the nominal 50Hz rating. If motor voltage is chosen correctly then rated torque can be maintained at all speeds such that the motor is able to deliver several times its rated power without overheating. An inverter is thus able to raise the power density of the motor, reducing the size and weight of the drive system. In the MKIII the four pole traction motors used each have a 50Hz rating of 2.2kW at a shaft speed of around 1450 rpm. The rated torque available from each is 15 Nm at all speeds such that a maximum continuous power of 6kW is developed at 4300 rpm (150Hz). With the batteries at full charge, torque can be temporarily increased at full speed to 20Nm giving each motor a peak power output of 11kW. Such a power output is sustainable for several minutes before the motors begin to overheat. With a mass of 23kg, the specific power available from the motors is similar to that of a normally aspirated internal combustion engine at 470W/kg [Goyne, 1993]. However, as the batteries become discharged and the bus potential falls to toward 200V, this peak power is significantly reduced.

Drawbacks do exist with this scheme. Increasing speed by raising the supply frequency increases the motor’s impedance reducing current. As a consequence, maximum torque and hence power, falls.

Boosting motor power at higher speeds then requires a controller able to supply a variable terminal voltage to the motor, or in other terms be able to maintain rated current and torque over a range of shaft speeds. The terminal voltage required to maintain full torque increases in proportion to the fundamental component of frequency (or ‘fundamental frequency’) [Rosink, 1980] hence for example, a standard 400V machine would require some 1300V to maintain rated torque at 150Hz.
Chapter One: An Introduction to the Electric Vehicle.

The peak sinusoidal line voltage able to be provided by the car's inverter can be no greater than the 240V available from the batteries, equating to a maximum RMS potential of 170V. In order to permit rated torque to be available at 150Hz, the machines have been rewound to operate at a 50Hz line to line potential of 90V RMS. Line current is correspondingly larger, with 25A RMS drawn (per machine) at rated torque and up to 70A at peak torque.

The original 12V electrical system (lights, horn and the like) developed by the car manufacturer, have been retained. To power these components a DC-DC converter rated at 350W was developed before the MKII was put into service. More recently this has been replaced by a more compact and lightweight resonant converter developed in conjunction with this project [Laird, 1992 (A)].

1.2 PROJECT OUTLINE

The original inverter installed in the Mark II car in 1976 utilised thyristors as its main switching elements as these were the only solid state devices readily available to control the large currents required by the drive motors. As a consequence, the inverter was complicated by the auxiliary circuitry required to force commutate each switch.

Analogue control circuitry was used to generate the gate drive signals for both the main and auxiliary thyristors, as the microprocessors available at the time were deemed too slow. Unfortunately the circuits used were prone to drift in their outputs causing the inverter to 'go out of tune', contributing to the general lack of reliability experienced over the two years it was in service from 1982 to 1984.

In 1984 then, in order to reduce the complexity of the inverter, a new design based on power bipolar junction transistors (BJTs) was undertaken, Although this inverter was completed it was never installed and the car project has remained dormant until the inception of this project.

The essence of this project has thus been to modify an existing micro-controlled motor speed controller manufactured by GEC (NZ) of Wellington, making it capable of driving the low voltage high current motors that propel the car so that it might be put back into service. Testing was then undertaken to examine the operating characteristics of the completed drive system, the results of which are presented and discussed in Chapter Six.
Chapter One: An Introduction to the Electric Vehicle.

The inverter uses a switching technique developed at Canterbury University [Penny, 1986] and Chapter Two describes this technique. Chapter Three expands on Chapter Two by describing the hardware used to realise the completed inverter system, detailing the specific modifications made to GEC's inverter to suit the needs of the Mark II electric car.

The BJT devices used in the output stage of the inverter must be driven with appropriately shaped current waveforms for efficient and reliable operation. So called 'base drive circuits' are responsible for the generation of such waveforms. Chapter Four introduces the operation of the BJT as a switch, and examines aspects of controlling (using the base drive circuits) and protecting these devices.

The car's motors are an important component of the completed drive system. Chapter Five, briefly touches on basic machine theory, including a discussion of performance when the supply waveform is not perfectly sinusoidal, as is the case with the inverter. Lab tests done from a sinusoidal mains supply are presented and discussed to serve as a comparison to results obtained during testing of the inverter.

The Thesis closes (Chapter Seven) by examining a closed loop frequency control system that could be implemented in the future to ensure a safe and predictable response by the car to the accelerator and brake controls under all driving conditions.
CHAPTER TWO:  
CONTROLLED CURRENT SWITCHING

The AC induction motor speed control inverter supplied by GEC, utilises a microcontroller system to operate a set of six power bipolar junction transistor (BJT) switches in a manner which forces motor currents to be as sinusoidal as possible. This is a process dubbed controlled current inversion (CCI) [Penny, 1986] and contrasts with another common technique, sinusoidal pulse width modulation (SPWM) which acts to control load voltage [Mohan, 1989]. Previous inverters installed in both cars had utilised such SPWM techniques. This chapter offers an explanation of the CCI process. It will be shown how the power transistors are switched to produce sinusoidal output currents, and how the controller calculates the magnitude of the current required to meet any given motor torque.

2.1 TRANSISTOR SWITCHING STRATEGY

The inverter’s transistors (Q1-Q6) are arranged in a three phase, full bridge configuration (figure 2.1).

![Diagram of 3 phase (six transistor) full bridge configuration.](image_url)

Figure 2.1 The 3 phase (six transistor) full bridge configuration.

Each transistor has a parallel or bypass diode (D1-D6), which has the same current and voltage ratings as the device itself. These diodes are necessary as the transistors can be destroyed if forced to conduct a reverse current, and in practice were an integral part of the transistor packages used (see the data sheets in Appendix one).
Chapter Two: Controlled Current Switching.

CCI is inherently a feedback/decision process. The micro-controller generates a voltage signal which is a scale model of the instantaneous fundamental component of output current which is required to meet motor torque and speed demand. Known as the reference sinusoid \( V_{\text{ref}}(t) \), this is then compared with feedback \( V_{\text{f}}(t) \) from a linear current to voltage transducer (TD) placed in each output line. The power transistors in the three phase bridge are then switched so as to force the output current to track the reference sinusoid as closely as possible. The reference sinusoid itself must be continually updated to meet changes in motor loading. A second, separate feedback system is required for accurate assessment of an optimum operating current, and will be described later in section 2.2.

CCI is best introduced by way of a single phase inverter driving a highly inductive load. The power section of this device consists of a pair of transistors and bypass diodes in the 'half H' bridge shown in figure 2.2a. Here, the bus potentials indicated are taken with respect to a neutral or earth, which in practice would be the star point of the three phase motor. The transistors and diodes are assumed at present to be perfect switches, with a zero on state volt-drop.

Consider initially the construction of the positive half cycle of load current \( (I_{\text{load}}) \) in the direction indicated in figure 2.3a. If at some arbitrary time \( t_0 \), the actual line current is less than that demanded by the reference sinusoid; then a comparator correlating the feedback and reference signals will be toggled, Q1 is switched on and the load connected to the positive DC supply (figure 2.2b). Load current rises (linearly) and some time later \( (t_1) \) will meet the target level, (this is shown most clearly by the exploded view of region A in figure 2.3a). The comparator now changes state, but current is permitted to continue rising for a further fixed period \( T \). Once \( T \) has expired Q1 is switched off and, current is commutated to the bypass diode D2.

With D2 as the conducting element, (figure 2.2c) the inductive load is connected to the negative DC bus and does work on the supply, resulting in the decreasing output current seen on the interval \( t_2 - t_3 \). At the instant \( t_3 \) (figure 2.3a) the load current is again equal to the level requested by the reference waveform and current is permitted to continue falling (again for the period \( T \)) before the process repeats itself after \( t_4 \). The negative half cycle of load current is generated in the same manner, but now with Q2 and D1 providing the conducting paths.
Chapter Two: Controlled Current Switching.

a) Single Phase Half H Bridge.

V_ref(t) Comparator Delay T C(t) Dead-time Q1 on Q2 on Dead-time V_fl(t)

b) Q1 on and current increasing.

V_ref(t) Comparator Delay T Q1 on Dead-time V_fl(t)

E + - I_load

Q1

TD

+Vdc

-I

Vdc

Vdc

Q2 on

Dead-time

V_fl(t)

c) Q1 off, D2 on and current decreasing

V_ref(t) Comparator Delay T Q2 on Dead-time V_fl(t)

D2

TD

+Vdc

-I

Vdc

Figure 2.2, A single phase half h bridge, and load current switching.
Current $I(t)$

Exploded view of Region A.

Region A

CCI Output waveform $\rightarrow$ Desired output waveform

Figure 2.3a, construction of the output current

Figure 2.3b, CCI output voltage waveform
Chapter Two: Controlled Current Switching.

A further condition is imposed on the switching of the transistors due to the nature of the control system used, whereby transistors in each phase are switched in a complementary fashion. As such then, when one transistor is switched off the second is switched on, even though in fact it will be a bypass diode that next comes into conduction. In practice, power transistors take time to switch off (typically 10-20μs). Hence if there is an insufficient delay between turning off one device and turning on the second, then a short circuit across the DC bus results, and both transistors may be destroyed.

A delay circuit triggered by the transitions in the transistor switching control signal is used to prevent such an event by holding both devices off for a so called dead time, ensuring that a transistor has time to stop conducting prior to turning on the second device. During the dead time current is carried by a bypass diode.

A three phase inverter employs one transistor pair and controller for each output line, with each operating independently of the other two. Three phase outputs are generated by supplying each with reference sinusoids mutually 120° apart in phase.

Choice of the period T is a trade off between reduced current harmonics and inverter switching efficiency. Using a small value of T results in faster transistor switching and the amount ΔI by which the output current deviates above and below the reference sinusoid level (figure 2.3a) is thus reduced. This in turn reduces the harmonic content of motor current and hence the power losses in the motor associated with this, such as parasitic torques (see Chapter Five). However, a price is paid in terms of inverter efficiency. Each time a transistor is switched, energy is lost as heat. Increasing the switching rate thus causes greater power loss within the inverter itself. The high current devices used in the car can generally only be switched at around 2-3kHz before switching losses become excessive, hence T was chosen such as to limit the maximum switching frequency to around 2kHz.

The phase-neutral output voltage waveform of a CCI inverter, as shown in figure 2.3b, is similar to that of a traditional PWM system, being a square wave of varying duty ratio. However with CCI, switching frequency is seen as not fixed, but rather is free to change (up to a given maximum) as required to track the reference sinusoid. The instantaneous phase-neutral voltage has only two values; +/- V_de, depending on whether an upper or lower device is in conduction (as described previously).
Chapter Two: Controlled Current Switching.

As with any conventional three phase system, summing any two of the inverter’s output phase-neutral voltages gives a corresponding line-line voltage. At any instant it is possible for two phase-neutral voltages to be identical (for example both may be \( +V_a \)) since each phase of the inverter is switched independently. Hence the line-line voltages can at times (as will be seen in some of the oscillograms presented in Chapter Six) be zero.

The asynchronous switching of CCI has an important advantage in some applications as it generates a relatively broad spectrum of switching harmonics in the line current. This serves to reduce the audible noise emitted by the motor [Penny, 1989]. Traditional SPWM systems with their fixed switching rate at any given fundamental output frequency can excite some mechanical components (such as a car’s chassis) into an audible resonance, leading to very noisy operation.

2.2 CALCULATING THE REQUIRED OUTPUT CURRENT

Computing the correct amplitude for the reference sinusoid, requires a second feedback calculation process based on the operating characteristics of an induction motor. The mechanism involved in this is perhaps best understood by first giving a brief consideration to the circuit model of one phase of a three phase induction motor, seen in figure 2.4 [Dubley, 1989]. Motor terminal voltage and current (\( V_t \) and \( I \)) shown are per phase, rather than line quantities.

![Figure 2.4 Circuit model of an induction motor](image)

Figure 2.4 Circuit model of an induction motor
Chapter Two: Controlled Current Switching.

The model is similar to that used for a transformer, except that the effective turns ratio is related to the rotor speed. It can be seen that the induction motor has a definite shunt magnetising impedance \( r_m \) and \( x_m \). The motor manufacturer designs the stator winding so as to ensure that a sufficient current \( i_m \) is drawn through the magnetising impedance to properly magnetise the air gap between the stator and rotor.

A weak air gap flux (insufficient magnetising current) lowers the peak torque available from the machine [Penny, 1989], making it more prone to stalling. Too great a magnetising current will saturate the steel of the stator and rotor cores, resulting in excessive line current and a loss of efficiency due to increased winding losses.

Motor supply current \( I \) is proportional to torque. When an induction motor is run from a conventional AC supply, phase voltage \( V \) and frequency are constant, and magnetising current is also approximately constant for all values of line current as the stator impedances \( x_i \) and \( r_i \) are small. Hence the airgap flux stays nearly constant as torque changes. However, running the motor from a variable frequency supply changes both the stator and magnetising impedance, changing the magnetising current accordingly. Thus the inverter must be able to vary the (fundamental component) of terminal voltage in proportion to the fundamental component of frequency in order to maintain the correct air gap flux as speed changes [Walton, 1988].

2.2.1 Constant Flux Excitation

If both leakage reactance and magnetising resistance are assumed as negligible then the phase displacement between motor terminal voltage and current is due entirely to the magnetising inductance. A phasor diagram for this simplified system is shown in figure 2.5.
If the line current I is to be chosen such that the correct flux and hence $i_m$ is maintained constant at all times, then (by measuring the phase displacement ($\theta$) between the fundamental component of voltage and current) the microprocessor is able to compute I by means of simple trigonometry:

$$i_m = I \sin \theta$$

$$\Rightarrow I = \frac{i_m}{\sin \theta}$$  \hspace{1cm} (2-1)

Values of $i_m$ vary according to the size of the motor. When a given motor is first coupled to the inverter, the operator enters; the nominal operating voltage, current and power into the micro-controller. From this data an estimate (interpolated from manufacturer's data) is made of the required magnetising current.

### 2.2.2 Computing Phase the phase Displacement ($\theta$)

Determining the phase displacement ($\theta$ from equation 2-1) between the fundamental components of voltage and current is performed by measuring the time delay $t_p$ between successive zero crossings of each. With knowledge of frequency then phase may be calculated using equation 2-2:

$$\theta = 2\pi f t_p$$  \hspace{1cm} (2-2)
Since by definition, the reference sinusoid is a scale model of the fundamental component of output line current, the only additional information needed by the microcontroller to use equation 2-1 is the fundamental component of output voltage. This is sensed by detecting the switching of the lower transistors in the three phase bridge, yielding a PWM feedback signal. Detection is accomplished by placing the input of an opto-isolator across each of the lower transistors (Q2, Q4, Q6), together with a high value series resistance to limit current. Use of opto-isolators is necessary to protect the microprocessor from the large, rapidly changing voltages which occur across the transistors.

By taking the difference between any two of the PWM feedback signals and then low-pass filtering, the fundamental component of the corresponding output line-line voltages are recovered. Using differential (line-line) signals suppresses common mode harmonics prevalent in the PWM outputs of the inverter, improving the quality of the feedback signal. However, since an additional phase shift exists between phase and line to line voltages, the phasor diagram of figure 2.5 becomes more complex, as shown in figure 2.6.

![Figure 2.6 Three Phase Phasor Diagram.](image)

To measure for example, the displacement ($\theta$) between the red phase voltage $V_r$ and current $I_r$, voltage feedback is taken between yellow and blue phases ($V_{yb}$) and current from the red phase $I_r$. From figure 2.6 it is seen that $V_{yb}$ leads $I_r$ by $90^\circ + \theta_r$, therefore $\theta_r$ can be resolved by subtracting $90^\circ$. Similar arguments hold for the remaining line potentials $V_{yr}, V_{br}$ and the currents $I_b, I_y$. 

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2.4 SUMMARY

Controlled current inversion (CCI) was introduced as a technique for switching the transistors in a three phase bridge in a manner which forces output currents to be as sinusoidal as possible. Consequently, the inverter was noted to differ from conventional SPWM systems in acting to control load current rather than voltage.

The inverter’s microprocessor was seen to be able to calculate the magnitude of the current required to meet any operating condition by ensuring that magnetising current (and hence flux) was maintained constant. This was done by measuring the phase displacement between the fundamental component of line voltage and current, and then using a simple trigonometric equation. By maintaining flux constant the inverter automatically ensures that peak motor torque is always available and that magnetic saturation is avoided.

The resulting output of the micro-controller was termed a reference sinusoid, a scale model of the fundamental component of output current required to ensure a constant flux. By comparing this with feedback from the actual output currents, the control circuits are able to make decisions regarding the switching of the power transistors.
CHAPTER THREE:

SYSTEM HARDWARE

Chapter three describes the hardware used to implement the CCI process, and outlines the modifications made to GEC's designs to suit the needs of the car's drive system. Current transducers, an important aspect of the CCI control process are discussed and a non-invasive, electrically isolated current transducer is presented. Protection of the power transistors by means of semiconductor fuses is outlined before the chapter closes with a brief description of the completed inverter, mounted in its purpose built enclosure.

3.1 AN OVERVIEW OF THE MOTOR SPEED CONTROLLER

The industrial motor speed controller upon which the car's drive is based may be considered as consisting of four main functional blocks, as shown in schematic form in figure 3.1.

![Figure 3.1 Block diagram schematic of motor speed controller system](image-url)
3.1.1 Microprocessor

At the front end of the system is a combined micro-controller and programmable logic controller (PLC). The micro-controller accepts information from the human operator, such as the desired output frequency. The operator is able to programme the micro-controller using a four line display and membrane key pad. In addition, closed loop control is possible and up to 4 analogue feedback signals can be accommodated. By means of software commands these may be incorporated into any of four available proportional, integral, derivative control (PID) loops. The PID outputs may be programmed to act either on the output frequency (as would be desirable for a tachometer feedback system to control shaft speed), or can be accessed as a voltage signal from the microprocessor to act upon external equipment.

3.1.2 Control Circuits

The primary output of the microprocessor, regardless of programmed specifications and feedback signals, is a digital representation of the reference sinusoids. Three signals are sent, differing only in phase. Each reference signal is used by one of three identical CCI control circuits (shown in figure 3.2), which undertakes the CCI feedback-decision process described in section 2.1.

All signals exchanged between the microprocessor and CCI control circuit are digital, and transmitted using opto-couplers to provide electrical isolation. This is necessary as the control circuit floats at the motor terminal voltage of its respective phase (the isolation boundary between the micro-controller and CCI controller is shown by the dashed line in figure 3.2). Providing isolation between all the inverter's subsystems is of importance and will be discussed in more detail in section 3.2.1. Data from the microprocessor is converted to analogue signals by a TDA 1543 digital to analogue (D/A) converter (U6). This has a current source output, and an amplifier (based on the operational amplifier U7) is used to convert this to a voltage signal. The gain of the amplifier may be varied (by means of the trimpot VR1), permitting each reference sinusoid to be scaled in order to overcome component tolerance. This ensures that balanced output line currents can be achieved.
Figure 3.2 Control circuit schematic.
An LM339 comparator (U10:B) compares the reference and feedback signals, and accordingly decides which transistor must be switched on. If the feedback signal is below the reference level then its output toggles to +14V, signalling that an upper transistor be turned on. Otherwise the output is -14V and a lower transistor turn on is signalled. The CCI process switching delay T (discussed in section 2.1) is set by means of the resistor-capacitor (RC) network of R3 and C12, which delays the propagation of the transistor control signal from U10:B to the input of a second comparator (U10:A). The output of this comparator, the transistor control signal (TCS), switches to zero volts when the output of U(10:B) is greater than zero volts and is -14V otherwise. These levels correspond to a control logic LOW and HIGH respectively. The final stage of the control board is a combinational logic system implemented by U8 and U9. This system; converts the single logic signal from U10:A into two separate drive signals A and B (for the upper and lower power transistors respectively), generates the necessary dead-time and shuts off the power transistors in the event of a fault.

A dual monostable multivibrator package (U8) provides the dead time $t_d$. Positive transitions in the transistor control signal are detected by U8:A and negative transitions by U8:B. Both devices respond by switching high for the duration of the dead time which is set by the RC delay circuits of C1,C5 and RP1-B, RP1-A (see Appendix One). When either is HIGH the outputs A and B are frozen HIGH, a state that ensures both power transistors in any one phase of the three phase bridge are held off.

Component U9 is a dual decoder. The outputs (OUT1-OUT3) of its constituent decoders switch LOW when the decimal value of its inputs (A0 and A1), where A0 is the least significant bit, switch HIGH. For example, if A0 is LOW and A1 is HIGH (decimal two) then OUT2 becomes LOW. The microprocessor is able to directly disable this IC, sending all its outputs high by means of a STOP signal, resulting in the shut down of both power transistors in the phase. Such a signal is transmitted in the event of the microcontroller detecting a fault, or during a normal stop procedure at the user’s request.
Also incorporated into the decoder is an input from the short circuit detector U10:C and U10:D. Here, the feedback voltage signal derived from the output line currents is compared to a level specified by the zener diodes ZD3 and ZD4, for the positive and negative directions of current respectively. If either level is exceeded, then one of the comparators in the circuit switches its output to -14 volts (a logic LOW). This sends the most significant bit of U9:A LOW, again forcing outputs A and B HIGH to shut off the power transistors. The microprocessor is signalled of this condition by way of the opto-coupler U5. As a result transmission of the reference sinusoids ceases and the operator is warned of an overload by means of an error message and a warning lamp. The system must subsequently be cleared of the fault and restarted.

The CCI control logic implemented by U9 is most conveniently summarised by the truth table of table 3.1.

<table>
<thead>
<tr>
<th>Input Signal</th>
<th>Output</th>
<th>MD Switching States</th>
</tr>
</thead>
<tbody>
<tr>
<td>TCS</td>
<td>DT1</td>
<td>DT2</td>
</tr>
<tr>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>X</td>
<td>HIGH</td>
<td>X</td>
</tr>
<tr>
<td>LOW</td>
<td>HIGH</td>
<td>LOW</td>
</tr>
<tr>
<td>HIGH</td>
<td>LOW</td>
<td>LOW</td>
</tr>
</tbody>
</table>

NB  X = Don’t Care.

Table 3.1  Truth Table for Transistor Control Logic.

3.1.3 Control Circuit Modifications

Only minor modifications were made to the CCI control circuits for the car’s inverter since the CCI switching process used by GEC was not altered, other than to reduce the switching frequency of the power transistors by increasing the delay T.
Maximum transistor switching frequency \((f_s)\) is approximately related to \(T\) by [Round, 1992]

\[
f_s = \frac{1}{4T} \quad \text{(Hz)} \quad (3-1)
\]

In turn \(T\) is related to the time constant of the delay circuit formed by \(R3\) and \(C13\) by the well known formula:

\[
T = 4(R3\cdot C12) \quad \text{(s)} \quad (3-2)
\]

On substituting equations 3-1 into 3-2 then it can be seen from equation 3-3 that if \(C12\) remains constant then the switching frequency is inversely proportional to \(R3\). By increasing \(R3\) from 33k\(\Omega\) to 120k\(\Omega\) the maximum switching frequency was thus reduced by a value of three to (approximately) 2500Hz.

\[
f_s = \frac{1}{16R3\cdot C12} \quad \text{(Hz)} \quad (3-3)
\]

The only other modification made to the control circuits was to reduce the gain of the current feedback signal amplifier (based on U12) from 31 to 10 to suit the current sensors employed in the inverter. Current sensing is further discussed in section 3.2.

### 3.1.4 Base Drive Circuits.

The power transistors in the three phase bridge are NPN devices, and as such are switched on by applying a small positive potential across their base-emitter terminals. In such a state the transistor is said to be forward biased and if \(V_{ce}\) is positive in the sense shown in figure 3.3, then a load current is conducted. It is usual to consider a transistor as a current rather than voltage amplifier, with collector \((I_c)\) current a multiple \(\beta\) (itself a function of collector current) of base current \((I_b)\). [Williams, 1987]:

\[
I_c = I_b\cdot \beta(I_c) \quad \text{(A)} \quad (3-4)
\]
It is also known that power transistors can be better turned off by applying a small reverse bias (negative value of \( V_{be} \)) [Rashid, 1988]. This results in a pulse of reverse base current from the power transistor which decays to zero several micro-seconds later as the transistor turns off. Chapter 4 discusses power transistor switching in more detail.

The CCI switching pulses generated by each control circuit are insufficiently powerful to meet base drive requirements and require amplification. This function is performed by the third section of the inverter, the base drive circuits. Each of the six base drive circuits is essentially a class B amplifier (fig 3.4) designed as a buffer to amplify the current level of the switching signals to satisfactorily operate the main power transistors.

Each phase of the control board drives two base drive circuits; one each from the signals A and B. The base drive circuits float at the potential of the emitter of the individual power transistors they are coupled to. Since these voltages can differ by the full bus potential, GEC had chosen to connect the upper base drive circuit directly to the control circuit and electrically isolate the lower by means of an opto-coupler. This results in each control circuit floating at its respective inverter output terminal voltage.
Figure 3.4 Base Drive circuit. All Resistors 0.25W unless otherwise noted.
In the upper base drive circuit of figure 3.4 (the lower circuit functions in an identical manner), it is seen that the logic signal A is converted into a +/− 14V signal by means of an N channel enhancement mode MOSFET, Q1. This device switches off only when its gate (g) voltage is made equal to or greater than its source (s) potential. Hence when a transistor on signal is transmitted (that is the signal A is LOW at-14V) the MOSFET switches off bringing in the two cascaded NPN transistors (Q2 and Q4), connected as current buffers to the MOSFET, into conduction. Current then passes from the +14V supply into the base of the main power transistor by way of the resistor R7. Similarly, a transistor off signal (0V) turns the MOSFET off, activating the PNP transistors in the base drive circuitry which results in a negative potential (reverse bias) and reverse base current flow.

Looking to the lower base drive, it is seen that an opto-coupler (U11) is used to transmit the control signal B to the base drive. This provides the isolation required between the lower base drive, the control circuit and upper base drive. It does not invert the signal B and hence the control of the lower base drive is identical to that previously described.

When either of the base drive transistors (Q4,Q5,Q9,Q10) switch on, a step change in current results. This can lead to a drop in the nominal base drive circuit supply potential of +/− 14V, due the impedance of the supply lines and tends to limit the rate at which current can initially be supplied to the power transistor. As will be seen in Chapter Four, this can have a detrimental effect on switching. Hence electrolytic capacitors (C15,16,20,21) are seen placed across the supply rails, close to the driver transistors to provide a low impedance voltage source during switching transitions. The 0μ1 capacitors placed at selected points in the circuits act to suppress transients and oscillations associated with the switching processes. Power transistors can only sustain a low reverse bias voltage (usually less than 10V) before the base emitter junction breaks down, destroying the device. The zener diode ZD2 clamps the reverse base emitter voltage applied during turn off to approximately 3V in order to prevent such damage. Notice however that the base drive board negative supply rail is maintained at a much greater potential than is required to turn the power transistors off. This promotes a more rapid charging of the capacitor C16, ensuring that energy is available for successive base drive turn off signals when switching frequencies are high.

The resistor R4 in the lower base drive circuit is not associated with base drive operation, but rather drives the opto-coupler U5 on the control board, providing the isolated PWM voltage feedback signal discussed in section 2.2.1.
3.1.5 Modification of the Base Drive Circuits.

The car's inverter is based on transistors with a considerably greater 300A (see the specifications given in Appendix One) current rating than those used by GEC (rated at 50A) in their commercial drives. As such, these require much large base current signals in order to be switched on and off. The base drive circuits reviewed in the previous section were intended to deliver a maximum continuous current of less than one ampere to a power transistor.

In contrast some 4A of base current is required to turn on the 300A devices and a pulse of up to 6 or 7A is must be drawn from the base at turn off. Hence the base drive circuits required modification to increase their current gain.

Considering again the upper base drive circuit (fig 3.5) the BD131,132 driver transistors Q4 and Q5, (rated at only one ampere) were first replaced with TIP3055 (NPN) and TIP2955 (PNP) devices. These are capable of conducting current of up to 10A, and were readily available, making them a suitable choice for this application. Their on-state power dissipation is also low, minimising the size of their heatsinks, and helping to keep the base drive circuits compact. In turn these driver transistors (Q4,Q5) themselves require a larger base current. To provide this the resistor R6 was reduced from 150Ω to 33Ω, and the pre-driver transistors (Q2,Q3) were uprated from a BC 547,557 pair rated at 200mA to a BC337,BC327 pair rated at 800mA. The resistor R5 was also lowered from 2k2 to 330Ω to increase base current to the pre-driver transistors.

Turn on base current to the power transistors is limited by the resistance R7 and is given by:

\[ I_{on} = \frac{V_{ce} - V_{be(on)} - V_{ee}}{R7} \]  \hspace{1cm} \text{(A)} \tag{3-5}

Where the \( V_{ce} \) is the nominal on state volt-drop across the collector-emitter of Q4 (about 1V - see appendix one), \( V_{be(on)} \) the on state base-emitter potential of the power transistor (2.5V) and \( V_{ee} \) the base driver supply potential (14V). Solving for R gives a value of 2.7 ohm. In practice 2.2 ohm was used, as the transistor voltages assumed in equation 3-2 are only typical and vary from device to device.
Figure 3.5 Modified base drive circuits. All resistors 0.25W unless otherwise noted.
The power dissipation of these resistors was found to be 20W (assuming 4A of current flowing into the 2.2Ω resistor and a 50% duty ratio). To accommodate this, metal clad, wire-wound 50W resistors were used, mounted off the base drive boards on the inverter's main heatsink to keep them cool. Power transistor turn-off currents were increased by lowering the value of the resistor R8 to 1Ω.

As will be discussed in section 3.2, it was considered best to provide full isolation between the upper and lower base drive circuits and the control circuits. This is the reason for the addition of an opto-coupler on the input to the upper base drive circuit.

3.1.6 Base Drive Circuit Testing

A prototype of the base drive circuits was initially tested using a single power transistor, switching current to a resistive load bank from a 200V DC rectifier supply. This was undertaken to ensure that the base drive circuits were capable of controlling the power transistors at voltages and currents similar to those expected for the car. Capacitors were placed across the power transistors as snubbers to overcome the effects of source inductance, (see section 4.4). A signal generator supplied a variable frequency/variable duty ratio stream of logic pulses to the base drive opto-coupler. Power transistor switching was monitored by way of a Tektronix (type 2430) digitising oscilloscope.

Figure 3.6 shows switching waveforms obtained with the transistor operating at 200V, delivering square current pulses (at a frequency of 2kHz and duty ratio of 50%) with a peak of 200A into the load. Testing was done for only short (two to three minute) intervals as the power dissipated in the load was some 20kW, and the load banks could only sustain this for short periods before overheating. Nonetheless results indicated that the base drive circuits were able to switch the power transistors at the voltage and current levels expected in the car.

The linear decay seen in the load current following each transistor turn on was due to the charging and discharging of the smoothing capacitors used to reduce the ripple generated by the rectifier used as the DC supply. Prior to the turn on of the transistor these are charged to the peak rectifier output voltage and begin discharging when current is drawn, leading to a progressive reduction in the supply potential.
Figure 3.6a $V_{ac}$ waveform recorded during initial tests of the base drive circuit.

Figure 3.6b $I_e$ waveform recorded during initial tests of the base drive circuit.

Figure 3.6c $I_e$ waveform recorded during initial tests of the base drive circuit.
3.2 CURRENT TRANSDUCERS

Accurate sensing of output line currents is of importance to the CCI feedback decision process. In the car sinusoidal peak currents of up to 200A can be expected when maximum acceleration is required, while at very low vehicle speeds, current may be reduced to as little as 35A (peak). Hence any current sensor chosen had to be able to cope with large peak currents, whilst providing reasonable accuracy (within 10% was considered sufficient) under light load conditions.

3.2.1 Resistive Sensing

Commonly, current sensing in inverters is done by means of low value series resistors or shunts inserted in each of the output lines. Although simple, cheap and accurate such transducers have their drawbacks.

The use of resistors leads to insertion loss, (Joule heating loss in the series resistance), which at high current levels can become appreciable. The car's original thyristor inverter utilised nichrome alloy resistors which at peak operating currents dissipated some 90W each [Van Rossen, 1985]. Such losses may obviously be reduced by lowering the value of the resistor, at the expense of reducing the magnitude of the feedback signal, making it prone to electromagnetic interference generated by the inverter. The use of resistive sensing can also require that extra isolation be provided for the control circuits since the feedback signal from each resistor floats at the corresponding instantaneous output line voltage.

In figure 3.7 each of the power transistors is shown connected to each of its respective base driver and control board circuits. As mentioned in section 3.1.3, each base drive board floats at the emitter potential of its associated power transistor. Each of the 'top' three base drive circuits (those for Q1,Q3,Q5) float at the instantaneous output voltages of the inverter, with the lower three tied to the negative DC bus voltage. Now consider the controller circuits. If they are connected to a resistive sensor (or shunt in figure 3.7) then each control circuit must also float at its respective inverter output voltage.
Figure 3.7 Isolation schematic (dashed lines indicate isolation boundaries)
For this reason, GEC had chosen to connect their control circuits directly to each upper base drive circuit as no isolation is then required between the resistive sensors, control circuits, and upper base drive, simplifying isolation requirements. The drawback in this system is that large potentials exist between control circuit, increasing the risk of electric shock and damage to testing equipment. Due to the experimental nature of the car project it was envisaged that there would be the need to make many measurements of the control systems with the inverter running. It was thus deemed desirable to electrically isolate the controller from all other circuitry for greater safety during measurement procedures.

3.2.2 Isolated Current Sensors

To provide isolation and avoid excess power dissipation, an alternative to resistive current sensing was utilised in the form of a proprietary device known as a ‘LEM’ sensor (see the data sheet in Appendix One), shown in figure 3.8. A LEM sensor is essentially a hybrid current transformer/Hall effect transducer. A magnetic core encloses the current carrying cable or busbar. This core is gapped and in the gap is placed a Hall sensor (labelled H in figure 3.9).

A secondary winding of \( N_2 \) turns is wound on the core and driven by a closed loop amplifier (figure 3.9) which has the Hall sensor as its input. The amplifier acts as a current source, driving the secondary coil so as to bring point A to zero volts (virtual ground), with this condition achieved only when the flux in the air gap is nullified. Under these conditions the ampere turns on the primary and secondary (assuming negligible flux leakage) are equal and opposite, that is:

\[
N_1I_1 = N_2I_m \\
\Rightarrow I_1 = \frac{N_2}{N_1}I_m
\]  

(3-6)

Here, \( N_1 \) is the single turn formed by the load current conductor passing through the core, carrying the current \( I_1 \). \( I_m \) is the current required to balance the ampere turns, and is proportional to load current. Hence this may be converted to a voltage feedback signal by means of a small external resistor. The current (or turns) ratio of the device chosen was \( I_1/I_m = 200 \).
3.2.3 LEM Sensor Performance

LEM sensors have an over-current capability. The LA 100/S/SP1 device used was chosen as it is rated continuously at 100A over a bandwidth well beyond the maximum switching rate of the inverter. Further it may be overloaded by 100% for up to 3 minutes at a time whilst still providing a signal claimed by the manufacturer to be accurate to within 10%. This overload feature permits the LEM to provide a useful feedback signal under maximum torque conditions. A full set of LEM specifications, as produced by the manufacturer is given in Appendix One.

Prior to installation, the sensors were tested to investigate their tolerance to differing measuring conditions, as specifications provided by the manufacturer were not detailed in this area. Of importance to use in the car was how the sensors coped with fluctuations in the supply voltage, and what effect the nature of the primary conductor (size and number of parallel conductors) had on sensor accuracy, since this was a principal factor governing the method of wiring the output transistors to their loads.
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A simple test circuit consisting of a high current transformer, run from a variac and load resistance was set up, with the LEM placed in the circuit to monitor load current. The output of the LEM was connected to a known resistance (measured with a Kelvin bridge) enabling it to be monitored by a Tektronix (type 520) oscilloscope and voltmeter. A high current shunt placed in the circuit, coupled to an AVO (type M2005) digital multimeter served as a basis for comparing the LEM accuracy. Current was varied from 10 to 80A by adjusting the variac and readings from the probe and LEM sensor were compared for one, two and three conductors passed through the rectangular primary current window seen in figure 3.8. Each conductor was PVC insulated, multi-stranded copper wire of 16mm² conductor cross sectional area for the one and two conductor cases, and 10mm² for the three conductor case.

The results are plotted on figure 3.10, at all times the LEM sensor readings were lower than those recorded by the shunt. It can be seen that the single cable gave best agreement with the current probe, with a maximum error of 8%. Use of three parallel conductors resulted in errors of up to 12%, suggesting that use of multiple conductors would be a less satisfactory means of wiring each pair of power transistors to the output terminals.

Figure 3.10, LEM sensor accuracy characteristics.
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It was initially thought that the supply for the LEMs (nominally rated at +/- 15V DC) might tend to fluctuate with changing load conditions and changing battery bus voltages (this fear was later proved unfounded). The tolerance to the LEM to falling supply voltage was thought to be determined to an extent by the choice of the external measuring resistance $R_m$ as the compliance of the LEM's output current source could be expected to improve for a lower value of $R_m$.

Manufacturer's data recommended $R_m$ in the range 0 - 50Ω, and experimenting with the LEM sensor found that a 10Ω resistor gave immunity to reduction in supply voltage down to 10V at primary currents of over 100A, which was considered to be ample tolerance.

3.3 OVER CURRENT PROTECTION USING FUSES

The high current power transistors used in the three phase bridge are expensive. Hence it was considered necessary to provide protection in the event of a short circuit during the testing of the inverter. In general, transistors are difficult to protect against over-current with fuses, as they can only sustain an over current for a very brief instant before being destroyed. Most common types of fuse are unable to react within such a time and are therefore of no use for transistor protection.

Fuses have two basic ratings. One is the current the fuse can carry continuously and the second is a measure of how much energy the fuse allows through to the circuit it is protecting (under fault conditions) before it blows. This known as the ‘$I^2t$’ or ‘let-through’ rating and has the units A²seconds [Brush].

Put simply, to protect a device with a known maximum $I^2t$ tolerance, the fuse chosen must have an $I^2t$ rating less than that of the device. This ensures that in the event of a fault the fuse blows first. The inverter's power transistors are able to tolerate a (non-repetitive) fault current of 600A for one millisecond, indicating an $I^2t$ rating of 360A²s.
Difficulty was had in finding fuses capable of conducting the 100A RMS of inverter output current whilst meeting let through requirements. A compromise was sought with the use of ‘Type F’ fast acting fuses intended for the protection of semiconductors. Those selected were Brush Fusegear type FE45 devices. With an \( P_t \) rating of 270A\(^2\)s, they could be expected to afford protection of the transistors. Their RMS continuous current rating of 45A, while not meeting inverter requirements at full output current, was considered sufficient to allow initial testing. This gave the opportunity to run the inverter and check for faults with protection in place, prior to running the inverter without fuses at greater currents. Six fuses were used, placed in the connections linking each transistor to its respective DC busbar.

3.4 CONSTRUCTING THE INVERTER

One of the design criteria for the inverter was that the majority of its components be accommodated within the existing enclosure, fabricated for the original transistor inverter. In this way the entire unit could be fitted under the floor of the car between the motors, as was shown in figure 1.1. Mounted in this manner the inverter's heatsink is exposed to the air flowing under the body of the car for improved cooling, and the unit does not intrude into the vehicle's interior.

3.4.1 Printed Circuit Board (PCB) Modifications

The control, base drive and three phase bridge of GEC's motor speed controller were mounted on a single PCB too large to be accommodated into the inverters enclosure. This combined with the circuit modifications outlined in the previous sections required substantial modification of the PCB layouts. All such work was carried out using the computer package Autotrax by Protel Software Ltd, and the original layouts were supplied on computer disk by GEC.
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The three phase control board (consisting of three of the control circuits of figure 3.2) was first entirely separated from the base drives, and its layout then modified to provide more space between each of its major components for greater ease of assembly and maintenance. In addition, extra plugs and sockets were required for communication to the now off board base drive circuits and LEM sensors. With the use of LEM sensors obviating the need for isolated supplies for each control circuit, the control board was given a single common set of supply rails.

The base drive PCB was reduced to a single unit accommodating two base drive circuits. Three such boards were subsequently manufactured to drive all six power transistors. The layout of the base drive boards was substantially altered to both accommodate the larger switching components outlined in section 3.1.4, and as with the control board, extra plugs and sockets were added to accommodate power supply and communication leads. The completed PCB layouts are presented in Appendix Two.

3.4.2 Mounting the Power Components in the Enclosure

A prime concern in assembling the inverter was that the more bulky power components and heavy current conductors be arranged as compactly as possible so that there would be room for the base drive and control circuits. This would in turn ensure that the length of the leads carrying the control signals would be minimised, reducing the effects of electromagnetic interference generated by the switching of the power transistors. The completed enclosure is shown in figures 3.11a-3.11d, on pages 40-42 (the fuses are not shown as their placement was only temporary).

Assembly began by mounting the power transistors onto the large finned aluminium heatsink seen in figure 3.11a and 3.11c. These were evenly spaced on the heatsink to promote an even temperature distribution and avoid hot spots. All mounting bolts securing the transistors were tightened to the screw torque of 3.5 Nm recommended by the manufacturer, ensuring a good thermal contact to the mounting surface of the heatsink. This was aided by a thermally conductive silicon paste applied to the contact surfaces.
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Once in place, the devices had to be electrically linked into the three phase bridge configuration of figure 2.1. This was achieved by means of solid aluminium bars. The maximum permissible current density for large aluminium conductors is approximately 2.5A/mm², (for a temperature rise of approximately 60°C) [Electrical Wiring Regulations, 1980] suggesting that the bars have a cross sectional area of 40-50mm² to carry a current of 100-120A. In practice the conductors chosen had a much larger area of some 160mm², minimising the conductor volt drop and temperature rise.

Looking to figure 3.11b, two large parallel bars are seen to run the length of the inverter, and these are the main DC bus bars. Specially ‘dogleg’ shaped bars were then machined to provide the intra-phase linking between collector and emitter terminals of each transistor pair, and these (see figure 3.11b) can be seen to span the space between each row devices.

Aluminium rapidly oxidises on contact with air, and the oxide tends to reduce the conductivity of any joints made with the metal. This was avoided in practice by polishing surfaces to be joined, and then treating each with an oxide inhibiting paste.

Where possible, all exposed conductor surfaces were insulated by means of heat-shrinking tubing (rated to 600V). While not eliminating all bare, live surfaces this did at least reduce the likelihood of metal objects from coming into contact with the busbars and causing a possible short circuit.

Short lengths of PVC insulated copper cable were required to connect the outputs of each transistor pair to the motor terminal block. As with the aluminium bars, there was a need to be sure that a sufficiently heavy gauge of wire was used to cope with the magnitude of the output currents. Further, these wires had to be able to pass through the rectangular window of the LEM sensors. It was initially envisaged that two or three parallel cables would be used for each connection, as these would be easier to pass through the LEM sensor window. However, the results presented in section 3.2 suggested that best LEM accuracy would be obtained using only a single conductor. A solid rectangular copper bar sufficient to carry 250A [Electrical Wiring Regulations, 1980] served this purpose, coupled at either end to two parallel 25mm² PVC insulated conductors to complete the connection between the transistors and motor terminal block. The bars were passed through the aluminium panel dividing the main and left hand compartments. Insulation here was provided by heat-shrink tubing and rubber grommets.
Figure 3.11a (Top photograph) overhead view of the inverter assembly with the top cover removed. The 'dogleg' interconnecting bars, base drive circuits and MDs are clearly visible. The main busbars can be seen running the length of the inverter (red is positive). The bottom photograph shows the inverter viewed from the rear, displaying the mounting of the base driver circuit boards and the mounting of the LEM sensors on the side panel.
Figure 3.11b  Overhead view of completed inverter assembly (with lid removed).
Figure 3.11c Inverter viewed from rear.

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Figure 3.11d Inverter viewed from front.
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The spaces left between the power transistors permitted the base drive circuit board to be slotted into the enclosure vertically. Care was taken to ensure that these were securely held in place. At the top of the boards, slotted plastic runners (commonly used to secure printed circuit) boards in rack equipment were employed, assembled into the L shaped holders visible at the tops of the base drive boards in figure 3.11d. These were in turn bolted onto aluminum backing plates and fastened to the sidewalls of the main compartment. The boards were secured at the bottom by the L shaped driver transistor heatsinks seen in figure 3.11a and 3.11c which rest against the sides of the power transistors, and by another PCB runner anchored to the main heatsink.

All power and communication links to the base drive boards were done via plugs and sockets, allowing easy disconnection and removal from the enclosure for maintenance.

A space was left available above the base drive boards, and this was used to accommodate the switch mode power supply developed to power the control and base drive circuits [Laird (B), 1993]. This was anchored to the lid of the enclosure, which doubles as the heatsink for the switching components of the power supply. When in place, the supply is suspended upside down within the space above the base drive boards (figure 3.11d).

Finally, a provision was made in the right hand side compartment, for the three phase CCI controller board. In this position it is close to the base drive boards and is surrounded on all sides by aluminium. Both features assist in reducing the electromagnetic interference of the inverter on the control signals.

3.5 SUMMARY

In Chapter three, the system hardware has been presented. The operation control and base drive circuits has been explained and modifications made to these outlined.

LEM current transducers were introduced as a means of isolated, non invasive current sensing. Provided a single conductor was passed through their current windows it was seen that they were capable of providing feedback signals accurate to within 10%. It was noted that although fuses were unable to be installed permanently into the inverter, protection of the transistors could be afforded during initial tests, provided full output current was not required. The Chapter closed with a description of how the inverter, complete with the base drive circuits, control circuits, and LEM sensors, was assembled into the enclosure provided.
CHAPTER FOUR:
TRANSISTOR SWITCHING AND CONTROL

The BJT switches (Fuji type 1DI300Z - 120) used in the inverter’s three phase bridge are capable of conducting 300A DC (with up to 600A permissible in 50μs pulses - see Appendix One). This combined with an off-state blocking capability of 1200V DC means the devices are rated well in excess of requirements for the inverter.

With all control and power circuits assembled, the inverter system was then coupled to the motors and a suitable DC supply (described in Chapter Six). The inverter was then operated and attention was paid to the switching waveforms of the power transistors as both bus voltage and output current were progressively increased.

Chapter four expands on the brief introduction to base drive requirements presented in section 3.2. Fundamentals of transistor operation are (briefly) explained and related to the response obtained from an optimum base drive current used to ensure a faster, more energy efficient switching. These ‘ideal’ drive waveforms are then compared to those applied in practice before the Chapter closes with a discussion on the snubbers installed to afford protection from transient over voltage incurred during the switching process.

4.1 TRANSISTOR CONTROL

Figure 4.1 portrays typical forward bias operating characteristics, from which three distinct regions can be seen. In the linear or active region, the transistor supports a high value of collector-emitter voltage ($V_{ce}$) whilst still conducting a collector current. Conduction loss, the product $V_{ce}I_c$ is thus large, and this mode of operation is generally avoided in power applications.

It is usual instead to drive the transistor into a saturated or quasi-saturated state where $V_{ce}$ is at or near its minimum value for a given collector current, minimising conduction loss. For a fixed load impedance and bus voltage, saturation is achieved by increasing base current above a given minimum (specified by the manufacturer). In this state, saturation is achieved, with load (=collector) current determined essentially only by the load impedance and supply potential.
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Transistor Voltage/Current Characteristics at Selected Base Currents.

I<sub>e</sub> (A) vs. V<sub>ce</sub>(max) and V<sub>ce</sub>(sat) vs. I<sub>b</sub> increasing

Linear Region

Breakdown Region

V<sub>ce</sub>(V)

Figure 4.1 Transistor forward bias characteristics.

For power transistors β tends to be low at around ten, and reduces at high values of collector current. In the inverter, I<sub>e</sub> has a peak value of 200A, and a base current of up to 40A would be required to ensure saturation. Since this does not flow into the load, the energy it carries is wasted, being dissipated as heat both in the transistor itself and the base drive circuit.

In an effort to reduce base current, manufacturers often sell power BJTs not as single devices but rather as two or three transistors cascaded in a Darlington configuration, all manufactured on a single wafer of silicon. Termed monolithic Darlingtones (MDs) these have a β in the order 50-150. Such devices are employed in the car and use the triple Darlington configuration seen in figure 4.2.
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Figure 4.2 The Triple Darlington configuration of the MDs used.

Here, the base drive circuit has only to drive the small, pre-driver transistor Qa into saturation. This in turn activates the driver transistor Qb, and finally the main transistor Q. Each of the driver transistors amplifies the original control current such that the overall $\beta$ of the MD is approximately the product of the $\beta$ of all three devices [Mohan, 1989]. For the Fuji type 1DI300Z-120 MDs $\beta$ is typically 75 (exact values of $\beta$ vary for any individual MD) at the rated maximum collector current of 300A. The improved current gain means that a base current of only three or four amperes is necessary to ensure saturation at a collector current of 300A (see Appendix 1).

A larger value of $V_{be}$ is required to turn on a MD, since current from the control circuits must pass through three series connected base emitter paths. At a base current of four amperes $V_{be}$ was found to be approximately 2.5V, whereas a single power transistor would operate with a forward bias in the range of two thirds to one volt.
4.2 FUNDAMENTALS OF TRANSISTOR OPERATION

Full details of transistor semiconductor physics are beyond the scope of this work, and this section provides only a brief reminder of transistor operation. The main difference in construction between low voltage, (logic level) switches and the those used in the car is examined, particularly with respect to the effect it has on switching characteristics.

Figure 4.3 shows a simplified silicon construction schematic for both a logic level and a high voltage power transistor. Both comprise of a p type semiconductor material (in the base) inserted between two n type regions [Rashid, 1988]. Two p-n junctions (diodes) are thus formed, one between base and emitter regions and the second between base and collector. Initially, under the assumption of a small collector current, both devices behave in a very similar manner, and the low voltage transistor model serves to describe both.

![Logic Level Transistor](image1)

![High Voltage Power Transistor](image2)

Figure 4.3 Simplified silicon construction schematic.

Assuming a positive value of bus voltage, at least greater than any expected value of $V_{be}$, then at turn on the base emitter p-n junction becomes forward biased and the base collector junction reverse biased. Electrons in the emitter n region are drawn into the p region of the base, as occurs with any forward biased diode. However, unlike a diode where all injected electrons undergo recombination in the p region, only relatively small numbers remain in the base to recombine with holes and support a base current.
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This is due in part to the relative thinness of the base region, such that mobile electrons entering the base are present for only a brief interval before being swept into the collector region by $V_{be}$ to support the collector current. The heavily doped $n^+$ regions shown, provide a low resistance interface from the silicon wafer to metal pads used to connect the transistor to the outside world.

The lightly doped $n^-$ collector drift region, used in power transistors, is the feature that permits them to block high voltages when switched off. When $V_{be}$ is less than or equal to zero, virtually no electrons are injected from emitter to base. A wide region depleted of free charge then forms in the collector drift region. This essentially acts as an insulator, isolating the collector and emitter [Billings, 1987], preventing the device from breaking down in the presence of high voltage.

Ordinarily such a lightly doped region has an inherently high resistance, leading to high conduction losses. However, as the transistor begins to conduct an appreciable current this is overcome by a process known as conductivity modulation. Consider a power transistor initially operating in the active region of figure 4.1. If base current is now increased then collector current rises and $V_{ce}$ falls. Initially the increasing current gives rise to an increased volt drop across the collector drift region and the reverse bias of collector-base junction is reduced. As current increases still further, this junction becomes forward biased (that is $V_{cb}$ is less than $V_{be}$).

Holes are now attracted from the base into the collector drift region. These in turn attract electrons from the collector $n$ region such that free charge density and conductivity increase. A transistor becomes saturated when charge entirely spans the drift region essentially shorting it out [Mohan, 1989].

In practice MDs are unable to go into full saturation, that is to say the collector drift region of the main transistor is never fully shorted by free charges. This occurs because the driver transistor $Q_b$ clamps the potential across the base-collector junction to its own saturation voltage, limiting the extent to which it can become reverse biased. This maintains the main transistor in a state of quasi-saturation, with $V_{ce}$ at $V_{ce(qsat)}$ as shown in figure 4.1. The resulting increase in $V_{ce}$ is small (approximately one volt), but at high current accounts for several tens of watts of added conduction losses.
Two important effects are worth considering with regard to the effects of conductivity modulation on the switching both diodes and transistors:

1) It takes a finite time for charges to be injected into the drift region. During the inversion process when current is commutated from transistor to diode, it follows that initially until conductivity modulation is established, the high resistance of the diode results in a large forward volt-drop [Philips, 1991]. This was found to have an effect on the transistor drive waveforms, as will be discussed in the section 4.4.

2) When a diode or transistor switches off, conduction cannot cease until the drift region has been cleared of free charge. This can result in a longer turn off time. In the case of transistor turn off such a delay can be reduced by appropriate shaping of base drive waveforms [Finney, 1987], as discussed in the next section. In the case of a diode, during turn off, when a reverse bias is applied, a current is initially conducted in the reverse of the normal direction until charges are cleared from the device when conduction ceases.

4.3 SWITCHING CONTROL WAVEFORMS

During both turn on and turn off, a transistor must pass through the linear region of figure 4.1, a process which takes a finite switching time \( t_s \). During this interval both high current and voltage are supported by the transistor as charge levels rise or fall, such that instantaneous dissipation is large [Clemente - Pelly, 1993].

The total energy lost \( (W_e) \) during a switching transition of duration \( t_s \) will be [McMurray, 1980]:

\[
W_s = \int_{0}^{t_s} V_{oa}(t)I_a(t)dt
\]  

(4-1)

Optimum shaping of the transistor control or base drive waveforms, by the base drive circuits can lessen switching times and hence \( W_s \).
4.3.1 Turn On

To provide the fastest possible turn-on, base current is initially made greater than that required to maintain saturation, promoting a more rapid injection of charge into the transistor base emitter junction. This in turn increases the rate of charge injection into the collector.

In the case of a MD, the need to provide such a large turn on current is reduced, as the integral drive transistors are able to provide a large turn on current into the main power transistor, and in general Darlington systems turn on more quickly than single transistors [Mohan, 1989].

4.3.2 Turn Off

A continuous flow of base current must be supplied to keep a transistor in a conducting state, since it is the forward bias on the base emitter junction that maintains the supply of electrons to the collector. Removal of base current leads to turn off. However, if current is simply removed then charge in the drift region is lost only by internal recombination processes, which are too slow for most practical purposes [Mohan, 1989] and lead to an increased turn off time.

Turn off can be hastened by applying a reverse bias to the base emitter junction. The turn on process outlined in section 4.2 is now essentially reversed, with a large portion of electrons in the drift region being swept back into the emitter where they are removed by the emitter current. As with turn on a small portion of the electrons undergo recombination in the base and a reverse base current must be conducted by the base drive circuits.

4.4 MD RESPONSE TO IDEAL SWITCHING WAVEFORMS

Figure 4.4 models the switching circuit of a single MD (Q2 shown for simplicity as a single transistor) in the three phase bridge, and figure 4.5 shows the response of the transistor to ideal base drive waveforms [Mohan, 1989]. Prior to switching the device, it is assumed that a bypass diode D1 was in conduction carrying a the load current I and that D1 is able to switch without delay.
Referring to figure 4.5, at time t=0 a positive bias is applied and $I_b$ rises steadily to its nominal on state value. During the interval $t=0$ to $t = t_0$ charge is injected into the base emitter regions of the MD. Following this at $t_0$ conduction begins and collector current rises. At this time the Diode D1 is still conducting a portion of the load current and hence remains on, clamping $V_{ce}$ to the bus voltage ($V_{bus}$).

At $t=t_1$ collector current has risen to the value of load current and D1 now switches off. $V_{ce}$ now begins to reduce, and conductivity modulation occurs shortly afterward ($t_2$), with quasi-saturation reached at $t=t_3$.

Some time later ($t_4$), turn off will be initiated and base current is reversed. Excess charge in the collector drift region of all three transistors is removed during the storage time interval, $t_5$ to $t_6$. The driver transistors QA and QB cease to conduct some time before the main transistor due to their smaller size. This reduces the number of parallel paths available to carry the collector current and causes the small increases seen in $V_{ce}$ seen over the intervals $t_5-t_6$ and $t_6-t_7$. At the same time, the diodes Da and Db (shown in figure 4.2) become forward biased, connecting the base drive circuit directly to the base of the main power transistor permitting charge extraction to continue.

As charge in the main transistor becomes exhausted, the overall $V_{ce}$ begins to rise more sharply at $t = t_8$. Diode D1 cannot conduct until $V_{ce}$ reaches $V_{de}$, hence the transistor must continue to carry the full load current, and losses in this interval are high. Switch off concludes at $t=t_9$ when $V_{ce}$ reaches the DC bus voltage and current commutates to the diode, with $I_c$ dropping rapidly to zero.
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Figure 4.5, Model transistor switching waveforms.
4.5 SNUBBERS

The busbars and heavy cables used to supply current to each MD all have a certain self inductance which appears as a source inductance $L_s$ to the MDs during switching [McMurray, 1972]. At turn off when current is commutated from MD to bypass diode, collector current flow ($I_c$) in this source inductance changes, and a potential is induced:

$$E = L_s \frac{dI_c}{dt} \text{ (V)} \quad (4-2)$$

Given that the lengths of the connections to each MD in the inverter are relatively large, $L_s$ is large. This, coupled with large values of collector current, means the potential induced in the source inductance can be very high, and may exceed the 1200V maximum blocking capability of the MDs. In such an event collector current increases exponentially, as avalanche breakdown takes place within the silicon wafer. Power dissipation is high (due to the large potential across the MD) and destruction follows virtually instantly.

A common approach to controlling over-voltage is through the use of conventional [Ferraro, 1982] turn off snubbers. In the car, the first form of snubber experimented with was a resistor-capacitor (RC) device snubber with a bypass diode. Operation of this circuit [Moshe, 1985], with reference to figure 4.6 is straightforward. The capacitor $C_s$ is normally in a discharged state prior to MD turn off. As turn off progresses, the rising value of $V_{ce}$ seen on the interval $t_5$ to $t_6$ of figure 4.5, charges the capacitor via $D_s$ to the DC bus potential. During this period the snubber does not absorb energy from the stray inductance, but rather from the DC bus.

It is not until after $t_6$ when current commutates to a bypass diode, that an EMF is induced in $L_s$ and the capacitor charges to a potential exceeding the DC bus voltage (figure 4.6b). The energy ($W_{L_s}$) stored in the source inductance prior to turn off is given by:

$$W_{L_s} = \frac{L_s I_c^2}{2} \text{ (J)} \quad (4-3)$$

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Figure 4.6, a) RC Device snubber.  b) Charging of capacitor during turnoff.
c) Initial discharge into DC bus.  d) Final discharge through transistor
The energy of the snubber capacitor charged to some voltage $V$ is:

$$W_c = \frac{1}{2} CsV^2 \quad (J) \quad (4-4)$$

Hence, the amount $\Delta V$ by which the capacitor overcharges is obtained by equating both energy expressions and solving for $V$:

$$\Delta V = \sqrt{\frac{LsI^2}{Cs}} \quad (V) \quad (4-5)$$

From equation 4-5 it is seen that over-voltage is proportional to the magnitude of output current. In practice, because $Ls$ was unknown, snubber capacitors were chosen experimentally by installing different values of capacitance into the snubber circuits and observing the over-voltage as output current was increased. A capacitance of 0.33 microfarad was found to limit over-voltage to 400V at an output current level of 100A RMS per phase.

Energy in the snubber capacitance is given up by two mechanisms:

1) As soon as current flow into the capacitor ceases, $Ds$ becomes reverse biased and the capacitor discharges into the DC bus via $Rs$ and the bypass diode of the second MD in that phase (figure 4.6c). A portion of this energy is thus returned to the DC supply. This mode ceases when $Cs$ falls back to the bus potential.

2) The remaining energy is lost as heat during a subsequent turn on of the MD, now with the snubber discharge current ($I_s$) flowing through both $Rs$ and the MD itself (figure 4.6d).

Device snubbers tend to be wasteful of the energy stored in $Cs$ as most is dissipated in $Rs$. This is particularly so at low output current levels where capacitor over voltage is low and most of the energy is lost via mechanism two. Average snubber power loss is proportional to frequency:

$$P_{\text{snubber}} = 0.5 CsV^2 f_s \quad (4-6)$$
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Due to the asynchronous nature of the MD switching strategy, the exact value of $f$, is unknown, and was assumed to be 2500Hz. Hence for an RMS output current of 100A per phase, snubber power loss calculated was at 30W.

The value of $R_s$ must not be too great, as the capacitor should be completely discharged within the minimum MD conduction time of four milliseconds. If not, then capacitor energy, and hence voltage will rise with each successive switching. Thus the RC time constant of the snubber should be chosen such that:

$$4R_s C_s \approx 4 \text{ms}$$
$$\Rightarrow R_s C_s \approx 1 \text{ms}$$  \hspace{1cm} (4-7)

Three parallel connected 39 Ω, 10W resistors were used in the snubbers as they were readily available and satisfied both dissipation and time constant requirements. The snubbers were found reliable at all currents during testing, for DC bus voltages below 200V. Above this the capacitors were found to fail after only a few minutes of operation. Failure was found to occur regardless of the magnitude of output current and it is thought that the capacitors were unable to cope with the stress of repeated charging directly from the 240V dc bus. All capacitors have a certain internal resistance [Billings, 1987] and direct connection across a high voltage leads to excessive dissipation in this resistance. The resulting localised heating can lead to damage of capacitor insulation and an internal short circuit is created.

In an attempt to overcome this problem and reduce snubber power loss, an alternative snubber system was sought in the form of bus, rather than device snubbers. These had been initially considered for the original transistor inverter [Van Rossen, 1985] and consequently some parts were available for their construction. The circuit for the bus snubbers is identical to that of figure 4.6a. However, instead of being connected across the collector emitter terminals of each device, the snubber is placed across a pair of devices.
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Bus snubber capacitors are placed under less charging stress than those used in device
snubbers since they are connected across the DC bus and do not discharge below the bus
voltage. Figure 4.7b shows the siting of a bus snubber and figure 4.7a indicates how if
affords protection. A bus snubber is able to protect both devices since when either Q1 or
Q2 switches off the direction of current prior to switching is identical for both. Hence
voltage induced in the source inductance always acts to raise the potential difference between
the connection points A and B (figure 4.7a). Such an over-voltage forward biases the diode
Dbs and charges the capacitor Cbs. Capacitor over voltage is given by equation 4-5 as
before.

The resistor Rbs is required to provide damping during the discharge of the capacitor
which occurs once current ceases flowing in the source inductance. Without this resistance
current flowing into the DC bus was found to exhibit noticeable oscillations, thought to be
due to resonant action between the snubber capacitance and ls.

Energy loss in the snubber resistor is much less than with the device snubber as
energy flow in and out of the bus snubber capacitor (Cbs) is only that energy stored in the
stray inductance prior to turn off. Furthermore only a portion of this energy is lost heating
Rbs, the remainder being returned to the supply. The greater efficiency of the bus snubbers
allowed Cbs to be made large at 4.7 μF. This afforded better protection of the MDs and
reduced the likelihood of capacitor failure, as larger capacitors tend to have a greater
tolerance to a large charging current. A 39 ohm, 10W resistor was found to give adequate
damping and did not become hot during testing, confirming low power dissipation.

Choice of the diode Dbs was found to have a bearing on snubber performance. Peak
snubber current is equivalent to peak output current at approximately 200A, and snubber
diodes must be rated to cope with this. BYX 30 devices had originally been used in the
snubbers and are tolerant of repetitive current surges of up to 310A (see Appendix one).
However immediately after the bus snubbers were installed voltage spikes were found in the
base emitter voltage waveforms. These were of concern as they reached peaks of up to
-10V, which is the maximum permissible reverse bias base-emitter voltage (see Appendix
One). The cause of the spikes was traced back to the snubber diodes.

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Figure 4.7a Bus Snubber circuit.

Figure 4.7b Bus Snubber Construction
In section 4.2, it was noted that diode internal resistance during turn on is initially high until conductivity modulation begins, and consequently a transient, negative value of $V_{ce}$ was generated at the end of the turn off process. As will be discussed in section 4.6 transients in $V_{ce}$ are able to couple across to the base by means of the MDs intrinsic parasitic capacitances. A cure for this was effected by using a larger BYX 25 diode. These in addition to offering an improved surge current rating of 440A, also exhibited a less noisy turn on, and an improved base drive voltage waveform resulted.

4.6 EXPERIMENTALLY RECORDED SWITCHING WAVEFORMS

A Tektronix 520 digitising oscilloscope and matching printer served to investigate and record the actual nature of the MD voltages and currents during switching when the inverter was operated from a 220VDC bus, supplying 50A RMS per phase to the car’s induction motors. The waveforms observed have a general appearance similar to those considered as ideal in section 4.4. All waveforms were recorded using a MD which had been disconnected from the DC busbar and was supplied by a separate cable from the DC supply to enable a current probe (Tektronix type AM 503) to be inserted into the collector circuit of the device. As will be described in section 4.7, capacitors were placed across the base-emitter terminals of the MDs to protect against very short lived transients which were found to be the cause of device failure during the early stages of inverter testing. To be effective the capacitors had to be placed as close as possible to the MDs, otherwise the inductance of their leads and connection wires markedly reduced performance. The MD base drive waveforms shown were done with this capacitance in place, and hence differ slightly from that which would be recorded without the protection in place.

4.6.1 Turn on.

From figure 4.8, base current is seen to rise rapidly following the initiation of turn on at time $(t) = 2\mu s$, seen on figure 4.2 (the time scale is $2\mu s$ per division). Initial base current is 5.8A, which occurs while protective capacitance placed across the base emitter terminals (see section 4.7) charges, before settling to the steady state on current of approximately 4A.
Base-emitter voltage rises steadily during the turn on process as the base-emitter regions of the MD accumulate charge, reaching a steady state value of 2.5V. At time $t=12\mu s$ collector current conduction begins, but as discussed in section 4.3 $V_{ce}$ cannot begin to reduce until collector current is equal to the load current, just prior to $t=14\mu s$.

An initial transient is seen in the collector current at turn on, and this is due to the reverse recovery current that is drawn by the bypass diode of the second MD in the same phase as it turns off (recall section 4.2). The total turn on time was observed to be approximately $11\mu s$ (taken from the initial rising edge of the base current).

### 4.6.2 Turn Off

Figure 4-9 is an oscillogram (with a timescale of $10\mu s$ per division) of events at turn off which is initiated at the time $t=10\mu s$, with base current undergoing a reversal from $+4A$ to $-6A$. An initially, larger reverse base current persists for approximately $5\mu s$, due in part to the discharging of the protective capacitance used (see section 4.7).

As predicted in section 4.3, MD turn off does not begin until time $t=30\mu s$, when a significant portion of the MD's stored charge has been removed from the base by the action of the reverse base bias. A small increase in $V_{ce}$ is seen at $t=30\mu s$ corresponding to the turn off of the internal driver transistors of the MD. Following this as predicted, the potential across the main transistor rises rapidly at $t=35\mu s$. As $V_{ce}$ reaches the bus potential of $230V$, load current is commutated to the bypass diode of the second MD in the same phase, and collector current begins to reduce. At the same time, this reduction in collector current induces an over-voltage across the transistor, visible as a spike in the $V_{ce}$ waveform. The peak of this limited by the charging of the bus snubber capacitor.

It should be noted that the collector current trace on the oscillogram is in fact the sum of the MD and bus snubber current, due to the difficulty in physically (but not electrically) separating the snubber from the MD for measurement purposes. Hence during (and only during) the falling edge of collector current, the waveform shown is not strictly representative of the current flowing in the MD. In reality, MD collector current flowing into the MD itself will reduce to zero more quickly than is shown. For this reason, the total turn off time recorded in practice was approximately $25\mu s$, compared to the $18\mu s$ turn off time quoted in the manufacturer's data (see Appendix One).
Figure 4.8 MD turn on waveforms. Timescale is 2μs/division.

Figure 4.9 MD turn off waveforms. Timescale is 10μs/division.
Base-emitter potential is seen to steadily change from +2.5V to about -3V during the turn off process as the base-emitter charges are removed, and a steady state reverse bias condition is achieved. A transient is seen in the trace, coinciding with the over-voltage in V_{ee}. This is in reality not as pronounced as is shown, and was made to appear worse by having both oscilloscope probes connected across the collector-emitter and base-emitter junctions simultaneously (necessary in order to display the correct time relationships between V_{ee} and V_{be}). The capacitance of the probes was sufficient to allow the coupling of the high frequency over-voltage into the channel used to record V_{be}. Removal of the probe across the collector-emitter terminals was observed to virtually eliminate this transient.

4.7 BASE - EMITTER TRANSIENT PROTECTION

During the early course of experimentation with the inverter (prior to installing bus snubbers) two MD failures were experienced. Since at this stage, the RC device snubbers were found to be working satisfactorily, and the base drive boards appeared to function correctly, the cause of this was not readily apparent.

Failure was exhibited as a short circuit across the collector-emitter and base-emitter terminals of the device. The cause of failure was eventually traced back to an unexpected event in the base drive waveforms. A transient some 200ns in duration, but with a peak amplitude exceeding -10V was detected, occurring well after completion of turn off. Such transients were thought to break down the base-emitter and base-collector junctions, leaving the MD in a permanently on state.

With the damaged device failing to a low impedance state, a DC short could be expected across a pair of MDs when the second device in that phase was switched on. Fortunately protection was afforded by the fast acting fuses (see section 3.3) limiting the extent of the damage to one MD.

Protection against the transients was sought in the form of capacitors placed across the base-emitter terminals of the MDs, as shown in figure 4.10. The capacitors chosen were multi-layer ceramic types intended for use in switch mode power supplies. These capacitors present a low impedance path at high frequencies, making them best suited for shorting out the transients.
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Additional protection was also provided in the form of a proprietary device known as a 'Tranzorb', (TZ in figure 4.10). Essentially a Tranzorb is a fast acting zener diode, acting to clamp the base emitter potential of the MDs to 8V. The reaction time of these devices is quoted as 1ps, which is very much less than the rise time of the transient spikes. A diode Dtz is needed to prevent the Tranzorb from becoming forward biased and drawing a large current when \( V_{be} \) is made positive at turn on. Schottky diodes were used for this purpose as they have a fast turn on and do not suffer conductivity modulation. Use of such protective circuitry was found to limit the amplitude of the spikes to around -8.5V at current levels of around 100A RMS per phase, giving adequate protection to the MDs.

![Diagram](image)

**Figure 4.10** MD Base-Emitter transient protection.

Further investigation revealed a probable cause of the transients in \( V_{be} \) to be related to turn on of the bypass diodes. As with the bus snubber diodes, the MD bypass diodes were found to suffer from poor conductivity during the first instant of turn on. Hence when current commutates from an MD to a bypass diode, the diode on state voltage is initially high (several volts). Transistors can have significant parasitic capacitances [Horowitz-Hill, 1981] across their base-collector and base emitter junctions (shown for the main transistor Q in figure 4.10). These can provide a path for transients to be coupled across the MD to its base [Ferraro, 1982]. Hence it was thought that transients generated by the bypass diode were able to influence the base drive waveforms via this capacitance.
Figure 4.11 shows events during the transient, which is clearly seen in the base-emitter potential (trace R2) waveform. Just prior to the occurrence of the transient, $V_{ce}$ (trace R3) is seen to reduce and $I_c$ begins to reverse, indicating that the MD's diode is turning on. Until conductivity modulation (recall section 4.2) sets in there exists an appreciable negative potential across the collector-emitter of the MD, which coincides with the transient almost exactly. By supplying external capacitance to the base-emitter junction a voltage divider is formed with the MD's parasitic capacitances and the magnitude of the spikes reduced accordingly.

Figure 4.11 Base-emitter waveforms during transient. Timescale is 200ns/division.

**Ref1 10.0mV 200ns**

Figure 4.11 Events during the transient in the base-emitter potential (under reverse bias conditions).
4.8 SUMMARY

Chapter four has expanded on the important topic of transistor switching, introduced briefly in Chapter three.

Ideal base drive waveforms were presented as a means by which MD switching times could be reduced, leading to lower switching losses. These were compared with waveforms generated by the base drive circuits, and it was observed that these were close to ideal. Consequently, the MDs were observed to switch in a manner similar to that predicted by theory.

Due to the large physical size of the inverter's interconnecting conductors, coupled with high currents, protection against over-voltage during MD turn off was seen to be an important consideration. Two forms of turn off snubber were introduced. The first, a device snubber was found (after some experimentation) to be an inferior form of protection, dissipating excessive energy and proving to be unreliable at higher bus voltages. An alternative bus snubber system gave improved reliability and reduced energy loss.

The Chapter closed by examining a difficulty experienced in operating the MDs, that of transients in the base-emitter voltage under reverse bias conditions. Capacitors and transient suppressors were seen as a method of reducing, but not eliminating these.
CHAPTER FIVE:
ASPECTS OF INDUCTION MOTORS

The car’s induction motors form an integral part of the drive system, and a basic knowledge of their operation is an important consideration in the analysis of inverter performance. In this chapter selected induction motor theory is presented, followed by an examination of the motor’s operating characteristics when run from a sinusoidal supply. Both discussions serve as a basis of comparison for results obtained during testing of the inverter. The chapter concludes by examining the effect that current harmonics generated by the inverter have on motor operation.

5.1 BASIC MOTOR OPERATION

The squirrel cage machines used in the car are based on an industry standard frame size, giving the machines a rated power of 2.2kW at 50Hz. The stator, when excited by a three phase supply generates a four pole magnetic flux rotating within the air gap between the stator and rotor at a synchronous speed \( \omega_s \). At the rated supply frequency \( f_s \) of 50Hz \( \omega_s \) is 1500rpm. The rotating field induces large currents in a series of aluminium bars embedded in a laminated steel rotor, and these in turn interact with the air gap flux to develop the shaft torque. For a potential to be induced in the rotor conductors, they must from Faraday’s law, experience a time changing flux. In practice this requires that the rotor rotates at some speed \( \omega_r \) less than the synchronous speed in order to cut the air gap flux (\( \Phi \)). This difference, normalised by \( \omega_s \) is termed slip where:

\[
\text{s} = \frac{\omega_s - \omega_r}{\omega_s} \quad (5-1)
\]

Torque (before friction) is proportional to the product of flux and induced rotor current \( I_r \). However, this current alternates at a frequency \( s \cdot f_s \) and consequently there exists a lag \( \theta_2 \) between rotor voltage and current, due to the inductance of the rotor circuit. This delay acts to reduce torque (T), which may be expressed as [Gray 1989]:

\[
T = k\Phi I_2 \cos \theta_2 \quad \text{(Nm)} \quad (5-2)
\]

The equation includes the constant \( k \) to account for parameters specific to any individual machine design.
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5.1.2 A Circuit Model

Figure 5.1 is based on the equivalent circuit for one phase of an induction motor originally presented in figure 2.4. Here however, all rotor quantities have been reflected back to the primary side (stator), and are distinguished as such by the use of upper case lettering.

![Induction motor equivalent circuit model](image)

Figure 5.1, Induction motor equivalent circuit model.

The rotor circuit induced voltage (E_r) and leakage reactance (X_2) shown, represent values taken when the rotor is locked and slip is unity. Under this condition rotor current frequency is constant at f_r such that both reactance and induced EMF are at a maximum and E_2 is now proportional only to the magnitude of flux. As rotor speed increases toward \( \omega_n \), both these values reduce in proportion to the decrease in slip. It is standard practice [McPherson, 1981] to cater for this in the equivalent circuit by making rotor resistance, rather than E_2 and X_2, slip dependent as shown. Note also that rotor resistance includes an extra component R_2(1-s)/s to model the mechanical power absorbed by the load. In this form the circuit of figure 5.1 is the model upon which all induction motor theory in Chapter Five is based.

By inspection from the model it is possible to write [Open Polytechnic, 1991]

\[
I_2 = \frac{E_2}{\sqrt{(X_2)^2 + \left(\frac{R_2}{s}\right)^2}} \tag{A}
\]

Where: \( R_2 + \frac{R_2(1-s)}{s} = \frac{R_2}{s} \)

(5 - 3)
Further, the rotor current phase lag term $\cos \theta_2$ may be rewritten as:

$$
\cos \theta_2 = \frac{R_2}{sZ} = \frac{R_2}{s \sqrt{(X_2)^2 + \left(\frac{R_2}{s}\right)^2}}
$$

(5-4)

Finally, substituting (5-3) and (5-4) into the expression for torque (5-2) yields:

$$
T = k\Phi \frac{sE_2 R_2}{(R_2)^2 + (sX_2)^2} \quad \text{(Nm)}
$$

(5-5)

Where $K = k\Phi E_2$

### 5.2 OPERATING CHARACTERISTICS

Equation 5-5 describes the important relationship between torque and slip [Open Polytechnic, 1991]. The exact values of $R_2$ and $X_2$ dictate this to an extent, but figure 5.2 portrays the general characteristic [McPherson, 1981].

The stable region indicated on figure 5.2 represents operation during normal motoring and within this region any change in load torque acting to slow the rotor increases slip; permitting the machine to develop more torque and stabilise at a new, slower speed. The torque indicated as rated, is that which the machine can sustain indefinitely without suffering overheating from excessive resistive power loss in its windings.

A definite bound on the maximum torque exists. Known as pullout torque, this is typically 2 to 3 times rated torque and can only be sustained for a short period before the excessive line current drawn leads to overheating. Any attempt to force the motor to exceed pullout torque results in entry into the unstable region. Here any increase in slip results in a subsequent reduction of available torque and the motor will stall.
Figure 5.2, Induction motor torque-slip characteristic

Approximations to equations 5-3 and 5-4 are possible. The locked rotor EMF \( E_2 \) is proportional to flux, hence if flux is considered as constant (which remember is true if the inverter control strategy is working) then the product \( \Phi E_2 \) will be a constant \( K \). Further, within most of the stable region where slip is relatively small, torque is seen (from figure 5.2) as approximately proportional to slip. This follows from equation 5-5 where for a small slip the reactance term \( X_2 \) is negligible compared to the resistance term. As a consequence of these approximations torque may be expressed more simply as:

\[
T = \frac{KsR_2}{(R_2)^2} = \frac{ks}{R_2} \quad \text{(Nm)}
\]  

(5-6)

In a similar manner, current may also be written as:

\[
I_2 = \frac{sE_2}{R_2} \quad \text{(A)}
\]  

(5-7)
Chapter Five: Aspects of Induction Motors

To recapitulate, for operation in the stable region, under constant flux conditions, two approximations are possible [Finney, 1987]:

- Torque is proportional to slip
- Rotor current is proportional to slip, and hence torque

Note also that since stator current is the sum of the rotor current reflected back to the stator and a constant magnetising component (\(i_m\)), then it follows that line currents too are proportional to torque [Mohan 1989].

5.3 EXPERIMENTAL DEDUCTION OF MOTOR CHARACTERISTICS

Data regarding parameters for the car's motors when run on a sinusoidal supply was unavailable (except that based on frame size, rated power would be 2.2kW and rated torque approximately 15Nm). Other important parameters and operating characteristics were deduced in the laboratory, so that they might serve as a basis for analysis and comparison to results recorded using the inverter supply.

It was assumed in Sections 2.2 and 5.2 that the inverter is capable of maintaining a near constant air gap flux for changing torque and output frequency. In practice this tends not to be true when motor torque becomes large at frequencies exceeding 100Hz. As will be detailed in Chapter Six, during such conditions the inverter is not always able to force a sufficient line current to ensure proper excitation of the air gap. To provide an insight into machine operation under both constant and weakening flux conditions, a single motor was connected to a variable voltage, low distortion mains supply. A YEW (type 2503) three phase Wattmeter served to monitor line voltages, current and total power (by the two Wattmeter method), while a YEW optical tachometer (model 3632) served to monitor speed.

In the first test, the motor was run from a 30A/phase variac, with line voltage chosen as the independent variable. Under no load conditions; current, power and shaft speed were recorded for selected voltage above and below the rated RMS line potential of 90V. This was then repeated with the rotor locked, but with voltage reduced to 15-32V so as to prevent the machine drawing excessive line current while stalled. From this data, a circle diagram for the machine was constructed.
A standard geometric technique, based on equations 5-3 to 5-5 and assuming flux remains constant at its no-load value, the circle diagram can be used to derive most machine parameters of interest. A brief summary of the procedure used to prepare the diagram and a copy of the one constructed for the motor are presented in Appendix Three. From the circle diagram, a set of graphs were derived portraying performance under constant flux conditions, using the PC package MATLAB.

The second test performed, known here as a constant voltage test, served to show behaviour under conditions where flux weakened with increasing shaft power. A high current moving coil regulator supplied a 90V line to line potential to the motor, kept constant by manual adjustment at all times.

Using one of the friction brakes photographed and detailed in Section 6.1, a known braking torque was applied. Beginning at 5Nm, this was increased in steps of 5Nm and at each interval power, current and shaft speed were recorded. Under these conditions, as torque and line current rise, so too does the potential difference across the stator winding impedance of each phase. From figure 5.1, it follows that $E_2$ will decrease, consequently magnetising current and hence flux are reduced. The general trends recorded from this experiment then served as a basis for examining performance characteristics when the inverter was to unable maintain a constant airgap flux with rising motor power.

5.4 RESULTS

5.4.1 Slip

Figure 5.3 shows slip as related to torque. In the case of constant flux (solid line) the results show slip to rising in approximate proportion to torque as predicted. Linearity is lost to a small extent only as torque approaches the estimated pull out value of 47Nm (see Appendix Three), and is likely to be the result of rotor leakage reactance becoming a more dominant component of rotor impedance such that the approximations used to write equations 5-6 and 5-7 lose their validity.
Figure 5.3, Induction Motor Torque - Slip Characteristic

Legend:
- Constant Flux
- Constant Voltage

Figure 5.4, Induction Motor Torque - Line Current Characteristic

Legend:
- Constant Flux
- Constant Voltage
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Under constant voltage excitation, as flux becomes weakened and the product of flux and induced emf reduces, it follows from equation 5-5 that an additional increase in slip must occur to maintain any given torque above 35Nm. Such a trend is apparent in figure 5.3 (broken line) where slip is seen to rise noticeably as torque exceeds this mark. At the recorded constant voltage pull out torque, (at which the motor was on the verge of stalling) slip was found to be some 27%, compared to 20% for constant flux.

5.4.2 Current

There is little to distinguish between the current-torque characteristics for both constant voltage and constant flux, as seen in figure 5.4. The circle diagram shows current to be proportional to torque up to the 35Nm mark, whereafter, as rotor reactance becomes a more dominant component of impedance, rotor power factor decreases and line current rises at a greater rate to maintain a given torque, coinciding with the increasing slip seen in figure 5.3.

Results recorded for constant voltage tend to show slightly less linearity, but current remains within 10% of values estimated from the circle diagram at all times. This suggests that the weakening of the airgap flux has little effect on the induced rotor current magnitude, and it is instead the phase delay term $\cos \theta_2$, of equation 5-2 that alters principally to maintain torque.

5.4.3 Efficiency.

The car's motors are able to maintain an efficiency of greater than 70% over a wide (5-30Nm) range of torque, for both constant voltage and constant flux excitation. The motors suffer significant loss of efficiency only under the extremes of very light and near maximum load.

For light loads poor efficiency can be attributed to the dominance of the constant losses. These are responsible for the 340W of power consumed at no load, and consist of losses in the magnetising circuit (due to hysteresis and eddy currents), friction and power taken by the shaft mounted cooling fans. The sum of these losses remains nearly constant under all loads [Open Polytechnic, 1991] and hence as torque rises from zero they are quickly eclipsed by rising shaft power, leading to the rapid rise in efficiency seen on the 0-5Nm range.
Figure 5.5, Induction Motor Torque - Efficiency Characteristic

Figure 5.6, Induction Motor Torque - Power Factor Characteristic
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As torque approaches its pullout value of 45Nm, losses in the rotor and stator resistance become large, and this coupled with a falling shaft speed results in a reducing efficiency. This is seen from figure 5.5 to be especially true for the constant voltage case where rotor speed declines more severely under high loads, thereby reducing the output power. As a result; efficiency at pull out torque is 53% under constant voltage conditions, compared to 61% for constant flux.

5.4.4 Power Factor

Input power factor is seen from figure 5.6 to be low at low shaft power, due to the dominance of the magnetising circuit. When the motor is lightly loaded the current through the shunt reactance $x_m$ is a large portion of the total line current, so that impedance appears as largely inductive, giving rise to a poor power factor. As the load and total line current increase, the relative magnitude of the magnetising current becomes a diminishing portion of total line current, and power factor improves steadily to reach a maximum value exceeding 0.8 for all torque greater than 30Nm.

In the case of constant voltage, power factor is seen to be consistently greater at high torque. This follows from discussion in Section 5.4.2, where it was noted that rotor phase lag ($\theta_r$) was thought to increase instead of rotor current, as flux weakened. Since power factor is clearly related to $\theta_r$ through equation 5-4, an overall improvement in power factor can be expected. The reduced magnitude of magnetising current also contributes to the improved power factor.

5.5 MOTOR PERFORMANCE FROM A NON-SINUSOIDAL SUPPLY

5.5.1 Harmonic Components in the Air Gap Flux

It was noted in Section 2.2 that the voltage waveform applied to the motor terminals is a square wave of variable frequency and duty ratio. As with many inverters CCI relies on the low pass filtering provided by the motor’s inductance to attenuate current harmonics.
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In general any nth order current harmonic creates a harmonic component in the air gap flux (a space harmonic) that rotates at n times the nominal synchronous speed [Shepherd-Hulley, 1987]. It follows then that the slip associated with each space harmonic is disproportionately large and losses in the rotor are consequentlly exacerbated.

A detailed Fourier analysis of CCI is difficult due to the asynchronous nature of its switching, which causes continual change in harmonic content. Discussion of harmonic effects is thus limited to a general argument for any nth order harmonic.

First, let the fundamental component of each phase current (under balanced conditions) be defined (where $K = $ magnitude of fundamental component) as:

\[
I_1 = K \cos(\omega t) \tag{5-8}
\]
\[
I_2 = K \cos\left(\omega t - 2\frac{\pi}{3}\right) \tag{5-9}
\]
\[
I_3 = K \cos\left(\omega t - 4\frac{\pi}{3}\right) \tag{5-10}
\]

On substituting $\theta_n = n\theta$ for the nth harmonic the equations become:

\[
I_{1n} = K_n \cos(n\omega t) \tag{5-11}
\]
\[
I_{2n} = K_n \cos\left(n\omega t - n\cdot 2\frac{\pi}{3}\right) \tag{5-12}
\]
\[
I_{3n} = K_n \cos\left(n\omega t - n\cdot 4\frac{\pi}{3}\right) \tag{5-13}
\]

Three forms of space harmonic follow from equations 5-11 to 5-13 depending on the value of $n$. Only odd ($n = 1 3 5 7 \ldots$) harmonics are considered here, as spectral analysis of the output waveforms found even harmonics in the currents to be markedly less prevalent than odd harmonics. This is most likely due to the constructional symmetry of the three phase stator windings of the motors [Gray, 1989] which suppress even order harmonics.
Consider then the case where $n = 3$ yielding:

\[ I_1 = K_3 \cos(3\omega t) \]  
(5-14)

\[ I_2 = K_3 \cos\left(3\omega t - \frac{6\pi}{3}\right) = K_3 \cos(3\omega t) \]  
(5-15)

\[ I_3 = K_3 \cos\left(3\omega t - \frac{12\pi}{3}\right) = K_3 \cos(3\omega t) \]  
(5-16)

Here the phase of all three currents (and hence phase potentials) is identical. Ideally, for a star connected motor, the triplen line voltages will sum to zero at the terminals (see figure 5.7) and a star connection eliminates all triplen harmonics [Brosan, 1966]. In practice the motors used did not have exactly balanced impedances, nor did the inverter generate exactly identical output currents and consequently triplen harmonics were detected in the outputs.

Triplen harmonics generate a stationary rather than rotating component of flux. This induces eddy currents in the rotor, leading to a braking effect which lowers net output torque and increases rotor losses.

![Diagram](image)

Figure 5.7: Cancellation of triplen harmonics by a star connection.
If \( n=5 \) then the equations become:

\[
I_{1s} = K_5 \cos(5\omega t)
\]

\[
I_{2s} = K_5 \cos\left(5\omega t - 10\frac{\pi}{3}\right) = K_5 \cos\left(5\omega t - 4\frac{\pi}{3}\right)
\]

\[
I_{3s} = K_5 \cos\left(5\omega t - 20\frac{\pi}{3}\right) = K_5 \cos\left(5\omega t - 2\frac{\pi}{3}\right)
\]

The phase sequence for \( n = 5 \) is the reverse of that defined by equations (5-9-5.11) resulting in harmonic component flux that rotates counter to the fundamental at 5 times the nominal synchronous speed. Correspondingly, a counter torque is developed, acting again to reduce shaft torque and increase losses, this is true also for \( n=(11,17,23,29,35...) \).

A third form of harmonic field is realised if \( n = 7 \) with the resulting currents:

\[
I_{1s} = K_7 \cos(7\omega t)
\]

\[
I_{2s} = K_7 \cos(7\omega t - 14\frac{\pi}{3}) = K_7 \cos\left(7\omega t - 2\frac{\pi}{3}\right)
\]

\[
I_{3s} = K_7 \cos\left(7\omega t - 28\frac{\pi}{3}\right) = K_7 \cos\left(7\omega t - 4\frac{\pi}{3}\right)
\]

Which, with an identical phase sequence to that of the fundamental generate a component of flux rotating in the same direction, but at seven times the speed. Although the torque developed by the seventh harmonic field acts to assist that from the fundamental, the large slip associated with it means that efficiency is poor.

### 5.5.2 Additional Losses Associated With Current Harmonics

In addition to parasitic torques, harmonics also cause increased stator losses. In the iron core, hysteresis loss is proportional to frequency and eddy current losses to the square of frequency. Consequently [Finney, 1987], the presence of harmonics exacerbates magnetising losses.
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Skin effect in both the stator and rotor conductors results in an elevated harmonic current density, which is to say the effective stator winding resistance presented to current harmonics is greater than that seen by the fundamental. Depending on the construction of the stator and the exact nature of the supply current, it has been demonstrated that stator copper losses can be increased by up to 50% [De Buck, 1979].

The overall increased losses from current harmonics generally require that a motor’s power output be derated by about 10% [Shepherd-Hulley, 1987]. However such a derating is dependent on shaft speed. At low speeds where cooling from the motors shaft mounted fans is poor, a greater derating is required. For example, during the experiments conducted with the cars’s inverter (described in Chapter Six) it was found that when speeds were less than approximately 850RPM (a supply frequency of 30Hz), rated torque could not be tolerated by the motors for more than 10 minutes before overheating set in. In contrast at high speeds, where cooling was much improved, the motors were found capable of sustaining 20Nm of torque for extended periods. In any event, it must be remembered that in the car the total continuous running times are unlikely to exceed one hour, since the batteries will become exhausted after that time, and the motors were observed to be capable of delivering rated torque at all speeds from rated (1450 RPM) and above for at least this duration.

5.6 SUMMARY

An overview of induction motor theory has been presented, from which expected performance characteristics (via the circle diagram method) have been presented, on the assumption of a constant air gap flux. These have been compared to operating characteristics recorded experimentally during which air gap flux was allowed to weaken with increasing torque, as can be expected when the inverter drives the motor at high speeds.

An explanation of the effects of current harmonics on performance has been offered, and from such it is seen that current harmonics in general act to reduce the available shaft torque whilst increasing both stator and rotor losses.
CHAPTER SIX
RESULTS and DISCUSSION

With the inverter's MDs having been found to switch satisfactorily at the voltage and current levels expected to be encountered when driving the car, testing proceeded toward evaluating the performance of the completed drive system. Chapter Six introduces the experimental test bed, describing the measuring equipment used and the testing procedures adopted. Results from all tests are presented in graphical form, and are discussed with reference made to topics presented in earlier sections of the thesis.

Chapter Five showed that harmonics is the motor's line currents could be expected to have a detrimental effect on performance, due to parasitic torques and other loss mechanisms. Chapter Six expands on this, firstly by examining the harmonic content of the inverter's output currents, and then relating this to the motor performance characteristics during testing.

6.1 EXPERIMENTAL TEST BED

Three variables; frequency, torque and bus potential were chosen as the test parameters. The first two are clearly related to the acceleration and speed that would be demanded by the driver's accelerator pedal. The third parameter was chosen to give an indication of how the performance of the drive system would be influenced by the state of charge (SOC) of the batteries. At full charge the DC bus voltage can be expected to stay close to 240V, but this decays toward 200V [Harman, 1988] as the batteries become exhausted. All tests were thus repeated for both a 240V and 200V bus.

The experimental test bed is displayed in figures 6.1a and 6.1b, and its component parts are identified in figures 6.1c and 6.1d. The car's motors can be seen mounted on two large solid concrete blocks used to provide a solid, vibration free mount for the mechanical components.

Each motor was coupled to a friction brake (seen as a rope wrapped around a drum) by means of a special shaft incorporating a torque transducer. Looking at figure 6.1, it is seen that the motor was loaded by suspending weights on one end of the rope to generate a friction torque.
Figure 6.1a View of the test bed showing the motors, brakes, blocks and in the background the Wattmeters and torque meters. The cast iron weights used to adjust the torque can be seen resting on the floor. When the motors run these are lifted by the developed torque.

Figure 6.1b Close up of the friction brake drum, showing the arrangement of the braking rope and the water cooling system.
Chapter Six: Results and Discussion

Figure 6.1c Testbed viewed from front.

Figure 6.1d Side view of Testbed.
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At higher speeds and torques, the power dissipation in each brake became appreciable (several kilowatts). To prevent overheating water was fed to inside the drum where centrifugal forces then served to distribute it evenly throughout the interior, ensuring adequate cooling. The brakes were prone to grabbing (a sudden increase in friction) and vibration, especially at low speeds. This was ameliorated by means of an oil based graphite lubricant applied liberally to both rope and drum.

The British Hovercraft (type TT2-4-CC) torque transducers used employ bonded foil type strain gauge sensing elements, and were purchased for the testing on the Mark I drive system some twenty years ago. Four elements are incorporated into each transducer, arranged as a Wheatstone bridge. Any applied braking torque causes deformation of the drive shaft, in turn altering the resistance of these elements. A matching analogue indicator unit (British Hovercraft Corporation type TM 30) sensed the consequent change in potential across the bridge, displaying the result as a torque in Newton metres (Nm) on an analogue meter. Torques of up to 150Nm, well in excess of the maximum able to be developed by the induction motors could be measured, at speeds of up to 6000rpm. The analogue indicator units, having a high voltage gain, were found to be very sensitive to the stray electromagnetic fields generated by the inverter, resulting in marked fluctuations of their output readings. This was overcome both by using a 24V battery to power the units, avoiding the antenna like effect of their normal supply leads, and by using screened three phase cables to connect the motors to the inverter. Motor speeds were recorded by means of a hand held YEW optical tachometer (model 3632), giving a digital readout of speed in revolutions per minute (rpm).

DC was supplied to the inverter from a three phase moving coil regulator and full wave diode rectifier, together with a large smoothing capacitance. The result was a supply that could be adjusted to provide a bus voltage from 150-260V DC at currents of up to 200A. During the course of experimentation the regulator was continually adjusted to maintain the required bus potential to within +/-5V. Current flowing into the bus was monitored by a clip-on Kaise (model SK 7711) digital ammeter, while bus voltage was monitored using a Philips type (PM 2718) true RMS digital multimeter.
Chapter Six: Results and discussion.

The output line voltage, current and power from the inverter were all monitored using a YEW polyphase true rms Wattmeter (type 2503). Line currents were coupled to this meter by means of two matching wide band Smith Hobson current transformers (type 7110) configured to give a 100:1 reduction in current. This was necessary as the Wattmeter had a maximum current rating of only 30A (RMS).

To summarise then, the variables monitored during all tests are as listed:

- Fundamental component of output frequency, \( f \)
- DC bus voltage, \( V_{bus} \)
- DC input current, \( I_{bus} \)
- Inverter RMS output line voltage, \( V_{ac} \)
- Inverter RMS output line current, \( I_{sc} \)
- Motor torque, \( T \)
- Motor speed (in rpm), \( w_r \)

6.2 EXPERIMENTAL PROCEDURE.

The experimental procedures used to test the system were uncomplicated but time consuming. At the selected bus potential and frequency, torque was increased from 5Nm in steps of 5Nm by successively adding weights to the friction brakes. The exact maximum value of torque attained was dependent on both the frequency and value of bus voltage, and will be further discussed in section 6.4 when results are presented. At each interval the variables listed at the end of section 6.1 were recorded, with adjustments made to the supply to ensure the correct bus voltage prior to taking any readings. Care was also taken to ensure that each motor was developing the same torque.

In a separate test, the ropes were removed from the brake, and results recorded with the motors spinning freely.

Despite the use of water cooling, the brakes were found to suffer from a form of thermal runaway especially at high torque. Localised heating on the exterior surface of the drum tended to cause torque to creep up, often by up to 5Nm within the space of 1-2 minutes. It was thus necessary to wait out this period and trim the weights accordingly to ensure motor torque would remain constant over the minute or so required to read from all the gauges and meters.
Chapter Six: Results and discussion.

At high torque (greater than about 15Nm) motor overheating, particularly at lower speeds, became a difficulty. Frequently between tests the motors had to be run lightly loaded at high speeds in order to be cooled by a strong air flow from their shaft mounted fans. This procedure, while cumbersome to perform repeatedly, provided much faster return to a more normal temperature than achieved by simply stopping the motors and leaving them to cool. The inverter, which had a large heatsink cooled by an electric fan, did not suffer from overheating at any time.

In order to gain an appreciation for the nature of the output waveforms at different frequencies, both time and frequency domain portraits were taken using a Hewlett Packard Dynamic Spectrum analyser (type 3651A), coupled to one output line via a Tektronix current probe/amplifier (type AM503). At intervals of 20Hz, with output line current held constant at 80A RMS (by using a micro-controller software command) the current waveforms and frequency spectra were observed and plotted for later analysis.

All torque tests were repeated at frequency intervals of 10Hz and for both a 200V and 240V DC bus. The resulting information was entered in matrix form into an IBM compatible personal computer for later analysis and graphing with the software package Matlab. Simple routines were developed for such processing (including polynomial and exponential interpolation routines for curves of best fit) and are presented together with the raw data in Appendix Four.

6.3 INVERTER WAVEFORM QUALITY

In section 2.2 it was noted that the switching frequency of the power switches in the three phase bridge had a maximum switching frequency of 2000Hz. This limited switching speed gives rise to current harmonics, since the actual line current is allowed to deviate above and below the desired value of the fundamental component of current (I₁) set by the reference sinusoid.

As was explained in Chapter Two, under most operating conditions switching frequency is constantly changing. Due to this the exact frequencies and magnitudes of harmonics present at any given output voltage, current and motor speed are in continual fluctuation, making a Fourier analysis of the waveforms difficult. Discussion regarding current harmonics is correspondingly limited to general observations.
6.3.1 Factors Influencing the Harmonic Content of Output Waveforms

The harmonic content of the inverter's output currents is determined by the difference between the rate of change in the actual output current (dI/dt) and that of its fundamental component (dI_f/dt), hereafter referred to as α.

The value of α is determined by the magnitude and frequency of the reference sinusoid. Since by definition, this is a scale model of the fundamental component of current it may, for the purposes of discussing harmonics, be considered as equivalent to such.

The instantaneous value of the output current itself is determined by several factors; DC bus voltage, motor speed, and the impedance of the stator windings. During the CCI switching process the motor's terminals are alternately connected to the positive and negative DC bus potentials (with respect to the star point) by the MDs and their bypass diodes. If each switch is on for a given (and continually changing) time t_on, then an expression for I(t) may be developed by using Kirchoff's voltage law around the equivalent circuit model presented in figure 2.4 to yield:

\[(\pm)V_{bus} - E_2(t) - L_1 \frac{dI(t)}{dt} - I(t) \cdot r_1 = 0\]  

\(6-1\)

Where:
- \(V_{bus}\) is the DC bus potential (relative to the motor star point)
- \(r_1\) is the stator winding resistance.
- \(L_1\) is the stator winding leakage inductance
- \(E_2\) is the induced rotor EMF, reflected back to the stator.

Equation (6.1) may be simplified on the basis of two assumptions. Firstly if the stator impedance is assumed to be predominantly inductive, then the resistance \(r_1\) can be approximated as zero. Secondly, if the period of the induced rotor currents is large compared to \(t_{on}\) then \(E_2(t)\) may be assumed constant over that interval. This is equivalent to assuming that the motor's inductance filters most of the harmonic content from the terminal voltage. The resulting expression is a first order linear differential equation which may be solved for I(t), where \(I_0\) is the output current just prior to \(t_0\) to give:

\[I(t) = \frac{\pm V_{bus} - E_2(t - t_1)}{L} \cdot t + I_0\]  

\(6-2\)
Chapter Six: Results and discussion.

The change in current $\Delta I$ over the interval $t_{on}$ will be:

$$\Delta I = \frac{\pm V_{bus} - E_2(t=t_0)}{L} \quad (6-3)$$

Equation 6-3 suggests that for any given $t_{on}$, the change in current is dependent on both the value of the bus voltage, and $E_2$. $E_2$ is in turn proportional to rotor speed and hence varies with any change in load torque and fundamental frequency. The car's motors have been rewound to operate at a nominal (50Hz) phase-neutral potential of 52V RMS (or 90V RMS line-line). If full torque (rated air gap flux) is to be maintained at all speeds (recall section 2.2) then the fundamental component of inverter output voltage ($V_1$) should be varied at the approximate rate of 1.7V/Hz, based on the nominal 50Hz line - line potential of 90V. At low speeds then, $V_1$ and hence $E_2$ is an order of magnitude smaller than $V_{bus}$ and $\alpha$ is large. As a result current changes by a larger amount $\Delta I$ (figure 6.2a) over the interval $t_{on}$ ($t_1$ to $t_2$) and the harmonic content of current is at or near its maximum.

![Figure 6.2a](image1.png) $\Delta I$ when $\frac{dI}{dt}$ is large

![Figure 6.2b](image2.png) $\Delta I$ when $\frac{dI}{dt}$ is small
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At the same time transistor switching rates are at or near their maximum of 2500Hz since the time it takes \( t_0 \) to \( t_1 \) for the current to intersect the reference value is small. Recall also that the output voltage waveforms applied to the motor are square waves with a frequency directly related to the switching speeds of the MDs and bypass diodes. Hence, the frequencies of the voltage (and in turn current) harmonics will also be at or near their maximum under such conditions.

As the frequency of the fundamental component of current increases; both \( \alpha \) and \( \Delta I \) decrease (figure 6.2b). This results in decreasing levels of harmonics in the currents (lower distortion). In addition, the time interval \( t_{on} \) becomes larger, and MD switching frequencies are reduced, lowering the frequency of the harmonics.

Changing the load torque also influences harmonic content. As the induction motors are loaded, both rotor speed and the rotor potential reflected back to the stator (\( E_2 \)) reduce in proportion to torque. As a result, stator current and hence \( \alpha \) increase in proportion to torque. From equation 6-2, it follows then that \( \Delta I \) is unaffected by changes in torque. However, as a proportion of total line current, \( \Delta I \) is reduced and correspondingly harmonic content is diminished.

6.3.2 Inverter Voltage Saturation

The instantaneous magnitude of the line - line potential applied to the motor cannot exceed the DC bus potential. Hence, the peak of the fundamental component of line-line potential too, is equal to the bus voltage. In RMS terms this equates to a maximum of 140V for a 200V DC bus and 170V for a 240V DC bus. Given (from the previous section) that motor terminal voltage must be increased at the rate 1.7V/Hz to maintain constant flux, it follows that for frequencies exceeding 80Hz (200V DC Bus) and 100Hz (240V DC Bus) the inverter is no longer able to meet this demand and air gap flux weakens. Under such conditions the inverter operates in a voltage saturated state.

With dI/dt now at times less than the gradient of the reference sinusoid, output currents are unable to reach the peak sinusoidal currents specified by the reference sinusoid and become distorted, losing their sinusoidal shape. An accompanied increase in harmonic levels is associated with this, as is shown in section 6.3.3. In this state \( t_{on} \) is larger than the interval \( t_2 - t_3 \) and each MD switches slowly, hence the frequency of the harmonics is low.
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At still higher frequencies (greater than 120Hz), output current is unable at any time, other than the reference sinusoid zero crossings, able to reach the requested value of the fundamental component. As a consequence, each transistor remains on for one half cycle of the reference sinusoid and the inverter operates in what is commonly termed a six pulse or six step mode [Finney, 1987].

6.3.3 Selected Output Current Waveforms.

During the course of experimentation the output current of the inverter was recorded with the HP spectrum analyser for a 20Hz (fundamental) frequency intervals with the inverter running from a 240VDC bus, and output current set constant at 80A RMS per phase.

Figure 6.3, recorded at a frequency of 20Hz, clearly shows the large ΔI that results from a large difference (α) between dI₁/dt and dI/dt. As expected (from section 6.3.2), the frequency of the switching ripple seen superimposed on the fundamental is high and is nearly constant over the entire period of the waveform. This is confirmed by the current spectrum where the principal harmonics are seen to be clustered closely about a centre frequency of 1800Hz.

At a fundamental frequency of 60Hz (figure 6.4), both switching frequency and ΔI are seen to be visibly reduced. The current spectrum reflects this, showing a wide distribution of harmonic frequencies, suggesting that the switching rate of the MDs changes considerably throughout each cycle of the fundamental.

At still higher fundamental frequencies (those greater than about 100Hz), as portrayed by figures 6.5 and 6.6 taken at 100 and 140 Hz respectively, there is insufficient potential available from the DC bus to force current to reach the reference level over each half cycle of the fundamental. As a result, the output waveforms are seen to lose their sinusoidal shape and switching rates can clearly be seen to be reduced. Consequently, harmonic peaks occur in the line current spectrum at frequencies below 500Hz.
Figure 6.3a Inverter output current spectrum for a fundamental frequency of 20Hz.

Figure 6.3b Inverter output current waveform for a fundamental frequency of 20Hz.

Figure 6.4a Inverter output current spectrum for a fundamental frequency of 60Hz.

Figure 6.4b Inverter output current waveform for a fundamental frequency of 60Hz.
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Figure 6.5a Inverter output current spectrum for a fundamental frequency of 100Hz.

Figure 6.5b Inverter output current waveform for a fundamental frequency of 100Hz.

Figure 6.6a Inverter output current spectrum for a fundamental frequency of 140Hz.

Figure 6.6b Inverter output current waveform for a fundamental frequency of 140Hz.
6.3.4 Selected Output Voltage Waveforms

The line-line output PWM voltages generated by the inverter contain (especially at low frequencies) a much greater harmonic content than the currents. The car's induction motors act as low pass filters (recall section 6.3.1), such that the current harmonics are reduced in comparison to those present in the line-line voltages. It also follows that the general trend of a reduction in harmonic content with increasing speed, observed in the previous section, carries over to the voltage waveforms presented in figures 6.7-6.9, taken for the same operating parameters as given previously. The voltage scales shown should be multiplied by 100 to obtain actual measured voltages as a 100:1 voltage attenuating probe was coupled to the analyser.

At 20Hz, (figure 6.7) the spectrum is dominated by harmonics at the switching frequencies (which as with current are centred about 1800Hz). Notice that the magnitude of the harmonics is approximately twice that of the fundamental, such that the motor is essentially driven by a 1800Hz, rather than a 20Hz supply. This will be shown in section 6.4.4 to result in a poor low frequency displacement factor.

As frequency increases, harmonic content (as seen with current) decreases. At 60Hz(figure 6.8), a large spread in harmonic frequencies is observed and all peaks are less than two thirds the magnitude of the fundamental. The number of switching transitions in the waveform are visibly reduced over that seen for 20Hz.

At 100Hz (figure 6.9) evidence of voltage saturation is seen with transistor switching occurring only near the zero crossings of voltage where current is reduced. At 140Hz, (figure 6.10) only one switching transition per half cycle of fundamental is seen, and in this state the inverter is unable to force its output current to track the reference sinusoid. The oscillations seen on each switching transition is thought to be the result of snubber action and the excitation of the motor inductance and stray capacitance into resonance by the step changes in potential.
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Figure 6.7a Inverter output line-line voltage spectrum for a fundamental frequency of 20Hz.

Figure 6.7b Inverter output line-line voltage waveform for a fundamental frequency of 20Hz.

Figure 6.8a Inverter output line-line voltage spectrum for a fundamental frequency of 60Hz.

Figure 6.8b Inverter output line-line voltage waveform for a fundamental frequency of 60Hz.
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Figure 6.9a Inverter output line-line voltage spectrum for a fundamental frequency of 100Hz.

Figure 6.9b Inverter output line-line voltage waveform for a fundamental frequency of 100Hz.

Figure 6.10a Inverter output line-line voltage spectrum for a fundamental frequency of 140Hz.

Figure 6.10b Inverter output line-line voltage waveform for a fundamental frequency of 140Hz.
6.3.5 DISTORTION FACTOR.

A measure of the distortion level in the output current is provided by computing the distortion factor $\mu$ [Arrillaga et al, 1985] according to the equation:

$$\mu = \frac{\text{RMS of the fundamental component of current}(I_t)}{\text{RMS of load current}(I)}$$  \hspace{1cm} (6-4)

From which it can be seen that the closer to unity $\mu$ lies, the lower the harmonic content of the output waveforms.

During the recording of the waveforms presented in figures 6.4-6.6, I was recorded using the true RMS Wattmeter and $I_t$ using the HP spectrum analyser. By computing $\mu$ for each case an approximate relationship between frequency and harmonic content could be assessed, and related to the performance of the motors at differing speeds.

Figure 6.11 shows the trend in $\mu$, which as expected is reduced at low frequencies, rising to a peak at 90Hz before declining at higher frequencies, supporting the discussion presented in section 6.3.4.

![Fundamental Frequency - Distortion Factor Characteristic for a 240V DC Bus](image)

Figure 6.11 Frequency - Distortion Factor characteristic for a 240V DC bus, 80A output current.
6.4 PROGRESSIVE LOAD TEST RESULTS

In section 6.4 the results obtained from the progressive load tests are presented. The trends recorded, show a similarity to those presented in Chapter Five for the motors running from a sinusoidal supply. Where differences occur, most can be linked to the effects of current harmonics.

Results have been categorised into three groups, depending on the fundamental component of inverter output fundamental frequency; the first covers the range 10-40Hz, the second 50-100Hz, and the third 110-150Hz.

The maximum torque able to be tested was 40Nm due to the limited availability of weights for the brakes. Further, at fundamental frequencies below 50Hz, it was found that the motors were found to overheat within the space of two to three minutes at high torque, (giving insufficient time to trim the brakes and record all meter readings). This was due both to the limited cooling effected by their shaft mounted fans at low speed, and the increased harmonic losses prevalent at low frequency. Maximum torque for these frequencies was thus chosen at 25Nm.

At fundamental frequencies exceeding 90Hz, (for a 200V bus) and 110Hz (240V) bus, the maximum torque the motors were able to supply before stalling was found to be less than 40Nm and reduced progressively with increasing frequency. This is due to the voltage saturation of the inverter discussed in section 6.3.2 whereby the fundamental component of inverter output voltage is unable to continue rising with increasing speed to ensure correct excitation of the airgap flux, and peak torque is hence reduced.

6.4.1 Slip

Figure 6.12 (page 97) presents torque-slip relationships recorded for both bus voltages. As was discussed in section 5.4.1 slip is seen to be proportional to torque, provided the inverter is not in a voltage saturated state and is hence able maintain constant air gap flux. At fundamental frequencies approaching those coinciding with the onset of voltage saturation, the weakened air gap flux causes slip to be increased, as was also discussed in section 5.4.1., and the curves become non linear and similar to that of figure 5.3.
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Torque-Slip Characteristics for Frequency Group One

Legend:
- 240V DC Bus
- 230V DC Bus

Torque-Slip Characteristics for Frequency Group Two

Legend:
- 240V DC Bus
- 230V DC Bus

Torque-Slip Characteristics for Frequency Group Three

Legend:
- 240V DC Bus
- 230V DC Bus
Chapter Six: Results and Discussion.

At low fundamental frequencies (less than 40Hz) slip for all torques is seen as considerably larger than results recorded for a purely sinusoidal supply. The reasons for this are twofold.

Firstly, the increased current harmonics and hence parasitic torques prevalent at lower fundamental frequencies act to slow the rotor and increase slip. This effect decreases as the fundamental frequency increases (up to the point where the voltage saturation is reached), due to an improving $\mu$.

Secondly, it must be remembered that slip is a normalised quantity. In actuality, the current induced in the rotor (and hence torque) is proportional to induced rotor current frequency which is equal to the difference between synchronous speed and the speed of the rotor (this is also termed slip speed). It is convenient, and standard practice to normalise this and term it slip. When frequency varies slip varies, but the rotor frequency required (assuming a constant flux and no harmonics) to maintain any given torque stays constant. Hence slip, regardless of any harmonic effects will be inversely proportional to rotor frequency. By the same reasoning, at higher fundamental frequencies, slip is seen to be less than that recorded for 50Hz sinusoidal conditions. As an example, at 90Hz (200V bus) a slip of 0.05 occurs at a torque of 25Nm compared to 0.02 for a 50Hz sinusoidal supply (from figure 5.3). Slip speed or rotor current frequency in both cases however is similar at 2.3Hz and 2.6Hz respectively.

6.4.2 Output Line (Motor) Current

The (RMS) current drawn by the motors for most fundamental frequencies was found to be approximately proportional to shaft torque (as seen in figure 6.13 on page 99) which agrees with the theory and results of Chapter Five. At frequencies of up to 80Hz current is generally slightly greater for a 240V bus, due to an increased harmonic content in the current. Since useful motor torque is essentially generated only by the fundamental component of current $I_t$, (see section 5.5) it follows that when the current contains greater levels of harmonics the total current must be increased to supply a sufficiently large fundamental component both to overcome the parasitic torques and develop the required load torque.
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Torque - Line Current Characteristics for Frequency Group One

Torque - Line Current Characteristics for Frequency Group Two

Torque - Line Current Characteristics for Frequency Group Three
Chapter Six: Results and discussion.

At fundamental frequencies above 100Hz however the trend becomes reversed, due to the decreasing flux and value of $\mu$, both of which are more pronounced for a lower DC bus voltage.

Nonetheless, the current required to develop any given torque is seen to be virtually identical for all frequencies, and rises at the rate of approximately 3.2A/Nm.

An anomaly is seen in the results at 100Hz (240VDC) Bus. Here current at no load was approximately treble that drawn in all other cases (60A), and remains unusually high until a torque of 25Nm is reached. This observation was initially attributed to experimental error, and hence the test was repeated, but yielded a similar result. It was thus thought that the current calculating process outlined in sections 2.2.1 and 2.2.2, which relies on a PWM feedback voltage signal from the outputs, was being upset. This may have been due to a particular harmonic frequency present at significant levels only at 100Hz.

6.4.3 Motor Efficiency

Results at any frequency (figure 6.14 on page 101) confirm the general trend seen in efficiency when the motors were operated from a sinusoidal supply. Again, following from the discussion presented in section 6.3, both bus voltage, and in particular frequency, have a bearing on the actual values of efficiency attained.

Recall that peak efficiency for the sinusoidal case was attributed to an optimum balance of the constant losses, conduction losses and power output. Under operation from a non-sinusoidal supply this balance must include the harmonic losses, which as with constant losses tend to be more significant at lower torque (current). It follows then that with harmonic losses diminishing with rising current, peak efficiency is likely to occur at higher torque.

This is reflected in the results, where efficiency peaks at torques greater than 20Nm for frequencies below 60Hz, whereas peak efficiency was developed at 17Nm for a sinusoidal supply. At higher frequencies, a reduced $\mu$ and increased cooling fan speeds, result in efficiency peaking at lower torques (10-20Nm).
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Torque-Efficiency Characteristics for Frequency Group One

Legend:
- 240V DC Bus \( \omega \)
- 200V DC Bus \( \omega \)

Torque-Efficiency Characteristics for Frequency Group Two

Legend:
- 240V DC Bus \( \omega \)
- 200V DC Bus \( \omega \)

Torque-Efficiency Characteristics for Frequency Group Three

Legend:
- 240V DC Bus \( \omega \)
- 200V DC Bus \( \omega \)
Chapter Six: Results and discussion.

For any given torque, efficiency was found to generally improve with increasing frequency. For example at efficiency at 25Nm is very low at 10Hz, not exceeding 40%, for a 200V bus and still less (32%) at 240V. This occurs for two reasons, firstly (and directly from section 6.3.1) ΔI and harmonic content is high at low frequencies. Hence all losses associated with current harmonics (such as parasitic torques and eddy current/hysteresis) are exacerbated. In addition, it should be noted that regardless of current harmonics, motor efficiency will always be reduced at low frequencies.

When shaft speed is low, power output is low, but torque and thus line current remains similar to that drawn at higher frequencies, as does magnetising current. Hence both magnetising and winding losses appear as a much greater portion of the total power consumed and efficiency is reduced.

Optimum motor efficiency was recorded at 82% for a frequency of 90Hz and torque of 25Nm at a bus potential of 200V, and (90Hz, 25Nm for a 240VDC bus) which coincides to the frequency range at which μ was observed to be maximised in section 6.3.5. This result is encouraging as the predicted efficiency under sinusoidal conditions was similar at 81%. This frequency range corresponds to vehicle speeds of 40-60km/hr [Harman 1992], hence peak motor efficiency is available at speeds which will tend to predominate as the car is driven in an urban environment.

At higher frequencies (above 110Hz) efficiency is reduced slightly. This is due to both a decreasing value of μ (recall section 6.3.5), and the power drawn by the motor's shaft mounted cooling fan which increases in proportion to the cube of speed. For example the total power consumed by the motors (for a 240V DC bus) at no load, 50Hz was 1300W, while at 150Hz this had increased to 2130W. Since line current was 26A in both cases copper (I²R) losses would remain similar, and hence the increased power consumption was principally due to increased cooling fan losses.

A higher bus voltage results in a reduced efficiency, particularly at lower frequencies, due to the effects of an increased ΔI and increased current harmonic levels.
6.4.4 Displacement Factor

Displacement factor DF, is the ratio of total real power, and volt-amperes where both include all harmonics, whereas power factor deals only with quantities pertaining to the fundamental. DF is thus defined [Rashid, 1988]:

\[
DF = \frac{\text{Power}}{\sqrt{3}\text{RMSVoltage}\cdot\text{RMSCurrent}} \tag{6-5}
\]

From figure 6.15 (on page 104), DF is seen to follow similar trends to those seen for efficiency. For any given frequency, DF is seen to rise with increasing torque, for the same reasons as those listed in section 5.4.3. Namely, the eclipsing of the constant magnetising current by an increasing total line current.

Frequency however is seen to have a profound effect on DF. At low frequencies, DF is low (less that 0.25), and increases in proportion to torque. As frequency increases DF increases and the relationship between DF and torque becomes more similar to that seen for operation from a sinusoidal supply (figure 5.6).

Results obtained for all tests showed RMS terminal voltage to be lie in the range 185-200V for a 240V DC bus, and 150-170V for a 200V DC bus at all times. This represents a deviation not greater than 10% in RMS line-line voltage. No correlation was observed between RMS terminal voltage, torque and frequency.

The reason for this can be attributed to the harmonic content of the output voltages. From the spectra presented in section 6.3.4, it can be seen that in fact the fundamental components of output voltage do vary in proportion to frequency. For the frequencies displayed (20Hz, 60Hz, 100Hz and 140Hz) the fundamental component of current has, respective RMS amplitudes of 37V, 122V, 192V and 200V. These (except at a fundamental frequency of 140Hz where the inverter is voltage saturated) are similar to those expected at 42V, 104V, and 170V (based on the assumption of 1.7V/Hz line-line).

It is the large harmonic content of the waveforms at this frequency that leads to the disproportionately large RMS values recorded at low frequencies. As frequency rises, the constant terminal voltages recorded suggest that the total RMS harmonic voltage decreases at almost exactly the rate the fundamental increases.
Chapter Six: Results and discussion.

Torque - Displacement Factor Characteristics for Frequency Group One

Torque - Displacement Factor Characteristics for Frequency Group Two

Torque - Displacement Factor Characteristics for Frequency Group Three
In consequence, at low frequency this large terminal voltage leads to a very low DF (less than 0.25 at 25Nm). This is particularly so for a 240V bus where the RMS terminal voltage is some 20-30V greater than for a 200V bus, but the magnitude of the fundamental component of voltage, dependent only on motor speed remains the same.

As frequency increases DF rises, due to a progressive reduction in voltage distortion. Above 90Hz (200V DC bus) and 110Hz (240V DC bus) when voltage saturation sets in and magnetising current becomes reduced, DF reaches a peak of between 0.8 and 0.85. This is similar to that obtained for operation on a sinusoidal supply for constant voltage excitation (see figure 5.6)

For all frequencies below 70Hz DF is reduced for a 240V DC Bus, which follows from section 6.4.2 where it was noted that the current drawn at any torque was greater than for a 200V DC bus. This, combined with higher RMS line voltage (due to a greater harmonic content) leads to a reduced DF. The effect is most pronounced for frequencies in the range 80-100Hz, since here voltage saturation is reached for a 200V DC bus but not for 240V. Magnetising current, is thus reduced at the lower voltage (recall Chapter Five) and consequently gives an improved DF over that for a 240V DC bus. As frequency approaches 100Hz, and voltage saturation sets in for a 240V DC bus, this effect becomes lessened.

6.4.5 Inverter Efficiency

The power dissipated by the inverter results from three principal mechanisms; switching losses, conduction losses and base drive losses. Of the three only base drive losses are invariant to fundamental frequency and torque, and these are considered first.

It was noted in both Chapter Three and Chapter Four that in order to be driven into a saturated state, each MD required a base current of approximately 4A. None of the energy associated with the base drive currents is delivered to the load, and instead was lost as heat in the both the MD base-emitter junction and base drive circuit.
Chapter Six: Results and discussion.

It was also noted in section 2.1 that switching is done in a complementary fashion, which is to say that (excluding the 100 μsecond dead time) for each phase (upper and lower transistor pair) of the three phase bridge, one MD is always forward biased and drawing a base current. At the same time the second MD in that phase is off and draws no appreciable base current. Further, the RMS value of the reverse bias current pulses that occur for up to 25μs during the turn off process is less than 1W, and may be considered as negligible. Hence, the per-phase base drive losses are the product of the base drive supply voltage (14V) and the 4A base drive current (56W), such that total base drive losses are 168W. The efficiency of the switchmode power supply used to power the base drives is approximately 70% and hence the total power lost in driving the MDs is almost constant at 240W.

Figure 6.16 (on page 107) portrays the efficiency characteristics of the inverter for all frequencies and currents tested. As would be expected, inverter efficiency is seen at any given frequency, to decline as current rises as both conduction and switching losses (from Chapter Four) are dependent on current.

Inverter efficiency is closely linked to DF, since this determines the ratio of inverter current (and hence inverter power loss) to inverter output power (motor input power). At light load, and in particular at low fundamental frequencies, when DF is low (less that 0.5) the inverter must deliver a large current in relation to the power supplied and its efficiency reduces. From figure 6.16 inverter efficiency is seen to be at its lowest for an operating frequency of 10Hz at approximately 0.7-0.88 depending on torque (and hence output current), coinciding with the low DF recorded for the same conditions.

In any instance, increasing the DC bus potential is seen to lower inverter efficiency, with this trend again most pronounced at low fundamental frequencies. Raising the bus potential reduces efficiency by both lowering DF and raising switching losses which from equation 4-3 were seen to be proportional to bus voltage.

However as frequency rises and motor torque is increased, inverter efficiency is seen to steadily improve, reaching a maximum of approximately 0.95 for all frequencies above 100Hz. This coincides with the weakened air gap flux exhibited over this frequency range which was observed to give a high DF.
Chapter Six: Results and discussion.

The tendency for efficiency to rise due to an increased motor DF is balanced to an extent by the increasing conduction losses that occur as the inverter becomes voltage saturated. It was noted in section 6.3.2 that at the onset of voltage saturation MD switching rates became reduced, with each device conducting at a steadily increasing duty ratio. Accordingly the bypass diodes conduct with a reduced duty ratio, and because the on state potential across the MD is approximately three times that of the bypass diodes at 3V, conduction losses become more appreciable at high inverter output fundamental frequencies.

6.5 SUMMARY

Chapter Six opened by describing the experimental procedures and equipment used to test the completed motor/inverter system. Current harmonics and transistor switching rates were then discussed with respect to the gradient of the fundamental component of current, bus voltage and motor speed.

Selected waveforms were then presented to illustrate the variation in the harmonics, present in both output voltage and current, with changing output frequency. The distortion factor ($\mu$) was introduced and used to show that minimum harmonic content occurred on the frequency range 70-100Hz.

Torque, current, slip and efficiency results were then presented and it was seen that at any given frequency general trends in all parameters were largely similar to those seen when the motors were operated from a sinusoidal supply. In addition, due to the harmonics in the currents and the effects of voltage saturation, the variation in motor performance with changing frequency was discussed.
CHAPTER SEVEN:
FUTURE WORK

7.1 CLOSED LOOP CONTROL

When the driver of a conventional ICV alters the position of the accelerator pedal both the torque and target speed of the engine are specified, according to the speed and acceleration the driver wishes from the vehicle.

If the Mark II EV is to simulate this, and drive in a manner similar to a conventional automobile (one equipped with an automatic transmission), then it should respond to the accelerator pedal in a similar manner. This is equivalent to having both the rate of change of the fundamental frequency (known as the ‘ramp rate’) and its target value made proportional to the depression angle of the accelerator pedal. However such a control strategy is complicated by the nature of the motor’s torque-speed characteristics.

It was shown in both Chapters Five and Six, that motor torque was proportional to slip. Consider then the case where the ramp rate is allowed to exceed the vehicle’s acceleration rate. Remembering that a fixed ratio transmission is used, then such an event will increase the slip, and (up to a point) increase the torque. However if the ramp rate continues to exceed the acceleration rate then the motors will enter the unstable region indicated on figure 5.2 and their output torque will reduce. The probable response of the driver to such an event would be to depress the accelerator pedal still further in an attempt to raise torque. This will result in an increased target fundamental frequency which will actually further reduce, rather than increase, motor torque. In any event, the microcontroller will react to the excessive line currents drawn under such conditions, and respond by shutting down the MDs. Restarting can only be accomplished by manually clearing the fault, as discussed in Section 3.1.1. This is likely to prove in the least inconvenient, and at worst the cause of a traffic accident.

The simplest method to avoid such difficulties is to pre-programme the microcontroller with an absolute maximum permissible ramp rate, chosen for the worst anticipated acceleration conditions, such as a fully laden vehicle pulling away on a hill. The disadvantage to this approach is that such a limit will markedly reduce the car’s potential acceleration performance when the vehicle is on level ground and carrying a lighter payload.
Chapter Seven: Future Work.

With an anticipated power to weight ratio of only 17kW/tonne (compared with 80 - 100kW/tonne for a modern ICV [Automobile Association, 1993], any such reduction is likely to make the vehicle too slow to be safe in urban driving.

A closed loop frequency control system, working on slip speed would provide the best solution (as shown in block diagram form in figure 7.1.)

![Diagram of closed loop slip speed control system]

**TFD = Internal Target Frequency Detector.**  
**PID = Internal Proportional Integral Derivative Block**

Figure 7.1 Closed loop slip speed (torque) control system

Both the accelerator and brake pedals of the Mark II are equipped with potentiometers to sense the depression angle of the pedals. The micro-controller unit has an expansion port to 'read' analogue signals, which are digitised to enable them to serve as inputs to the micro-controller. Hence it is envisaged that a minimum of external hardware is required to implement the control system shown in figure 7.1.

Torque (or slip speed) control, is provided by using an external tachometer feedback loop and one of the four available software PID loops incorporated into the micro-controller unit.

A slip speed signal ($\omega_s$) taken as the difference between shaft speed read from a tachometer and the fundamental component of frequency. The latter could be read from either the frequency log kept by the micro-controller or from the reference sinusoid signals available from the CCI control board. The PID controller then acts to maintain slip speed (and hence torque) constant at that ($\omega_s$) demanded by the accelerator pedal, regardless of the acceleration rate of the vehicle.
Chapter Seven: Future Work.

Provided all signals used in the loop are scaled correctly such that the maximum value of $\omega_s$ corresponds to the value of $\omega_s$ at the motor's maximum slip speed, then entry into the unstable region should be avoided at all times.

At higher motor speeds, the torque-slip relationship loses its linearity and such a control system may fail. To avoid this, the microcontroller can be programmed to place a maximum on the rate of change in the fundamental frequency once voltage saturation is reached. Since this frequency is dependent on bus voltage, it could be sensed and used to dynamically set the changeover frequency to take advantage of the greater high speed torque available from a fully charged battery bus.

The closed loop system affords regenerative braking, whereby to decelerate the car, the induction motors are run as generators by making slip negative (that is by making the fundamental component of frequency less than that corresponding to the instantaneous rotor speed). During regeneration, some of the kinetic energy possessed by the moving car is returned via the motors and inverter's bypass diodes to the batteries and a braking force on the rear wheels results.

Regeneration is incorporated by using a second potentiometer placed on the brake pedal to provide a retarding torque demand ($\omega_b$) in a similar fashion to that used for the accelerator. Since the two pedals will not, under usual driving conditions, be depressed simultaneously it is possible to simply sum their signals as shown in figure 7.1. The brake pedal signal is configured such that target frequency is inversely proportional to the depression angle. Slip speed remains proportional to depression angle as before, hence depressing the brake specifies both a (retarding) torque and a (lowered) target frequency.

An alternative control system would be to use the fundamental component of AC current as the feedback variable (taken as the reference sinusoid from the CCI control circuits) as this retains a higher degree of linearity (with respect to torque) at all frequencies. However, maximum motor current would have to be indexed to fundamental frequency, decreases progressively (as does torque) following the onset of voltage saturation. Again, maximum current is influenced by bus voltage, hence the incorporation of bus voltage sensing would enhance performance.
CHAPTER EIGHT:
CONCLUSION

The University of Canterbury Mark II EV has been out of service for an extended period due to the lack of a functional inverter to supply its three phase motors with variable frequency AC.

This project has addressed this by designing and constructing a suitable inverter based on an existing motor speed controller produced by GEC NZ Ltd. This inverter differs from conventional sinusoidal pulse width modulation (SPWM), motor speed control inverters in that it acts to directly control and shape load current rather than voltage. Inherent to this control strategy is the asynchronous switching of the power devices in the three phase bridge.

The principal modification made to GEC's equipment was to increase its output current capability to suit the car's low voltage motors. The six original 50A bipolar junction monolithic Darlington transistors (MDs) in the inverter's three phase bridge were replaced with 300A devices. This in turn required modifications to the control circuits responsible for the efficient switching of the new high current devices. Switching frequency was lowered by a factor of approximately three to avoid excessive switching losses, and new base drive circuits were developed to supply the larger base currents required to switch the larger MDs. These new base drive circuits were subsequently demonstrated to be capable of allowing the MDs to switch up to 200A from a 240V DC supply, equal to the peak sinusoidal currents drawn by the car's motors. Examination of the MD switching waveforms showed these to be similar to those considered 'ideal'.

All the power and control circuits were able to be accommodated within an already existing inverter enclosure, designed to be mounted between the motors in the rear of the car. Care was taken to ensure that all cables and bus bars were more than rated to conduct the maximum operational inverter currents.

Source inductance was identified as a possible cause of MD failure due to the induction of a significant over-voltage across the MD during turn off. This was countered to a sufficient extent by means of snubbers. After experimentation with differing snubber configurations, bus snubbers (able to protect both transistors in each phase of the three phase bridge) were found to give reliable, energy efficient performance.
Chapter Eight: Conclusion

A cause of MD failure was traced to transients in the base-emitter potentials under conditions of reverse bias. MDs can tolerate only small reverse bias potentials, and this was found to be exceeded during the turn on of the bypass diodes. Until the onset of conductivity modulation these diodes suffer from an excessive forward bias volt-drop. Intrinsic, parasitic capacitance between the base and collector of each MD was thought to provide a path for transients to be coupled from the collector-emitter to base-emitter junctions and so interfere with the base drive waveforms. The use of low impedance capacitors and transient suppressors was found to reduce the transients to safe levels, but not completely eliminate them.

With the inverter subsequently capable of supplying up to 130A (RMS) output current, emphasis was placed on load testing the motor inverter system. Trends in slip, output current, motor efficiency, power factor and inverter efficiency were established and presented graphically with respect to the independent variable, motor torque. In order to provide a basis for comparison, the motors were also tested using a 50Hz AC mains supply, free of the harmonics found in the inverters outputs.

In general the performance of the inverter was found to be poor at low fundamental frequencies, due in part to the high levels of harmonics observed in both output voltage and waveforms, and to the inherent operating characteristics of the induction motors themselves. It was also found that at low speeds ineffective cooling from the motor’s shaft mounted fans, coupled with a poor efficiency, precluded higher torques from being obtained for more than a very short interval.

However, all performance figures improved substantially with increasing frequency. Maximum recorded motor efficiency and power factor were found similar to those recorded for operation from a sinusoidal supply. This combined with a peak inverter efficiency exceeding 95% for the same fundamental frequency range suggested that the drive system could be expected to deliver an overall efficiency (from battery to motor shaft) approaching 80%. Further these fundamental frequencies were noted coincide with vehicle speeds typical of urban driving, hence optimum efficiency can be expected to be realised during the course of normal urban driving.

This work concluded by noting the importance of a satisfactory closed loop speed control system both intended to emulate the response of a conventional ICV and avoid the possibility of loss of motor torque during acceleration.
Chapter Eight: Conclusion

Overall this project has realised an inverter capable of both providing a sufficiently large enough current to exploit the peak torque rating of the cars induction motors, and permitting motor operation at at least rated torque for fundamental frequencies of up to 150Hz. While this will not give the vehicle the acceleration performance of most conventional cars, it has been shown in the past to give acceptable performance in urban driving conditions, based on the experience gained with the original thyristor inverter.
REFERENCES


BRUSH, "Type 'T' Fast Acting Fuselinks Product Guide", Brush Fusegear Ltd.


References


REFERENCES


APPENDIX ONE:
DATA FOR SELECTED COMPONENTS
Ratings and Characteristics of Fuji Power Transistor

1D1300Z-120 (TENTATIVE)

1. Outline Drawing

Unit:mm

*Isolation Voltage: AC 2500 V 1 minute

Mounting hole

4-#6.5-0.1

2. Equivalent Circuit

3. Absolute Maximum Ratings (TC=25°C)

<table>
<thead>
<tr>
<th>Item</th>
<th>Symbol</th>
<th>Maximum Ratings</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Collector-Base Voltage</td>
<td>VCEO</td>
<td>1200</td>
<td>V</td>
</tr>
<tr>
<td>Collector-Emitter Voltage</td>
<td>VCEO</td>
<td>1200</td>
<td>V</td>
</tr>
<tr>
<td>Emitter-Base Voltage</td>
<td>VCEO</td>
<td>10</td>
<td>V</td>
</tr>
<tr>
<td>Collector Current</td>
<td>IC</td>
<td>300</td>
<td>A</td>
</tr>
<tr>
<td>DC</td>
<td>ICP</td>
<td>600</td>
<td>A</td>
</tr>
<tr>
<td>E</td>
<td>DC</td>
<td>300</td>
<td>A</td>
</tr>
<tr>
<td>Base Current</td>
<td>IB</td>
<td>16</td>
<td>A</td>
</tr>
<tr>
<td>DC</td>
<td>IBP</td>
<td>32</td>
<td>A</td>
</tr>
<tr>
<td>Collector Power Dissipation</td>
<td>One Transistor</td>
<td>PC</td>
<td>2000</td>
</tr>
<tr>
<td>Operating Temperature</td>
<td>Tj</td>
<td>+150</td>
<td>°C</td>
</tr>
<tr>
<td>Storage Temperature</td>
<td>Tstg</td>
<td>-40 to +125</td>
<td>°C</td>
</tr>
<tr>
<td>Screw Torque</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Mounting #1</td>
<td>M1</td>
<td>17</td>
<td>kg·cm</td>
</tr>
<tr>
<td>Terminals #2</td>
<td>M6</td>
<td>4.5</td>
<td>kg·cm</td>
</tr>
</tbody>
</table>

Isolation Voltage | AC 2500 V |

Note:

*1 Recomendable Value: 25 to 35 kg·cm (M5 or M6)

*2 Recomendable Value: 13 to 17 kg·cm (M4)

35 to 45 kg·cm (M6)
### 4. Electrical Characteristics (Tj = 25°C unless otherwise specified)

<table>
<thead>
<tr>
<th>Characteristics</th>
<th>Symbol</th>
<th>Conditions</th>
<th>MIN</th>
<th>MAX</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Collector-Emitter Voltage</td>
<td>VCEO</td>
<td>IC = 4mA</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Collector-Emitter Voltage</td>
<td>VCEO</td>
<td>IC = 4mA</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Collector-Emitter Voltage</td>
<td>VCEO</td>
<td>IC = 4mA</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Collector-Emitter Voltage</td>
<td>VCEO</td>
<td>IC = 4mA</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Collector-Cutoff Current</td>
<td>ICEO</td>
<td>VCEO = 1200V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Collector-Cutoff Current</td>
<td>ICEO</td>
<td>VCEO = 1200V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>DC Current Gain</td>
<td>hFE</td>
<td>IC = 300A, VCE = 2.8V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>DC Current Gain</td>
<td>hFE</td>
<td>IC = 300A, VCE = 5V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Collector Saturation Voltage</td>
<td>VCE(sat)</td>
<td>IC = 300A</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Collector Saturation Voltage</td>
<td>VCE(sat)</td>
<td>IC = 300A</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Base Saturation Voltage</td>
<td>VBE(sat)</td>
<td>IB = 4.0A</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Switching Time</td>
<td>tON</td>
<td>IC = 300A</td>
<td></td>
<td>3.0</td>
<td>μs</td>
</tr>
<tr>
<td>Switching Time</td>
<td>tOFF</td>
<td>IC = 300A</td>
<td></td>
<td>15.0</td>
<td>μs</td>
</tr>
<tr>
<td>Switching Time</td>
<td>tRC</td>
<td>IC = 300A</td>
<td></td>
<td>2.0</td>
<td>μs</td>
</tr>
<tr>
<td>Emitter-Collector Voltage</td>
<td>VCEO</td>
<td>ICEO = 300A</td>
<td></td>
<td>2.0</td>
<td>V</td>
</tr>
<tr>
<td>Reverse Recovery Time</td>
<td>tRR</td>
<td>ICEO = 300A</td>
<td></td>
<td>0.8</td>
<td>μs</td>
</tr>
<tr>
<td>Short Circuit Capability</td>
<td>#3 Ed</td>
<td>IB1 = 4.0A, IB2 = 0.1A</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>#3 Ed</td>
<td>IB1 = 4.0A, IB2 = 0.1A</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### 5. Thermal Characteristics

<table>
<thead>
<tr>
<th>Characteristics</th>
<th>Symbol</th>
<th>Conditions</th>
<th>MIN</th>
<th>MAX</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thermal Resistance</td>
<td>Rth(c-c)</td>
<td>Power Transistor</td>
<td></td>
<td>0.063</td>
<td>°C/W</td>
</tr>
<tr>
<td></td>
<td>Rth(c-c)</td>
<td>Fast Recovery Diode</td>
<td></td>
<td>0.20</td>
<td>°C/W</td>
</tr>
<tr>
<td>Contact Thermal Resistance</td>
<td>Rth(c-c)</td>
<td>Mounting torque 35kg·cm</td>
<td>(TYP)</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Rth(c-c)</td>
<td>Mounting torque 35kg·cm with thermal compound</td>
<td>0.03</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### #3 Test Circuit

- **Base Current (Single Pole)**
  - Collector: ≤ 10 mA
  - Emitter: ≤ 10 mA

---

**DATE** | **NAME** | **APPROVED**
---|---|---
MS | M 1 | M 1 1 1 6
**Definition**

The "LEM Module LA 100-S/SP1" is a current sensor for the electronic measurement of currents: DC, AC, IMPL, etc., with galvanic isolation between the primary (high current) and the secondary (electronic) circuits.

**Electrical data**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Nominal current $I_N$</td>
<td>$100 , \text{A rms.}$</td>
</tr>
<tr>
<td>Measuring range</td>
<td>$0 \text{ to } +/1200 , \text{A}$</td>
</tr>
<tr>
<td>Measuring resistance</td>
<td>$R_M , \text{min.}$</td>
</tr>
<tr>
<td>with $+/-15 , \text{V}$</td>
<td>$0 , \text{ohm}$</td>
</tr>
<tr>
<td>at $+/-100 , \text{A max.}$</td>
<td>$150 , \text{ohm}$</td>
</tr>
<tr>
<td>at $+/-200 , \text{A max.}$</td>
<td>$50 , \text{ohm}$</td>
</tr>
<tr>
<td>Nominal analog output current</td>
<td>$50 , \text{mA}$</td>
</tr>
<tr>
<td>Turns ratio</td>
<td>$1 : 2000$</td>
</tr>
<tr>
<td>Overall accuracy at $+25^\circ \text{C}$</td>
<td>$+/-0.5 % , \text{of } I_N$</td>
</tr>
<tr>
<td>Supply voltage</td>
<td>$+/-15 , \text{V} , (+/-5%)$</td>
</tr>
<tr>
<td>Dielectric Strength</td>
<td>$3 , \text{kV rms/50 Hz/1 min.}$</td>
</tr>
</tbody>
</table>

**Accuracy - Dynamic performances**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Offset current for zero primary current at $25^\circ \text{C}$</td>
<td>max. $+/-0.1 , \text{mA}$</td>
</tr>
<tr>
<td>Drift with temperature of offset current (between $-10^\circ \text{C}$ and $+70^\circ \text{C}$)</td>
<td>typical $+/-0.2 , \text{mA}$</td>
</tr>
<tr>
<td>Linearity</td>
<td>max. $+/-0.4 , \text{mA}$</td>
</tr>
<tr>
<td>Delay time</td>
<td>better than $0.1 %$</td>
</tr>
<tr>
<td>di/dt accurately followed</td>
<td>better than $1 , \text{ps}$</td>
</tr>
<tr>
<td>Bandwidth</td>
<td>better than $50 , \text{A/µs}$</td>
</tr>
<tr>
<td></td>
<td>$0 \text{ to } 150 , \text{kHz} (-1\mathrm{dB})$</td>
</tr>
</tbody>
</table>

**General data**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operating temperature</td>
<td>$-10^\circ \text{C}$ to $+70^\circ \text{C}$</td>
</tr>
<tr>
<td>Storage temperature</td>
<td>$-25^\circ \text{C}$ to $+85^\circ \text{C}$</td>
</tr>
<tr>
<td>Current drain</td>
<td>$22 , \text{mA} + 1 , \text{output current}$</td>
</tr>
<tr>
<td>Secondary internal resistance</td>
<td>$85 , \text{ohm (at } +70^\circ \text{C})$</td>
</tr>
<tr>
<td>Package</td>
<td>moulded into an insulated self-extinguishing plastic case</td>
</tr>
<tr>
<td>Weight</td>
<td>$65 , \text{g.}$</td>
</tr>
<tr>
<td>Fastening</td>
<td>by 2 holes $3.2 , \text{mm dia. between centers} 46 \times 8 , \text{mm}$</td>
</tr>
<tr>
<td>Connection to primary circuit</td>
<td>through-hole $15 \times 10 , \text{mm}$</td>
</tr>
<tr>
<td>secondary circuit</td>
<td>on Molex connector 5045-04 AG straight pin friction lock header</td>
</tr>
<tr>
<td>Signal sense</td>
<td>a positive measuring current is obtained on terminal M, when the primary current flows in the direction of the arrow.</td>
</tr>
</tbody>
</table>

**Particularity**

<table>
<thead>
<tr>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>turns ratio $1 : 2000$</td>
</tr>
</tbody>
</table>

**Note**: The temperature of the primary conductor should not exceed $100^\circ \text{C}$.

910125/1
N-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in TO-92 variant envelope and intended for use in relay, high-speed and line-transformer drivers.

Features
- Low $R_{DSon}$
- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown

QUICK REFERENCE DATA

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drain-source voltage</td>
<td>$V_{DS}$ max.</td>
<td>80 V</td>
</tr>
<tr>
<td>Gate-source voltage (open drain)</td>
<td>$V_{GS0}$</td>
<td>20 V</td>
</tr>
<tr>
<td>Drain current (DC)</td>
<td>$I_{D}$ max.</td>
<td>0.5 A</td>
</tr>
<tr>
<td>Total power dissipation up to $T_{amb} = 25 , ^{\circ}C$</td>
<td>$P_{tot}$ max.</td>
<td>1 W</td>
</tr>
<tr>
<td>Drain-source ON-resistance</td>
<td>$R_{DSon}$ typ.</td>
<td>2 $\Omega$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>max. 4 $\Omega$</td>
</tr>
<tr>
<td>Transfer admittance</td>
<td>$</td>
<td>V_{fs}</td>
</tr>
<tr>
<td>$I_{D} = 500$ mA; $V_{DS} = 15$ V</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

MECHANICAL DATA

Fig. 1 TO-92 variant.

Pinning:
1 = source
2 = gate
3 = drain

Dimensions in mm

Note: Various pinout configurations available.
**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC134)

<table>
<thead>
<tr>
<th>Voltages*</th>
<th>BYX25–600(R)</th>
<th>800(R)</th>
<th>1000(R)</th>
<th>1200(R)</th>
<th>1400(R)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Crest working reverse voltage $V_{RWM}$ max.</td>
<td>600</td>
<td>800</td>
<td>1000</td>
<td>1200</td>
<td>1400</td>
</tr>
<tr>
<td>Continuous reverse voltage $V_{R}$ max.</td>
<td>600</td>
<td>800</td>
<td>1000</td>
<td>1200</td>
<td>1400</td>
</tr>
</tbody>
</table>

**Currents**

- Average forward current (averaged over any 20 ms period) up to $T_{mb} = 125 \, ^{\circ}C$
  \[ I_{F(AV)} \text{ max.} = 20 \, A \]
- Repetitive peak forward current
  \[ I_{FRM} \text{ max.} = 440 \, A \]
- Non-repetitive peak forward current
  - $t = 10 \, ms$ (half sine-wave); $T_j = 175 \, ^{\circ}C$ prior to surge;
  - with reapply $V_{RWM_{\text{max}}}$
  \[ I_{FSM} \text{ max.} = 360 \, A \]
  \[ I^2 t \text{ max.} = 650 \, A^2 s \]

**Reverse power dissipation**

- Average reverse power dissipation (averaged over any 20 ms period); $T_j = 175 \, ^{\circ}C$
  \[ P_{R(AV)} \text{ max.} = 38 \, W \]
- Repetitive peak reverse power dissipation
  - $t = 10 \, \mu s$ (square-wave; $f = 50 \, Hz$); $T_j = 175 \, ^{\circ}C$
  \[ P_{RRM} \text{ max.} = 3 \, kW \]
- Non-repetitive peak reverse power dissipation
  - $t = 10 \, \mu s$ (square-wave)
  - $T_j = 25 \, ^{\circ}C$ prior to surge
  - $T_j = 175 \, ^{\circ}C$ prior to surge
  \[ P_{RSM} \text{ max.} = 18 \, kW \]
  \[ P_{RSM} \text{ max.} = 3 \, kW \]

**Temperatures**

- Storage temperature
  \[ T_{stg} = -55 \text{ to } +175 \, ^{\circ}C \]
- Junction temperature
  \[ T_j \text{ max.} = 175 \, ^{\circ}C \]

*To ensure thermal stability: $R_{th j-a} < 5 \, K/W \ (a.c.)$
RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC134)

<table>
<thead>
<tr>
<th>Volatges</th>
<th>BYX30-200(R)</th>
<th>300(R)</th>
<th>400(R)</th>
<th>500(R)</th>
<th>600(R)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Crest working reverse voltage</td>
<td>$V_{RWM}$ max. 200</td>
<td>300</td>
<td>400</td>
<td>500</td>
<td>600</td>
</tr>
<tr>
<td>Continuous reverse voltage</td>
<td>$V_{R}$ max. 200</td>
<td>300</td>
<td>400</td>
<td>500</td>
<td>600</td>
</tr>
</tbody>
</table>

Currents

Average forward current (averaged over any 20 ms period) up to $T_{mb} = 100 \, ^{\circ}C$

at $T_{mb} = 125 \, ^{\circ}C$

$I_{F(AV)}$ max. 14 A

$I_{F(AV)}$ max. 7.5 A

R.M.S. forward current

$I_{F(RMS)}$ max. 22 A

Repetitive peak forward current

$I_{FRM}$ max. 310 A

Non-repetitive peak forward current

$t = 10 \, ms$; half-sine wave; $T_{j} = 150 \, ^{\circ}C$ prior to surge;

with reapplied $V_{RWM}$ max.

$I_{FSM}$ max. 250 A

$I_{t^2}$ max. 312 $A^2s$

Reverse power dissipation

Repetitive peak reverse power dissipation

$t = 10 \, \mu s$ (square wave; $f = 50 \, Hz$) $T_{j} = 150 \, ^{\circ}C$

$P_{RRM}$ max. 5.5 kW

Non-repetitive peak reverse power dissipation

$t = 10 \, \mu s$ (square wave) $T_{j} = 25 \, ^{\circ}C$ prior to surge

$T_{j} = 150 \, ^{\circ}C$ prior to surge

$P_{RSM}$ max. 18 kW

$P_{RSM}$ max. 5.5 kW

Temperatures

Storage temperature

$T_{stg}$ -55 to +150 $^{\circ}C$

Junction temperature

$T_{j}$ max. 150 $^{\circ}C$

THERMAL RESISTANCE

From junction to ambient in free air

$R_{th \, j-a} = 50 \, ^{\circ}C/W$

From junction to mounting base

$R_{th \, j-mb} = 1.3 \, ^{\circ}C/W$

From mounting base to heatsink

$R_{th \, mb-h} = 0.5 \, ^{\circ}C/W$

1) To ensure thermal stability: $R_{th \, j-a} < 2.5 \, ^{\circ}C/W$ (continuous reverse voltage) or $< 5 \, ^{\circ}C/W$ (a.c.).

For smaller heatsinks $T_{j}$ max should be derated. For a.c. see page 5.

For continuous reverse voltage: if $R_{th \, j-a} = 5 \, ^{\circ}C/W$, then $T_{j}$ max $= 135 \, ^{\circ}C$.

if $R_{th \, j-a} = 10 \, ^{\circ}C/W$, then $T_{j}$ max $= 120 \, ^{\circ}C$. 

600 March 1978
### MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Rating</th>
<th>Symbol</th>
<th>BC327</th>
<th>BC328</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Collector-Emitter Voltage</td>
<td>$V_{CEO}$</td>
<td>45</td>
<td>25</td>
<td>Vdc</td>
</tr>
<tr>
<td>Collector-Base Voltage</td>
<td>$V_{CBO}$</td>
<td>50</td>
<td>30</td>
<td>Vdc</td>
</tr>
<tr>
<td>Emitter-Base Voltage</td>
<td>$V_{EOB}$</td>
<td>5.0</td>
<td></td>
<td>Vdc</td>
</tr>
<tr>
<td>Collector Current — Continuous</td>
<td>$I_C$</td>
<td>800</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>Total Device Dissipation at $T_A = 25^\circ$C</td>
<td>$P_D$</td>
<td>675</td>
<td>5.0</td>
<td>mW</td>
</tr>
<tr>
<td>Derate above 25°C</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Total Device Dissipation at $T_C = 25^\circ$C</td>
<td>$P_D$</td>
<td>1.5</td>
<td>12</td>
<td>W</td>
</tr>
<tr>
<td>Derate above 25°C</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Operating and Storage Junction Temperature Range</td>
<td>$T_J$, $T_{stg}$</td>
<td>-55 to +150</td>
<td></td>
<td>$^\circ$C</td>
</tr>
</tbody>
</table>

### THERMAL CHARACTERISTICS

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Symbol</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thermal Resistance, Junction to Case</td>
<td>$R_{JEC}$</td>
<td>63.3</td>
<td>$^\circ$C/W</td>
</tr>
<tr>
<td>Thermal Resistance, Junction to Ambient</td>
<td>$R_{JEC}$</td>
<td>200</td>
<td>$^\circ$C/W</td>
</tr>
</tbody>
</table>

### ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ$C unless otherwise noted)

#### OFF CHARACTERISTICS

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Collector-Emitter Breakdown Voltage (&lt;IC = 0 mA, IG = 0)</td>
<td>$V_{BRICEO}$</td>
<td>45</td>
<td>25</td>
<td></td>
<td>Vdc</td>
</tr>
<tr>
<td>Collector-Emitter Breakdown Voltage (&lt;IC = 100 mA, IG = 0)</td>
<td>$V_{BRICES}$</td>
<td>50</td>
<td>30</td>
<td></td>
<td>Vdc</td>
</tr>
<tr>
<td>Emitter-Base Breakdown Voltage (&lt;IE = 10 uA, IC = 0)</td>
<td>$V_{BRIEBO}$</td>
<td>5.0</td>
<td></td>
<td></td>
<td>Vdc</td>
</tr>
<tr>
<td>Collector Cutoff Current (&lt;VC = 30 V, IC = 0)</td>
<td>$I_{CB}$</td>
<td></td>
<td>100</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>Collector Cutoff Current (&lt;VC = 45 V, IC = 0)</td>
<td>$I_{CES}$</td>
<td></td>
<td>100</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>Emitter Cutoff Current (&lt;VC = 4.0 V, IC = 0)</td>
<td>$I_{EOB}$</td>
<td></td>
<td>100</td>
<td></td>
<td>mA</td>
</tr>
</tbody>
</table>

#### ON CHARACTERISTICS

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC Current Gain (&lt;IC = 100 mA, $V_{CE} = 1.0$ V)</td>
<td>$h_{FE}$</td>
<td>100</td>
<td></td>
<td>630</td>
<td></td>
</tr>
<tr>
<td>Collector-Base On Voltage (&lt;IC = 300 mA, $V_{CE} = 1.0$ V)</td>
<td>$V_{BE(on)}$</td>
<td></td>
<td>1.2</td>
<td></td>
<td>Vdc</td>
</tr>
<tr>
<td>Collector-Emitter Saturation Voltage (&lt;IC = 500 mA, $I_B = 50$ mA)</td>
<td>$V_{CE(sat)}$</td>
<td></td>
<td>0.7</td>
<td></td>
<td>Vdc</td>
</tr>
</tbody>
</table>

### SMALL-SIGNAL CHARACTERISTICS

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output Capacitance (&lt;VCB = 10 V, IF = 0, f = 1.0 MHz)</td>
<td>$C_{OB}$</td>
<td>15</td>
<td></td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>Current-Gain Bandwidth Product (&lt;IC = 10 mA, $V_{CE} = 5.0$ V)</td>
<td>$f_t$</td>
<td>260</td>
<td></td>
<td></td>
<td>MHz</td>
</tr>
</tbody>
</table>

---

MOTOROLA SMALL-SIGNAL SEMICONDUCTORS

2-92
### MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Rating</th>
<th>Symbol</th>
<th>BC337</th>
<th>BC338</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Collector-Emitter Voltage</td>
<td>VCEO</td>
<td>45</td>
<td>25</td>
<td>Vdc</td>
</tr>
<tr>
<td>Collector-Base Voltage</td>
<td>VCB</td>
<td>50</td>
<td>30</td>
<td>Vdc</td>
</tr>
<tr>
<td>Emitter-Base Voltage</td>
<td>VEBO</td>
<td>5.0</td>
<td></td>
<td>Vdc</td>
</tr>
<tr>
<td>Collector Current — Continuous</td>
<td>IC</td>
<td>800</td>
<td></td>
<td>mA, A</td>
</tr>
<tr>
<td>Total Device Dissipation in TA = 25°C</td>
<td>PD</td>
<td>625</td>
<td>5.0</td>
<td>mW, W</td>
</tr>
<tr>
<td>Derate above 25°C</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PD</td>
<td></td>
<td>1.5</td>
<td>1.5</td>
<td>W, W/°C</td>
</tr>
<tr>
<td>Operating and Storage Junction</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Temperature Range</td>
<td>TJ, TSS</td>
<td>-55 to +150</td>
<td></td>
<td>°C</td>
</tr>
</tbody>
</table>

### THERMAL CHARACTERISTICS

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Symbol</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thermal Resistance, Junction to Case</td>
<td>RθJC</td>
<td>83.3</td>
<td>°C/W</td>
</tr>
<tr>
<td>Thermal Resistance, Junction to Ambient</td>
<td>RθJC</td>
<td>200</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

### ELECTRICAL CHARACTERISTICS (TA = 25°C unless otherwise noted.)

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Collector Emitter Breakdown Voltage</td>
<td>VIBRCEO</td>
<td>BC337</td>
<td>45</td>
<td></td>
<td>Vac</td>
</tr>
<tr>
<td>(IC = 10 mA, IC = 0)</td>
<td></td>
<td>BC338</td>
<td>25</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Collector-Emitter Breakdown Voltage</td>
<td>VIBRICES</td>
<td>BC337</td>
<td>50</td>
<td></td>
<td>Vac</td>
</tr>
<tr>
<td>(IC = 100 mA, IC = 0)</td>
<td></td>
<td>BC338</td>
<td>30</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Emitter Base Breakdown Voltage</td>
<td>VIBRIEB</td>
<td>BC337</td>
<td>5.0</td>
<td></td>
<td>Vac</td>
</tr>
<tr>
<td>(IB = 10 µA, IC = 0)</td>
<td></td>
<td>BC338</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Collector Cutoff Current</td>
<td>ICBO</td>
<td>BC337</td>
<td></td>
<td>100</td>
<td>µA</td>
</tr>
<tr>
<td>(VCE = 30 V, IC = 0)</td>
<td></td>
<td>BC338</td>
<td></td>
<td>100</td>
<td></td>
</tr>
<tr>
<td>Collector Cutoff Current</td>
<td>ICES</td>
<td>BC337</td>
<td>100</td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>(VCE = 45 V, VBE = 0)</td>
<td></td>
<td>BC338</td>
<td>100</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Emitter Cutoff Current</td>
<td>IEBE</td>
<td>BC337</td>
<td>100</td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>(VCE = 4.0 V, IC = 0)</td>
<td></td>
<td>BC338</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### ON CHARACTERISTICS

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC Current Gain</td>
<td>hFE</td>
<td>BC337-BC338</td>
<td>100</td>
<td></td>
<td>—</td>
</tr>
<tr>
<td>(IC = 100 mA, VCE = 1.0 V)</td>
<td></td>
<td>BC337-16/BC338-16</td>
<td>100</td>
<td></td>
<td>—</td>
</tr>
<tr>
<td>BC = 300 mA, VCE = 1.0 V)</td>
<td></td>
<td>BC337-26/BC338-25</td>
<td>100</td>
<td></td>
<td>—</td>
</tr>
<tr>
<td>BC = 300 mA, VCE = 1.0 V)</td>
<td></td>
<td>BC337-40/BC338-40</td>
<td>100</td>
<td></td>
<td>—</td>
</tr>
<tr>
<td>Base-Emitter On Voltage</td>
<td>VBE(on)</td>
<td>BC337-BC338</td>
<td>1.2</td>
<td></td>
<td>Vdc</td>
</tr>
<tr>
<td>Collector-Emitter Saturation Voltage</td>
<td>VCE(sat)</td>
<td>BC337-BC338</td>
<td>6.7</td>
<td></td>
<td>Vcc</td>
</tr>
</tbody>
</table>

### SMALL-SIGNAL CHARACTERISTICS

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output Capacitance</td>
<td>CBBP</td>
<td></td>
<td>15</td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>(VCB = 10 V, IC = 0, f = 1.0 MHz)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Current-Gain Bandwidth Product</td>
<td>fT</td>
<td></td>
<td>210</td>
<td></td>
<td>MHz</td>
</tr>
</tbody>
</table>
COMPLEMENTARY SILICON POWER TRANSISTORS

- designed for general-purpose switching and amplifier applications.
- DC Current Gain — hFE = 20-70 @ IC = 4.0 Adc
- Collector-Emitter Saturation Voltage — VCE(sat) = 1.1 Vdc (Max) @ IC = 4.0 Adc
- Excellent Safe Operating Area

MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Rating</th>
<th>Symbol</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Collector-Emitter Voltage</td>
<td>VCEO</td>
<td>60</td>
<td>Vdc</td>
</tr>
<tr>
<td>Collector-Emitter Voltage</td>
<td>VZER</td>
<td>70</td>
<td>Vdc</td>
</tr>
<tr>
<td>Collector-Base Voltage</td>
<td>VCB</td>
<td>100</td>
<td>Vdc</td>
</tr>
<tr>
<td>Emitter-Base Voltage</td>
<td>VEB</td>
<td>7.0</td>
<td>Vdc</td>
</tr>
<tr>
<td>Collector Current — Continuous</td>
<td>IC</td>
<td>15</td>
<td>Adc</td>
</tr>
<tr>
<td>Base Current</td>
<td>IB</td>
<td>7.0</td>
<td>Adc</td>
</tr>
<tr>
<td>Total Power Dissipation @ TC = 25°C</td>
<td>PD</td>
<td>90</td>
<td>Watts</td>
</tr>
<tr>
<td>Derate above 25°C</td>
<td></td>
<td>0.72</td>
<td>W/°C</td>
</tr>
<tr>
<td>Operating and Storage Junction Temperature Range</td>
<td>TJ,TSTG</td>
<td>-65 to +150</td>
<td>°C</td>
</tr>
</tbody>
</table>

THERMAL CHARACTERISTICS

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Symbol</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thermal Resistance, Junction to Case</td>
<td>RJak</td>
<td>1.39</td>
<td>°C/W</td>
</tr>
<tr>
<td>Thermal Resistance, Junction to Ambient</td>
<td>RJAa</td>
<td>35.7</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

FIGURE 1 — DC CURRENT GAIN

- hFE_C = 4.4 V
- TJ = 25°C
Figure A2.1 Control circuit top overlay.
Figure A2.2 Control circuit top layer.
Figure A2.3 Control circuit bottom layer.
Figure A2.4 Base drive circuit top overlay.
Figure A2.5 Base drive circuit top layer.
Figure A2.6 Base drive circuit bottom layer
APPENDIX THREE:
THE CIRCLE DIAGRAM

The circle diagram (CD) is based on the approximate equivalent circuit of an induction motor (figure A3.1). This differs from the diagrams presented in Chapters Two and Five in that the magnetising impedance is shifted to the supply side of the stator leakage impedance. Current through the magnetising impedance and hence air gap flux is thus constant.

![Diagram of Circle Diagram](image)

Figure A3.1 Constant flux equivalent circuit model for the Circle Diagram.

Data for the circle diagram is obtained from the open circuit and locked rotor tests that were described in Chapter Five. From equation 5-3 (repeated here for convenience as equation A3-1) it can be shown [Open Polytechnic, 1992] that as slip is varied, the locus of a vector representation of \( I_2 \) is a semi-circle with a diameter equal to that value of \( I_2 \) when \( R_2 \) is zero, and this forms the basis of the diagram. Further this semi-circle is offset from the origin by the vector co-ordinates representing the motor’s no load current. All quantities are normalised by dividing by root three times the nominal line-line voltage, before being plotted on the diagram.

\[
I_2 = \frac{E_2}{\sqrt{\left(\frac{R_2}{s}\right)^2 + X_2^2}} \tag{A3-1}
\]
Figure A3.2 shows the CD prepared for one of the car's induction motors. The axis OV represents the line-line potential, and OI the line current. All voltage and current displacement angles are plotted relative to the voltage axis OV. Construction of the diagram begins by plotting both the no load (OA) and locked rotor (OB) current vectors (both taken at the rated 90V line-line motor voltage). These vectors make the angles $\theta_m$ and $\theta_r$ to the OV axis where each is the respective no load and locked rotor power factor angles recorded experimentally. Since both OA and OB lie on the current locus semi-circle, by constructing the mediator to the line AB the circumcenter of the diagram may be located.

Any line drawn parallel to OV represents a component of current in phase with voltage, and hence is proportional to power. The circle diagram makes the assumption that the sum of magnetising losses and friction/windage is constant regardless of load. This is represented by the constant loss line AP. A line drawn from any point on the circumference of the diagram to this constant loss line represents the balance of the total power drawn from the supply and is the sum of; the developed mechanical output power, stator copper losses (SCL) and rotor copper losses (RCL).

When the rotor is locked and mechanical power is zero, then this line represents only the sum of stator and rotor copper losses and is shown on the diagram as the line BE. If the stator resistance is measured, then the stator copper losses (SCL) can be calculated (for a locked rotor) and marked off on BE to form DF. The remaining segment BF is thus rotor copper loss (RCL). Lines extended from A to B and A to F subsequently allow the RCL and SCL can be measured for any given value of $I_2$. For example at the point G:

\[
\sqrt{3}V \cdot GM = \text{Total Input Power} \tag{A3-2} \\
\sqrt{3}V \cdot KL = \text{Stator Copper Losses (SCL)} \tag{A3-3} \\
\sqrt{3}V \cdot HK = \text{Rotor Copper Losses (RCL)} \tag{A3-4} \\
\sqrt{3}V \cdot GK = \text{Rotor Input Power} \tag{A3-5} \\
\sqrt{3}V \cdot GH = \text{Mechanical Output Power} \tag{A3-6} \\
\sqrt{3}V \cdot LM = \text{Constant Losses} \tag{A3-7}
\]
Test Results (all for the rated 90V line-line potential)

- Current at No Load = 19.2A
- Current drawn with rotor locked = 138A
- Power drawn on no load = 322W
- Power drawn with rotor locked = 12,656W
- Measured stator resistance = 0.104 ohm

Key (NB magnitudes are normalised by \( \sqrt{3}90 \))

- OA = No load current = 0.096
- OB = Locked rotor current = 0.45
- \( \theta_\infty \) = No load power factor angle = 84°
- \( \theta_L \) = Locked rotor power factor angle = 54°
- DE = No load losses = 2.1
- BF = Stator copper losses = 38.1
- FD = Rotor copper losses = 43

Figure A3.2 Induction Motor Circle Diagram.
Appendix Three: The circle diagram.

At any point on the boundary semicircle, it is possible based on these quantities to calculate motor operating characteristics using the equations listed below:

\[ \frac{GH}{GM} = \text{efficiency} \]  \hspace{1cm} (A3-8)

\[ \frac{HK}{GK} = \frac{\text{rotor loss}}{\text{power transferred stator-rotor}} = \text{slip} \]  \hspace{1cm} (A3-9)

\[ \frac{GM}{\sqrt{3}V \cdot OG} = \text{input power factor} \]  \hspace{1cm} (A3-10)

Maximum output power (which coincides with maximum slip) can be found by locating where GH is at its maximum.
## EXPERIMENTAL RESULTS

### 200V DC BUS

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### 300V DC BUS (similar format)

### SYMBOL KEY

- **f** = fund. frequency
- **Vdc** = DC Bus Potential
- **Idc** = DC Bus Current
- **Vac** = RMS Inverter Output Line-Line Potential
- **Iac** = RMS Inverter RMS Output Line Current
- **Pout** = Inverter Output Power
- **RPM** = Motor Shaft Speed (RPM)
## 200V DC BUS

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**SYMBOL KEY**

f = fund. frequency  
Vdc = DC Bus Potential  
Idc = DC Bus Current  
Vac = RMS Inverter Output Line-Line Potential  
Iac = RMS Inverter RMS Output Line Current  
Pout = Inverter Output Power  
RPM = Motor Shaft Speed (RPM)
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**Symbol Key**
- \( f \) = fundamental frequency
- \( V_{dc} \) = DC Bus Potential
- \( I_{dc} \) = DC Bus Current
- \( V_{ac} \) = RMS Inverter Output Line-Line Potential
- \( I_{ac} \) = RMS Inverter RMS Output Line Current
- \( P_{out} \) = Inverter Output Power
- RPM = Motor Shaft Speed (RPM)
## Appendix four: Experimental Results

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### SYMBOL KEY

- \( f \) = fund. frequency
- \( Vdc \) = DC Bus Potential
- \( Idc \) = DC Bus Current
- \( Vac \) = RMS Inverter Output Line-Line Potential
- \( Iac \) = RMS Inverter RMS Output Line Current
- \( Pout \) = Inverter Output Power
- \( RPM \) = Motor Shaft Speed (RPM)
### 240V DC Bus

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**Symbol Key**

- $f$ = fund. frequency
- $V_{dc}$ = DC Bus Potential
- $I_{dc}$ = DC Bus Current
- $V_{ac}$ = RMS Inverter Output Line-Line Potential
- $I_{ac}$ = RMS Inverter RMS Output Line Current
- $P_{out}$ = Inverter Output Power
- RPM = Motor Shaft Speed (RPM)
## Appendix four: Experimental Results

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<th>Vac (V)</th>
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**SYMBOL KEY**

- f = fund. frequency
- Vdc = DC Bus Potential
- Idc = DC Bus Current
- Vac = RMS Inverter Output Line-Line Potential
- Iac = RMS Inverter RMS Output Line Current
- Pout = Inverter Output Power
- RPM = Motor Shaft Speed (RPM)
### 240V DC Bus

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**Symbol Key**

- $V_{dc}$ = DC Bus Potential
- $I_{dc}$ = DC Bus Current
- $V_{ac}$ = RMS Inverter Output Line-Line Potential
- $I_{ac}$ = RMS Inverter RMS Output Line Current
- $P_{out}$ = Inverter Output Power
- RPM = Motor Shaft Speed (RPM)