Dynamic Frequency Scaling to Improve Converter Efficiency

Robert Turner, Richard Duke, and Simon Walton

***Abstract*--A controller, suitable for medium to high power switching converters (1kW to 1MW), is proposed that dynamically changes the output PWM carrier frequency. The control objective is to optimise the choice of switching frequency so as to maximise overall converter efficiency, while providing a good transient performance. A range of control techniques which can determine when to change the PWM switching frequency are investigated. The practical limitations imposed by conventional PWM controllers and DSPs used in switching converter control are also considered.**

***Index Terms*—PWM, Converter Efficiency, Digital Controller.**

I. Introduction

IN all switching converters the switching frequency used is directly related to the converter efficiency due to switching losses in the converter switches. Inherently for medium to high power converters this becomes a concern as the relative switching losses increase for increasing power devices. Therefore, conventionally in constant switching frequency medium to high power converters, such as power line conditioners, the switching frequency is typically around 10kHz when using IGBTs or lower for thyristor systems [1], [2]. Due to the Nyquist sampling theorem, the maximum bandwidth of the system theoretically attainable is half that of the sampling frequency, while practically this is usually in the order of one tenth of the switching frequency. Therefore converters with low switching frequencies achieve relatively low bandwidths.

To maintain low switching losses when switching medium to high power devices, the switching frequency must maintain a low average frequency. This presents us with the idea that it may be possible for short periods of time to switch at a higher switching frequency. This temporarily achieves a wider bandwidth, suitable for dealing with transients, while maintaining a lower average switching frequency during steady-state conditions. The control scheme presented in this paper involves switching at an integer fraction of the sampling frequency during steady-state, while during transients the switching frequency is increased up to the limit of the sampling frequency to temporarily achieve a wider desired bandwidth. This technique is ideal for power conditioners that run predominantly steady-state loads while experiencing transients, for example when loads are turned on and off.

The Dynamic Frequency Scaling (DFS) technique is an additional control that operates alongside a conventional digital controller. Figure 1 shows the relative difference between a conventional fixed frequency digital controller for a buck regulator (a) and a DFS digital controller for a buck regulator (b). The fixed frequency buck controller comprises of a digital controller driving an LC filter and load. The output voltage is sampled through a Zero Order Hold (ZOH) and is subtracted from the reference voltage (V_{ref}) to give the output error (V_{err}) fed into the controller. The DFS technique replaces the fixed frequency ZOH with a Variable ZOH unit and a Frequency Chooser. The Frequency Chooser monitors the output error (V_{err}) and changes the switching frequency due to the Variable ZOH to produce the desired response. The Variable ZOH has a selectable switching frequency at integer fractions of the maximum switching frequency, implemented using a DSP PWM module.

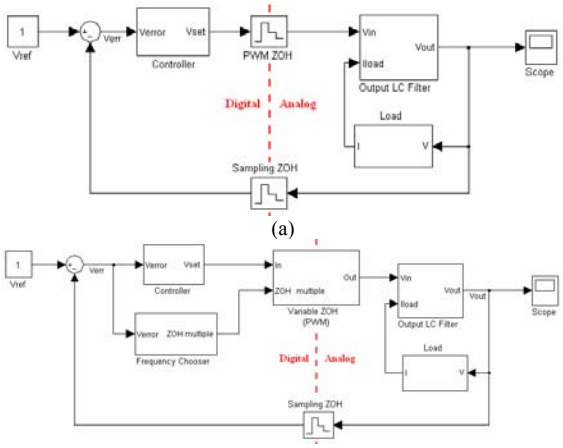

Fig. 1. a) Fixed frequency digital controller, b) dynamic frequency scaling PWM digital controller.

II. Dynamic Frequency Scaling Operation

DFS is primarily intended for medium to high power converters such as active power conditioning, where the efficiency gains are of greatest concern. To demonstrate the DFS technique a buck regulator is used to reduce converter analysis and simulation complexity.

The DFS Frequency Chooser module monitors the output

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error signal (V_{err}) common in all controllers and sets the PWM frequency via the Variable ZOH accordingly. When the output error is large the PWM frequency is increased, reducing the control loop delay. Reducing the closed loop delay increases the phase margin making the system more stable, but does not decrease the loop gain, so the system response is not sacrificed.

By using a fixed range of integer fractions of the sampling frequency for the switching frequencies, DFS can easily be used in high-power synchronised parallel systems. The integer fractions of switching frequencies lend the implementation strongly to existing microcontrollers which usually provide integer ratios for the switching frequency in the PWM modules [3] – [5].

Using integer fractions for the Variable ZOH switching frequencies has several implications. The inherent disadvantage is that it does not provide a smooth transition of the bandwidth when the frequency is changed. The effect of increased error from this can either be determined to be negligible or may be eliminated almost entirely by the use of internal model referencing within the Frequency Chooser (with the added cost of complexity and required computational power).

Increasing the frequency mid period needs to done carefully. If a switching period is not completed, the effective period length is that portion of the period up to when it is changed. For example, if the present output is a 50% duty cycle and the switching frequency is increased in the middle of the present period the inductor flux (current) will build up, but will not have a chance to collapse. Therefore when increasing the switching frequency it may be necessary to have an internal model of the inductor flux to allow the controller to account for a flux offset in the next few cycles. If not spikes on the output may occur due to the flux build-up.

A. Frequency Range Stability

As the DFS technique varies the switching frequency it is a Variable Structure non-linear system. As with all non-linear analysis approaches, the system can be analysed as a set of linear systems over a defined range of inputs [6]. The DFS technique effectively has a different state for each possible switching frequency. So for a system which has three different frequency levels, stability criteria must be analysed for each one. To ensure global stability the system must ensure that only the state (switching frequency) that is stable for a given input is selected. If an input has more than one stable state, the one with lowest switching frequency will be chosen.

The buck regulator with a resistive load and modelled by the system shown in Figure 1a is analysed at three different switching frequencies to determine the system stability for each one. When analysing the stability a proportional controller is used to produce a 2nd order system allowing straightforward analysis. The open loop transfer function for a resistive load and a proportional controller with gain K_p is given as:

$$H(s) = K_p \cdot \frac{1}{LC} \cdot \frac{1}{s^2 + s\frac{R}{C} + \frac{1}{LC}} e^{-sT_s} \qquad (1)$$

The system delay T_s is the sum of all the delays around the system which for a digital controller includes the sampling delay, processing delay and the PWM delay. For the buck regulator analysed here the sampling delay is the same as the maximum switching frequency delay, similar to fixed frequency systems. The example system is analysed with the following component values:

$$L = 100\mu H$$
$$C = 1000\mu F$$
$$R = 1\Omega$$

The proportional gain is set at one. The stability of the system can be shown for different size loads and different switching frequencies using Nyquist diagrams. Figures 2, 3 and 4 show the Nyquist stability where the delay as a result of different switching frequencies shifts the system stability from stable through to unstable. These results are due to the system delay introducing an added phase shift which eventually causes instability.

As with all stability analysis problems an acceptable gain and phase margin must be chosen which provide both adequate performance and a robust system. The gain and phase margins will be discussed later as they can be used when determining which switching frequency should be chosen by the Frequency Chooser.

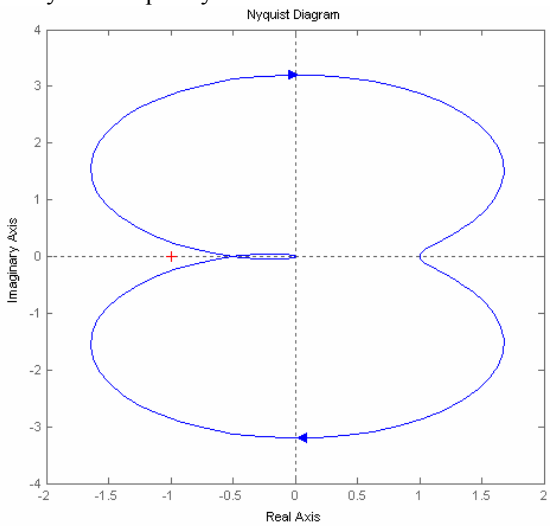

Fig. 2. System with 20kHz PWM (stable).

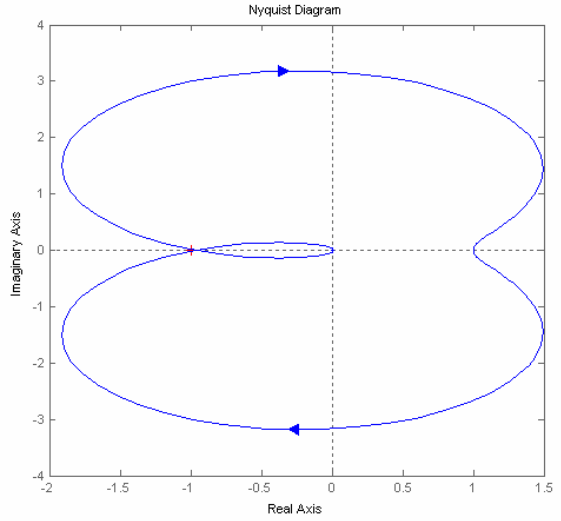

Fig. 3. System with 10kHz PWM (marginally stable).

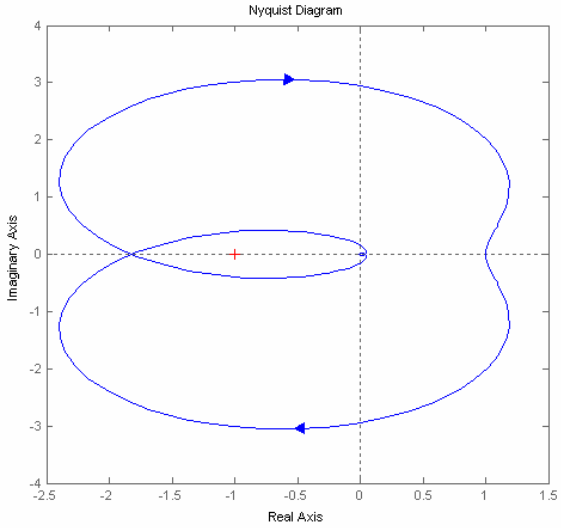

Fig. 4. System with 5kHz PWM (unstable).

B. Methods To Determine When To Change Frequency

As discussed in the previous section, the key to attaining global stability while ensuring a high efficiency is in choosing the switching frequency. As well as being able to quickly increase the system frequency to ensure system stability, the Frequency Chooser will ideally also have hysteresis to reduce the possibility of chattering where the system could oscillate between two switching frequencies.

The output error signal is used as the point of reference for determining the switching frequency. When the error is large the switching frequency is increased. When the system stabilises, the switching frequency is reduced to a point where it is marginally stable. An envelope detector was chosen as a Frequency Chooser as it has a rapid response to a large input and has an inherent decay.

An envelope detector has been shown to work satisfactorily in the following section but there are other factors that can be taken into account to improve the performance. The output voltage ripple due to the LC filter can result in chattering of the Frequency Chooser around the stable switching frequency due to the effective over-sampling that occurs. To prevent the associated ripple a model of the inductor current can be used to compensate for an expected voltage ripple [7].

To further prevent chattering, hysteresis between two switching frequencies can be introduced by enforcing a gain and/or phase margin on the present switching frequency. By forcing these margins the steady-state switching frequency in most cases will be inherently greater with a lower operating efficiency, but ensures a greater margin of stability.

C. Performance

The application of the DFS technique to a buck converter with a resistive load is shown in Figure 1b and has been modelled in Simulink with a sampling frequency of 10kHz. A PI controller was used for the simulated model to remove proportional offset error. The Frequency Chooser uses an envelope detector. As the load resistance increases the system becomes closer to being marginally stable. The system response is simulated with a 0.1 ohm load and then after five seconds is switched to a 0.7 ohm load, as shown in figure 5. As shown in the simulated system the 0.1 ohm load finds equilibrium at a switching frequency of one fourth of the sampling frequency (four times the PWM switching delay).

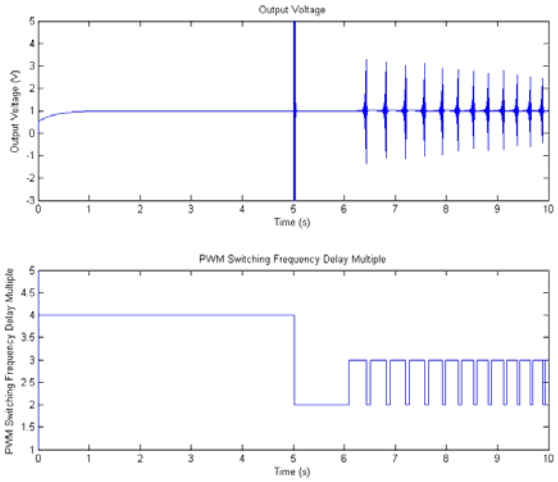

Fig. 5. System response with change in resistive load after 5 seconds.

When the load resistance is increased to 0.7 ohms the controller increases the switching frequency to half the sampling frequency. After about 6 seconds chattering is observed where the switching frequency is oscillating between a stable and unstable point. As shown in figure 6, when a system is only just unstable, the Frequency Chooser increases the switching frequency to quickly reduce the error. It is proposed that by inserting hysteresis into the Frequency Chooser the chattering could be eliminated.

The delay caused by the envelope detector decay is also observed in figure 6 where the switching frequency does not jump straight back after the oscillations have settled.

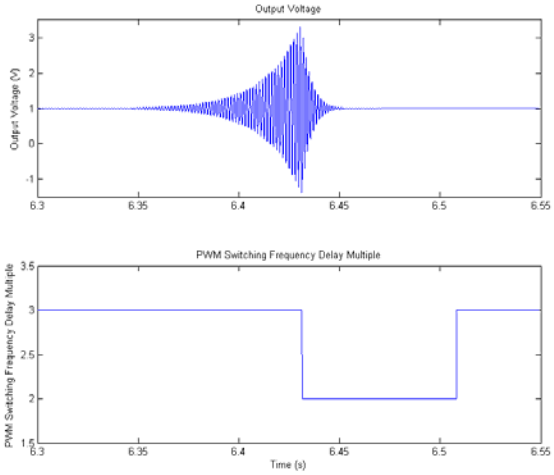

Fig. 6. Close up chattering at frequency change.

Without adjusting for the switching frequency chattering the system presents itself as a form of hysteretic control. The frequency chooser lowers the switching frequency until the system becomes unstable (resulting in an output voltage error), which in turn causes a switching frequency increase to make the system stable again. The hysteresis bands are determined by the different switching frequency levels produced by the Variable ZOH.

The chattering presents itself as an undesirable operation resulting in intermittent output errors and regular frequency switching. Alternative methods to determine the lowest stable switching frequency for a given system are currently being investigated. One approach that looks promising is to vary the controller bandwidth gains to determine a satisfactory output error before reducing the switching frequency. Then once having determined an acceptable output error, the switching frequency is decreased to a level that will just satisfy the controller bandwidth that will not cause the system go unstable.

D. Model Improvements

Modelling the PWM module using a ZOH provides a crude representation which for fixed frequency systems is usually adequate. Ongoing investigation is being done to consider the effects of changing the switching frequency of an actual PWM module driving an output LC filter. When changing the switching frequency of a PWM module the output current ripple must be taken into account to ensure that the average output current remains the same. A technique is being developed for use in a microcontroller scenario that ensures the average output current is kept constant.

III. Alternative Comparisons

DFS is similar to several converter switching techniques, most notably hysteretic control, which has no truly fixed switching frequency. Other techniques of variable frequency control which have a continuously variable switching frequency also exist. The limitation of continuously variable PWM modules is that it they require specialised PWM modules. The switching frequency for PWM modules within DSPs and microcontrollers usually must be at integer fractions of the CPU clock frequency.

Alternative switching control schemes such as hysteretic control are inherently less well defined in terms of a switching frequency (although they can be approximated [8]). DFS provides clock-synchronised PWM, which lends itself easily to paralleling of devices.

IV. Efficiency Implications

The key characteristic of DFS is its ability to provide a degree of flexibility in trading off converter efficiency and control bandwidth. By selecting a low average switching frequency that maintains system stability and the desired response, the converter can attain efficiency at least as good as that of a fixed frequency system. The efficiency of a DFS system is the same as an equivalent fixed frequency system where the switching frequency is equal to the DFS average switching frequency.

V. Application Areas

DFS is intended to be applied to medium to high power converters to provide a flexible trade-off between efficiency and bandwidth. Many applications are in AC systems and include active power conditioners, variable speed drives and soft-starters. Further investigation into the application of DFS is to be done to conclude the performance benefits for AC systems which is the ultimate focus of this research.

VI. Conclusion

In this paper a novel switching technique targeted towards medium to high power converters is presented. DFS is a variable frequency PWM intended for conventional DSP type PWM modules that offer integral multiples of the switching frequency. The switching frequency is chosen based on the present output error to ensure the system is stable yet operating at a low average PWM frequency to achieve a greater efficiency by reducing switching losses. The DFS system is implemented digitally alongside a digital controller within a DSP, exploiting the operation of the DSP PWM module.

Analysis on the non-linear variable structure system has been presented to show that for any given input there is a stable PWM frequency that will be chosen by the Frequency Chooser, making the system globally stable.

An envelope detector for the Frequency Chooser is discussed as it provides a rapid change when the output voltage error increases with a decay which prevents the frequency from quickly jumping back and forth. Hysteresis in the Frequency Chooser and an inductor current model to prevent frequency chattering have been discussed but not demonstrated in this paper.

Provided that the frequency chooser ensures a low average switching frequency, the efficiency of a DFS system will be at least comparable to that of a fixed frequency system with a

higher bandwidth system response.

VII. REFERENCES

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