FINITE STATE MACHINE CONTROLLER FOR A THREE-LEVEL ACTIVE HARMONIC COMPENSATOR

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Abstract

A three-level Active Harmonic Compensator (AHC) switching controller is implemented using a Field Programmable Gate Array (FPGA). An FPGA enables quick implementation of complex logic circuits that can be easily modified through reprogramming. The switching control logic uses a finite state machine within the FPGA to implement fixed band hysteresis current control. The three-level inverter uses a new topology that is presently used in an existing analogue AHC. Simulations are presented using the finite state machine design and operation is verified through a low power experimental unit operating as a current injection unit.

1. INTRODUCTION

With the growing demand for tighter limits on the harmonics being generated by equipment, the requirement for cost-effective active filters is increasing. The main requirement of such a unit is that it is able to accurately inject the required compensation current up to at least the 20th harmonic. To achieve this an Active Harmonic Compensator (AHC) with a fast response time is required [1].

The AHC comprises of three main parts, the power stage, harmonics controller and the switching controller. The harmonic controller monitors the load and determines the compensation current required. The switching controller takes this information to enable the appropriate power devices. The power stage uses a three-switch topology that results in three voltage levels being applied to the output inductor to produce the required compensation current.

A switching controller based on the current hysteresis control method has been designed using a finite state machine (FSM). This FSM has been incorporated into a Field Programmable Gate Array (FPGA) to enable control of a three-level inverter. The FPGA features a gate-array-like architecture, which includes two major configurable elements: Configurable Logic Blocks (CLBs) and Input/Output Blocks (IOBs). The CLBs provide the functional elements for constructing the users logic and includes the basic logic functions and flip-flops. The IOBs provide the interface between the package pins and the internal signal lines, which also contain flip-flops and buffers and can be either configured as an input, output or bi-directional pin. To connect these elements together interconnects can be programmed through a configuration file. This configuration information only remains valid while the power is on [2].

2. POWER STAGE

The power stage of the three-level controller is shown in Figure 1. The advantage of using this topology is that by enabling an extra level, the switching frequency and the electromagnetic interference (EMI) is reduced. The three-levels for this circuit are +400V, 0 and –400V. Two of these three-level circuits were connected in parallel via a current sharing choke thus providing twice the current capability. The switching current in the capacitors is also reduced which will increase their life expectancy. The switches used comprise of discrete devices in TO247 and TO264 packages. The power stage is able to provide up to 70A RMS of harmonic correction.

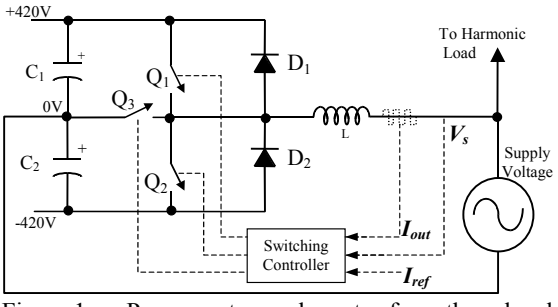


Figure 1 Power stage layout for three-level switching

3. SWITCHING CONTROLLER

Current mode control was chosen for the switching controller as it lends itself well to current sharing when several inverters are to be connected in parallel.

It also allows for direct control of the peak current in each cycle thus protecting the inverter from overloads or transformer saturation and has been proven through previous work [3]

The basic block diagram of current mode control is shown in Figure 2. This can be divided into an inner and an outer loop. The inner loop regulates the inductor current (I_L) while the outer loop specifies the value of phase current (I_P) required to regulate the bus voltage (V_{dc}). The amplitude of the reference signal $\boldsymbol{i_{ref}}$ should be such as to maintain the bus voltage at the required $\boldsymbol{V_{dc(ref)}}$ level in spite of load changes (I_{demand}) and changes in the supply voltage ($\boldsymbol{V_s}$). The mains supply voltage is multiplied with the error that exists between the actual and required bus voltage.

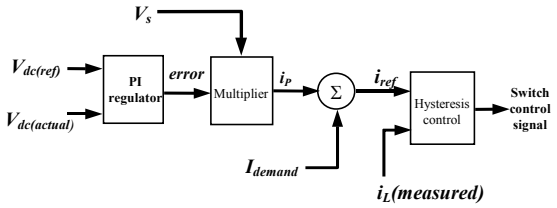


Figure 2 Block diagram of the inverter controller for operation in current regulated mode.

There are various ways of implementing the current mode block for the inverter. The method chosen was the constant tolerance band or hysteresis control as it is easy to implement and provides minimal switching noise at the output [4]. It is also well suited to active harmonic compensation where any arbitrary current waveform can be produced as the switching is determined by a comparison of the input and output current waveforms.

With hysteresis control, the actual measured current ($i_{L(measured)}$) is compared to a reference current (i_{ref}). Figure 3 shows the block diagram of the hysteresis control method and the waveforms produced. The switches are controlled so that the measured current stays within defined limits called the hysteresis band. With this method the switching frequency depends on the time it takes the current to change from one limit to the other. This depends on the size of the hysteresis band, the bus voltage V_{dc}, supply voltage V_s, and the value of the injection inductor. Since V_s is changing so does the switching frequency. With a small hysteresis band and large loads, this switching frequency can reach some very high levels.

A finite state machine is well suited to this method of control where the condition of the switches define a state while the boundary conditions define the conditions under which a state change is made [5]. This was implemented in a FPGA as it enables flexibility for future changes in the control method. It also enabled implementation of the frequency limiting circuit internally thus minimising external analogue circuitry.

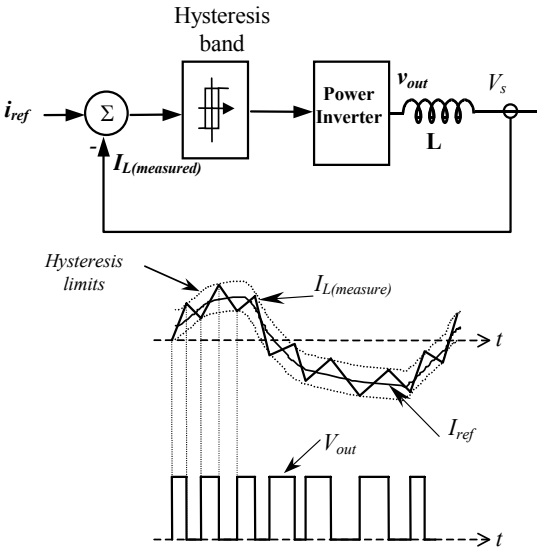


Figure 3 Block diagram of hysteresis current control method with example output current and voltage waveforms.

3.1 Simulations

Simulations were under taken of the three-level switching controller to confirm the operation under finite state machine control and look at the effects of frequency limiting on the operation of the inverter. Histograms of the switching frequency for each of the switches were generated [6]. These provide an indication of the average switching frequency. Figure 4 shows the histogram for one of the switches where a peak of 115 switching actions occurs near 20kHz and with some switching frequencies reaching as high as 50kHz. This results in an average switching frequency of 21.3kHz. By enabling frequency limiting the maximum switching frequency can be controlled.

As a consequence overshoot of the hysteresis band occurs. This is where the current passes through the hysteresis band as the switching controller is prevented or unable to bring the current within the limits. This is shown in Figure 5 in which the top plot shows the error signal (I_{ref}-I_{out}) while the bottom plot shows the absolute value of the hysteresis band overshoot. The dotted line indicates the hysteresis band limits.

Using the histograms and the overshoot plots, the best compromise can be determined for the implemented design where the maximum frequency is selected with acceptable overshoot. The level of acceptable

overshoot depends on the end use of the inverter controller.

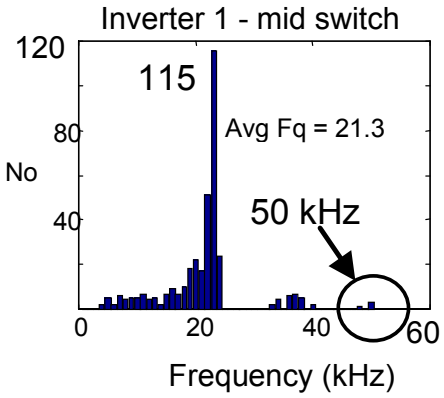


Figure 4 Distribution of switching actions for a small hysteresis band

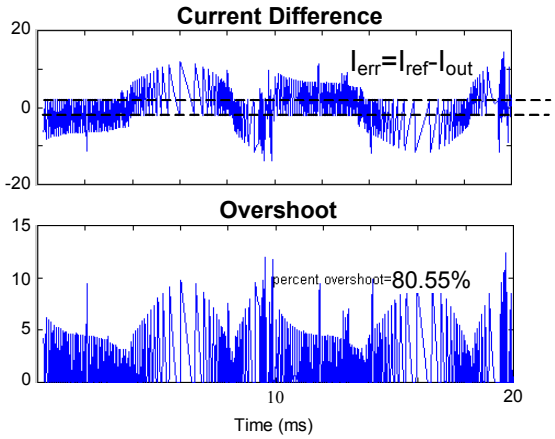


Figure 5 Current error signal and the absolute value of the hysteresis band overshoot

Under multi-level control it is necessary to consider when the extra level should be enabled. Two techniques are proposed in this paper. The first is called the hysteresis timer method and the second is called the current slope method.

With the current slope control method the slope of the reference signal is compared to the calculated slope of the output current signal. For this operation, the polarity of the output current must be known. In the situation shown in Figure 6, the current is positive and its slope is greater than that of the reference signal. The voltage across the inductor must be reduced until the current is again within the hysteresis band. The time *dt* is required to allow a settling time *dt(min)* before any comparisons are made. A small transient exists on the output current as a result of the switching operation. This current slope method has not currently been implemented in hardware.

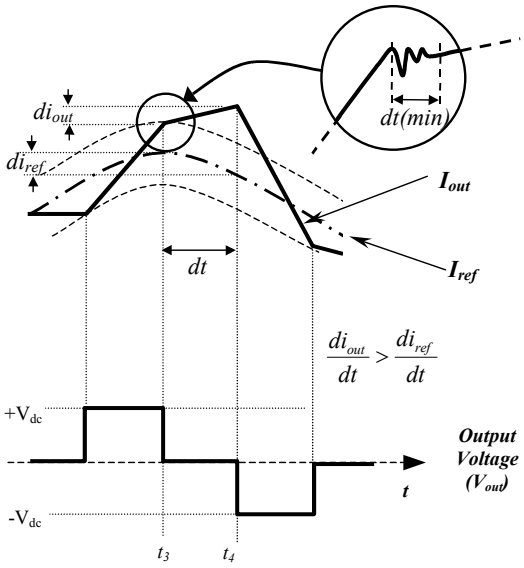


Figure 6 Current slope control method

With the hysteresis timer method as soon as the current is seen to exceed the hysteresis band, a timer is initiated. If the current does not return inside the hysteresis band after a specific time out period, the controller will switch to the next available level. The resulting waveform is similar to that shown in Figure 6 where *dt* becomes the time-out period. The overshoot that results will typically be larger than that for the current slope method and is dependant on the time-out period used. This requires some investigation as some compromise must be made between the switching frequency and acceptable overshoot.

4. HARDWARE IMPLEMENTATION

The block diagram of Figure 7 shows the hardware connection of the switching controller to the two 3-level inverters connected in parallel via a current sharing choke. The Switching Controller activates the switches of each inverter in parallel to increase or decrease the current through the main choke in order to follow the desired shape of the reference signal. The actual output current is measured using a shunt connected between the neutral as shown. The input analogue signals are converted into digital signals that are processed by the FPGA that then drives the gate drivers directly.

The Switching Controller can be broken down into a number of blocks as shown in Figure 8. Block 1 contains the interface circuitry between the sensing and measurement signals and the analogue comparator circuit.

Block 2 contains the comparator circuits to determine when the input signals have reached set limits. The resulting outputs of this block are TTL level signals

with very fast transitions times that can then be processed by the FPGA chip [2].

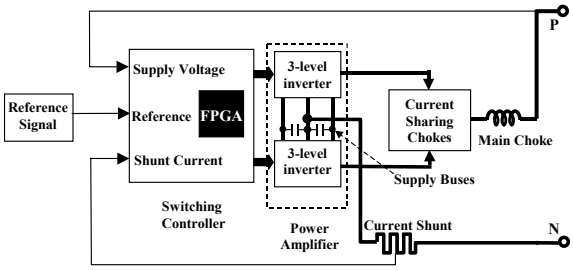


Figure 7 Block diagram of the three-level active filter

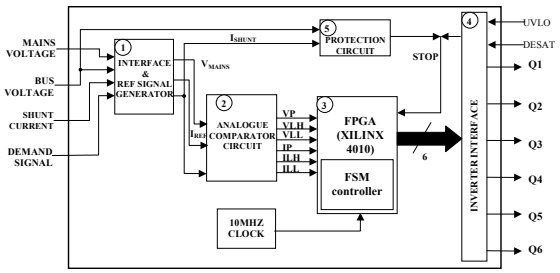


Figure 8 Block diagram of the switching controller showing the various circuits

The FPGA in block 3 contains the logic implementation of the FSM that determines which of the switches are to be activated in order to follow the reference signal.

Block 4 provides the current drive to operate the gate drivers opto-couplers. The protection circuit in block 5 includes feedback signals from the gate drivers as well as peak current and bus voltage protection.

The FPGA enables quick implementation of complex logic circuits that can be easily modified. This makes it a cost effective and versatile method that can help reduce development time [5]. The Xilinx 4010E FPGA chip was used in this switching controller. Xilinx provides extensive supporting software for ease of design implementation and debugging.

4.1 The Finite State Machines

The design of the FSM requires a good understanding of the operation of the system that is to be controlled. This means that the designer must be aware of the conditions required for a state change (voltage level change) to occur [5]. The Finite State Machine used for three-level control is shown in Figure 9. The inputs and outputs are defined at the top of the state diagram. The arrows show the direction of operation during a change in state.

An example generated through simulations is shown in Figure 10. At time t_1 the current polarity signal IP changes from positive to negative For a state change to occur, the current limit input must also be high as indicated by the condition (1). This occurs at time t_2 at which point the change in the state (to P) results in the output voltage level changing from zero volts up to 400V.

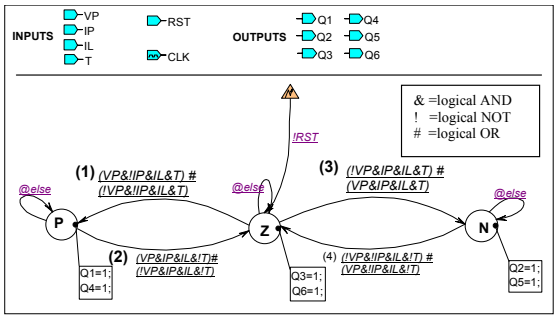


Figure 9 Finite State Machine for three-level control used in the Switching controller Xilinx chip

This results in an increase in the current till time t_3 when condition (2) is satisfied resulting in a return to the zero state (Z0). During this zero state there is still a slight rise in the current that remains outside the hysteresis band. At time t_4, the hysteresis timer input 'T' indicates that the current has been outside the hysteresis band for too long which satisfies condition (3) resulting in a change to the negative state (N) setting the output voltage to –400V. The current is now forced to decrease until the opposite hysteresis band is reached at time t_5 when condition (4) is satisfied forcing a return to the zero state. This process continues thus implementing the required current hysteresis control using the hysteresis timer method. To simplify the explanation of this finite state machine, the frequency limiting logic is not shown. In the actual system this is implemented using the monostable inputs that add further conditions that must be satisfied before a change in state can occur

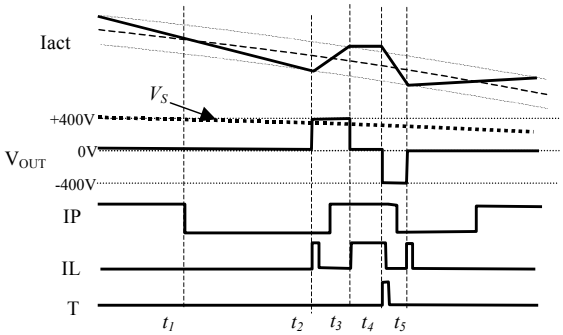


Figure 10 Simulation plot showing the operation of the three-level finite state machine design.

5. CONTROLLER OPERATION

A low power experimental version of the current injection unit has been constructed to verify operation and compare against simulations made of the design. A current of 10Arms at 150Hz was injected into the mains. This was accomplished at the full bus voltage of ±400VDC and 230Vrms mains supply. The output voltage and current waveforms are shown in Figure 10. In the experimental unit only the hysteresis timer method was used.

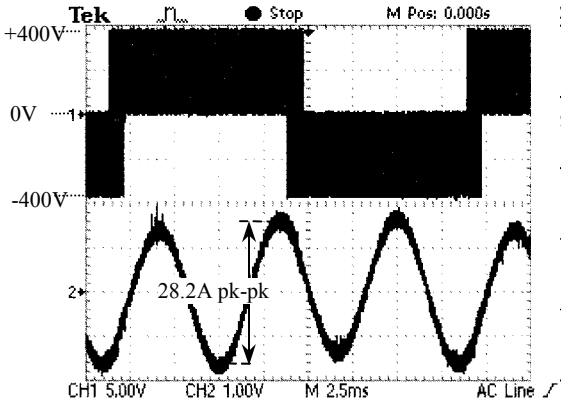


Figure 10 Switching voltage and output current waveforms

The close-up of Figure 10 shown in Figure 11 shows the operation of the hysteresis timer during the zero crossing of the mains voltage. The overshoot is due to the process delay time of the FPGA that results in the hysteresis timer being activated. This is because the slope of the current is not great enough to bring the current within the hysteresis bands in time.

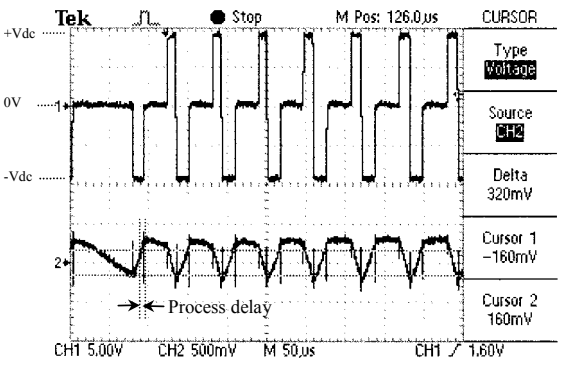
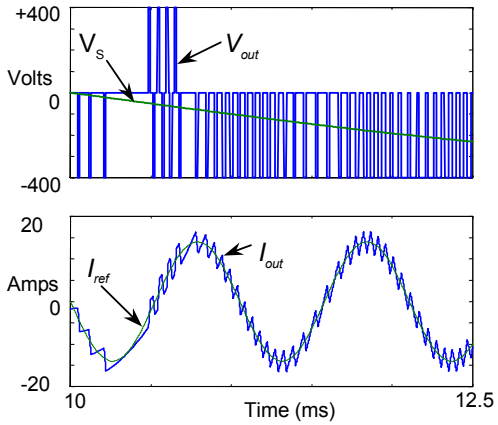


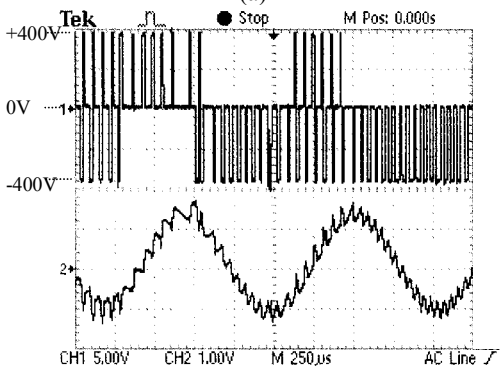
Figure 11 Close-up view of the generated output voltage waveform (Ch1) and the error signal (Ch2) with the hysteresis limits indicated by the two cursor lines

Figure 12 shows a comparison between the simulated results and the actual results for a sine wave of 950Hz at 10Arms. These show a close correlation between the two thus verifying the use of the simulation results to make the comparisons of the overshoot and average switching frequency.

The simulation plot shows the how the switching controller passes through all three levels in order to keep the current within the hysteresis limits. This occurs near the zero crossing of the mains voltage. A similar action occurs on the actual controller indicating a slightly different position on the current waveform but clearly showing the controller operating as required in keeping the current within a fixed band.



(a)



(b)

Figure 12 Output voltage and current waveforms of (a) simulation and (b) actual controller for a sine wave at 950Hz at 10Arms

6. DISCUSSION

The simulation results indicated the limitations of using the hysteresis timer control method as apposed to using the current slope method for multi-level control. With hysteresis timer control the overshoot of the hysteresis limits can become excessive particularly for higher frequency reference signals or when under frequency limiting control. Reducing the hysteresis time period can minimise this overshoot, with the minimum time being determined by the length of the process delay that exists.

By using the current slope method the overshoot can be greatly reduced as the decision time taken to change to another state can be reduced to a very small period (say 3μs).

The simulations of the frequency limiting circuits were demonstrated using a very small hysteresis band of ±2A. The mono-stables were set to 33μs so that the maximum switching frequency possible was 30kHz. Using the frequency limiting method the average switching frequency was reduced from 20kHz to 11kHz. The resulting overshoot was in excess of 80.55%.

In reality the unit would not be expected to operate with such a narrow hysteresis band and was only used to clearly show that the frequency limiting circuit would prevent high frequency switching. With a nominal hysteresis band of ±5A the percentage overshoot that resulted with the frequency limiting enabled was just 9.09%. The results from the injection unit showed very similar results to those obtained through simulation and this verified that the inverter was operating as predicted.

7. CONCLUSION

This paper investigated and implemented different switching control techniques using the hysteresis control method for a new three-level inverter topology to decrease the average switching frequency of an existing three-level system already in use as an active filter.

Two techniques for multi-level control were presented in this paper. These were the hysteresis timer control and current slope control. These were both compared through simulations and indicated that a more efficient controller could be achieved using the current slope technique. The added advantage of the current slope technique is that it enabled the overshoot to be reduced.

The simulations were also used to test the implementation of a frequency limiting technique. The major limitation of the frequency limiting technique was the excessive overshoot. The results obtained from the experimental unit verified those from the simulations at the low current level of 10Arms under three-level operation.

The work presented in this paper shows that the use of a finite state machine, implemented in an FPGA, is a viable method of control with minimal processing delays. The 'process' delay implemented in the design was used to prevent unwanted transients in the output signals from causing state changes. The FPGA provided flexibility and enabled efficient design for the new switching controller board that can be reprogrammed at any stage when particular requirements arise.

8. ACKNOWLEDGEMENT

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9. REFERENCES

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