EXPERIMENTAL CHARACTERISTICS AND AN ENHANCED PSPICE MODEL FOR POWER DIODES FROM 77K TO 300K

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Abstract
The development of high temperature (77K) superconductors has resulted in a need for their control and switching. Modelling semiconductor switches at cryogenic temperatures using presently available models results in erroneous simulations. Power diodes have been subjected to the full temperature range from 77K to 300K and their performance evaluated and compared to theory and the existing models. This paper presents experimental results and an improved PSpice model for P-i-N Power Diodes over the temperature range 77K to 300K.

1. INTRODUCTION

High Temperature Superconductors (HTSC) are being developed for use in such wide-ranging fields as energy storage, magnetism, and DC transmission. The electrical control of HTSC technology implies the use of power electronic devices. In an attempt to put this technology to use one must either subject the switching devices to low temperatures, elevate the superconductor to ambient temperature, or introduce an intermediate stage in the switching and control topology. Indeed, without the ability to control and switch the current, the applications of the HTSC may be very limited.

Decisions about the physical placement of the semiconductor diodes and their operational environment need to be made in an informed manner. To make such a decision the characteristics of the diodes over a wide temperature range needs to be known and simulation models need to be accurate. Experimental data is presented for a selection of power diodes, along with a relationship to temperature dependent semiconductor theory presented here.

The power diode simulation models available to date fail to adequately model these devices over a wide temperature range. This paper presents an enhanced PSpice model for power diodes operating over the temperature range 77K to 300K, using data taken from a cryostat built at the University of Canterbury [1]. A model has been developed and tested for a diode, giving an excellent match to experimental data.

2. THE P-i-N POWER DIODE

2.1 Structure of the Device

A power diode, as shown in Figure 1, consists of a heavily doped ($N_A \cong 10^{19}\text{cm}^{-3}$) narrow P^+ type semiconductor separated from an equally heavily doped ($N_D \cong 10^{19}\text{cm}^{-3}$) narrow layer of N^+ type semiconductor by a lightly doped ($N_D \cong 10^{14}\text{cm}^{-3}$) thicker N^- intrinsic material. The wide drift layer provides the high reverse voltage characteristic, and allows for charge storage when conducting in the forward mode. The curvature of the P^+ material is a function of lateral diffusion, and the radius of the curvature is proportional to the reverse breakdown voltage of the device [2]. Most of the potential drop occurs across drift region due to the low doping.

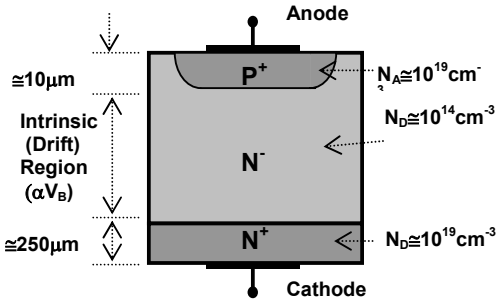

Figure 1 Structure of the Power Diode

2.2 Potential Barrier

A potential barrier is produced at the PN junction of a diode due to the majority carrier diffusion into the other region where they are in the minority. Holes are diffused from the P-type material into the N-type, and electrons diffuse from the N-type material into the P-type. This diffusion produces what is called a space charge layer on either side of the junction. Integrating over the resultant electric field yields a value for the barrier potential, Equ. (1), [2] that must be overcome for the diode to conduct. This same expression is used to describe junction voltage.

$$\phi_C = \frac{kT}{q} \ln\left[\frac{N_A N_D}{n_i^2}\right] \qquad \textbf{(1)}$$

n_i is the thermal equilibrium density, and is given in Equ. (2).

$$n_i^2 = C\exp\left(\frac{-qE_g}{kT}\right) \qquad \textbf{(2)}$$

The forward voltage characteristic of the power diode is represented as a sum of the junction voltage, Equ. (1) and the drift region voltage drop, Equ. (3). The linear nature of the on state voltage, V_d, is attributable to the on state resistance of the drift region, which dominates and suppresses the exponential nature of the typical (signal) PN junction.

$$V_d = \frac{W_D^2}{(\mu_n + \mu_p)\,\tau} \qquad \textbf{(3)}$$

where τ is the carrier lifetime, defined as;

$$\tau = \frac{W_D^2}{\frac{kT}{q}(\mu_n + \mu_p)} \qquad \textbf{(4)}$$

Singh, [3], shows that a decrease in temperature from 300K to 77K will;
Increase the hole mobility, μ_p, by 13 times,
Increase the electron mobility, μ_n, by 20 times.

2.3 The PN Junction Breakdown

Breakdown from a reverse applied voltage of the PN junction can occur as a result of three mechanisms;
Tunnelling, the usual method if the breakdown voltage is less than $4E_g/q$,
Thermal instability,
Avalanche breakdown, the usual method if the breakdown voltage is greater than $4E_g/q$,
If breakdown occurs between $4E_g/q$ and $6E_g/q$, it is usually a mixture of tunnelling and avalanche breakdown. For an abrupt parallel plane junction [3] where the only unknown values are the donor concentration, N_D, the breakdown voltage can be found in Equ. (5).

$$V_{B,NPT} = \frac{1}{2}\left(\frac{x_b+1}{x_a}\right)^{\frac{2}{x_b+1}}\left(\frac{qN_D}{\varepsilon_{Si}}\right)^{\frac{1-x_b}{1+x_b}} \qquad \textbf{(5)}$$

where ε_{Si} is the permittivity of silicon and x_a and x_b are empirically derived ionisation coefficients in accordance with Equ. (6) and (7).

$$x_a = 2\times10^{-28}e^{-16.22\times\left(\frac{T}{300}\right)} \qquad \textbf{(6)}$$

$$x_b = 5.8 + 1.2\left(\frac{T}{300}\right) \qquad \textbf{(7)}$$

Singh [3] derives Equ. (5) from the assumption that the depletion region field is triangular, and so the diode is of the non-punch-through type. Most medium-voltage diodes, however, are punch-through, and thus the depletion region field is trapezoidal [2].

The standard ionization equation cannot be solved analytically in this case. The approximation was therefore made that the maximum field strength was equal between the punch-through and non-punch-through cases, for a given temperature. The breakdown voltage for a punch-through diode is then given in Equ. (8).

$$V_{B,PT} = W_D\left(\frac{x_b+1}{x_a}\right)^{\frac{1}{x_a+1}}\left(\frac{qN_D}{\varepsilon_{Si}}\right)^{\frac{1}{x_b+1}} - \frac{qN_D}{\varepsilon_{Si}}W_D^2 \qquad \textbf{(8)}$$

This equation has a maximum in N_D. By using this maximum value as an approximation for N_D, we are effectively assuming that the device is optimised for a given drift region width, W_D. This gives the approximate equation, Equ. (9), that uses the same temperature dependent variables in Equ. (6) and (7).

$$V_{B,PT} = W_D^{\frac{x_b-1}{x_b}}\left(2/x_a\right)^{\frac{1}{x_b}}\left(\frac{x_b}{1+x_b}\right) \qquad \textbf{(9)}$$

2.4 Reverse Recovery

The typical reverse recovery characteristic of the soft recovery diode is shown in Figure 2.

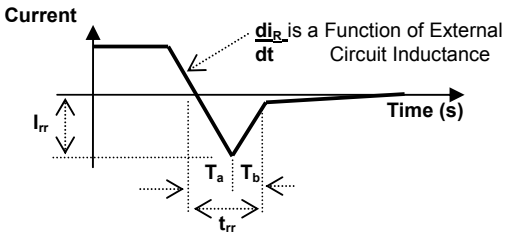

Figure 2: Typical Reverse Recovery Characteristic of a Soft Recovery Power Diode

The reverse recovery current, (I_{rr}) is the peak current overshoot. The reverse recovery time, (t_{rr}) is the time taken from I_{rr} to decay away to 25% of its peak value. The overshoot seen, (Figure 2), is a result of the conduction after turn off by the minority carriers stored in the intrinsic region of the P-i-N diode [3] that require a certain time to be neutralised by recombination with opposite charges. This must occur before the PN junction can be reverse biased. The reverse recovery current of the diode can be extracted from the reverse recovery waveform, (Figure 2,) or can be approximated [2] from Equ. (10).

$$I_{rr} \approx 2.8\times10^{-6}V_B\sqrt{\frac{I_F}{di_R/dt}} \qquad \textbf{(10)}$$

The only variable in Equ. (10) is the reverse breakdown voltage, V_B, whose temperature dependence is discussed in Sections 2.3 and 3.2.

Alternatively, the limit can be found from Equ. (11) [2].

$$I_{rr} < \sqrt{2\tau I_F \, di_R/dt} \qquad \textbf{(11)}$$

From Equ. (11) it can be seen that the only variable is the temperature dependent carrier lifetime given in Equ. (4) and thus this is proportional to the reverse recovery current.

The reverse recovery time, (t_{rr}), of the PN junction is an important design characteristic that limits the devices switching speed. This figure can be extracted from the reverse recovery current waveform, or can be approximated [2] from Equ. (12).

$$t_{rr} \approx 2.8\times10^{-6} V_B \sqrt{I_F \left(di_R/dt \right)} \qquad \textbf{(12)}$$

The only variable in Equ. (12) is the reverse breakdown voltage, V_B, whose temperature dependence is discussed in Sections 2.3 and 3.2. Alternatively, the limit can be found [2] from Equ. (13).

$$t_{rr} < \sqrt{\frac{2\tau I_F}{di_R/dt}} \qquad \textbf{(13)}$$

From Equ. (13) it can be seen that the only variable is the temperature dependent carrier lifetime given by Equ. (4) and thus this is proportional to the reverse recovery time.

The stored charge in the device must be removed from the intrinsic region for the device to become reverse biased. It is defined as an integration over the entire region defined as $T_a + T_b$, and can be calculated by;

$$Q_{rr} \approx \frac{I_{rr} \, t_{rr}}{2} \qquad \textbf{(14)}$$

3. EXPERIMENTAL RESULTS

Various P-i-N Power diodes rated from 5A to 20A and from 800V to 1600V were tested [1] up to 25A. These devices are operated over a temperature range of 77K to 300K and selected results are presented.

3.1 Forward Characteristic

When the device is forward biased and subjected to differing temperatures within rated current it can be seen that the potential drop associated with the junction voltage increases significantly, (Figure 3), with minimal noticeable effect on the drift region voltage.

When the device is operated above the maximum manufacturers current rating the effect on the drift region volt drop is apparent in Figure 4. At high current densities the potential drop associated with the drift region decreases, and this occurs to such a degree that it overcompensates for the increase in the junction voltage potential drop, resulting in a lower on state volt drop at high current densities. Equ. (3) shows that this is a result of the temperature dependent variables of mobility or lifetime.

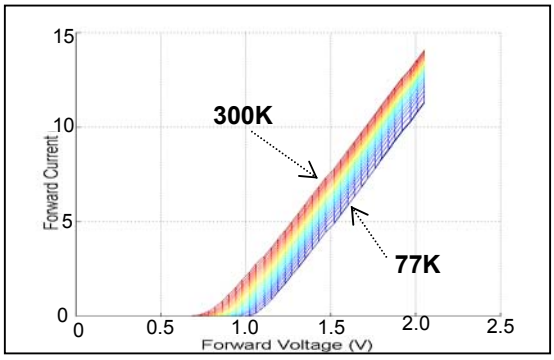

Figure 3 20ETS08 (800V, 20A) Power Diode Forward Characteristic

Figure 4 shows that when operating the BYT106-1300 up to 3.5 times rated current the forward volt drop can be decreased if the device is operated at a temperature around 120K. At currents greater than 4 times rated current the device shows the best characteristic at 77K.

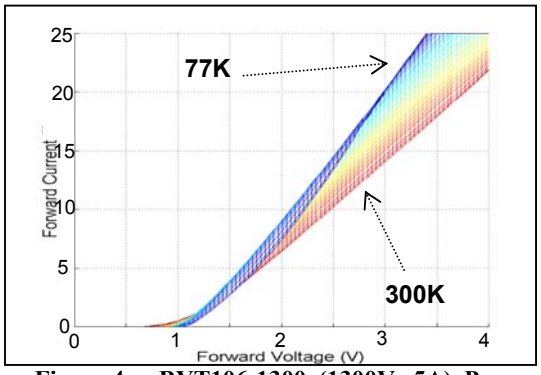

Figure 4 BYT106-1300 (1300V, 5A) Power Diode Forward Characteristic

3.2 Breakdown Characteristic

The reverse blocking characteristic of a diode decreases with temperature, (Figure 5), as predicted in Section 2.3.

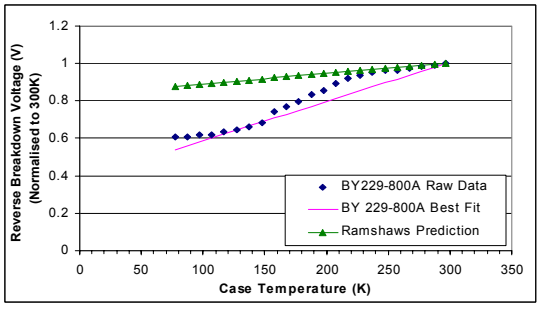

Figure 5 Breakdown Voltage Temperature Dependence

From Figure 5 it is apparent that a device may no longer meet its reverse blocking voltage specification when operated over such a wide temperature range. Ramshaw [4] makes the observation that the breakdown voltage of a PN junction has a positive temperature coefficient and that it decreases at a rate of approximately 0.7V/°C. The results from this particular diode do not support such a prediction over the range 77K to 250K, although it appears to be accurate above 250K.

3.3 Reverse Recovery Characteristic

The reverse recovery characteristic of a power diode undergoes significant changes over the range 77K to 300K and these changes are not linear. The reverse recovery current and reverse recovery time decrease significantly, as shown in Figure 6.

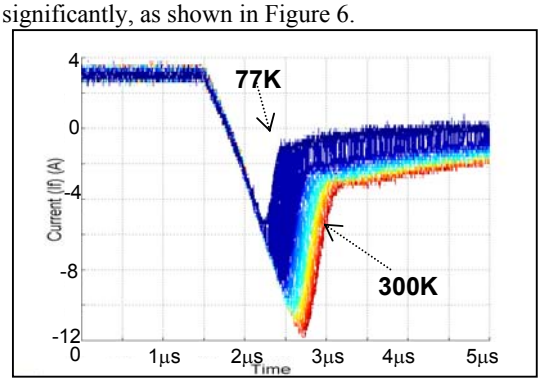

Figure 6 20ETS08 (800V, 20A) Power Diode Reverse Characteristic

The stored charge in the drift region of the device as defined in Equ. (14) is reduced significantly.

The non-linear effect on the reverse recovery current shown in Figure 7 and the reverse recovery time in Figure 8. This shows a match at 300K and 77K with the approximation of Equs. (10) and (12), and the limit imposed by Equs. (11) and (13). However at other temperatures there is a difference between the predicted and measured results. The reduction of the turn off time of the device by a factor of two implies that the maximum operating frequency of the device can be doubled.

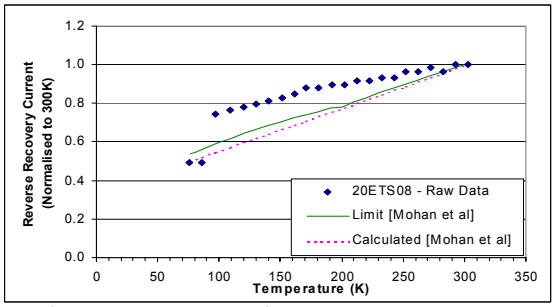

Figure 7 Power Diode Reverse Recovery Current Temperature Dependence

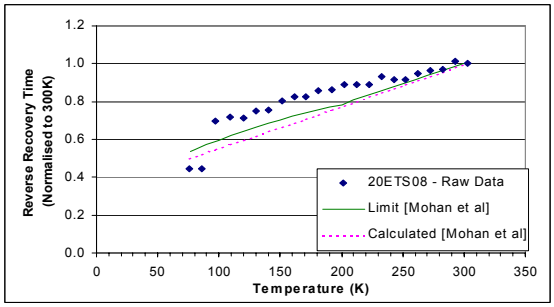

Figure 8 Power Diode Reverse Recovery Time Temperature Dependence

3.4 Leakage Characteristic

Figure 9 shows that the leakage current in the power diode is heavily temperature dependent, and only rises above the level of noise above 250K. The exponential nature of the leakage current is expected given that presence of the thermal equilibrium constant, Equ. (2), in the expression for saturation current, Equ. (15).

$$I_s = qn_i^2\left[\frac{x_p}{N_A\tau_n} + \frac{x_n}{N_D\tau_p}\right] \qquad \textbf{(15)}$$

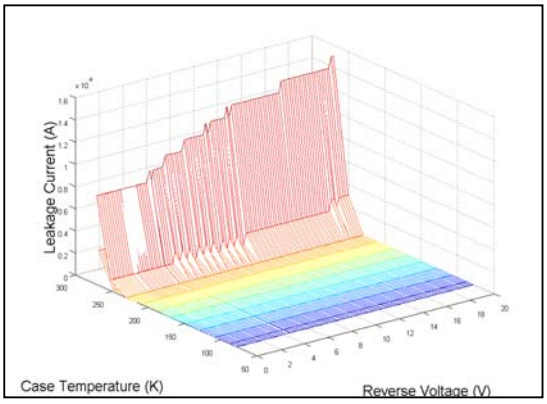

Figure 9 20ETS08 (800V, 20A) Leakage Current Temperature Dependence

This leakage current, I_s, according to theory, the same as the saturation current in the forward characteristic equation as given,

$$I = I_s\left(\exp\left(\frac{qV_j}{nkT}\right) - 1\right) \qquad \textbf{(16)}$$

4. NEW PSPICE MODEL

4.1 Differential Modelling

To create this new model which is accurate over a wide cryogenic temperature range, a "differential modelling" technique has been developed. This eliminates the need to deal with saturation current, a small parameter whose temperature dependence is inadequately known.

The saturation current, I_s, appears in the Shockley diode equation (16), which is the basis of the PSpice model. It is of the order of nanoamps and depends very strongly on temperature. Such a tiny parameter is difficult to measure accurately and is thus unsuitable for use in modelling when temperature is not fixed.

Many diodes have an operating point (V_0, I_0) that is stationary with temperature [3]. Shockley's equation then becomes

$$\Delta I = (I_0 + I_s)\left(\exp\frac{q(\Delta V - \Delta I \cdot R_s)}{nkT} - 1\right) \quad \textbf{(17)}$$

where $\Delta I = I - I_0$ and $\Delta V = V_D - V_0$ and all other symbols have their usual meaning. I_s is much smaller than I_0, and so becomes negligible for modelling forward current. This equation was found to lead to more robust cryogenic models than the Shockley equation.

4.2 Static Parameter Fitting Procedure

Data from a DTV32-1200 diode was taken from the cryostat for investigating PSpice modelling at low temperatures. According to this data, V_0 is temperature dependent for this device. I_0 was arbitrarily fixed at 2A, and V_0 was very closely fitted as a linear function of temperature. Resistance was nearly constant, varying by only 15% across the cryogenic range. It was fitted by a quadratic function, with an anomalous linear correction for temperatures below 98K.

Breakdown was included using Equ. (9), with a drift width of 75μm. This gives a breakdown voltage of 1300V at a temperature of 300K. The rated reverse voltage for this device is 1200V.

4.3 Dynamic Parameter Fitting Procedure

The differential static model was combined with a dynamic charge stored model [5]. Fitting was enabled by assuming that the turn-off slope is constant. This assumption is reasonable, as slope depends only on stray inductance, a quantity which is temperature independent. Moreover, the reverse turn-off charge, Q_{rr}, was roughly linear below 260K, and a linear fit was taken from this data. Above 260K, the reverse turn-off charge is greater than modelled, mainly due to a small but protracted tail current. Fitting to experimental data gave $T_M^{2.2}$ and $\tau^{1.5}$ as being approximately linear with temperature. These fits were used in the model. Here T_M is device transit time and τ is carrier lifetime.

4.4 Model Verification

As shown in Figure 10, the static characteristics fit well at all temperatures. The usual built-in PSpice model is clearly not suitable for use over this temperature range. As can be seen from Figure 10, this

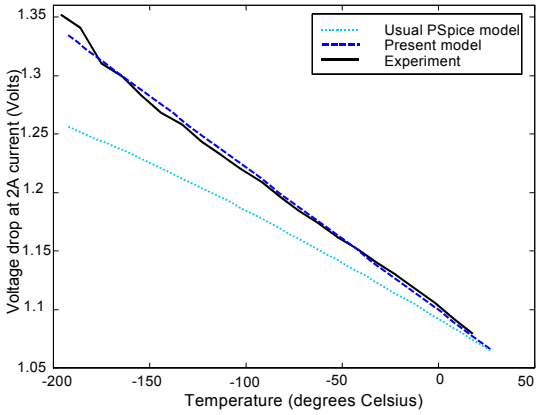

Figure 10 Models Forward Voltage Drop Temperature Dependence

characteristic deviates from the experimental data below 300K. The fit shown in Figure 10 is the best that could be obtained, and takes resistance and high-level injection into account.

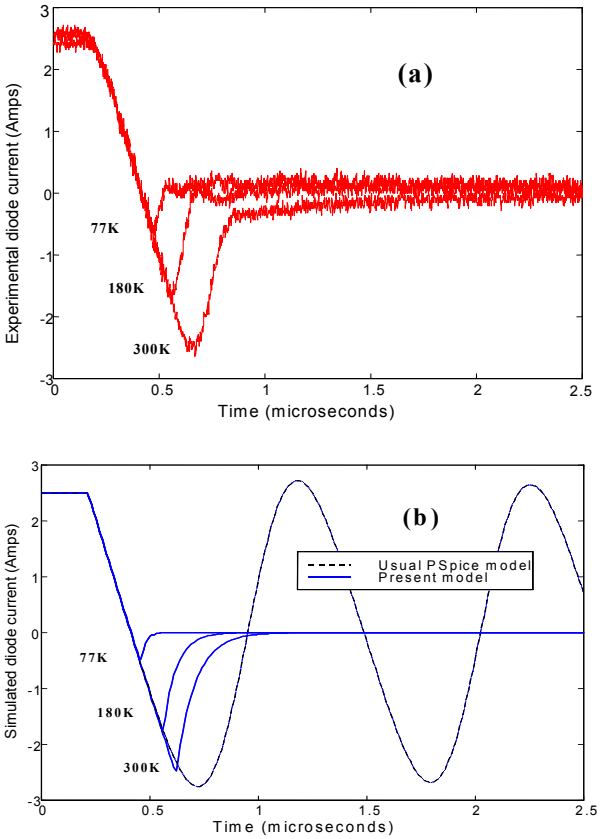

Figure 11 Experimental (a) vs Modelled (b) Reverse Recovery

Dynamic response also fits the experimental results well, except for tailing current, which is not modelled. The usual PSpice diode model does not account for the three-layer construction of the power diode, and reverse recovery is not correctly simulated. This is shown by the oscillating dotted line in Figure 11b, from a simulation at 300K.

The new model gives much more realistic results, which are shown line in Figure 11b. It has an accurate temperature dependency down to 77K, as shown by comparing simulation against experiment for three particular temperatures.

5. CONCLUSIONS

Based on semiconductor theory and the observed experimental results presented it is concluded that as the temperature of a P-i-N power diode falls the hole mobility increases, and the electron mobility increases, the carrier lifetime falls, and the current density increases. These physical effects manifest themselves in an increase in the junction voltage of the device and a decreased drift region voltage at high current densities. The maximum operating frequency increases, and there is a decrease in the maximum reverse recovery current. Leakage current falls exponentially and the reverse breakdown voltage of the device decreases.

Operation of these devices at temperatures down to 77K can provide significant improvements in some aspects of their performance, but the degradation of some parameters, such as the reverse blocking voltage, means that the implementation of these devices in the cryogenic environment is not a straightforward process.

A PSpice model was developed for a power diode which matched experimental data over the range 77K to 300K. It was accurate in modelling both the static characteristics and the dynamic reverse behaviour. This simulation model will help to greatly simplify the design of power electronic circuits for use at cryogenic temperatures.

6. REFERENCES

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7. APPENDIX

7.1 Nomenclature

C is a constant,
D_n is the electron diffusion constant,
D_p is the hole diffusion constant,
E_g is the energy gap of the semiconductor,
I is the device current,
I_F is the forward current,
I_s is saturation current,
i_R is the reverse current,
I_{rr} is the reverse recovery current,
I_0 is the reference current,
k is Boltzmann's constant,
n is the diode ideality factor, between 1 and 2,
N_A is the acceptor concentration,
N_D is the donor concentration,
n_i is the thermal equilibrium density,
q is the magnitude of electron charge,
Q_{rr} is the stored charge in the device,
R_s is the series resistance,
T is Temperature (Kelvin),
T_M is transit time,
t_{rr} is the reverse recovery time,
$V_{B,PT}$ is the breakdown voltage for a Punch-Through device,
$V_{B,NPT}$ is the breakdown voltage for a Non-Punch-Through device,
V_d is the volt drop across the drift region,
V_j is the junction voltage over the P^+-N^- junction,
W_D is the width of the drift region,
x_a is an ionisation coefficient,
x_b is an ionisation coefficient,
x_n is the depletion region into the N-type material,
x_p is the depletion region into the P-type material,
Δ is the difference operator,
ε_{Si} is the dielectric constant of the semiconductor.
μ_n is the electron mobility,
μ_p is the hole mobility,
τ is the carrier lifetime,
τ_n is the electron carrier lifetime,
τ_p is the hole carrier lifetime,