Digital Control of a Series-Loaded Resonant Converter

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ABSTRACT

Primarily because of its low cost and ease of implementation, analogue control has been the dominant control strategy in modern switch-mode power supply designs. The 'on/off' nature of power switches is essentially digital, which makes it tempting for power electronics engineers to combine the emerging capability of digital technologies with existing switch-mode power supply designs. Whereas an analogue controller is usually cheaper to implement, it lacks the flexibility and capacity to implement the complex control functions which a digital controller can offer.

The research presented in this thesis addresses the practical implementation of a digital controller for a Series-Loaded Resonant Converter (SLR). The resonant frequency of the SLR converter is around 60 kHz, and the switching frequency varies up to around 80 kHz to regulate the $12V$dc output voltage across a $100W$, variable resistive load, from a variable $46.6V$–$60.2V$ input voltage. This provides a fair challenge for digital waveform generators as the digital processor needs to have a high clock rate to produce high speed, high resolution and linearly varying frequency square waves, to regulate the output voltage with adequate resolution. Digital compensation algorithms also need to be efficient to minimise the phase lag caused by the instruction overhead.

In order to completely understand the control needs of the SLR converter, an analogue controller was constructed using a UC3863N. The feedback compensation consists of an error amplifier in an integrator configuration. Digital control is accomplished with a TMS320F2812 Digital Signal Processor (DSP). Its high throughput of 150 MIPS provides sufficient resolution to digitally generate linearly varying frequency switching signals utilising Direct Digital Synthesis (DDS).

Time domain analysis of the switching signals, shows that the DDS generated square

waves display evidence of jitter to minute variations in pulse-widths caused by the digitisation process, while in the frequency domain, this jitter displays itself as additional sidebands that deteriorate the fundamental frequency of the switching signal. Overall, DDS generated square waves are shown experimentally to be adequate as control signals for the MOSFET power switches. Experiments with step load changes show the digital controller is able to regulate the output voltage properly, with the drawback of the settling time being a little longer than the analogue counterpart, possibly caused by the unpredictable damping effects of switching signal jitter. Variations in input voltage shows that the digital controller excels at operating under noisier conditions, while the analogue controlled output has slightly greater noise as input voltage is increased.

As the digital technology continues to improve its speed, size and capacity, as well as becoming more affordable, it will not be long before it becomes the leading form of control circuitry in power supplies.

ACKNOWLEDGEMENTS

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Secondly, I would like to express my gratitude to fellow technical staff for their constant support. I am very grateful towards both Mr Ron Battersby and Mr Ken Smart for putting up with my lack of practical experience in power supply construction, and the numerous times they helped me in acquiring various experimental apparatus. Special thanks to Mr Malcolm Gordon for lending me various sophisticated equipment that allowed me to complete various experiments. I also need to thank Mr Philipp Hof for computer software support, as well as Mr Scott Lloyd and Mr Steve Weddell for providing the much appreciated DSP info sessions.

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Chapter 1

INTRODUCTION

The idea of implementing resonant switches in common switch-mode power supplies, is an attempt to reduce the losses in switches by switching during zero voltage/zero current states. This leads to better overall efficiency from the power supply and thus improve the power density of the same topology. One example of a resonant converter is a SLR converter [1], which consists of a series combination of a capacitor and an inductor as the resonant tank. The regulation of the converter is done by altering the switching frequency, and thus changing the quality factor of the resonant components, to give the desired output voltage levels.

At present, analogue circuitry has been the dominant control technology in switch-mode power supplies, including the resonant type converters described earlier, for being low cost and having more specialised controllers. Yet engineers tend to run power switches and diodes at either 'on' or 'off' conditions, therefore it is only natural to produce the driving signals of power switches straight from the pins of a digital controller, let it be a microprocessor or a DSP. With the ability to place vast numbers of transistors into small digital Integrated Circuits (IC), modern nanotechnology allows digital ICs with less components to acquire far greater potential than analogue controllers. Therefore, in order to take advantage of the greater potential and the more intuitive nature, digital control will be the future of power supply technology. Furthermore, digitising the control loop of a power supply allows different control strategies and product variations to be implemented by software means, rather than replacing or adding additional hardware. This versatility in the application of software will contribute to lower costs in the long run.

The goal of this research is to combine both ideas above and design a digitally controlled SLR converter that requires minimum circuitry. Ideally, the whole topology shall consist

only an SLR converter, an array of resistive loads, voltage/current sensing circuits, and a digital processor. What differs this research from a digitally controlled Pulse-Width Modulated (PWM) converter, is a digital controller with the ability to produce high frequency switching signals that linearly varies the frequency, with adequate resolution, at realtime to regulate the SLR converter.

The SLR converter can have a resonant frequency of around 60 kHz, and regulates output voltage by varying the switching frequency up to around 80 kHz. This frequency range is achievable with present digital technology and is sufficiently high to demonstrate the advantages of resonant switching technology. The digital processor needs to be reasonably fast to generate high speed, high resolution and linearly varying frequency square waves, to regulate the output voltage properly, with adequate resolution. Digital compensation algorithms within the controller need to be designed such that it provides adequate stability with minimum overhead.

The organisation of the thesis is as follows:

Chapter 2 describes the concepts behind a working SLR converter operating above resonance, as well as the important components and considerations used towards building an uncompensated SLR converter.

Chapter 3 introduces the concept of controlling an SLR converter through the use of an analogue compensator in a feedback loop. The compensation is designed by looking at both the simulated and measured Bode plots of the SLR converter. The specifications of the analogue SLR converter are described as well.

Chapter 4 shows the advantages and disadvantages of digital control, as well as the algorithms proposed to generate waveforms by software and digital compensation.

Chapter 5 provides the methods for implementing a digital controller with waveform generation to the SLR converter. Both hardware and software considerations are included.

Chapter 6 shows the results of the digital controller and compares them with the per-

formance of the analogue controller. The results include the frequency spectra of the digitally generated switching signals and the voltage transients during load changes.

Chapter 7 concludes the research and provides some pointers in terms of further improvements for the digital controller.

Chapter 2

CONSTRUCTION OF AN SLR CONVERTER

This chapter describes the basic knowledge needed in order to build an SLR converter, and the selection of various electronic components. The background knowledge includes how the incorporation of resonant components would affect an otherwise hard-switching converter to reduce its switching losses, and the effect on the output voltage when the switching frequency is changed. The description of component selection includes the choice of controller, isolated gate driver and the design of the converter load.

2.1 SLR CONVERTER BASICS

A typical series-resonant circuit consists of a resistor connected to a series combination of an inductor and a capacitor. The resonant components have characteristic impedance Z_0, and resonant frequency ω_0 defined by

$$Z_0 = \sqrt{\frac{L}{C}} \tag{2.1}$$

$$\omega_0 = \frac{1}{\sqrt{LC}} \tag{2.2}$$

Another quantity of interest in the circuit is the quality factor, Q, defined as

$$Q = \frac{\omega_0 L}{R} = \frac{1}{\omega_0 C R} = \frac{Z_0}{R} \tag{2.3}$$

If the circuit is excited by an ac source, as in Fig. 2.1a, the overall impedance, Z_s, of the circuit changes in accordance to the frequency of the alternating source, ω_s. Z_s is minimum and purely resistive ($Z_s = R$) at resonance, and increases dramatically as ω_s deviates from ω_0. Q is the ratio of reactive to resistive components in the circuit and it

influences the rate at which Z_s changes. The greater Q is, the bigger the rate of change. The circuit impedance as a function of source frequency is shown in Fig. 2.1*b*.

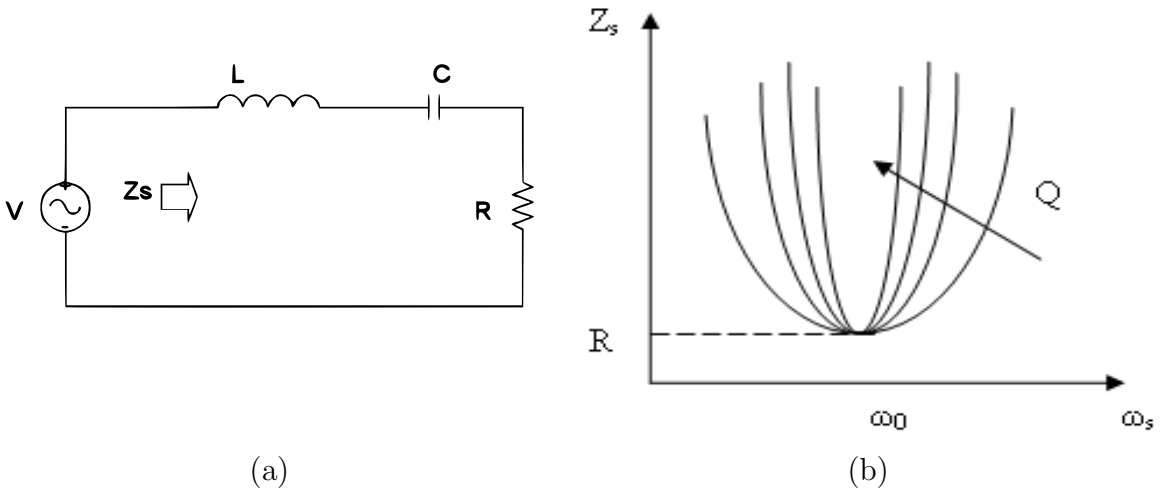


Figure 2.1 (a) A series-resonant circuit, (b) overall circuit impedance as a function of the source frequency.

In order to construct an SLR converter, the ac source in Fig. 2.1*a* is replaced by a half bridge inverter attached to a dc source, the user is able to vary the source frequency applied to the series-resonant circuit by changing the switching frequency of the half bridge inverter, and therefore regulate the voltage drawn across the resistive load. The alternating current going through the resistor can be further rectified by four diodes to give a dc output voltage. The resulting dc-dc SLR converter topology is shown in Fig. 2.2.

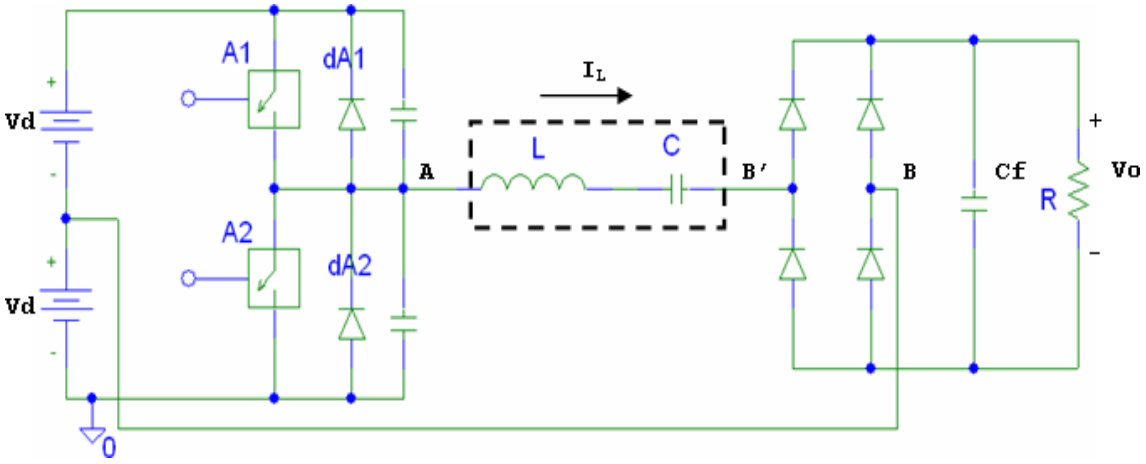


Figure 2.2 A dc-dc SLR converter.

Selecting switching frequencies above resonance, the SLR converter operates in continuous conduction mode, and the transistors are able to turn on at both zero voltage and zero

current states, with the help of the parallel clamping diodes. Although the switches are required to turn off the full inductor current, this can be improved by using lossless snubber capacitors. There are four operating states to an SLR converter operating above resonance, shown in Table 2.1 [1], which depend on the action of the switches and the direction of inductor current, I_L.

Table 2.1 Four operating states of an SLR converter.

Direction of I_L	Conducting Switch	$\mathbf{V_{AB}}$	$\mathbf{V_{AB'}}$
$I_L > 0$	A1	V_d	$V_d - V_o$
	dA2	$-V_d$	$-V_d - V_o$
$I_L < 0$	A2	$-V_d$	$-V_d + V_o$
	dA1	V_d	$V_d + V_o$

Whenever a switch turns on, the resonant tank is charged up from the supply; at turn-off, the voltage in the resonant tank opposes the current flow, allowing the current to decay quickly through the free-wheeling diode, resulting in zero voltage and zero current turn-on for the next switching cycle. The simulated switching waveforms for the SLR converter are shown in Fig. 2.3.

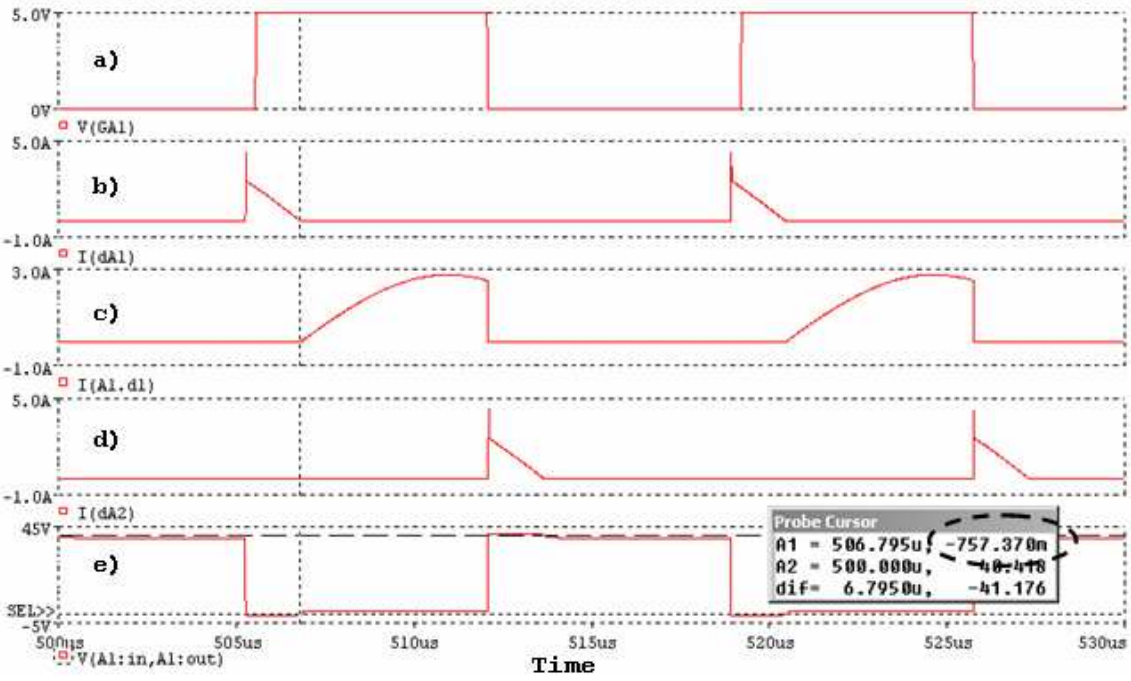


Figure 2.3 Simulation of (a) gate signal to A1, (b) current of dA1, (c) current of A1, (d) current of dA2, (e) voltage across A1.

As shown in Fig. 2.3, if the control signal, V(GA1), is activated while dA1 is still on, no current flows into A1 until the current in dA1 ceases to flow. This effectively clamps

the voltage across A1 to nearly $0V$ (as shown in the dashed circle) before turn-on, for zero voltage switching (ZVS). The current in A1 shall follow a sinusoidal shape, with its period dependent on the LC combination in the resonant tank. Therefore, if the switching frequency is the same as the resonant frequency, zero current switching (ZCS) can be achieved. If switching frequency is greater than resonant frequency, lossless turn-off snubber capacitors can be used in parallel with the switches to relieve the turn-off current stress.

2.2 DESIGN OF AN SLR CONVERTER

The design of an SLR converter can start by choosing an appropriate analogue controller, which also determines the available frequency range of the SLR converter. Then an isolated gate driver for the half-bridge is chosen to provide adequate isolation and drive from the controller to the power switches. The design of the passive components such as resonant tank and resistive load, are done to conform to the operating frequency specified by the controller. Lastly, a voltage sensor shall be designed to feedback the output voltage to the compensation circuit and the controller. The proposed block diagram of the SLR converter is shown in Fig. 2.4.

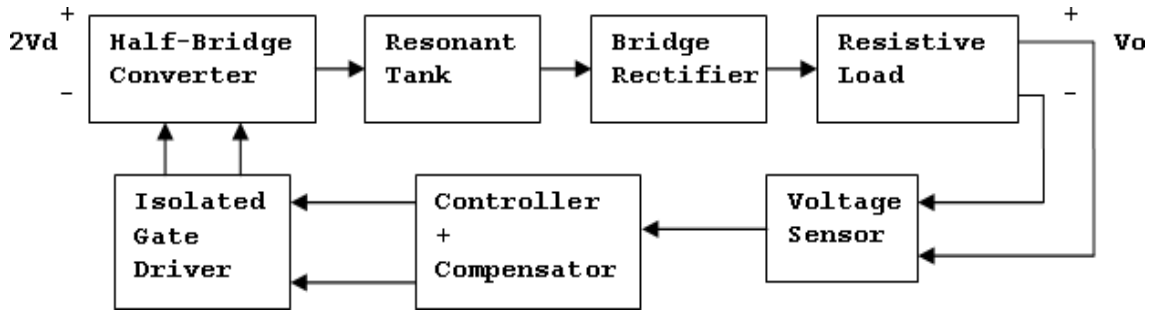


Figure 2.4 Block diagram of the SLR converter.

2.2.1 Controller Selection

The most suitable analogue controller available is the UC3863N controller from Unitrode [2]. It is commonly used for push-pull switching configurations, and has a wide oscillator frequency range of 50 kHz to 500 kHz. The functional block diagram of the controller is shown in Fig. 2.5.

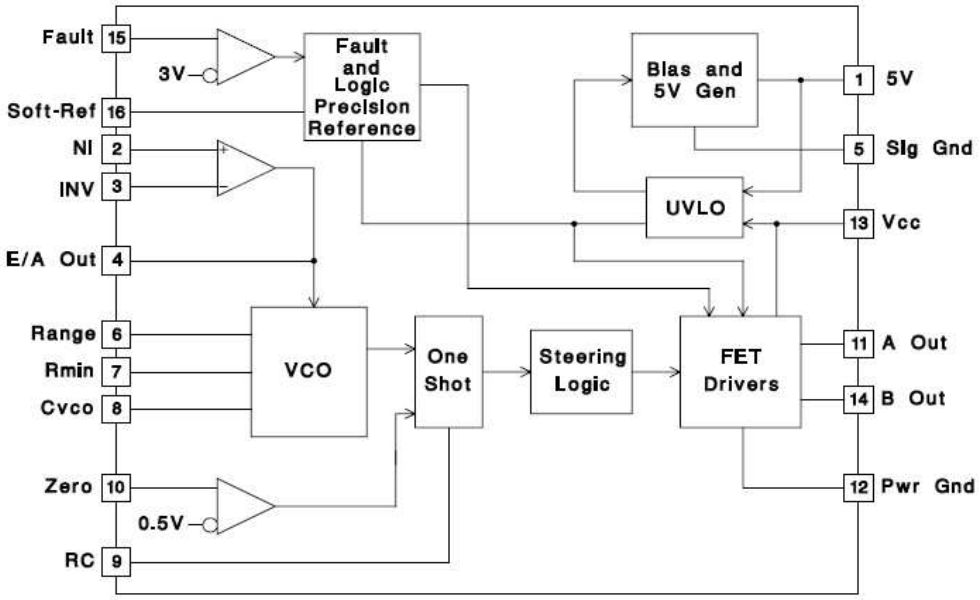


Figure 2.5 Block diagram of the UC3863N controller.

A useful feature of the controller is the adjustable deadtime between non-overlapping switching signals. An ideal deadtime must be small enough to set each gate signal during the discharge phase of the parallel diode, as required for SLR converter operation described in Section 2.1, yet it has to be long enough to make sure both switches do not short the input terminals together. The steering logic internal to the UC3863N that produces the desired alternating square waves is shown in Fig. 2.6.

It is evident from Fig. 2.6*b* that both the frequency and deadtime of the non-overlapping signal is determined by the frequency and pulse-width of the internal one shot. The maximum and minimum frequency parameters are approximated by the respective resistor and capacitor values at pins 6–8.

$$F_{MIN} \approx \frac{4.3}{R_{MIN} \cdot C_{VCO}} \tag{2.4}$$

$$F_{MAX} \approx \frac{3.3}{(R_{MIN} \parallel Range \cdot C_{VCO})} \tag{2.5}$$

While the minimum and maximum pulse-widths are approximated by a parallel combination of a resistor and a capacitor at pin 9.

$$Tpw(min) \approx 0.3 \cdot R \cdot C \tag{2.6}$$

$$Tpw(max) \approx 1.2 \cdot R \cdot C \tag{2.7}$$

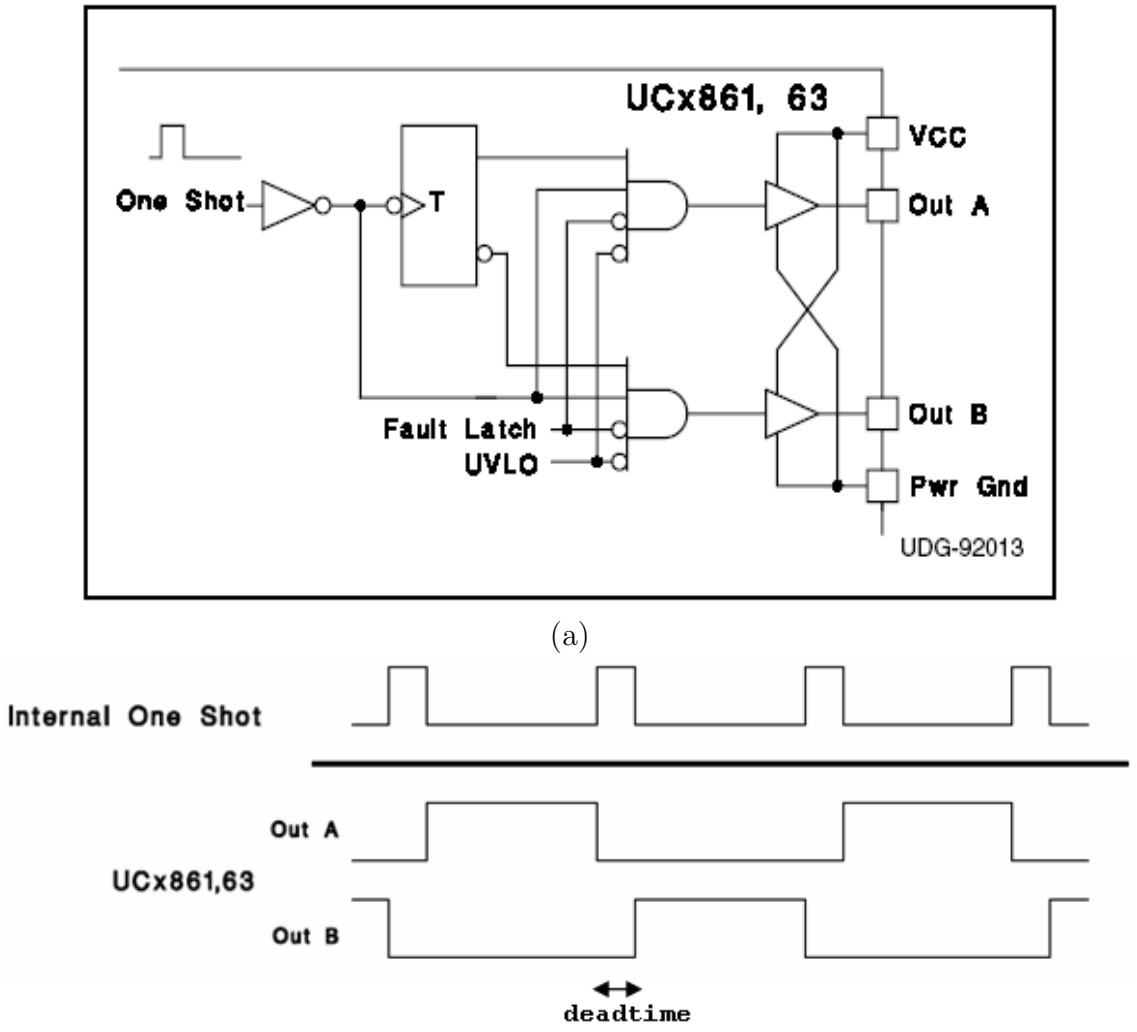


Figure 2.6 (a) The steering logic in the UC3863N that produces (b) dual non-overlapping square waves from the one shot signal.

The SLR converter is designed to operate above 60 kHz, which is at the low frequency end of the implementation of UC3863N controller, and high enough to pose a challenge for digital control. The high frequency range of the controller is set to be around 80 kHz, as it is more than the half-power frequency for the proposed load, described later in Section 2.2.3. Therefore, one shot signals between 120 kHz to 160 kHz are required. By Eqs. 2.4 and 2.5, the passive components involved are $R_{MIN} = 33k\Omega$, $Range = 82k\Omega$, $C_{VCO} = 1nF$. The deadtime of the non-overlapping square waves have been found to be at best less than $1\mu s$, therefore $R = 6.8k\Omega$ and $C = 100pF$, to give minimum and maximum deadtime of $0.2\mu s$ and $0.8\mu s$ respectively, according to Eqs. 2.6 and 2.7. As a result, the provisional schematic for the open-loop (OL) analogue controller is shown in Fig. 2.7.

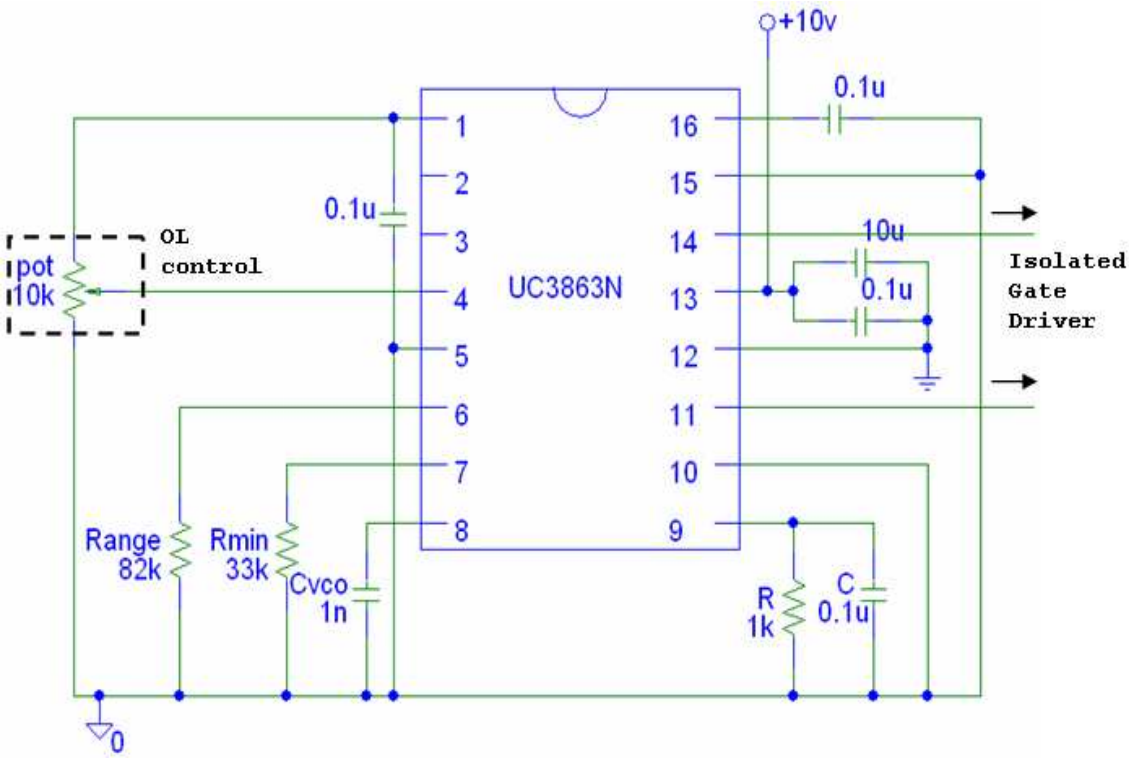


Figure 2.7 OL configuration for the analogue controller.

The capacitors connected between pins 1–5 and pins 12–13 are used to provide adequate filtering for $5V$ and $10V$ supplies respectively, while the capacitor from pin 16 is used to implement the soft-start time of $1ms$. Pins 2–3 are disconnected for now as the internal error amplifier is not used for the OL configuration. A $10k\Omega$ potentiometer is connected across the $5V$ reference voltage and signal ground to provide a variable voltage to the input of the voltage controlled oscillator (VCO) at pin 4.

2.2.2 Isolated Gate Driver Selection

Some form of isolation is essential to drive the half bridge, because the two switches operate with different reference voltage levels, therefore an isolated gate driver with two output levels will be ideal. The chosen gate driver is IR2112 for its low component count and the ability as a high and low side driver. An example of its wiring diagram is shown in Fig. 2.8 [3].

The gate driver develops high and low side signals using three capacitors. While capacitor

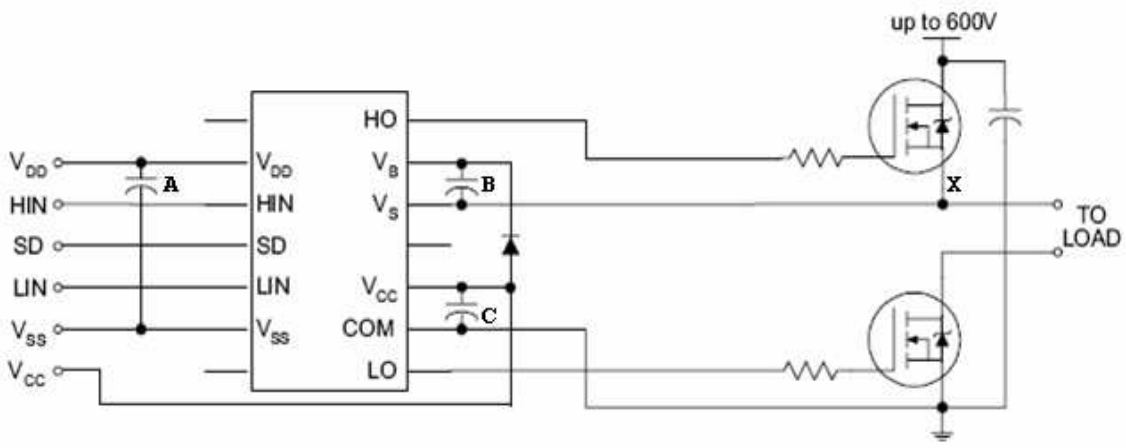


Figure 2.8 Wiring diagram of IR2112.

A is used to filter the power lines V_{DD} and V_{SS}, capacitors B and C are charged up by V_{CC} to establish the voltage potential to drive the external transistors. IR2112 is to be used under the condition that point X is lowered to ground as part of the converter operations, it is during this time, the high side capacitor B is charged up via the diode by V_{CC}. When the potential at point X raises again, the high side output is stepped up and sourced by capacitor B. The high and low side outputs, HO and LO, are sought to be in phase with the inputs, HIN and LIN respectively, with negligible delay, and peak-to-peak voltage equal to V_{CC}.

In order to calculate the minimum bootstrap capacitance for B that will maintain the voltage potential while point X fluctuates, the following equation is used [4].

$$C = 15 \times \frac{2\left[2Q_g + \frac{I_{qbs(max)}}{f} + Q_{ls} + \frac{I_{Cbs(leak)}}{f}\right]}{V_{CC} - V_f - V_{LS}} \tag{2.8}$$

where

Q_g = Gate charge of high side FET
$I_{Cbs(leak)}$ = Bootstrap capacitor leakage current
V_f = Forward voltage drop across the bootstrap diode
V_{LS} = Voltage drop across the low side FET or load
Q_{ls} = level shift charge required per cycle = $5nC$ ($500V/600V$ ICs)
f = frequency of operation
$I_{qbs(max)}$ = maximum quiescent current for high side circuitry

The various parameters described in Eq. 2.8 are: $Q_g = 65nC$ for IRF540 [5], $f = 60$ kHz since it requires a larger capacitor at lower frequency, $I_{Cbs(leak)} = 0A$ for non-electrolytic

capacitors, $I_{qbs(max)} = 60\mu A$ [3], $V_f = 0.7V$, $V_{LS} = 0V$ when low-side switch is on, and finally, $V_{CC} = 10V$. As a result, the minimum required bootstrap capacitance for B is $453nF$, so a $470nF$ capacitor is used. The resultant schematic for the design of the isolated gate driver is shown in Fig. 2.9.

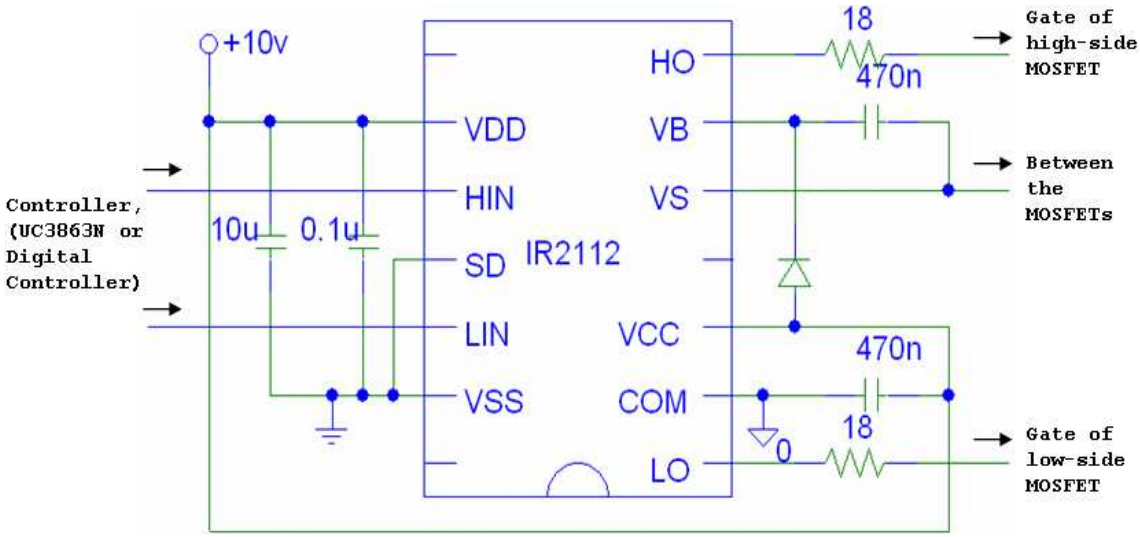


Figure 2.9 Schematic diagram of IR2112.

A $10V$ source is used to provide power to the IR2112 to prevent excess overshoot in the output switching signals, and is filtered by a combination of $0.1\mu F$ and $10\mu F$ capacitors. $470nF$ capacitors are the result of Eq. 2.8, and used as bootstrap the high-side switching signal. The pair of 18Ω resistors reduces switching speed, with a resultant decrease in overshoot to the switching signals.

2.2.3 Resonant Tank and Load Design

The SLR converter in Fig. 2.2 is designed to resonate at 60 kHz, and to deliver regulated $12V$dc to a resistive $100W$ load. Therefore, the maximum output current is $8A$, while a minimum current shall also be set to prevent the SLR converter from stopping as current ceases to flow. This minimum output current is set as $2A$, giving the resistive load range of 1.5Ω to 6Ω, which are established by different parallel combinations of 3.3Ω, 5.3Ω and 12Ω, shown in Fig. 2.10. The combination of BJTs and LEDs are used to indicate to the user of the SLR converter the status of the switches, in order to identify the equivalent load resistance at any given time. An output capacitor of $220\mu F$ is used to maintain the

dc level of the load voltage.

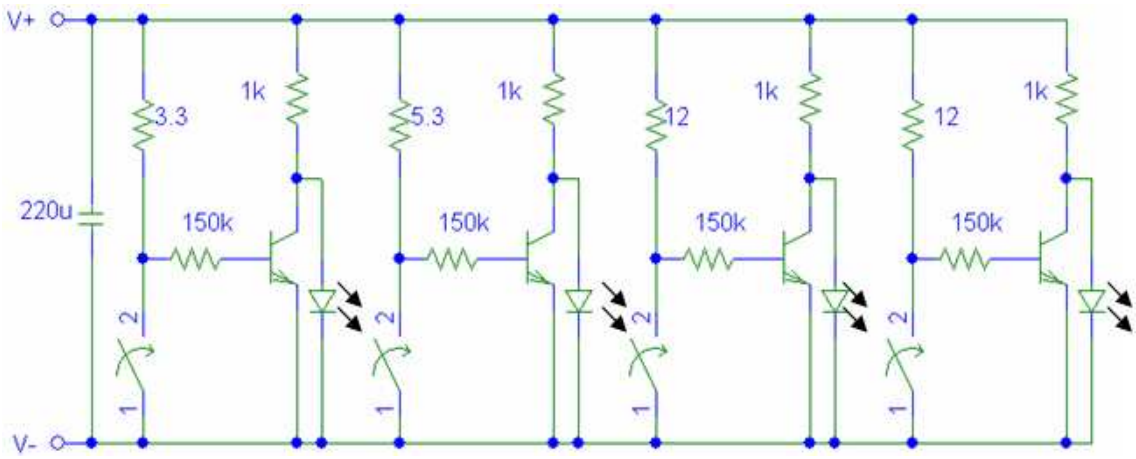


Figure 2.10 The array of load resistors, respective switches, the corresponding indicators and a smoothing capacitor.

The Q within the SLR converter is set to vary when R changes, with a minimum value of 2.5 when $R = 6\Omega$, because it is understood to be the minimum quality factor that produces near-sinusoidal currents [6]. Therefore, the upper limit of $Q = 10$ when $R = 1.5\Omega$. With the resonant frequency and the range of Q set, the inductor and capacitor values in the resonant tank are calculated to be $39.8\mu H$ and $177nF$ respectively, by Eq. 2.3. Actual component values as measured in circuit are $41.6\mu H$ and $180nF$. The upper frequency range for regulating the SLR converter can be set as the cutoff frequency or the half-power point of the LCR combination, which is when the impedance of the resonant tank is equal to the output resistance. This can be calculated by the equation below

$$\left| jn\omega_0 L + \frac{1}{jn\omega_0 C} \right| = R \tag{2.9}$$

where n is the factor that the half-power frequency is to the resonant frequency. After the calculations included in Appendix A, the following quadratic equation can be found

$$n^2 - R0.0667n - 1 = 0 \tag{2.10}$$

For $R = 6\Omega$, the lowest Q, $n \approx 1.22$; for $R = 1.5\Omega$, the highest Q, $n \approx 1.05$. Therefore, the half-power frequencies for lowest and highest Qs are around 73 kHz and 63 kHz respectively. So the operating range of 60 kHz to 80 kHz described in Section 2.2.1 is adequate to cover the bandwidth of the SLR converter specified by the LCR combinations.

2.2.4 Voltage Sensor

Unlike an isolated converter that has output transformers, the output of the proposed SLR converter is presented as a differential voltage, rather than a signal referenced to clean ground. Therefore a voltage measuring op-amp is used to produce a voltage signal that is referenced to ground for feedback control implementation.

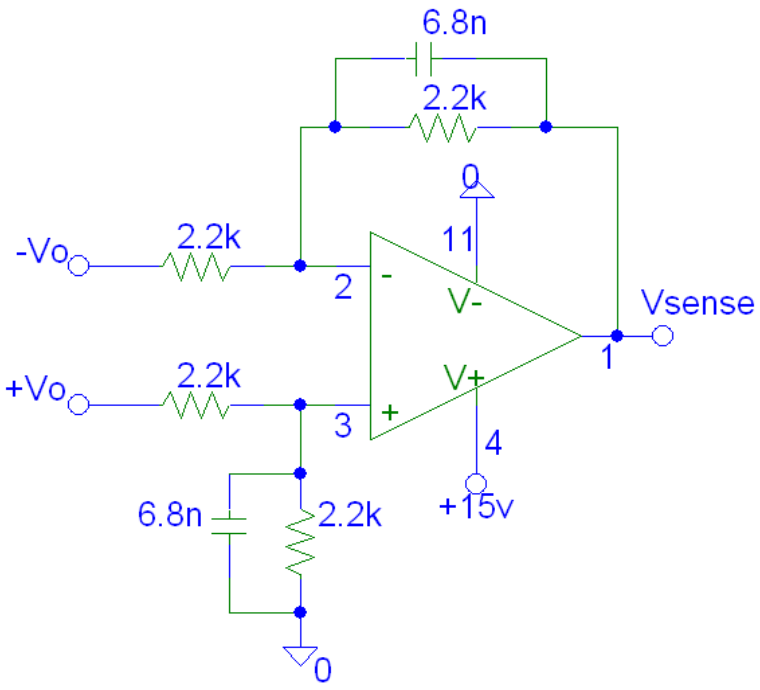


Figure 2.11 A unity-gain inverting operational amplifier used to measure differential voltage.

The op-amp shown in Fig. 2.11 is implemented in a unity-gain inverter with bandwidth limited by the filtering capacitors. The transfer function of the measuring device is calculated by the Eq. 2.11, and the bode plot is shown in Fig. 2.12.

$$T_S(s) = \frac{1}{1 + sRC} = \frac{1}{1.496 \times 10^{-5}s + 1} \tag{2.11}$$

From Fig. 2.12, the cutoff frequency of the measuring amplifier is $\approx$ 10.6 kHz, 1/6 of the resonant frequency of the circuit. The phase shift incurred at high frequencies shall be taken into account in the small-signal analysis in Section 3.2.

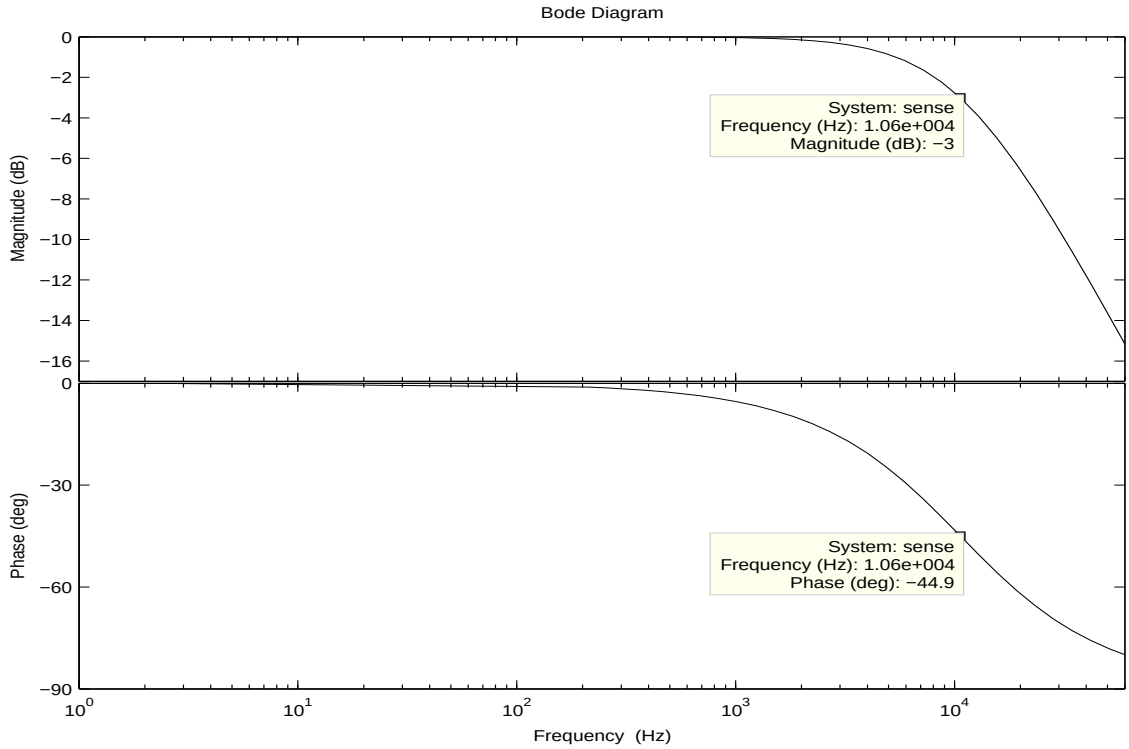
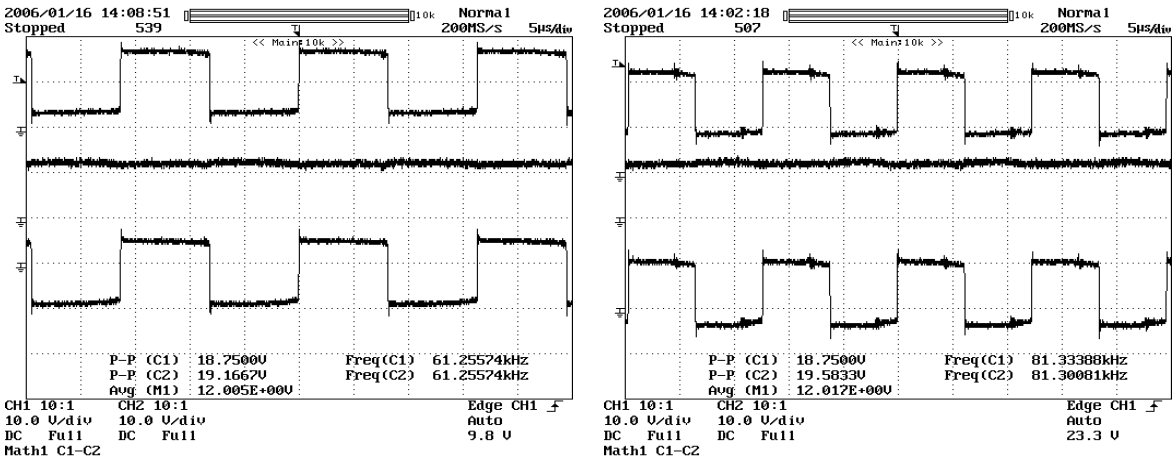


Figure 2.12 Bode plot of the voltage sensor.

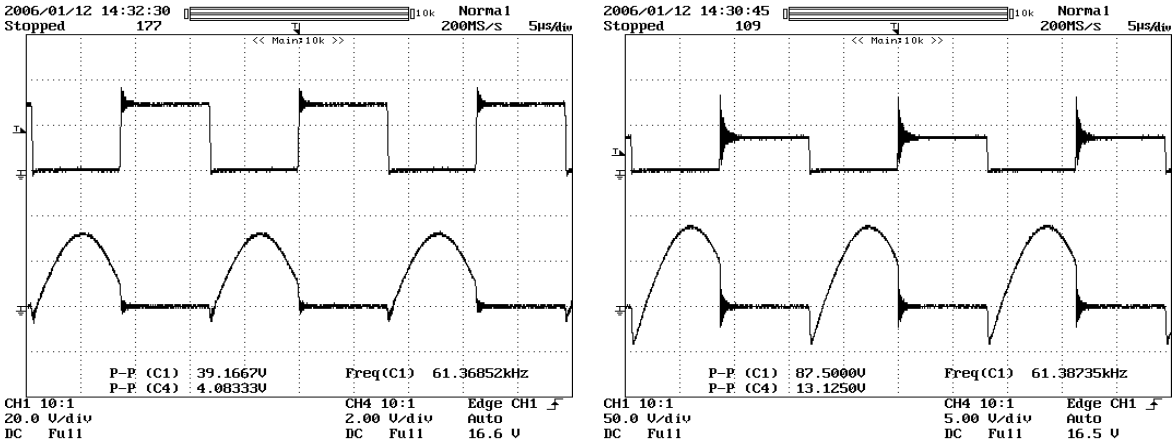
2.3 OPERATING WAVEFORMS

In this section, various operating voltage/current waveforms are recorded for the proposed OL SLR converter.



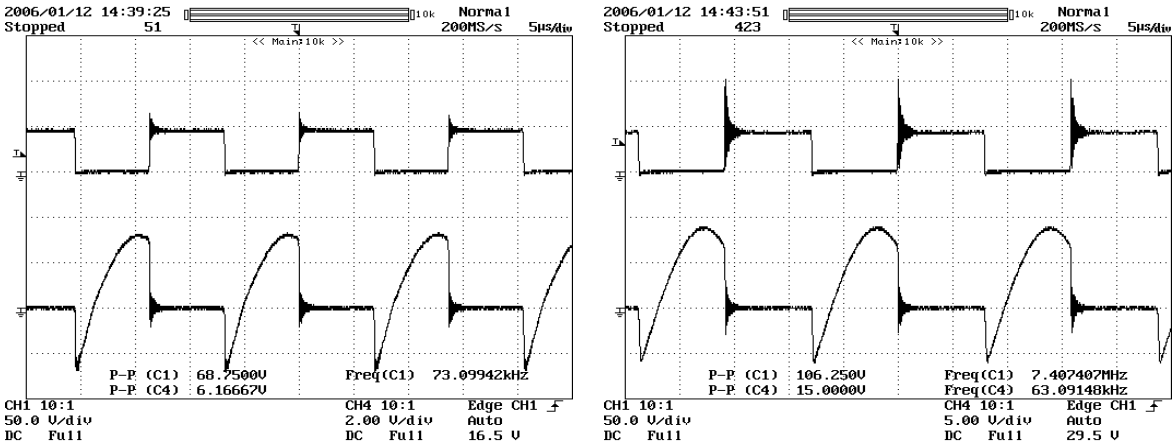
(a) (b)

Figure 2.13 Top trace: +Vo, bottom trace: -Vo, middle trace: differential output; for 6Ω load at (a) minimum frequency and (b) maximum frequency.



(a) (b)

Figure 2.14 Top trace: voltage across MOSFET, bottom trace: current in MOSFET; for (a) 6Ω load and (b) 1.5Ω load near resonance.



(a) (b)

Figure 2.15 Top trace: voltage across MOSFET, bottom trace: current in MOSFET; for (a) 6Ω load and (b) 1.5Ω load at cutoff frequency.

It is by inspection of the waveforms in Figs. 2.13, 2.14, 2.15, the resultant waveforms from the designed SLR converter show similarities to the waveforms produced by the simulated SLR converter in Fig. 2.3. The SLR converter is able to produce $12V$dc at the output, with higher current flowing through the MOSFETs when R is low. When the SLR converter is operating near resonance, the switches are operated in both ZVS and ZCS. As the switching frequency moves away from resonance, only ZVS is performed. The difference between the above waveforms and Fig. 2.3 is that the diode current forms the negative part of the switch current, since the clamping action is done by the body diode of each MOSFET.

2.4 LAYOUT OF PROPOSED CONVERTER

The photograph of the actual SLR converter built is shown in Fig. 2.16. The resonant components are hidden underneath the rectifying diodes, and the inductor is wound on an RM core. Also included is the digital implementation of the compensator done using an F2812 eZdsp Starter Kit from Spectrum Digital Incorporated, which will be discussed later in Chapter 5. The complete specifications of the analogue SLR converter is included in Section 3.5, where feedback control is implemented.

2.5 SUMMARY

A brief background theory about using resonant components to reduce switching losses by ZVS and ZCS techniques has been reviewed in this chapter. As a result, an OL frequency controlled SLR converter driven by an analogue controller chip, UC3863N, and including an isolation MOSFET driver, IR2112, has been built with a variable resistive load that draws up to $8A$ from a proposed $12V$dc output.

The resonant frequency of the SLR converter is designed to be as close to 60 kHz as the actual component values allow, while the controller is able to regulate the converter from 62 kHz to 82 kHz. The differential output across the load is not referenced to ground, therefore a voltage measuring sensor in the form of a unity-gain inverting amplifier is designed. Low pass filters in the form of RC combinations provide a cutoff frequency of ≈ 10 kHz are used to reduce noise caused by switching transitions. Magnitude and phase shifts of the low pass filters are to be considered as part of the SLR converter frequency

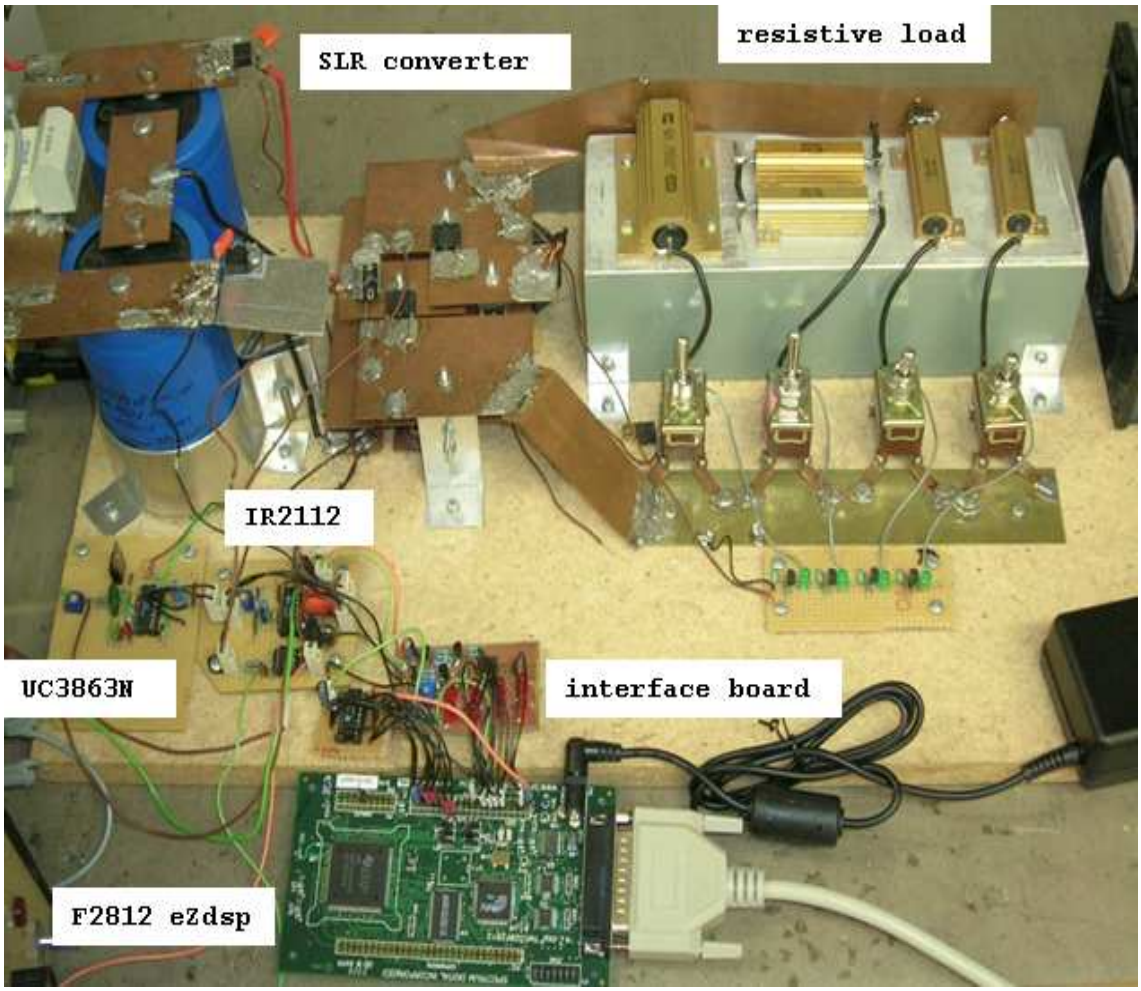


Figure 2.16 Photograph of the constructed SLR converter.

response, when compensation is to be designed for feedback control, which is described later in Section 3.2.

A series of voltage/current waveforms have been provided as proof of proper operation of the analogue OL SLR converter. It is shown that as the SLR converter operates near resonance, the switches are able to perform both ZVS and ZCS. As the switching frequency is increased, only ZVS is possible due to the clamping effect of the body diode of the MOSFETs.

Chapter 3

ANALOGUE CONTROL STRATEGY

This chapter describes the necessary steps towards designing a stable control loop for the SLR converter constructed in Chapter 2. These steps include the small-signal analyses of the SLR converter at various operating conditions, then a feedback compensator is designed that provides stability under all the operating conditions. The specifications of the analogue SLR converter are described at the end of this chapter.

3.1 FEEDBACK CONTROL BASICS

In order to obtain a stabilised and regulated output for the converter, a feedback controller is a convenient way of getting there.

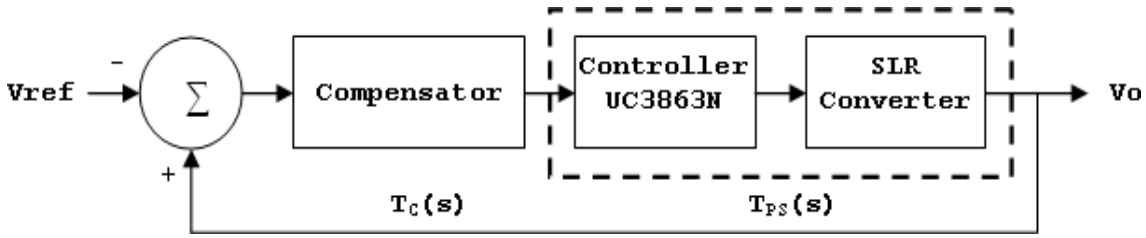


Figure 3.1 Feedback control block diagram for the SLR converter.

The uncompensated SLR converter, in dashed box, in Fig. 3.1 requires a feedback loop to regulate the output in the presence of perturbations, which makes a compensator indispensable to achieve both stability and/or improved performance in the overall closed-loop (CL) system. Since the SLR converter is operating above resonance, the negative feedback action is, in fact, implemented by subtracting the reference from the feedback voltage, as shown above.

The stability of a system is indicated by two parameters, gain margin (GM), and phase margin (PM). GM and PM are defined by [7] as

> "The gain margin is the amount of gain increase required to make the loop gain unity at the frequency where the phase angle is $-180°$."
> "The phase margin is the difference between the phase of the response and $-180°$ when the loop gain is 1.0."

In order to achieve stability, an OL system must have both positive GM and PM. The general idea behind building an adequate compensator is to correct the uncompensated OL system that otherwise has either negative GM or negative PM, or both.

Therefore, compensators usually perform jobs such as improving GM by reducing gain at the predetermined 0 dB crossover frequency, and improving PM with phase boost, by adding poles and zeros in the frequency domain. With adequate GM and PM in OL, the system is certain to be stable in CL.

3.2 SMALL-SIGNAL ANALYSIS OF SLR CONVERTER

In a system where only slow variables exist, like most constant frequency converters, average state-space analysis can be used with resonant voltage/current as state variables. But in a frequency regulated converter like the SLR converter, the resonant variables change quickly with respect to any change in frequency, therefore, it is common to use extended describing functions (EDF) [8], with the drawback of having complex and higher order models.

Another method documented in [9] is to use average analysis with magnitude/phase of the resonant voltage as the designated state variables. This method assumes the resonant voltage/current are always sinusoidal, therefore, it does not give an accurate account of the SLR converter when the voltage/current are distorted as a result of $\omega_s \neq \omega_0$.

It is the interest of this research to approximate the transfer function of the SLR converter, using [10], which is both straightforward and effective. The control-to-output frequency response of an SLR converter is said to resemble a single pole at low frequencies, and

a quadratic at higher frequencies. Therefore, the linearized control-to-output transfer function is described by the following equation

$$T_{PS}(s) = \frac{\hat{x}(s)}{\hat{f}(s)} = \frac{A}{\left(1 + \frac{s}{\omega_{fs}}\right)\left(1 + \frac{s}{\omega_{0s}Q_{0s}} + \frac{s^2}{\omega_{0s}^2}\right)} \tag{3.1}$$

Where A is the low frequency gain and ω_{fs} is the low frequency pole. The high frequency quadratic is determined by ω_{0s} and Q_{0s}.

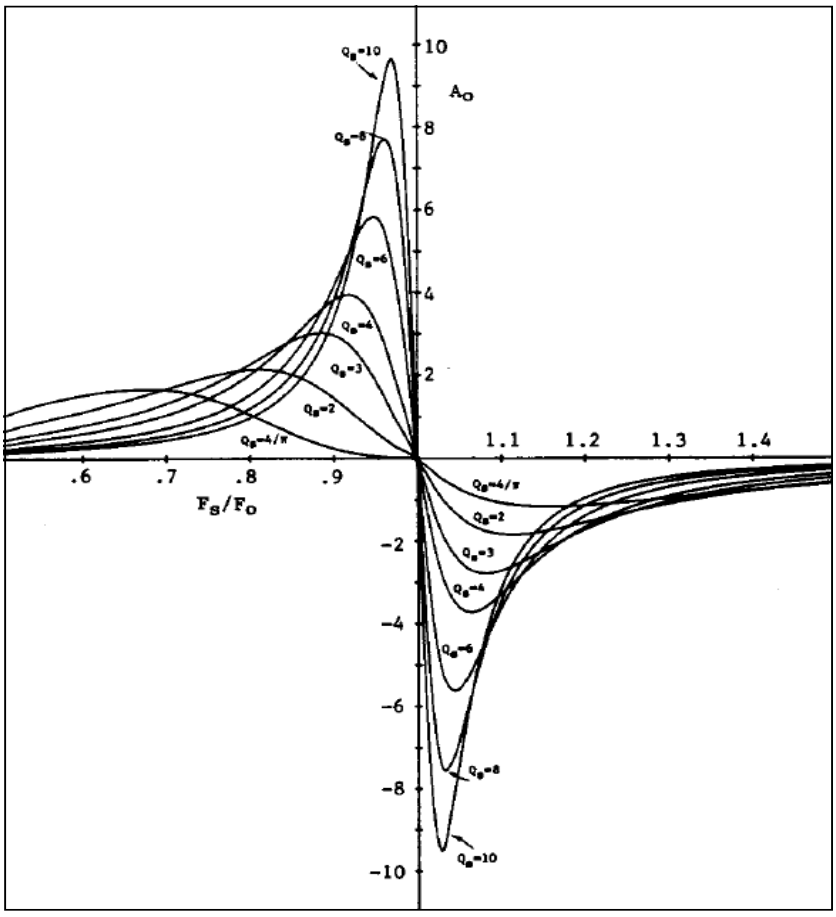


Figure 3.2 Slope of conversion ratio characteristics of SLR converter in continuous conduction mode.

The low frequency gain, A, is proportional to the slope of the conversion ratio characteristic A_0 described by

$$A = A_0 \frac{V_d}{F_0} \tag{3.2}$$

The quantity A_0 is dependent on the voltage presented across each switch, V_d, and the ratio of switching frequency, F_s, to resonant frequency, F_0, shown in Fig. 3.2 [11]. There is a different set of values for A_0 for a different quality factor, Q_s, in the circuit.

The low frequency pole, ω_{fs}, is dependent on the load, R, and the output capacitor, C_f, described by

$$\omega_{fs} = \frac{\kappa}{RC_f} \tag{3.3}$$

The factor κ in turn is given by

$$\kappa = 1 + \frac{1}{\left(Q_s \frac{\gamma}{2} \cot \frac{\gamma}{2}\right)^2 \left(1 - \frac{2}{\gamma M Q_s}\right)} \tag{3.4}$$

$$Q_s = \text{quality factor of the circuit, } M = \text{conversion ratio} = \frac{V_o}{V_d}, \gamma = \pi \frac{F_0}{F_s}$$

The parameters that define the high frequency quadratic nature of the transfer function, ω_{0s} and Q_{0s}, are given by

$$\omega_{0s} = \omega_s - \omega_0 \tag{3.5}$$

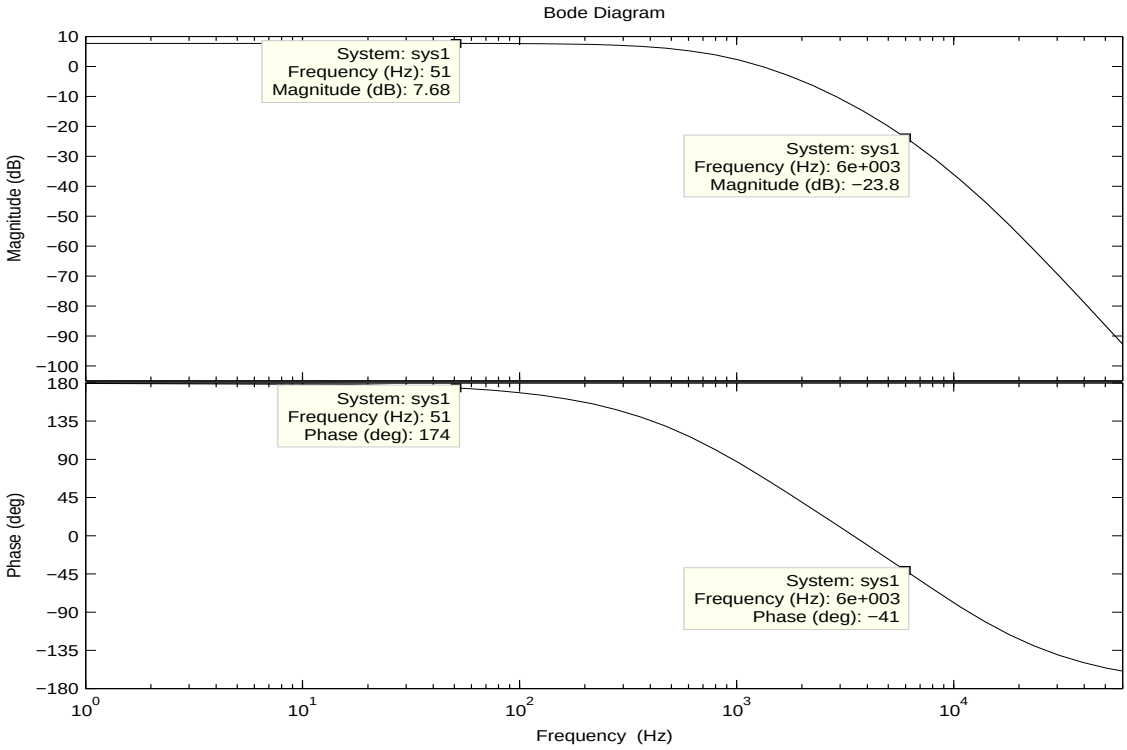
$$Q_{0s} = \frac{Q_s}{\kappa} \tag{3.6}$$

Substituting Eqs. 3.2–3.6 into Eq. 3.1, a control-to-output transfer function can be deduced for each different set of operating conditions that produce the desired output of $V_o = 12V$. The four boundary operating conditions are categorized by the upper and lower bounds of Q_s, the switching frequency range and the power supply available. Four operating conditions and the respective transfer functions are shown in Table 3.1.

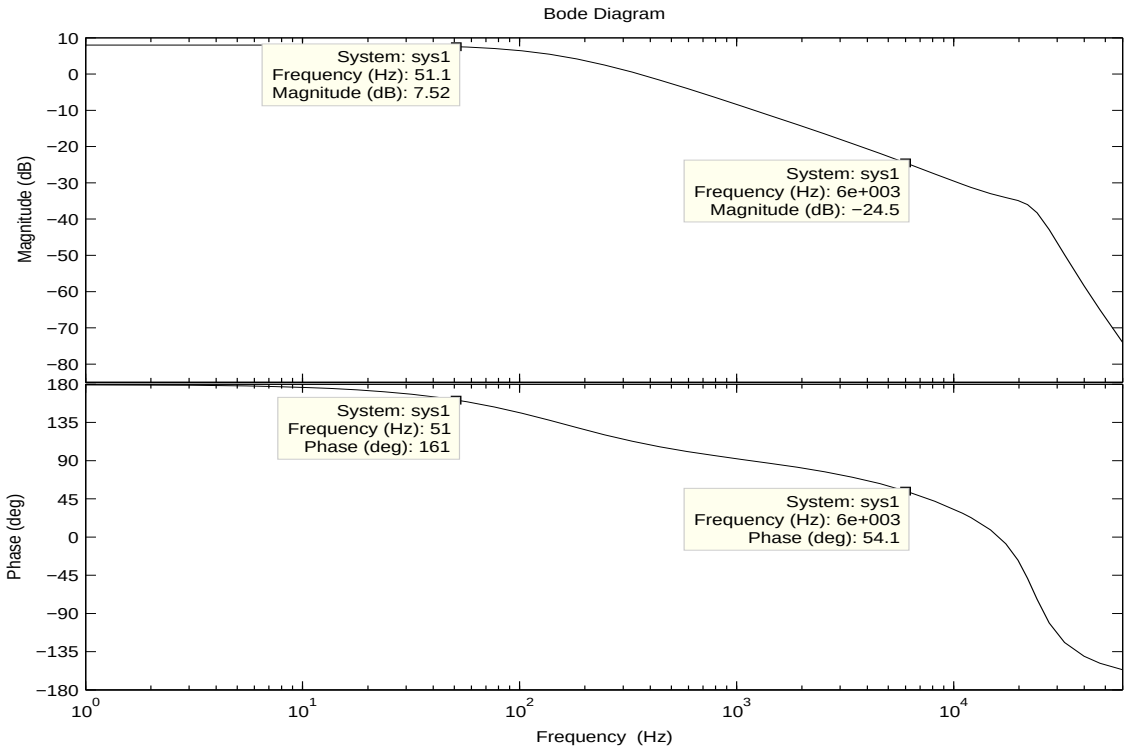
Table 3.1 Four steady-state operating conditions of an SLR converter.

	$\mathbf{Q_s}$	$\mathbf{F_s}$	$\mathbf{2V_d}$	$\mathbf{A_0}$	**Transfer Function, $\mathbf{T_{PS}(s) \times T_S(s)}$**
A	2.5	62 kHz	$29.13V$	-2	$\frac{-2.427}{3.388\times10^{-13}s^3+2.318\times10^{-8}s^2+0.000307s+1} \times \frac{1}{1.496\times10^{-5}s+1}$
B	2.5	81.6 kHz	$60.2V$	-1	$\frac{-2.508}{4.745\times10^{-14}s^3+3.579\times10^{-9}s^2+0.001034s+1} \times \frac{1}{1.496\times10^{-5}s+1}$
C	10	62 kHz	$46.6V$	-9	$\frac{-17.48}{3.974\times10^{-13}s^3+3.043\times10^{-9}s^2+0.0002394s+1} \times \frac{1}{1.496\times10^{-5}s+1}$
D	10	64 kHz	$62.3V$	-4	$\frac{-10.38}{2.041\times10^{-13}s^3+1.622\times10^{-9}s^2+0.0002798s+1} \times \frac{1}{1.496\times10^{-5}s+1}$

The Bode plots of the four steady-state operating conditions, taking into account the voltage sensor frequency response, $T_S(s)$, in Section 2.2.4, are plotted from DC to 60 kHz in Figs. 3.3 and 3.4. It seems both Q_s and F_s dictate the shape of the Bode plots. The effects of high frequency quadratic become greater when Q_s is high, while the higher F_s is, the higher frequency the quadratic is located.

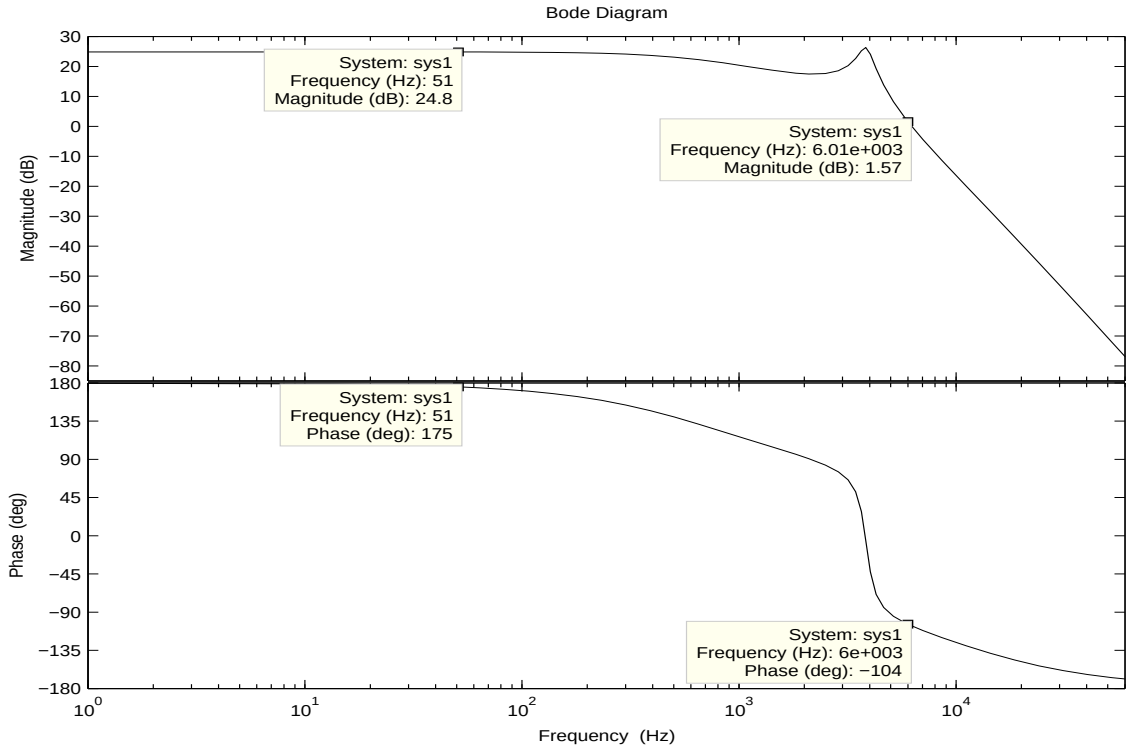


(a)

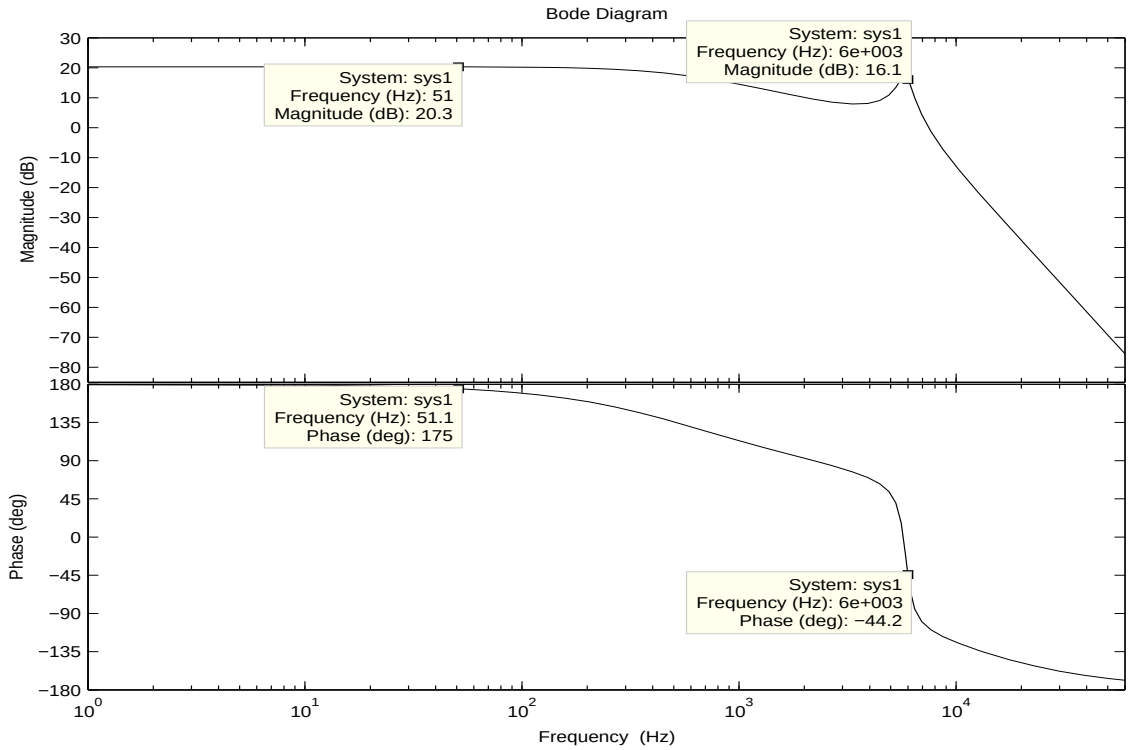


(b)

Figure 3.3 Frequency response of $Q_s = 2.5$ operating at (a) 62 kHz, and (b) 81.6 kHz.



(c)



(d)

Figure 3.4 Frequency response of $Q_s = 10$ operating at (c) 62 kHz, and (d) 64 kHz.

The frequency of interest is 6 kHz, because it is 1/10 of the resonant frequency, a good bandwidth for feedback compensation [12]. The magnitude and phase at 51 Hz is also noted since it is the lowest frequency available of the measuring apparatus. Another important thing to note from the Bode plots is that the low frequency phase of the systems start at approximately 180° and ends at approximately −90° at high frequencies. This is due to the fact that while the SLR converter is running above resonance, it has the advantage of requiring minimal control effort due to adequate gain and phase margin, and can to be controlled with a first-order compensator like an integrator.

3.2.1 Measured Frequency Response of SLR Converter

In order to make sure the simulated results in Figs. 3.3 and 3.4 are fit for further feedback analysis, it is important to compare the approximated ideal transfer function to the actual measured transfer functions. The measuring device of choice is an *HP35665A Dynamic Signal Analyzer*, that does a sinusoidal sweep from 51.2 Hz to 51.2 kHz, connected to an *HP7470A Plotter* for printing outputs. The equipment setup for testing the frequency response of uncompensated SLR converter is shown in Fig. 3.5.

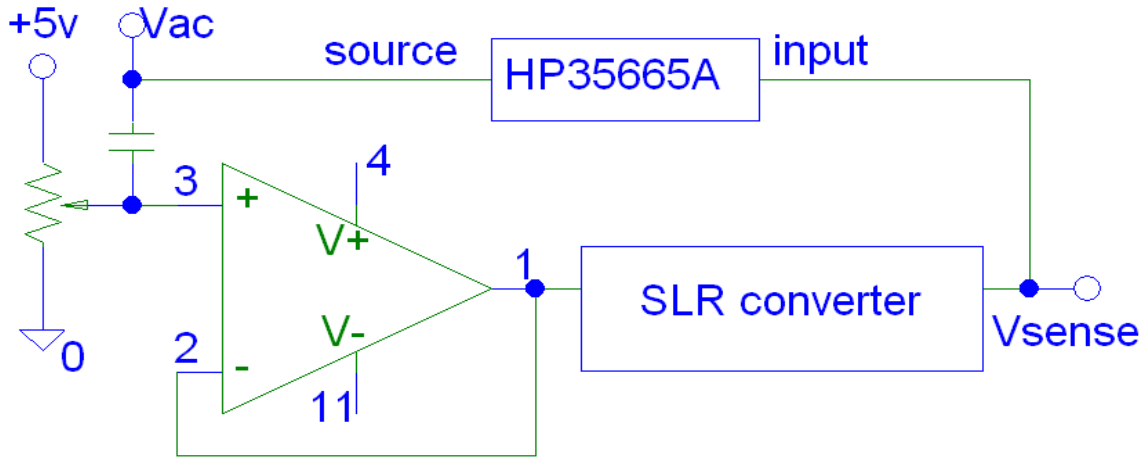
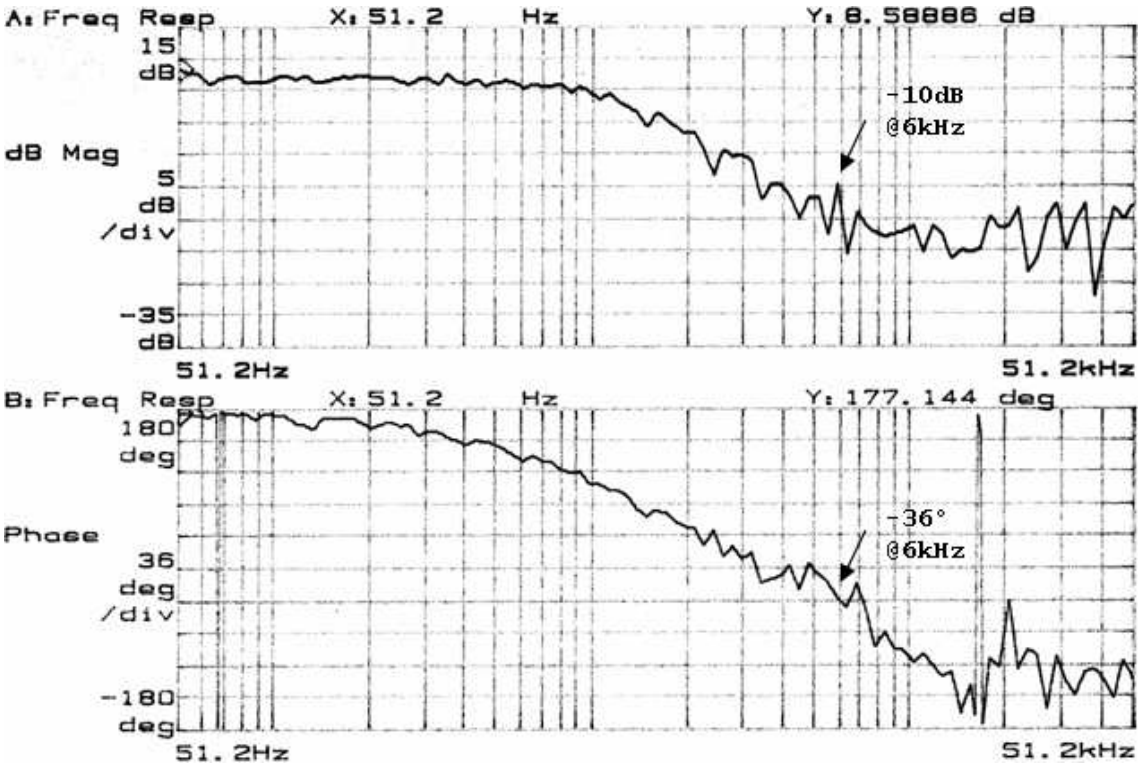
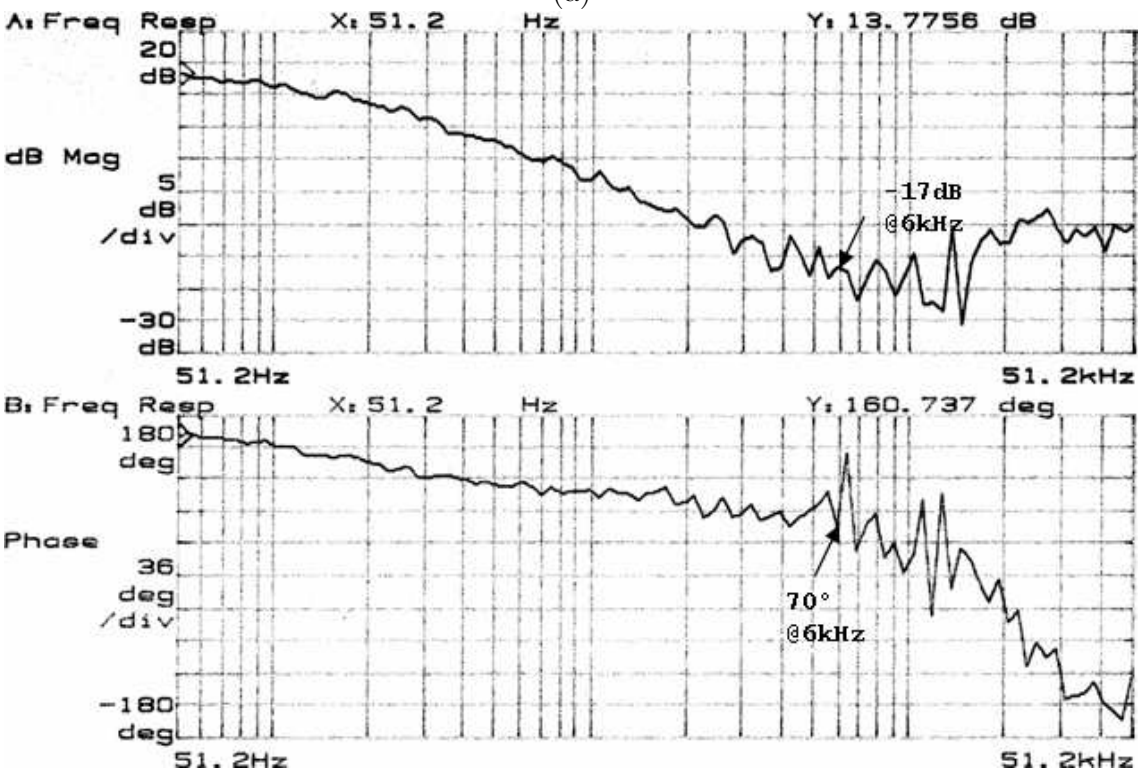


Figure 3.5 Experimental setup for measuring frequency response of the uncompensated response.

The *HP35665A* sends a frequency varying small perturbation, $V_{ac} \approx 5mVrms$, that couples into the error amplifier of UC3863N, in voltage follower configuration, via a capacitor. The resultant change in output is measured from the output of the voltage sensor at V_{sense}. The transfer functions are measured for different operating conditions, shown in Table 3.1. The acquired Bode plots as plotted by *HP7470A* are shown in Figs. 3.6 and 3.7. The magnitude and phase at the crossover frenquency, 6 kHz, is labeled for each graph.

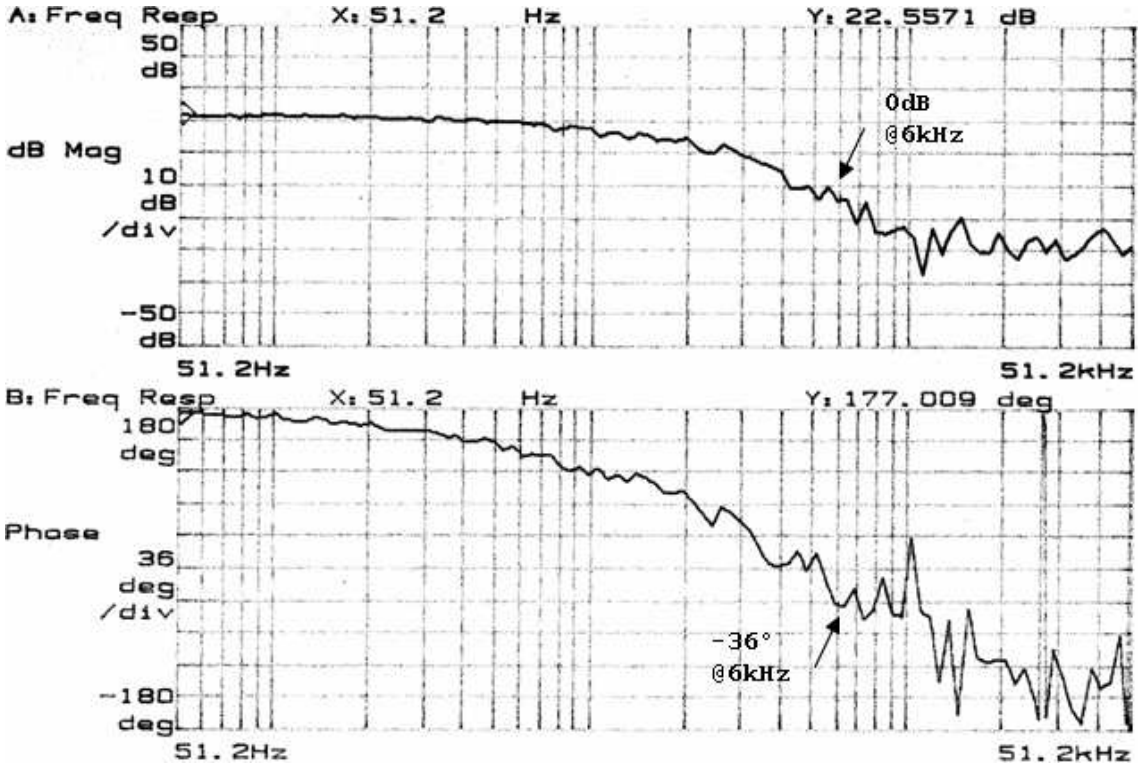


(a)



(b)

Figure 3.6 Measured frequency response of $Q_s = 2.5$ operating at (a) 62 kHz, and (b) 81.6 kHz.



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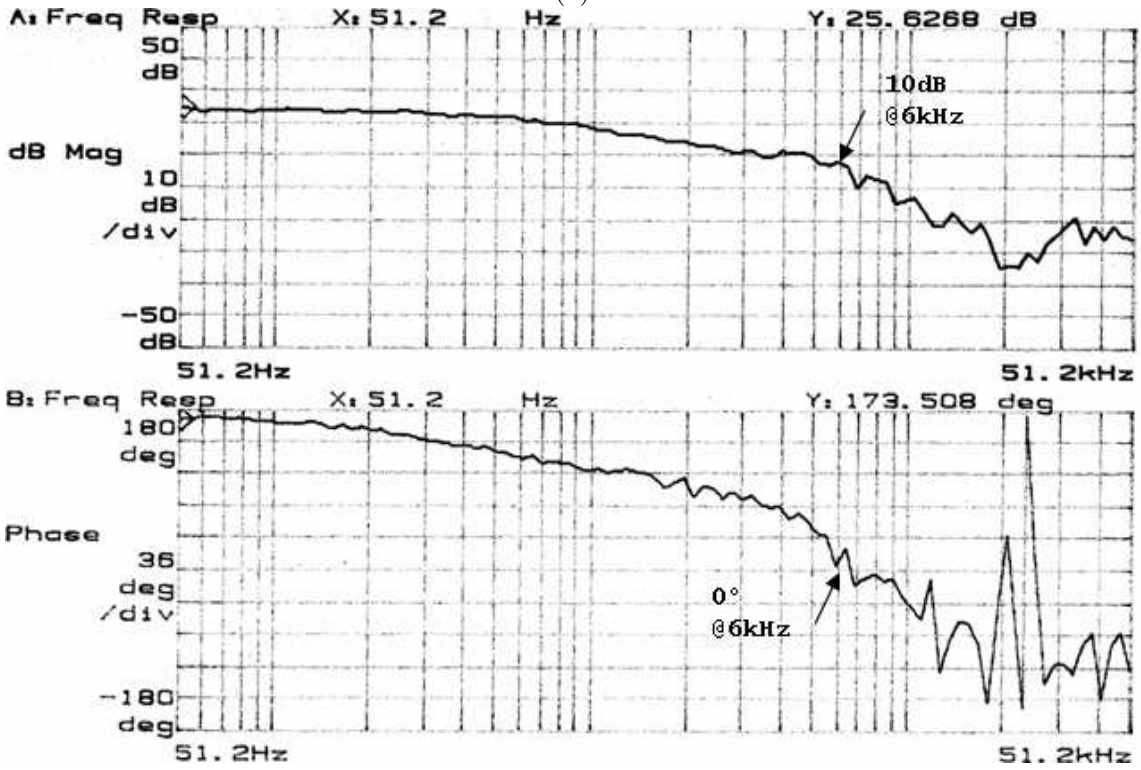


(d)

Figure 3.7 Measured frequency response of $Q_s = 10$ operating at (c) 62 kHz, and (d) 64 kHz.

By comparing Figs. 3.3 to 3.7, it is by inspection that both simulated and measured Bode plots follow similar shapes from DC to 51.2 kHz. The measured Bode plots become fairly noisy beyond 6 kHz, due to distortions such as measurement noise, but the high frequency trends are still similar to the simulated Bode plots. A brief summary of the comparisons between the simulated and measured transfer functions are shown in Table 3.2.

Table 3.2 Comparisons of simulated and measured transfer functions at various frequencies.

		Magnitude		**Phase**	
		@51.2 Hz	@6 kHz	@51.2 Hz	@6 kHz
A	simulated	7.68 dB	-23.8 dB	174°	−41°
	measured	8.59 dB	-10 dB	177°	−36°
B	simulated	7.52 dB	-24.5 dB	161°	54.1°
	measured	13.8 dB	-17 dB	161°	70°
C	simulated	24.8 dB	1.57 dB	175°	−104°
	measured	22.6 dB	0 dB	177°	−36°
D	simulated	20.3 dB	16.1 dB	175°	−44.2°
	measured	25.6 dB	10 dB	174°	0°

Overall, the magnitudes at various frequencies of interest are quite comparable between the simulated and measured Bode plots, while the phase of the Bode plots match very well when Q_s is low, but have fairly distant values at 6 kHz for maximum Q_s. These differences may be caused by errors in measurements due to the additional EMI generated when the SLR converter does not have proper ZCS and ZVS operations at high frequencies, especially more evident when Q_s is high.

3.3 COMPENSATOR DESIGN

The proposed compensation design method is the *K Factor Design Method* described in [12]. This method starts by selecting a desired 0 dB crossover frequency, which is typically around 1/10 of the switching frequency. For the interest of this research, 6 kHz is selected as the 0 dB crossover frequency.

The attenuation required in the compensator to give 0 dB at 6 kHz is found by the reciprocal of the system magnitude at 6 kHz,

$$G = \frac{1}{\left|T_{PS}(6\text{ kHz})\right|} \tag{3.7}$$

From Table 3.2, the greatest measured magnitude, $\left|T_{PS}(6\text{ kHz})\right| = 10$ dB, is in case D. Therefore the required attenuation is, $G = \frac{1}{3.16}$.

Then the required phase boost is calculated by subtracting the phase of system at 6 kHz, $\angle T_{PS}(6\text{ kHz})$, from the desired phase margin, $PM_{desired}$. The non-inverting compensator required in an SLR converter running above resonance does not introduce a phase shift at high frequencies.

$$Boost = PM_{desired} - \angle T_{PS}(6\text{ kHz}) - 180^\circ \tag{3.8}$$

A typical phase margin in a compensated system is 45°, therefore, using the worst measured $\angle T_{PS}(6\text{ kHz})$ shown in Table 3.2 of -36°, the resultant phase boost is -99°. Since the required phase boost is $< 0^\circ$, a TYPE I compensator can be used, which is a simple integrator consisting of only one resistor, R_1, and one capacitor, C_1.

The value of R_1 is set as $1k\Omega$, such that it is of similar magnitude to the output impedance of the voltage sensor described in Section 2.2.4. Then C_1 is calculated using the attenuation found in eq. 3.7 and the 0 dB crossover frequency, f.

$$C_1 = \frac{1}{2\pi f G R_1} \tag{3.9}$$

The resultant $C_1 = 83.9nF$ is rounded off to the standard value of $100nF$. The integral compensation is implemented using the internal error amplifier of UC3863N controller, shown in Fig. 3.8. The $5k\Omega$ potentiometer, $10k\Omega$ and $2k2\Omega$ resistors are matched to scale the measured voltage as well as matching the input impedances of the error amplifier.

The transfer function of the integral compensation is calculated as

$$T_C(s) = 1 + \frac{1}{sR_1C_1} = \frac{0.0001s + 1}{0.0001s} \tag{3.10}$$

As a result, the simulated frequency response of the non-inverting integrator is shown in Fig. 3.9. The non-inverting integrator produces high gain and phase shift at low frequencies, plus no gain and no phase shift beyond the predetermined bandwidth.

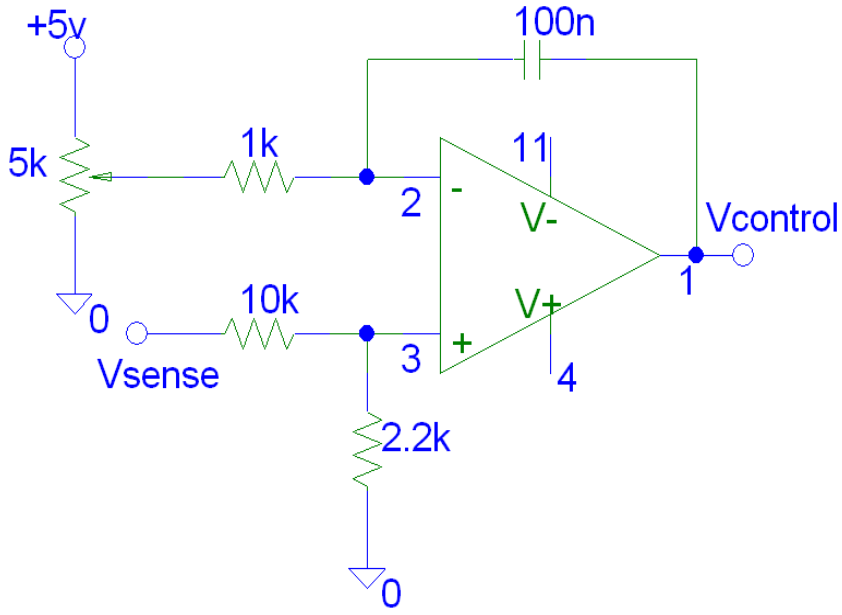


Figure 3.8 Schematic of the integral compensation.

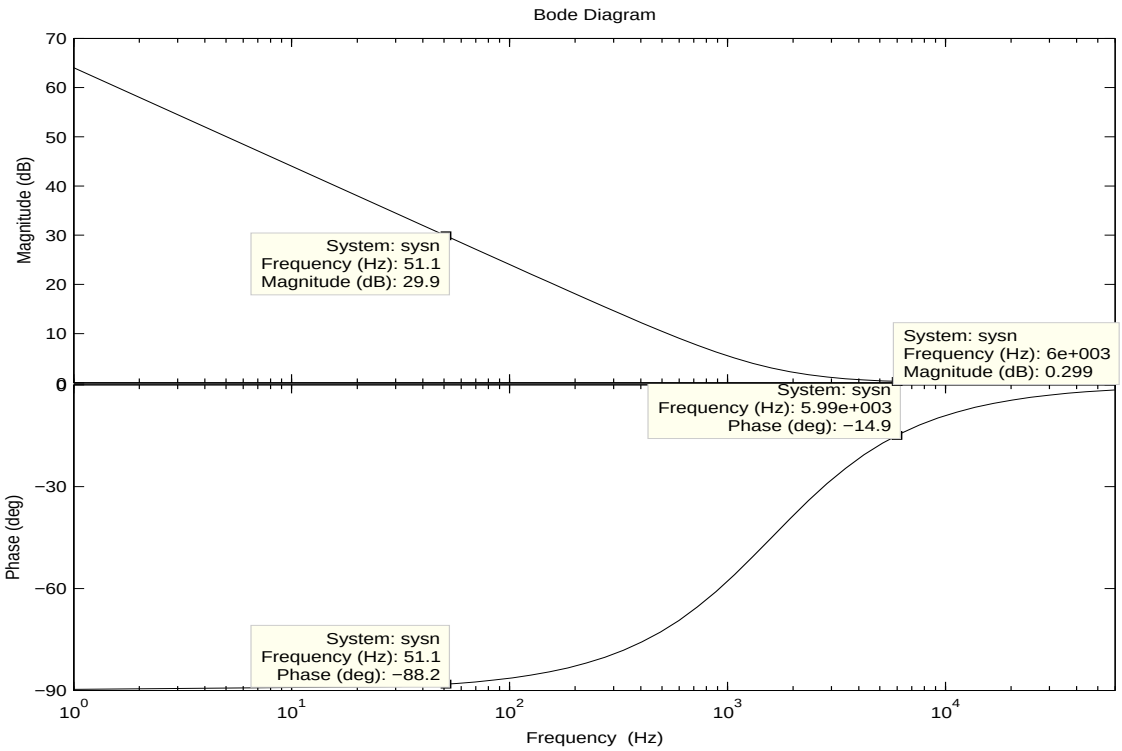


Figure 3.9 Bode plot of the non-inverting integral compensator with 6 kHz bandwidth.

3.4 ANALYSIS OF COMPENSATED SLR CONVERTER

Given the frequency responses investigated in Sections 3.2 and 3.3, the new OL transfer function is characterised by the product of both the SLR transfer function and the compensator transfer function.

$$H(s) = T_C(s) \times T_{PS}(s) \times T_S(s) \tag{3.11}$$

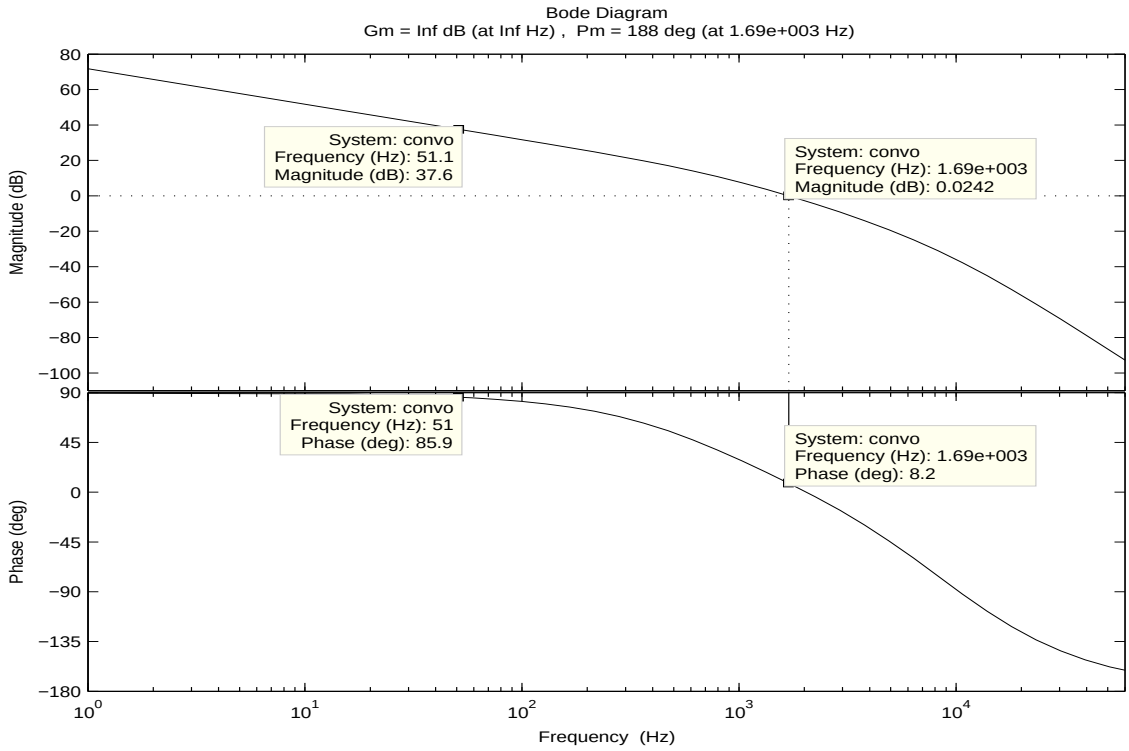
The resultant Bode plots of the new OL systems are simulated for each operating condition in Table 3.1, and illustrated in Figs. 3.10 and 3.11. The GM and PM of each Bode plot are also noted. The major difference between the compensated systems and their respective uncompensated versions, in Figs. 3.3 and 3.4, is the major boost in low frequency gain caused by the integrator, while the high frequency characteristics remain unchanged.

It is shown that all the new systems have infinite GM, because the phase of the new system never reaches $-180°$ within the frequency range of DC to 60 kHz. The PM for each system is positive, therefore, it is certain that the CL SLR converter will be stable for each set of different operating states. Although the compensator is designed to have a bandwidth of 6 kHz, according to Section 3.3, the proposed non-inverting integrator has minimum gain of 1, therefore, it does not provide attenuation at 6 kHz, and the bandwidth of the new system is the same as that of the uncompensated system described in Section 3.2.

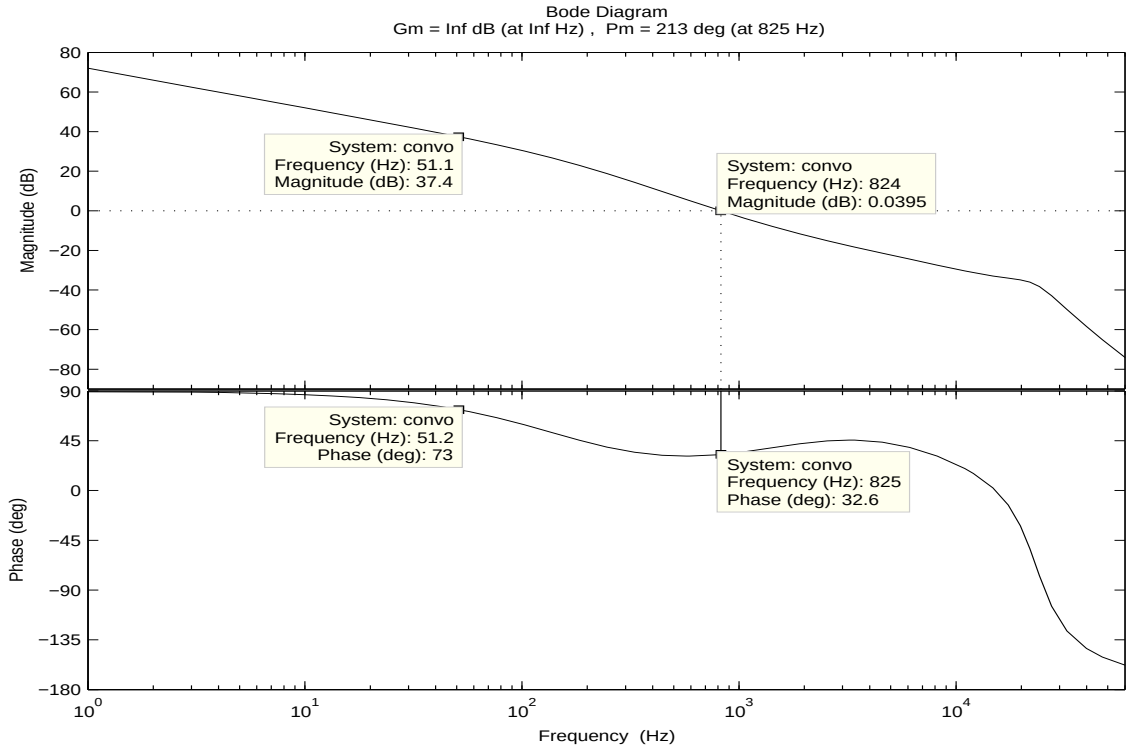
The MATLAB codes used in the modelling of transfer functions are included in Appendix B.

3.4.1 Measured Frequency Response of Compensated SLR

Following the simulations in Section 3.4, it is predicted that integral compensation is sufficient to provide adequate GM and PM for the SLR converter to achieve stability in CL. The integrating function also improves system gain at low frequencies, eliminating steady-state error.

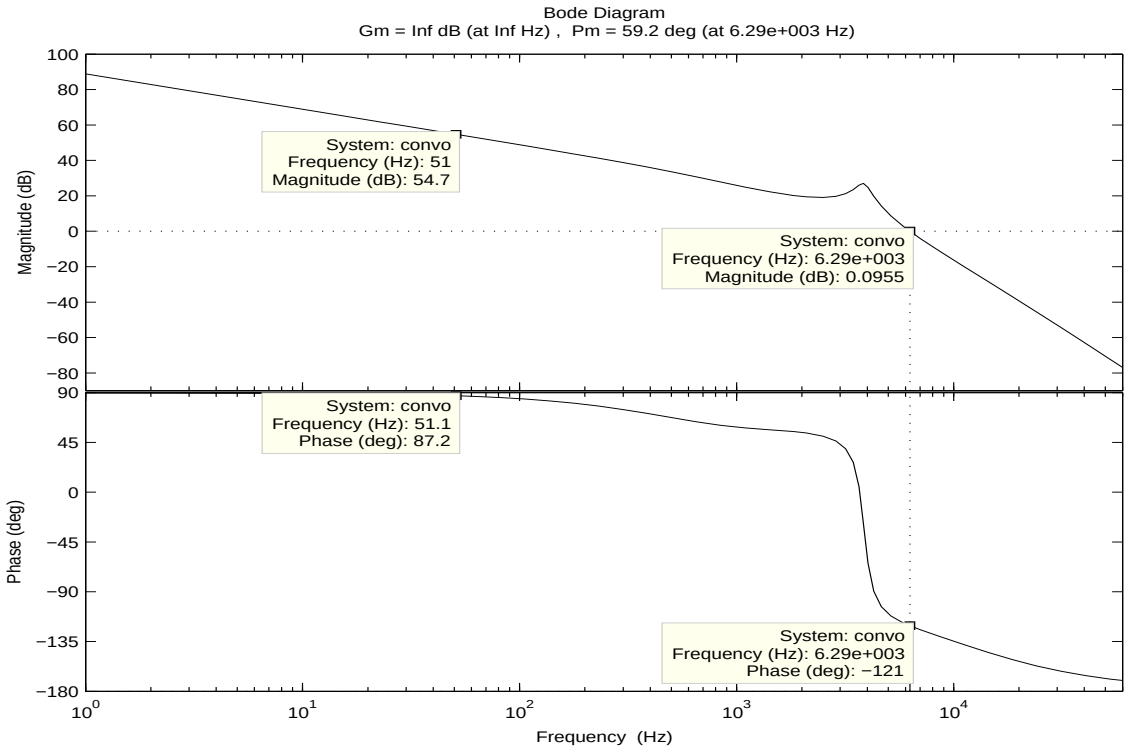


(a)



(b)

Figure 3.10 Simulated frequency response of the compensated SLR converter with $Q_s = 2.5$ operating at (a) 62 kHz, and (b) 81.6 kHz.



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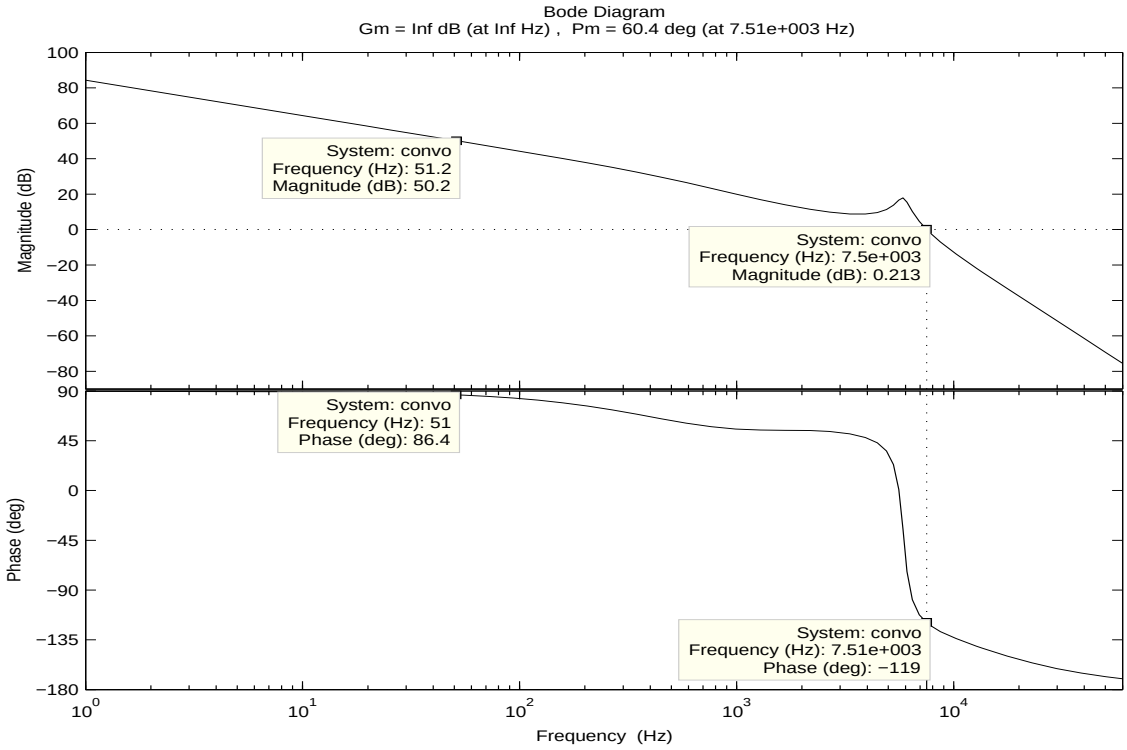


(d)

Figure 3.11 Simulated frequency response of the compensated SLR converter with $Q_s = 10$ operating at (c) 62 kHz, and (d) 64 kHz.

Fig. 3.12 shows the perturbation, V_{ac}, produced by *HP35665A* to perform the sinusoidal sweep is in the form of $\approx 20mVrms$, is fed into the positive terminal of the compensator via a capacitor. Referring to the control block diagram in Fig. 3.1, even though the circuit is in CL configuration, but since the negative terminal of the summation node is constant, the variation in the positive terminal can be assumed to be identical to the variation to the result after the summation node. Therefore, the apparatus setup is, in fact, measuring the OL frequency response of the compensated system.

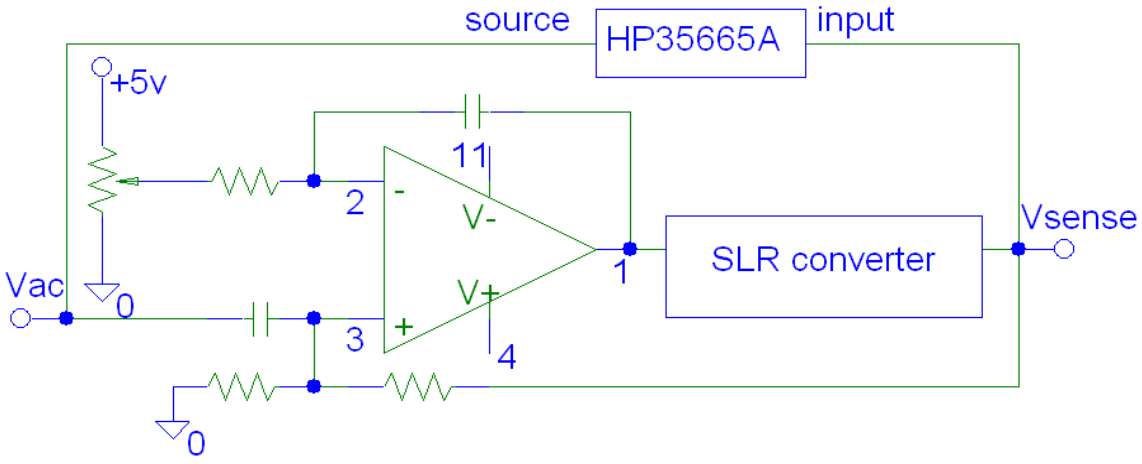
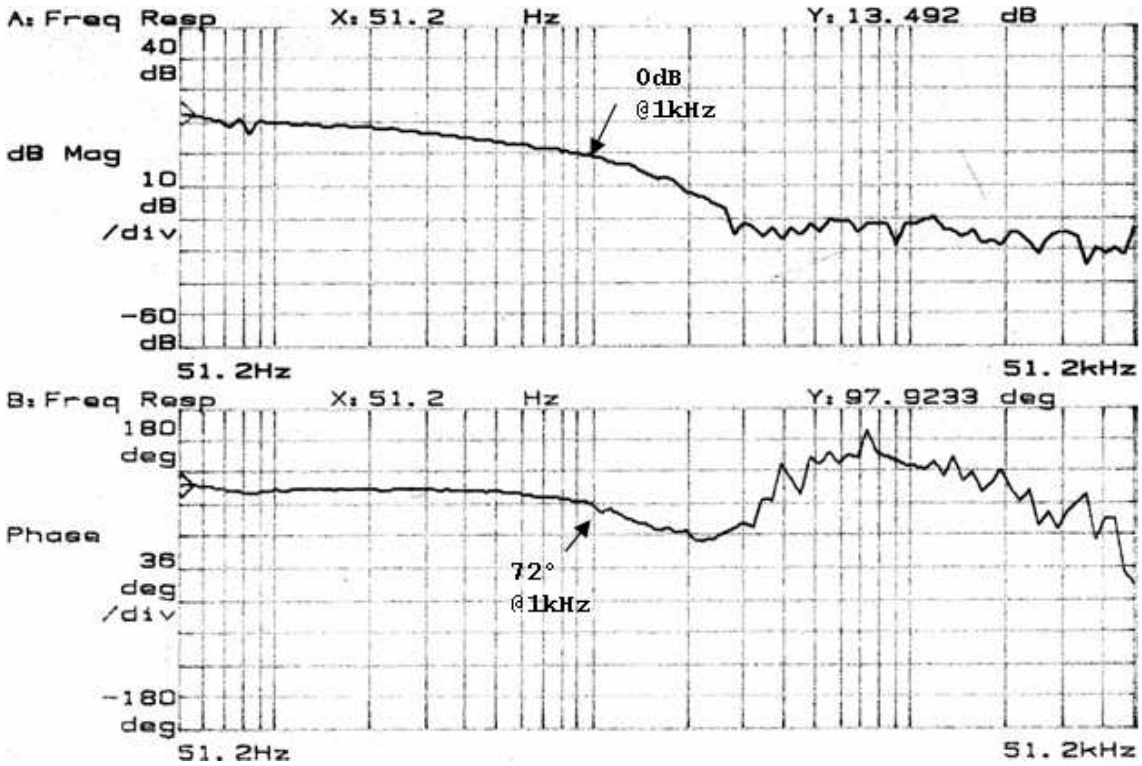


Figure 3.12 Experimental setup for measuring frequency response of the compensated response.

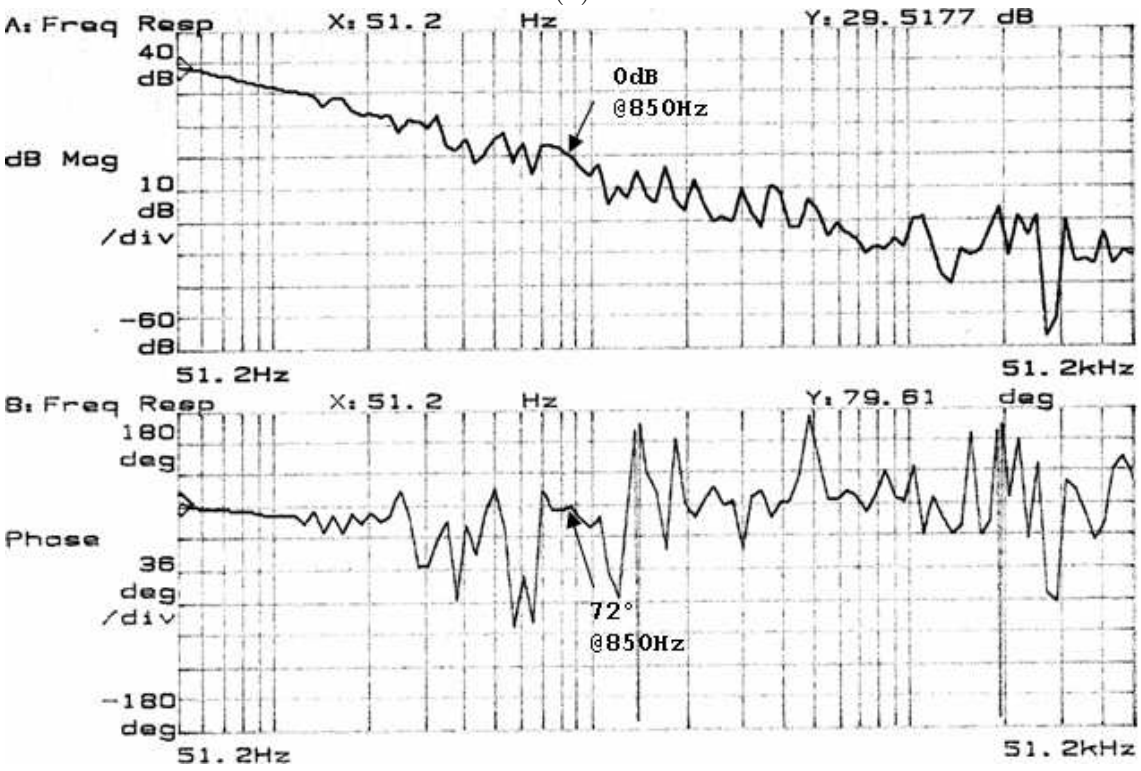
The Bode plots are plotted, similar to Section 3.2.1, using the change in V_{sense} with respect to the small change in V_{ac}. The measured compensated OL frequency responses are illustrated in Figs. 3.13 and 3.14. It seems the measured compensated OL Bode plots are similar to the simulated results in Figs. 3.10 and 3.11.

In the comparisons shown in Table 3.3, it seems that the simulated figures overrate the low frequency magnitude improvements given by the integral compensation, while the values for phase at low frequency are quite similar. As expected from a non-inverting compensator, the bandwidth of the compensated SLR converter is not controlled by the compensation as it does not provide any form of attenuation beyond 0 dB. The compensated SLR converter is stable in a feedback configuration because it has infinite GM and positive PM, both due to the fact that the system does not reach below $-180°$ in the frequency range of interest.

The evaluation of the analogue controller performance will be compared with the digital controller later in Chapter 6.

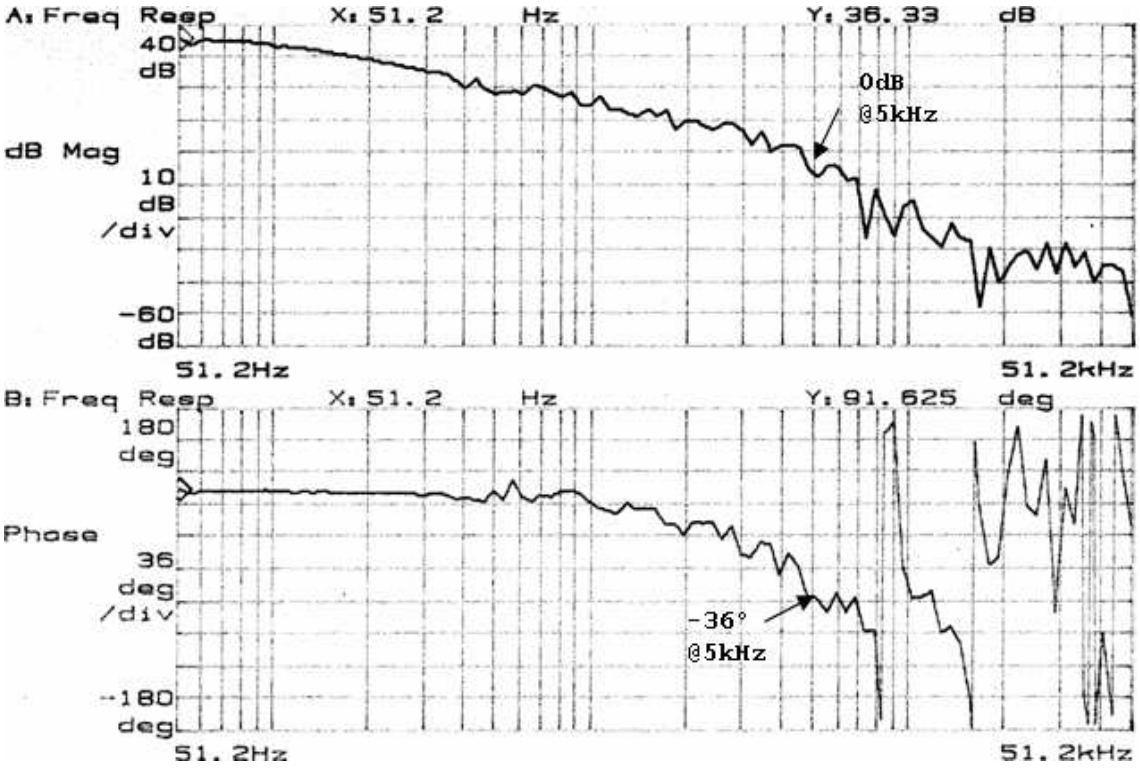


(a)

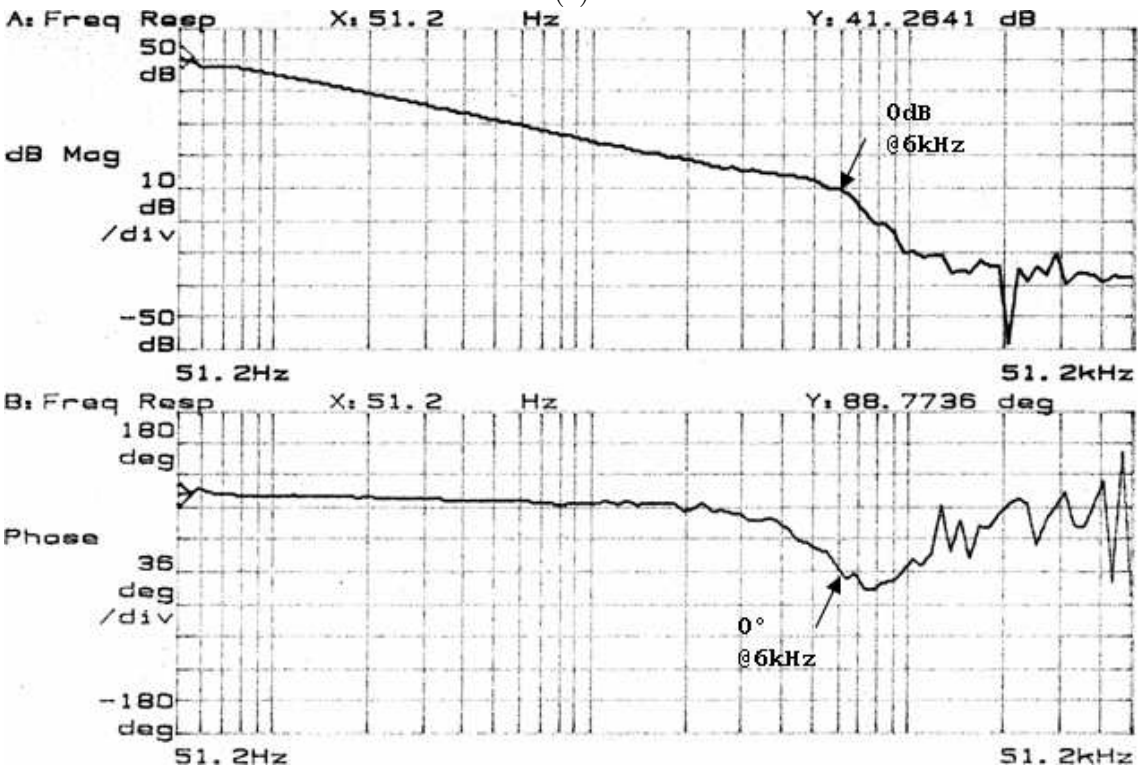


(b)

Figure 3.13 Measured frequency response of the compensated SLR converter with $Q_s = 2.5$ operating at (a) 62 kHz, and (b) 81.6 kHz.



(c)



(d)

Figure 3.14 Measured frequency response of the compensated SLR converter with $Q_s = 10$ operating at (c) 62 kHz, and (d) 64 kHz.

Table 3.3 Comparisons of simulated and measured compensated SLR transfer functions.

		@51.2 Hz		**Bandwidth**	**GM**	**PM**
		Magnitude	Phase			
A	simulated	37.6 dB	85.9°	1.69 kHz	inf	188°
	measured	13.5 dB	97.9°	1 kHz	inf	252°
B	simulated	37.4 dB	73°	825 Hz	inf	213°
	measured	29.5 dB	79.6°	850 Hz	inf	252°
C	simulated	54.7 dB	87.2°	6.29 kHz	inf	59.2°
	measured	36.3 dB	91.6°	5 kHz	inf	144°
D	simulated	50.2 dB	86.4°	7.51 kHz	inf	60.4°
	measured	41.3 dB	88.8°	6 kHz	inf	180°

3.5 ANALOGUE SLR CONVERTER SPECIFICATIONS

Following the implementation of the feedback loop, the specifications of the analogue SLR converter are shown below:

- Resonant Frequency: 58 kHz (for actual component values)
- Switching Frequency: 61 kHz–82 kHz
- Input Voltage: $46.6V$–$60.2V$ (operating range for all conditions in Table 3.1)
- Output Voltage: $12V$ with $0.9V_{pp}$ ripple (without rectifier snubbers)
- Output Current: $2A$–$8A$
- Load Resistance: 1.5Ω–6Ω

3.6 SUMMARY

The uncompensated SLR converter has been analysed using the approximation technique described by [10], and coupled with the frequency response of the voltage sensor in Section 2.2.4, to acquire the simulated Bode plots under four different operating conditions. Measured Bode plots of the SLR converter under the same set of four operating conditions are done using sinusoidal sweep of the *HP35665A*, and plotted using *HP7470A*.

The similarities between the simulated and measured results show that the approximated model provides adequate analysis of the SLR converter, so an integral compensation is designed to stabilise the Bode plots. Further comparisons of the simulated and measured

versions of the OL compensated SLR system shows that the simulated results overestimate the low frequency magnitude boost by the integrator.

Within the frequency range of interest, 51.2 Hz to 51.2 kHz, the compensated SLR converter has infinite GM and positive PM due to the fact that the SLR transfer functions do not reach below $-180°$. The bandwidth of the compensated SLR converter at different operating conditions are not corrected to 6 kHz as originally wanted, because the non-inverting compensator arrangement used do not provide attenuation more than 0 dB. Overall, a stabilised CL SLR converter has been designed.

Chapter 4

DIGITAL CONTROL STRATEGY

This chapter documents the design effort required to replace the analogue control circuitry with a digital controller. It starts by outlining the advantages and limitations that need to be considered by the designer when using digital components, followed by descriptions of DDS, which is an algorithm that replaces an analogue VCO. Then the design of the replacement digital compensator is explained, followed by simulation of the expected performance of the compensated system.

4.1 DIGITAL CONTROL CONSIDERATIONS

In an analogue control system, the measured result is continuously compared with the reference value, then the difference is used to regulate the output accordingly. However, in a digitally controlled system, rather than monitoring output perturbations uninterruptedly, the result is only measured in discrete instances in time, separated by a fixed sampling interval. In comparison to Fig. 3.1 in Section 3.1, the digital control block diagram is shown in Fig. 4.1.

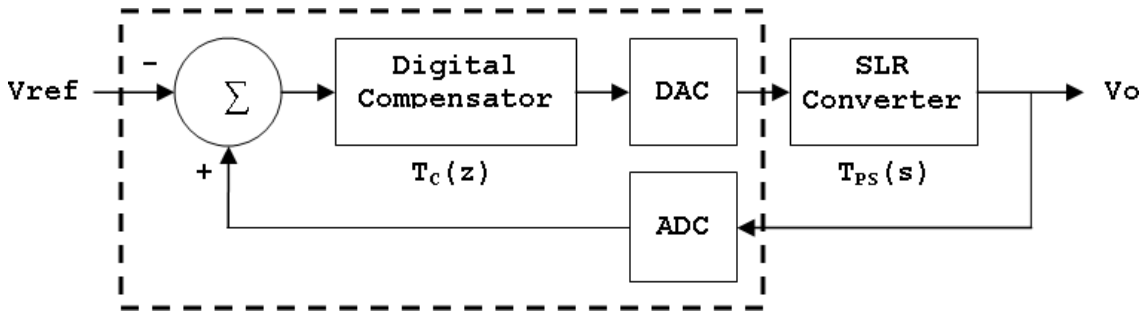


Figure 4.1 Digital control block diagram for the SLR converter.

The digital controller is bounded by the dashed box, which usually consists of the hard-

ware implementation of Analogue to Digital Converters (ADC), and Digital to Analogue Converters (DAC) that interface the controller to the analogue circuits. Algorithms embedded in the digital controller perform the required control strategies, such as digital compensation, to regulate the system accordingly. Each discrete control cycle starts by reading the measured output signal from the ADC, comparing the measured signal with the reference value (can either be an external reference read by ADC, or an internal software defined value), the difference is manipulated in the digital compensation, then the control result regulates the SLR converter via the DAC.

4.1.1 Advantages of Digital Control

As written in [13], there are at least seven advantages of a digitally controlled system over an analogue controlled one.

i. *Improved sensitivity.* The sampling operation of the controller uses very little power, therefore sensitivity of the control system is not compromised with low energy signals.

ii. *Digital transducers.* Digital signals have good immunity to distortion by noise and nonlinearities compared to analogue counterparts.

iii. *Digital coded signals.* Discrete information can be stored for long time intervals, to process complicated algorithms.

iv. *System design.* A digitally implemented compensator can increase its complexity without adding to noise problems, as is the case with analogue compensation.

v. *Telemetry.* Multiplexing allows transmission of data to multiple control systems in one communication channel.

vi. *Control systems with inherent sampling.* It is simpler to interface digital controllers with digital systems.

vii. *Digital computers.* The technology available in the form of digital processors has great capacity to implement complex control algorithms in an economic and efficient way, and as the technology continues to improve, more can be expected from the digital processors of the future.

4.1.2 Disadvantages of Digital Control

Similarly, there are at least six shortcomings of a digitally controlled system, as noted by both [13] and [14].

i. *System design.* The mathematical analysis and design of a digitally controlled system is usually more complex than the mathematical model used for an analogue system.

ii. *System stability.* Converting continuous signals into a series of discrete impulses, shown in Fig. 4.2, introduces a fixed latency determined by the sampling frequency. The latency in turn results in a phase lag in the frequency domain of the system, affecting stability.

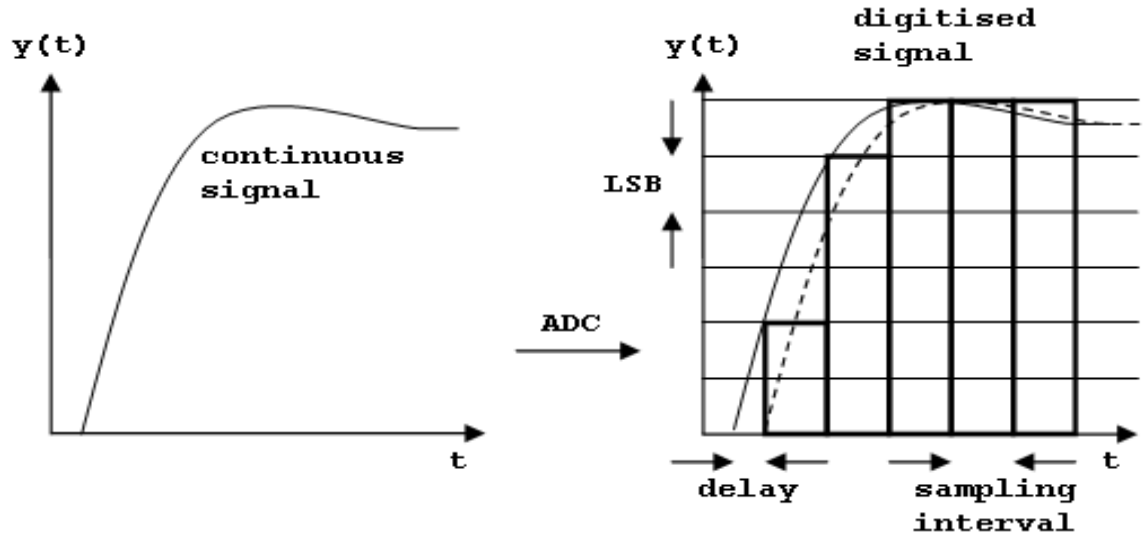


Figure 4.2 Digitising a continuous signal with an ADC. The dashed line is the sum of the digitised signals.

iii. *Finite word lengths.* Conversions between continuous and discrete signals introduce quantisation rounding errors relative to the magnitude of the least significant bit (LSB). The same rounding errors can be found in the numeric representation of numbers in algorithms. Numbers are rounded to the nearest base-2 representations.

iv. *Timer resolution.* This is similar to the previous problem, where the output states can only change at fixed instances in time, determined by the internal clock pulses of the digital controller, shown in Fig. 4.3, where a transition in the output can only happen at the rising edge of the controller clock.

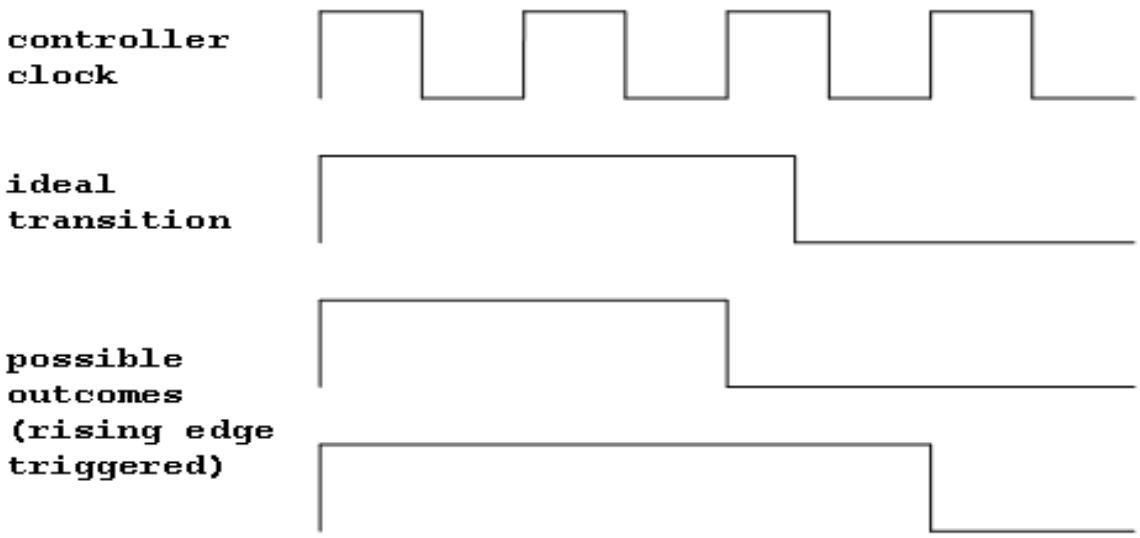
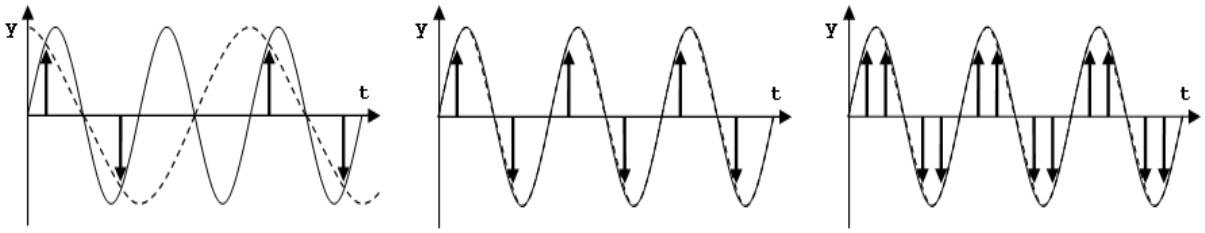


Figure 4.3 The error in transition time caused by the lack of resolution in the controller clock.

v. *Aliasing.* In order to acquire the full bandwidth of the circuit being sampled, the sampling frequency of the ADC must be at least twice the highest frequency of the circuit to prevent aliasing. Otherwise the reconstructed signal will be of a lower frequency, shown in Fig. 4.4.



(a) (b) (c)

Figure 4.4 Sampling and reconstruction of a continuous signal with (a) $f_s < 2f$, (b) $f_s = 2f$, (c) $f_s > 2f$. The dashed line is the reconstructed signal.

vi. *Power requirements.* Digital controllers may not be able to supply the power required to drive the external analogue circuits.

4.2 DIRECT DIGITAL SYNTHESIS BASICS

In the attempt to replace as much analogue circuitry with a digital controller, the DDS algorithm is proposed as a way to produce varying frequency square waves to drive the MOSFETs, instead of a VCO.

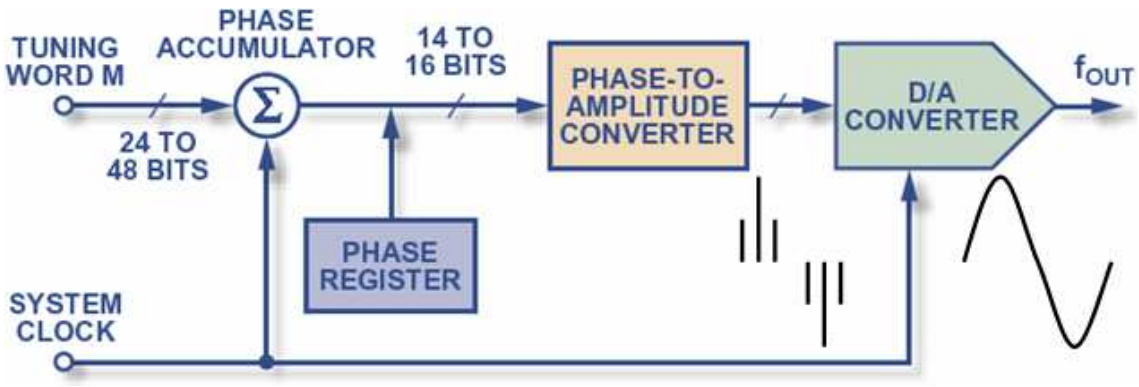
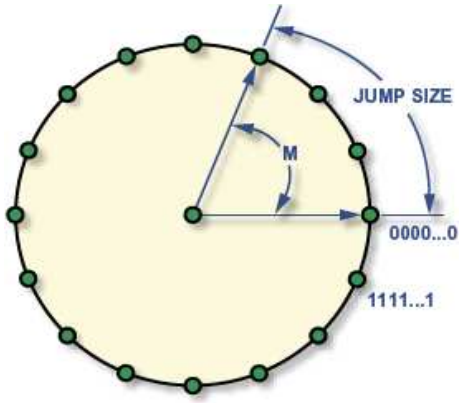


Figure 4.5 The DDS block diagram.

Fig. 4.5 [15] presents a typical DDS system that can be implemented using either hardware, software or a combination of the two. The DDS system works by repetitively adding a tuning word to a phase accumulator every clock cycle. The accumulated phase value is mapped to a predefined set of registers that produce an amplitude value for each different phase value. The series of digitally coded values goes through the DAC to construct the analogue equivalent of a periodic signal.



n	NUMBER OF POINTS
8	256
12	4096
16	65535
20	1048576
24	16777216
28	268435456
32	4294967296
48	281474976710656

Figure 4.6 The digital phase accumulator.

A closer inspection of the phase accumulator gives the arbitrary phase circle shown in Fig. 4.6 [15]. The quantity, n, defines the number of bits to allocate for the phase accumulator, such that it defines the whole range of points that map to the whole period of a repetitive signal, 0 to 2π. The tuning word, M defines the size of each accumulative step

around the phase circle for each period of the DDS operation. So the output frequency, f_{OUT}, is dependent on n, M, and f_D, which is the equivalent frequency to execute the DDS operation.

$$f_{OUT} = \frac{M \times f_D}{2^n} \tag{4.1}$$

The quantity f_D determines the maximum value of f_{OUT} to be half of f_D due to the *aliasing* issue described in Section 4.1.2, hence setting the maximum possible M to 2^{n-1}. Therefore, by linearly changing the quantity M, the output frequency produced by DDS can be varied linearly at the resolution, Δf_{OUT}, determined by n.

$$\Delta f_{OUT} = \frac{f_D}{2^n} \tag{4.2}$$

The shape of the DDS output signal is determined by the type of phase-to-amplitude conversion used in Fig. 4.5. For example, it could be sinusoidal, triangular or square, the registers that map the conversion process will store a different set of values. An example of the phase-to-amplitude conversion table is shown in Table 4.1.

Table 4.1 Phase-to-amplitude conversion table for $n = 3$ and 8-bit DAC.

		Phase							
		0x0	0x1	0x2	0x3	0x4	0x5	0x6	0x7
Amplitude	sine	0x80	0xDA	0xFF	0xDA	0x80	0x25	0x00	0x25
	triangle	0x00	0x40	0x80	0xC0	0xFE	0xBE	0x7E	0x3E
	sawtooth	0x00	0x20	0x40	0x60	0x80	0xA0	0xC0	0xE0
	square	0x00	0x00	0x00	0x00	0xFF	0xFF	0xFF	0xFF

The downside of DDS is that it is directly affected by the *timer resolution* issue described in Section 4.1.2. Whenever the tuning word does not divide completely into the phase accumulator, the delays in the transition of amplitude affects the signal pulse-widths, resulting in jitter. This is especially apparent for piecewise-continuous waveforms, such as square waves and triangular waves. Also, since f_D is determined by the amount of overheads (usually measured as an integer number of clock cycles) in each DDS operation, it is desirable to minimise the overheads to improve the DDS capability of the controller clock, f_C.

$$f_D = \frac{f_C}{overhead} \tag{4.3}$$

4.3 DIGITAL COMPENSATION DESIGN

The digital implementation of the compensator is produced as the discrete version of the analogue controller sampled at a proposed sampling interval. It is shown from Table 3.1 that the highest operating frequency of the SLR converter is 81.6 kHz, so by the *aliasing* consideration in Section 4.1.2, the sampling frequency of the compensator shall be at least twice as high as 81.6 kHz. As a result, 200 kHz is set as the sampling frequency, sampling interval of $5\mu s$, for converting the analogue compensator to a digital one. This sampling frequency has a much higher bandwidth than the proposed analogue compensator, 6 kHz, which provides some flexibility for future digital compensation. The conversion process is done using the *c2d* function (it converts a continuous system into a discrete system by sampling at predetermined sampling intervals) in MATLAB on the analogue transfer function, $T_C(s)$, in Section 3.3 to give the equivalent digital compensator, $T_C(z)$.

$$T_C(z) = \frac{z - 0.9411}{z - 1} \tag{4.4}$$

According to the *finite word length* consideration in Section 4.1.2, it is more efficient for the digital controller to represent the coefficient of 0.9411 in Eq. 4.4 as 0.9375, which is the nearest base-2 number, 15/16, without using too many binary digits. It would require as many as 8-bits, $241/256 \approx 0.9414$, to improve on the accuracy of the same coefficient. As long as the compensated results in Table 3.3 showed adequate GM and PM, the system stability should not be affected by such rounding errors. The frequency response of the digital compensator is shown in Fig. 4.7, which shows a slightly greater phase lag at higher frequencies when compared to the analogue version in Fig. 3.9. This is due to the *system stability* problem in Section 4.1.2, that is common in discrete systems. Then $T_C(z)$ can be rewritten as

$$T_{C,new}(z) = \frac{z - 0.9375}{z - 1} \tag{4.5}$$

4.4 ANALYSIS OF DIGITAL COMPENSATION

Using the digital compensation described in Section 4.3, the OL digitally compensated system looks like the block diagram in Fig. 4.8. The error between the reference value and the measured voltage output is sampled by a zero-order-hold (ZOH) function performed by the ADC, and fed into the compensation algorithm before being reconstructed by ZOH

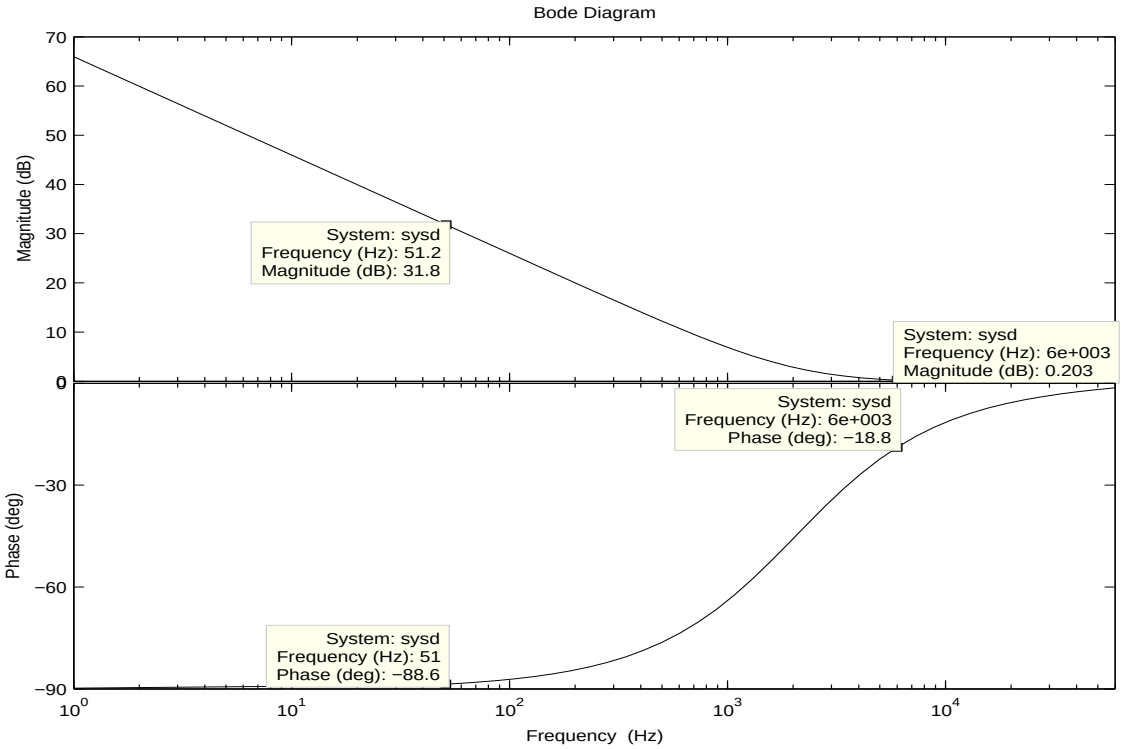


Figure 4.7 Bode plot of the digital compensator.

of the DAC to control the uncompensated SLR converter. The dashed box indicates the operations done in the digital controller, since the reference value of the system is assumed to be produced digitally at this point, the error between the reference and measurement is bounded by the dashed box.

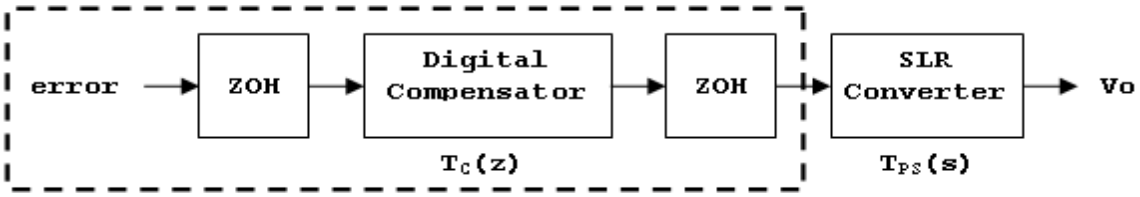
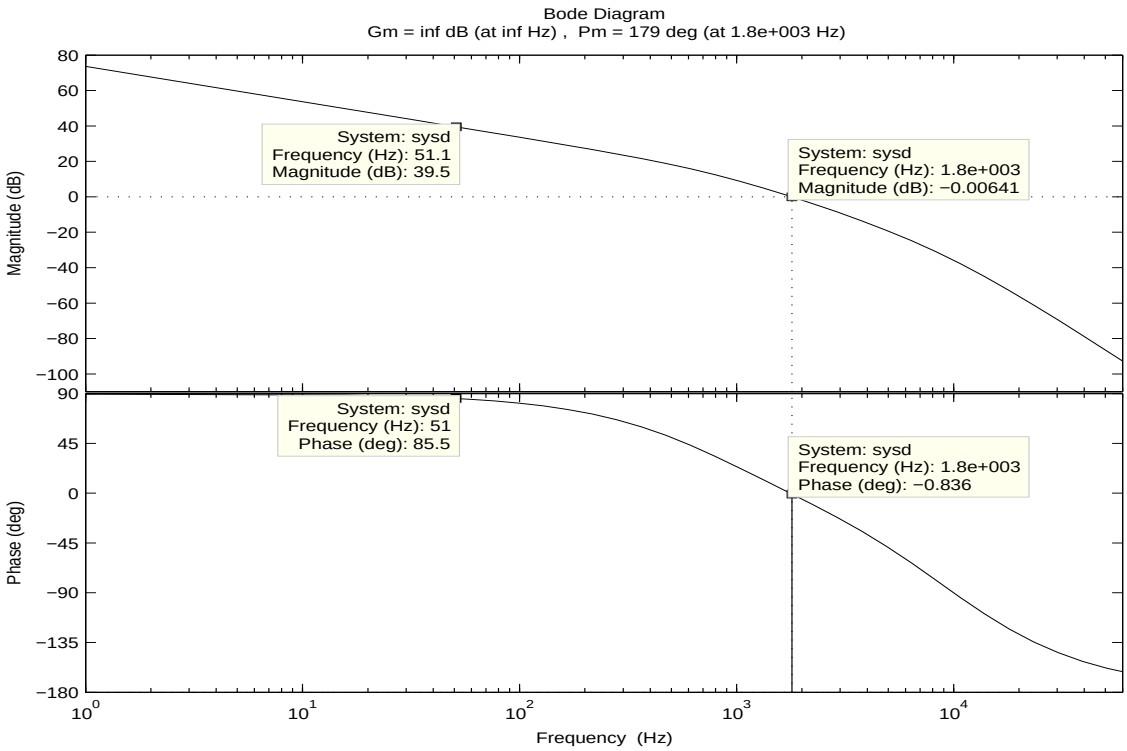


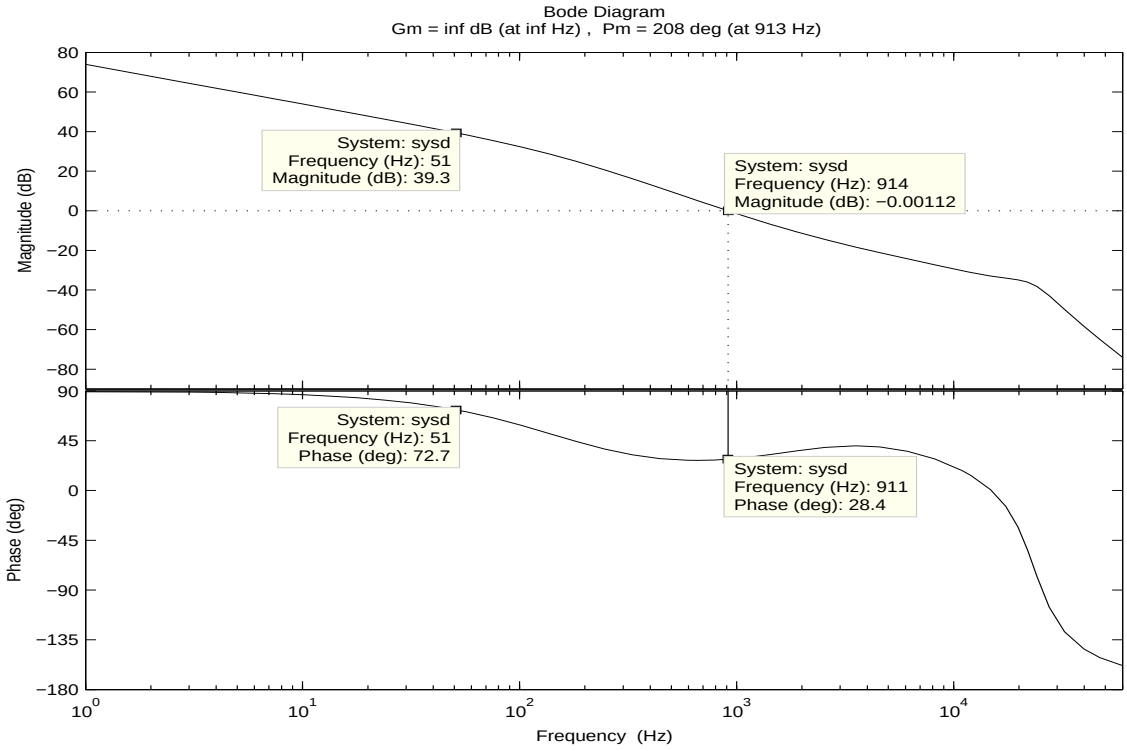
Figure 4.8 Block diagram of the digitally compensated OL system.

In practice, the effects of the ZOH functions are inherently included when the SLR converter output is digitised for computation, followed by the reconstruction to analogue space by the DAC. So, when simulating with MATLAB, it is important to convert the digital compensator back to analogue space, to find the OL transfer function of the digitally compensated SLR system.

$$H(s) = T_C(z)\big|_{reconstructed} \times T_{PS}(s) \times T_S(s) \tag{4.6}$$

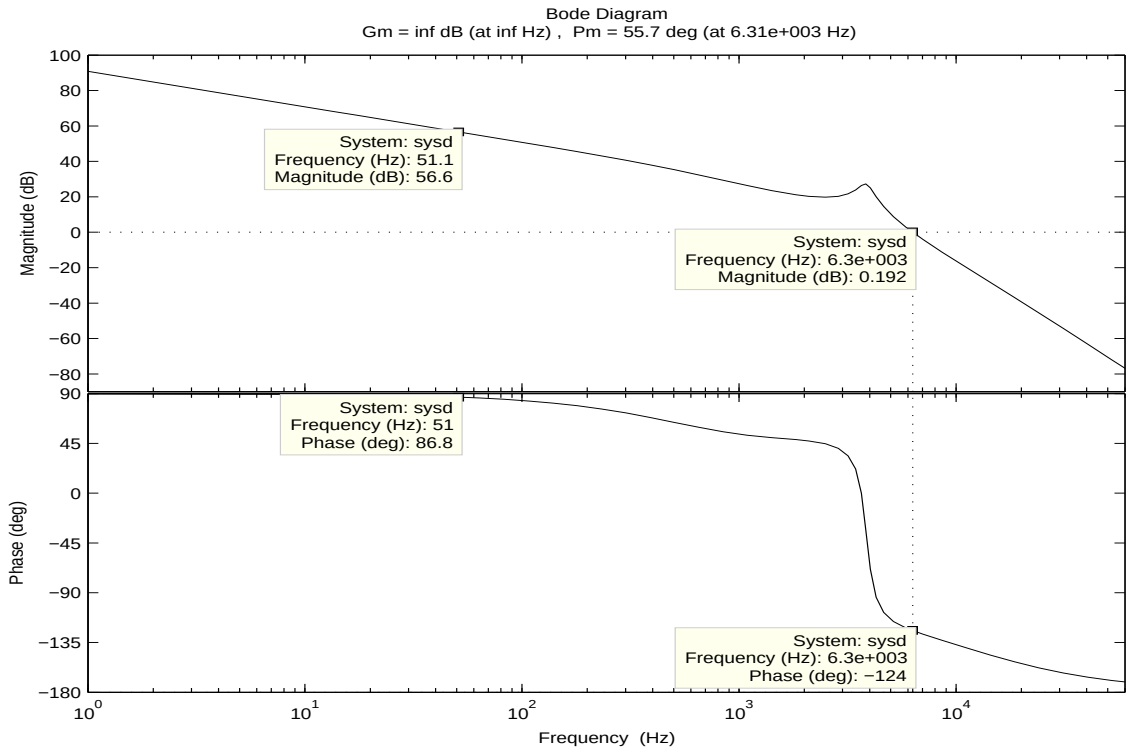


(a)

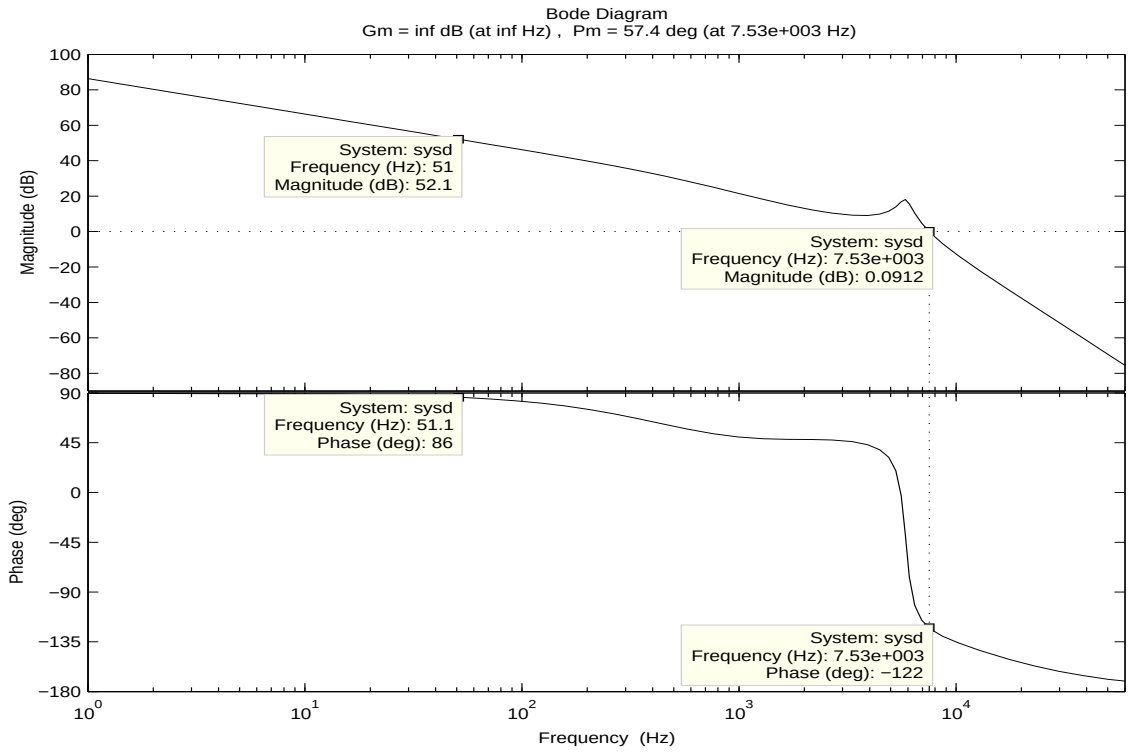


(b)

Figure 4.9 Simulated frequency response of the digitally compensated SLR converter with $Q_s = 2.5$ operating at (a) 62 kHz, and (b) 81.6 kHz.



(c)



(d)

Figure 4.10 Simulated frequency response of the digitally compensated SLR converter with $Q_s = 10$ operating at (c) 62 kHz, and (d) 64 kHz.

The resultant Bode plots of the digital OL systems are simulated for each set of operating conditions in Table 3.1, and shown in Figs. 4.9 and 4.10. Table 4.2 shows the comparison in frequency domain between analogue and digitally compensated systems.

Table 4.2 Comparisons of analogue and digitally compensated SLR transfer functions by simulation.

		@51.2 Hz		**Bandwidth**	**GM**	**PM**
		Magnitude	Phase			
A	analogue	37.6 dB	85.9°	1.69 kHz	inf	188°
	digital	39.5 dB	85.5°	1.8 kHz	inf	179°
B	analogue	37.4 dB	73°	825 Hz	inf	213°
	digital	39.3 dB	72.7°	913 Hz	inf	208°
C	analogue	54.7 dB	87.2°	6.29 kHz	inf	59.2°
	digital	56.6 dB	86.8°	6.31 kHz	inf	55.7°
D	analogue	50.2 dB	86.4°	7.51 kHz	inf	60.4°
	digital	52.1 dB	86°	7.53 kHz	inf	57.4°

As expected by the *system stability* problem described in Section 4.1.2, the digitised system has less margin for stability, as clearly shown by the reduced PM values for each different set of operating conditions.

The MATLAB codes used in modelling the digitally controlled SLR converter are included in Appendix B.

4.5 SUMMARY

A number of commonly known advantages and disadvantages of digital control have been identified, which affect both the design and implementation of the digital controller.

The DDS technique described has the ability to produce varying frequency signals digitally, and can replace the analogue VCO commonly used to do the same job, given the drawbacks of the *timer resolution* issue. The frequency range of the DDS outputs are determined by the internal clock frequency of the controller, the sizes of both the tuning word and the phase accumulator. At a closer inspection, the size of the phase accumulator and the clock frequency directly affect the resolution of the DDS ouputs. Therefore, to produce higher frequency signals, a faster clock is needed and a bigger accumulator should be used to maintain the fineness of resolution. The DDS is also pretty versatile in terms of outputting different shapes of periodic signals. It can change the output shapes

by substituting a different set of phase-to-amplitude conversion table.

A digital compensation has been produced by sampling the analogue counterpart at a sampling frequency of 200 kHz. That sampling frequency is chosen to measure system variations up to 80 kHz as indicated by the *aliasing* problem. A coefficient of 0.9411 in the compensator is replaced by 0.9375, which is easier to be represented in a base-2 format, based on the *finite word lengths* consideration. During the digitising process, the phase lag introduced by the ZOH operation is clearly shown in the Bode plots of the compensator itself, as well as the OL simulations of the digitally compensated systems. The phase lag due to the digitising process affects the stability of the system by reducing the PM slightly.

Chapter 5

DIGITAL CONTROLLER IMPLEMENTATION

This chapter describes the digital hardware and software implementations used to realize the digital controller described in Chapter 4. The choice of the digital processor and its capabilities are reported, as well as the development board used in the design process. Then, software algorithms that define the control loop are described in detail.

5.1 PROCESSOR SELECTION

The proposed digital processor for this research is the TMS320F2812, part of a fixed point DSP generation, TMS320C28x^{TM}, from Texas Instruments, that operates as fast as 150 MIPS to provide a low-cost, low-power, and high performance platform for applications such as automotive, industrial automation, appliance/white goods, and power conversion. Table 5.1 lists the features of the TMS320F2812 DSP [16].

The high speed, 150 MHz, feature of the DSP is used to apply a higher timer resolution to the DDS technique described in Section 4.2. The on-chip Flash allows for cost-effective reprogrammable prototyping of designs. The Event Managers on-chip allows for periodic interrupts that synchronise the ADC operation and perform the control algorithms in the corresponding interrupt service routines.

5.1.1 DSP Development Board

In order to simplify the digital controller design process, a general purpose development tool in the form of an F2812 eZdsp Starter Kit from Spectrum Digital Incorporated is used. The block diagram of such a development board is shown in Fig. 5.1 [17]. It comes

Table 5.1 Hardware features of TMS320F2812 DSP.

Descriptions	Features
Instruction Cycle (at 150 MHz)	6.67 ns
Single-Access RAM (SARAM)(16-bit word)	18K
3.3V On-Chip Flash (16-bit word)	128K
Code Security for On-Chip Flash/SARAM	Yes
Boot ROM	Yes
OTP ROM (1K X 16)	Yes
External Memory Interface	Yes
Event Managers	EVA, EVB
General-Purpose (GP) Timers	4
Compare (CMP)/PWM	16
Capture (CAP)/QEP Channels	6/2
Watchdog Timer	Yes
12-Bit ADC	Yes, 16 channels
32-Bit CPU Timers	3
Communication Interface	SPI, SCIA, SCIB, CAN, McBSP
Digital I/O Pins (Shared)	56
External Interrupts	3
Supply Voltage	1.9V Core, 3.3V I/O

with a programmable TMS320F2812 processor and various compatible memory and peripheral devices that allow users to evaluate designs with the TMS320F2812 DSP easily.

The key features of the F2812 eZdsp board include the following [17]:

- TMS320F2812 Digital Signal Processor
- 150 MIPS operating speed
- 18K words on-chip RAM
- 128K words on-chip Flash memory
- 64K words off-chip SRAM memory
- 30 MHz clock
- 2 Expansion Connectors (analog, I/O)
- Onboard IEEE 1149.1 JTAG Controller
- 5V only operation with supplied AC adapter

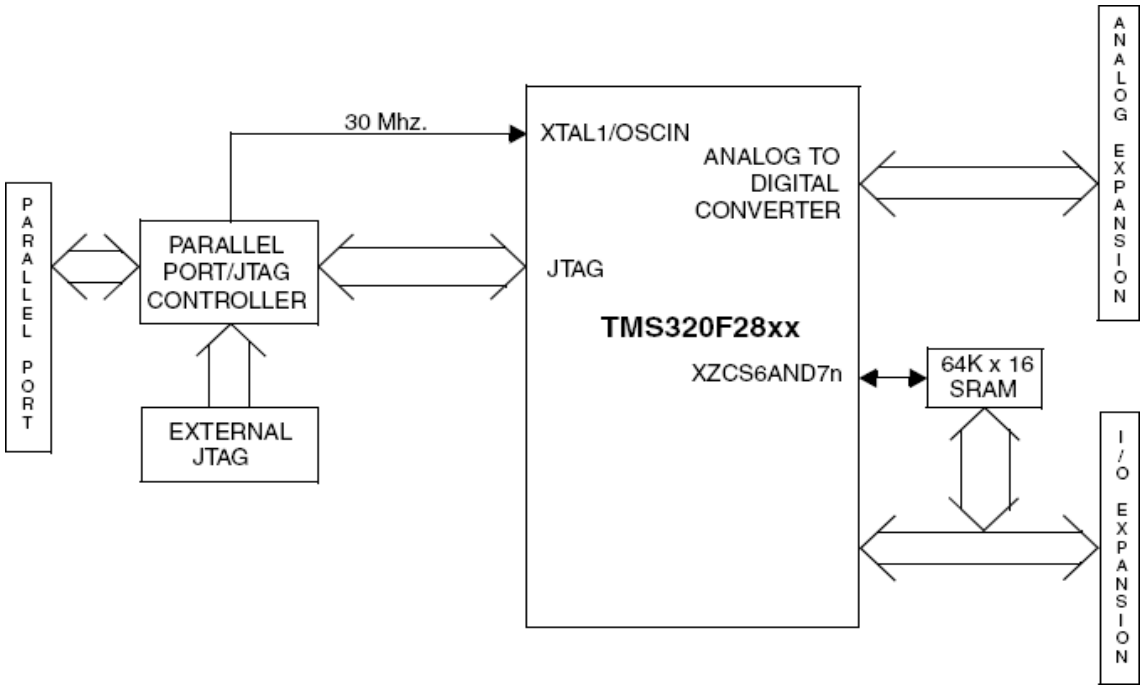


Figure 5.1 Block diagram of the F2812 eZdsp Starter Kit.

- TI F28xx Code Composer Studio tools driver
- On board IEEE 1149.1 JTAG emulation connector

As shown in the block diagram, the eZdsp connects to the computer by the JTAG emulation connector via the parallel port, and is programmed with the Code Composer Studio software. The Code Composer allows evaluators to code in either C or Assembly, therefore making the evaluation/development process shorter and easier.

5.2 INTERFACE BOARD DESIGN

This section describes the necessary circuits used to interface the digital processor to the analogue SLR converter.

5.2.1 Interfacing Digital Outputs to Gate Driver

Since the TMS320F2812 DSP is $3.3V$ compatible only, in order to make the digital controller interface compatible with the analogue MOSFET drive circuitry, a level shifter is needed for each power MOSFET driving signal to shape it to the required $10V$ square waves.

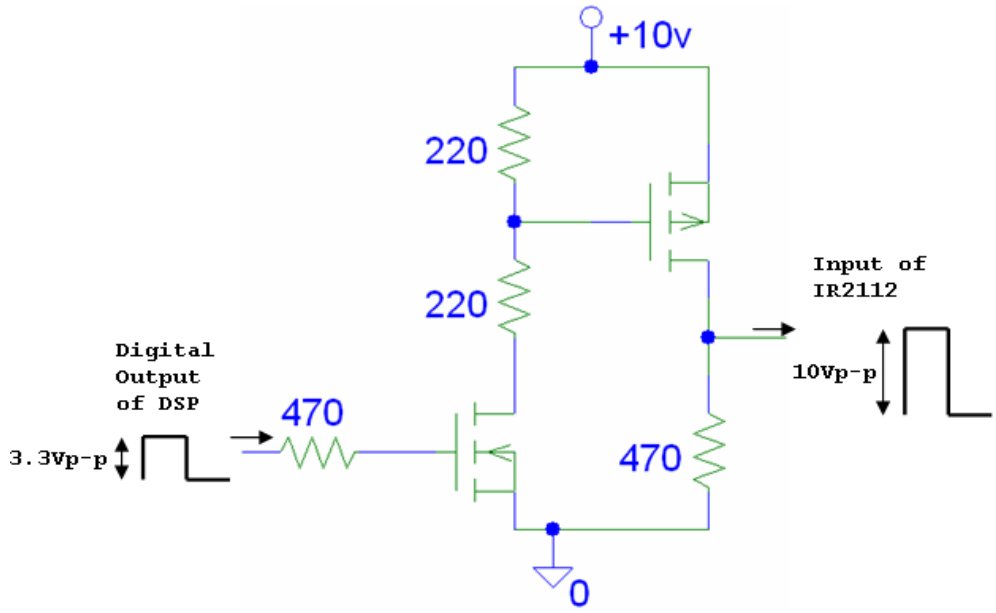


Figure 5.2 Schematic of a level shifter.

Fig. 5.2 shows the schematic of the level shifter for one channel of digital output. The circuit uses two logic MOSFETs to amplify the digital signal with minimum phase shift.

5.2.2 Implementation of an External ADC

Even though the DSP of choice has internal ADCs, it is the interest of this research to demonstrate the implementation of an external ADC with a digital controller, so the digital controller can be repeated and applied to processors that do not have built-in ADCs.

The external ADC used is AD7813 [18], which is a microprocessor compatible ADC that can be driven with both $5V$ and $3.3V$ compatible processors. It has an 8-bit parallel interface and has resolution as high as 10-bits. The conversion time of $2.3\mu s$ means the ADC can sample as fast as 400 kHz, which is more than adequate for the required 200 kHz sampling frequency described in Section 4.3.

Fig. 5.3 shows that in order to interface the AD7813, at least three digital outputs from the DSP are needed to operate the ADC, and eight digital inputs are used to receive the 8-bit data. To start a conversion cycle, the signal at $\overline{\textbf{CONVST}}$ goes low to indicate the start of conversion. No result can be read when **BUSY** is high, but as soon as it goes low, the ADC conversion is complete, and the result can be read from **DB7–DB0** after

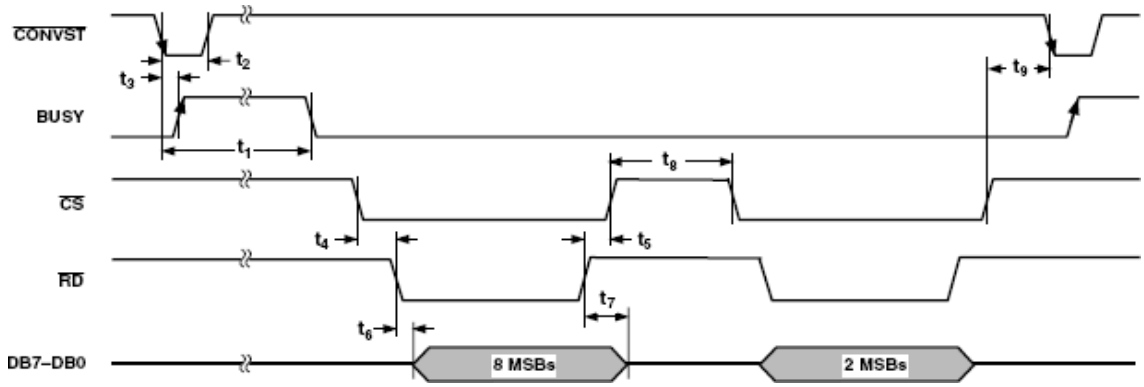


Figure 5.3 Timing diagram of the AD7813 ADC.

both $\overline{\mathbf{CS}}$ and $\overline{\mathbf{RD}}$ go low. After both $\overline{\mathbf{CS}}$ and $\overline{\mathbf{RD}}$ go high, AD7813 waits for another low at $\overline{\mathbf{CONVST}}$ to repeat the ADC conversion process.

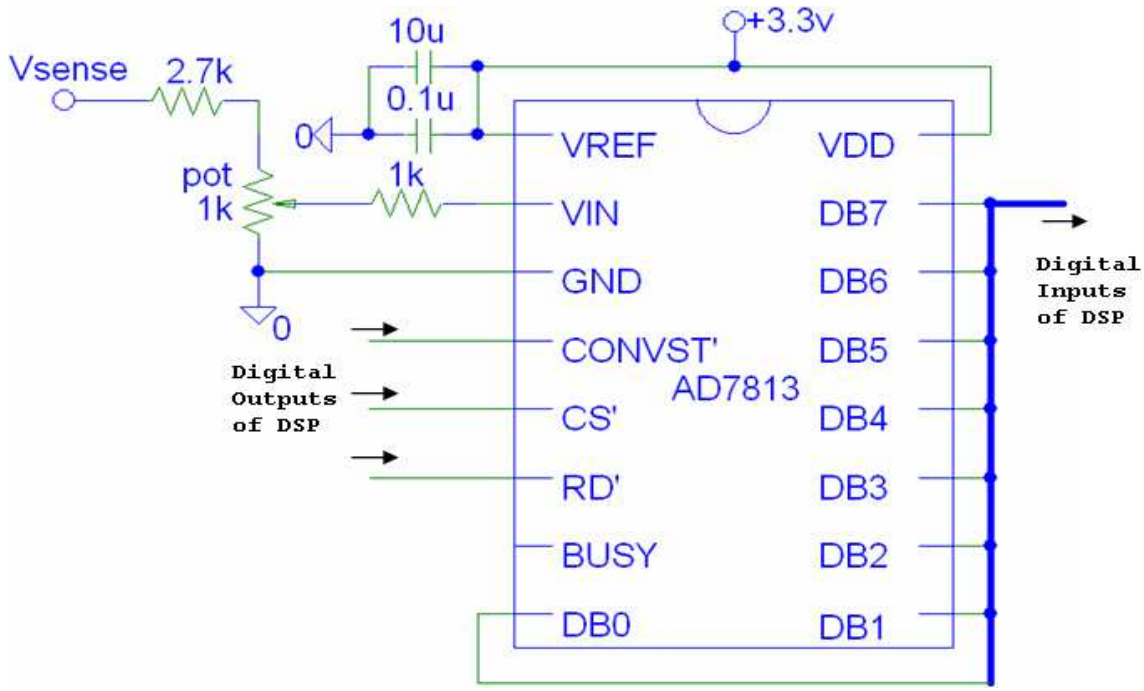


Figure 5.4 Schematic of the AD7813 ADC.

The schematic of the implementation of AD7813 is shown in Fig. 5.4. The chip is powered by $3.3V$ to make it power supply and pin compatible with the TMS320F2812. The **BUSY** pin is disconnected since the DSP does not use an external interrupt to perform the ADC read, but uses a 200 kHz periodic signal to read the ADC values instead. The resistor and potentiometer arrangement scales down the measured voltage, V_{sense}, to be no larger than $3.3V$ during normal operation of the SLR converter. Overall, three outputs from the DSP are used to drive the ADC and an 8-bit bus is used to read the ADC values.

5.2.3 8-Bit LED Indicators

An LED indicator, shown in Fig. 5.5, is fitted to each of the eight digital outputs from the DSP for debugging ADC operations and other functions of the controller.

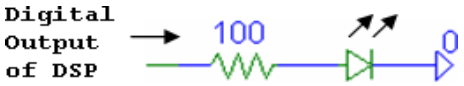


Figure 5.5 A branch of LED indicator.

5.3 SOFTWARE IMPLEMENTATION

The program used to perform digital control is written in C, and compiled using Code Composer Studio. The following subsections describe the software considerations in designing the digital controller.

5.3.1 Control Algorithm

The proposed program written in C for the digital controller follows the flowchart shown in Fig. 5.6.

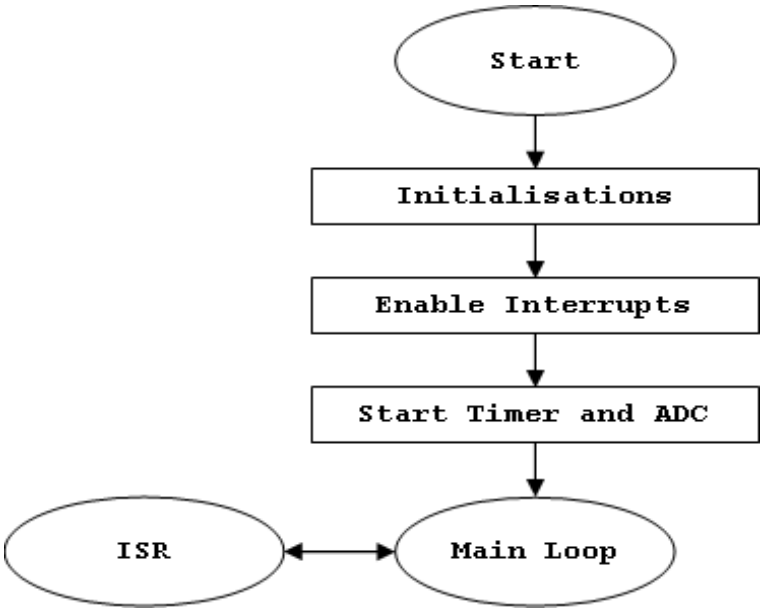


Figure 5.6 The program flow diagram.

The program starts by initialising the necessary features and peripherals of the DSP shown in Section 5.1. An interrupt is enabled and its respective timer activated to allow the ADC

to sample at specific intervals. Then the timer used for incurring interrupts has to start, while various control signals are sent to the external ADC to power-up and start ADC conversion. The actual controlling action is done within the Main Loop and the Interrupt Service Routine (ISR). The Main Loop consists of the generation of varying frequency square waves, while the ISR implements digital compensation.

5.3.2 Initialisation Definitions

In order to use the features and peripherals in the DSP, corresponding registers have to be initialised. The initialisation functions include:

- *System control.* Initialises the system control registers to a known state. Such as setting the clock frequency to execute instructions and enabling various peripherals.
- *PIE control.* Initialises the Peripheral Interrupt Expansion (PIE) control registers to a known state.
- *ADC.* Since the conversion is done using the external ADC, only the ADC ISR is set up.
- *Event Manager.* Initialises the Event Manager registers. The ADC interrupt frequency is set by comparing Timer 1 with a set PWM frequency.
- *GPIO.* Initialises the General Purpose Input/Output (GPIO) registers. This assigns the chosen GPIO ports as either inputs or outputs, as well as their initial values.

5.3.3 Digital Synthesis of Switching Waveforms

As described by Section 4.2, it is in the interest of maximising DDS performance for the same DSP clock, to reduce the overheads in waveform generation. Therefore, the Main Loop of the program consists of DDS instructions only, while the ADC results and digital compensation are performed in the ISR described later.

The flow chart in Fig. 5.7 shows that Main Loop starts by adding the tuning word, M, to the accumulator, followed by checking the resultant phase of the sum. If phase is less than halfway, **Output1** is cleared followed by a predetermined deadtime, before **Output2** is set; if the phase is over halfway, **Output2** is cleared before **Output1** is set. The same

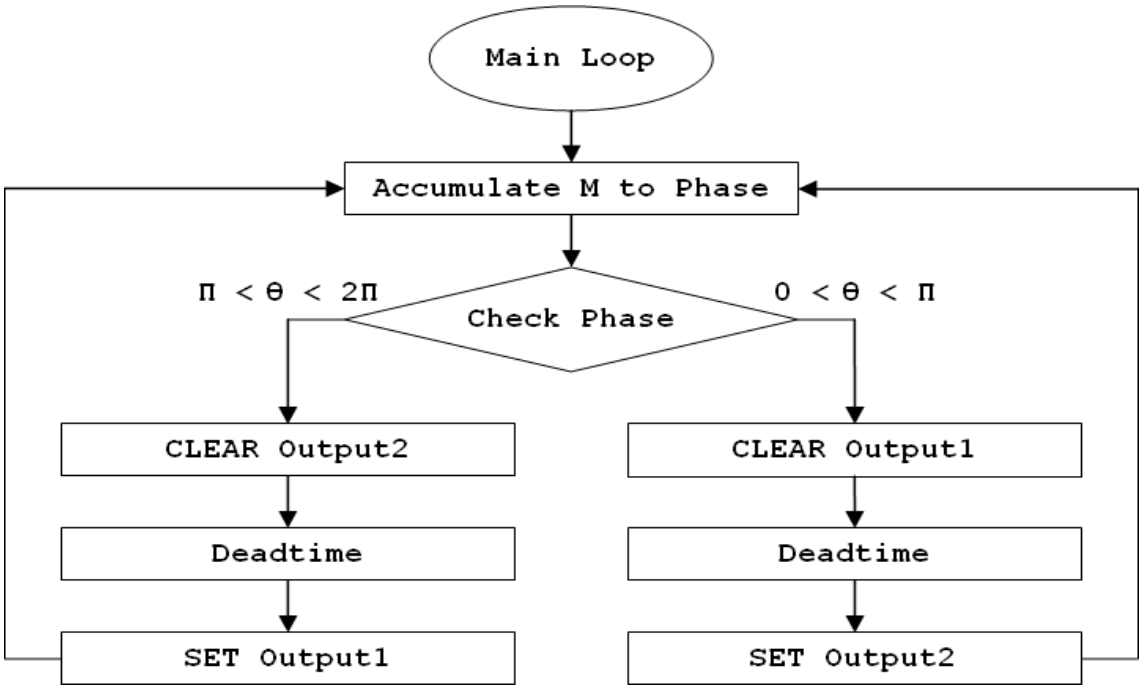


Figure 5.7 The Main Loop flow diagram.

DDS instructions are repeated indefinitely to produce the same output frequency until M is updated by the ISR for a different output frequency.

5.3.4 Interrupt Service Routine

The ISR is performed every $5\mu s$ (sampling frequency of 200 kHz) to read from ADC and perform digital compensation of the SLR converter. At the same time, the DDS operations performed by the Main Loop is temporarily idled, so having a long ISR can contribute to bad signal integrity of the output square waves.

Fig. 5.8 shows the sequence of instructions to be executed in the ISR. When an interrupt occurs, the program breaks from the Main Loop and executes ISR. This starts by acknowledging the interrupt and reading the 8-bit values from the external ADC. Digital compensation shown in Eq. 4.5, in Section 4.3, is converted into a difference equation below

$$y[k] = x[k] - 0.9375 \cdot x[k-1] + y[k-1] \tag{5.1}$$

A new M is updated each time the difference equation is executed. The value for M has to be bounded by the limit imposed by the user to make sure the SLR converter operates

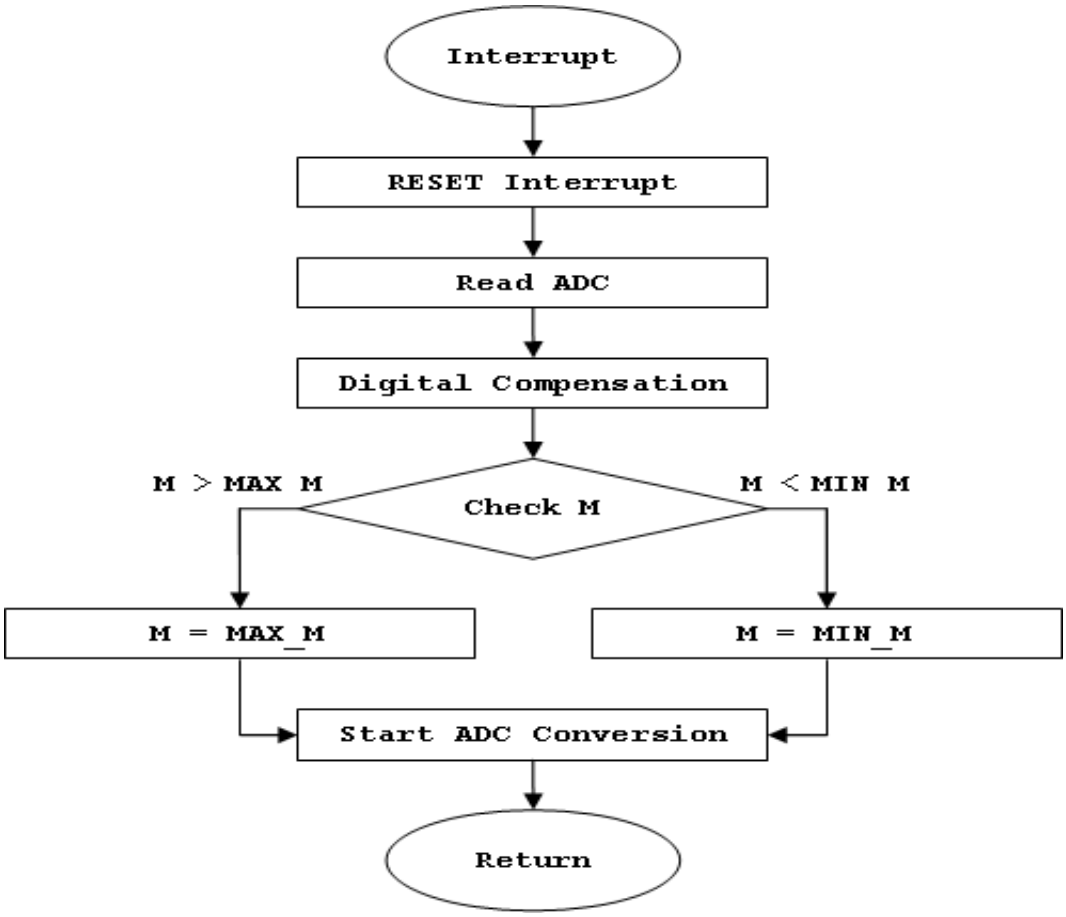


Figure 5.8 The ISR flow diagram.

correctly. Then the ADC is signalled for another start of conversion at the completion of the ISR. An alternative digital controller may be to use two separate controllers, one dedicated for compensation, the other for waveform generation. In such case, no ISR is used to delay waveform generation.

The program codes written in C to drive the TMS320F2812 are included in Appendix C.

5.4 SUMMARY

A practical approach to the digital controller has been discussed and implemented by programming the proposed algorithms onto the hardware available. The core of the controller is a TMS320F2812 DSP onboard to an F2812 eZdsp development board. The research takes advantage of the high clock speed of the DSP to provide adequate timer resolution to the DDS waveform generation technique.

In order to interface the analogue SLR converter to the digital controller, interfacing circuitry consists of level shifters, an external AD7813 ADC and 8-bit LED indicators. The level shifters are necessary to convert the $3.3V$ compatible outputs from the DSP into $10V$ peak-to-peak square waves to drive the gate drivers. The external ADC measures the output voltage of the SLR converter for the controller. The LEDs are only used when debugging the ADC and other aspects of the digital controller.

The structure of the software implementation consists of a never-ending Main Loop and an ISR. According to Section 4.2, it is important to make the algorithm concise and the calculations fast to improve performance of DDS waveform generation. So, the Main Loop specialises in DDS algorithms while the ISR concentrates on reading ADC values and digital compensation.

Chapter 6

EVALUATION OF DIGITAL CONTROL

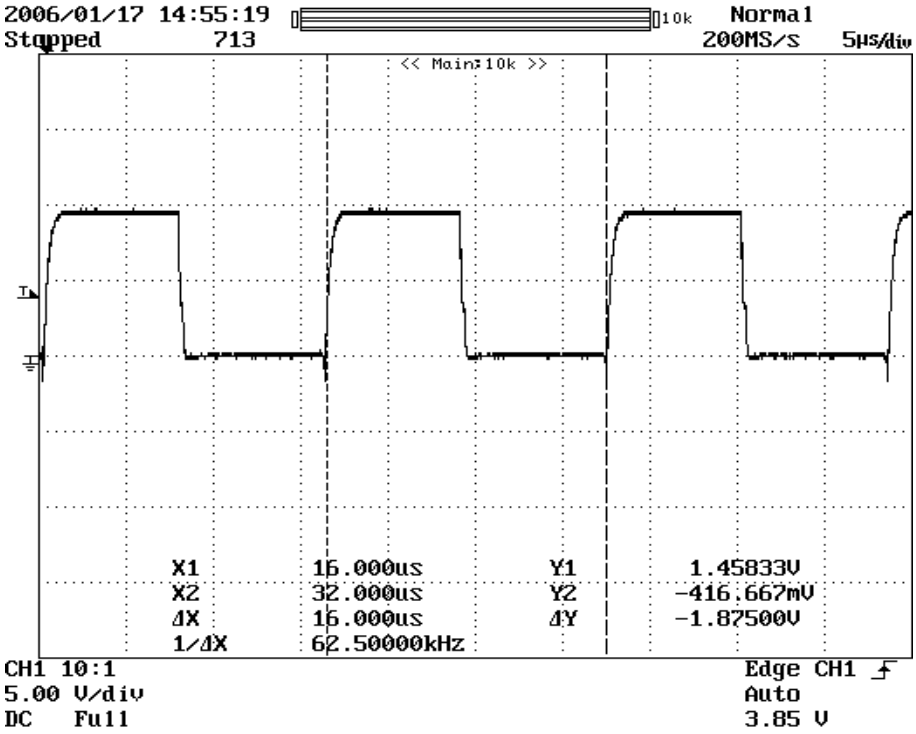
This chapter evaluates the performance of the digital controller described in Chapter 5. The interesting aspects of the digital controller include the time domain and frequency domain analyses of the digitally generated waveforms, and the transient responses to changes in both resistive load and input voltage. Each aspect is compared with the analogue equivalent as reference.

6.1 TIME DOMAIN ANALYSIS OF DDS SWITCHING WAVEFORMS

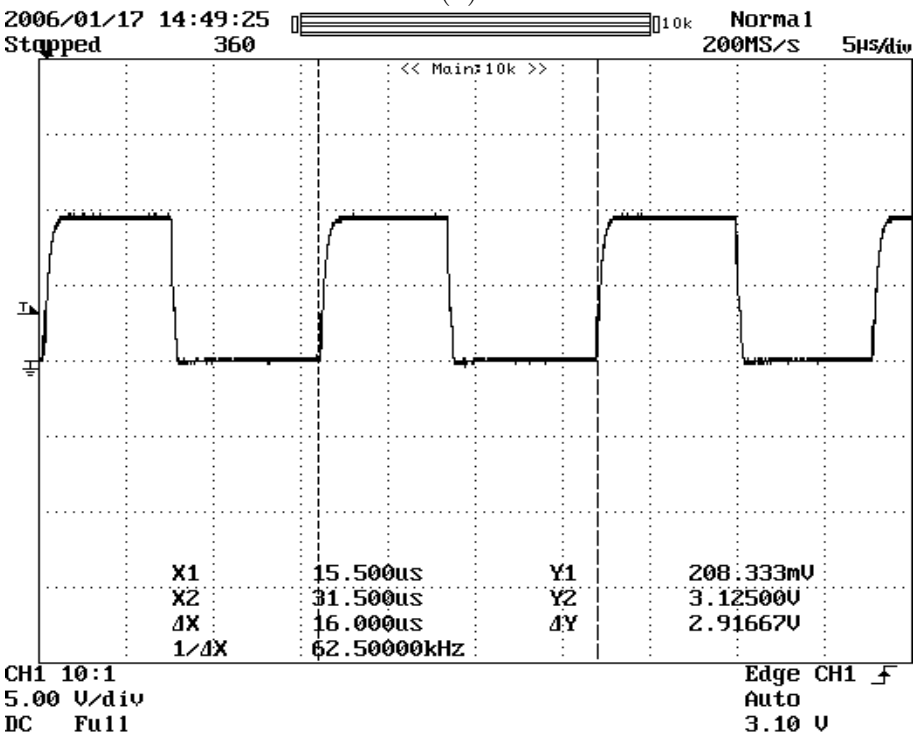
As discussed in Section 4.2, jitter in the DDS generated square waves reduces the integrity of the switching signals. Therefore, the digitally generated signals are compared with the VCO generated signals in the time domain to determine the variation in pulse-widths.

Figs. 6.1 and 6.2 show an example of square wave jitter that exists in DDS produced signals. The consecutive pulse-widths in a 62 kHz VCO square wave are both $\approx 16\mu s$, while the example of a 62 kHz DDS signal shows varying periods, with the first pulse $\approx 15.5\mu s$ in width, and $\approx 16\mu s$ the next. A similar effect can be seen in the 80 kHz square wave example, where the VCO signal has identical pulse-widths, $\approx 12.5\mu s$, throughout, and the DDS equivalent has both $\approx 12.5\mu s$ and $\approx 12\mu s$ pulse-widths in the same square wave signal.

As expected, it is evident that DDS generated piece-wise continuous signals exhibit jitter, which is evident in the pulse-width variations in the time domain.

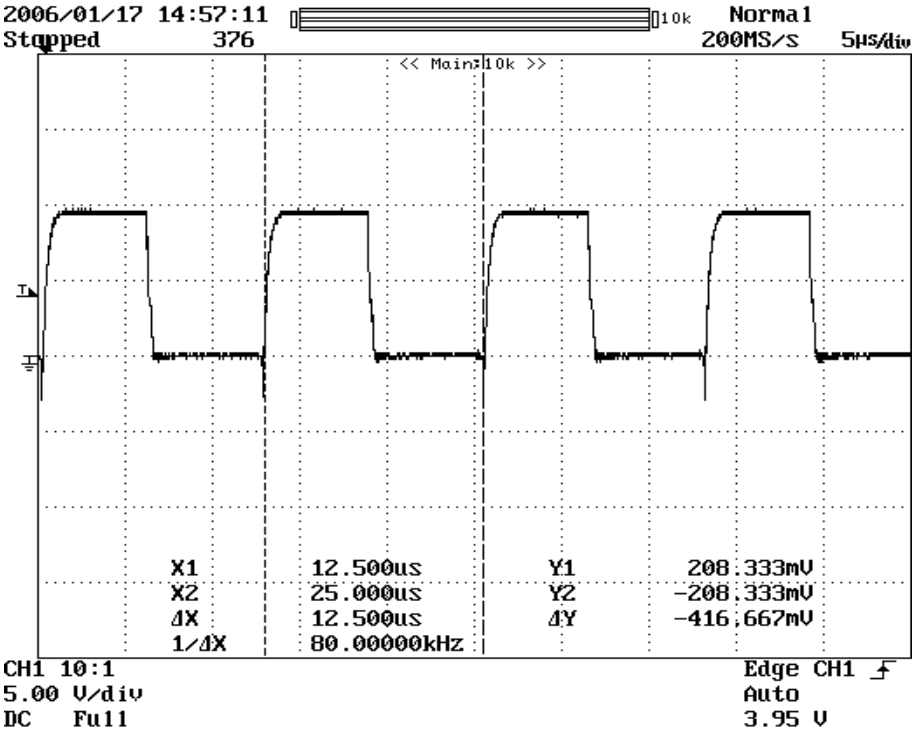


(a)

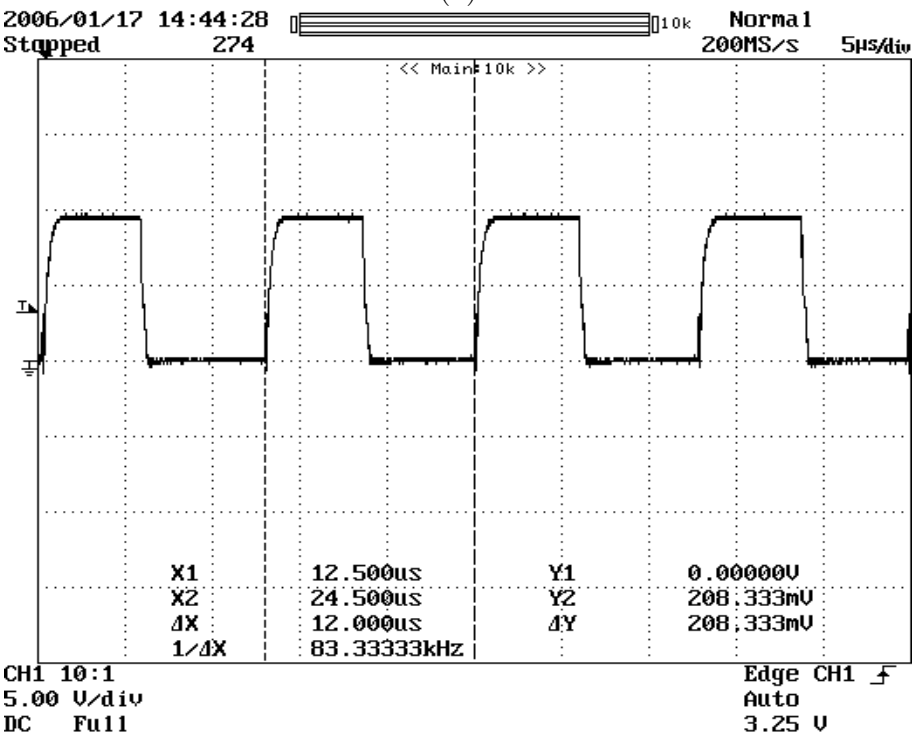


(b)

Figure 6.1 Time domain comparisons of 62 kHz square waves produced by (a) VCO, and (b) DDS.



(a)



(b)

Figure 6.2 Time domain comparisons of 80 kHz square waves produced by (a) VCO, and (b) DDS.

6.2 FREQUENCY SPECTRA OF DDS SWITCHING WAVEFORMS

An *HP3588A Spectrum Analyzer* is used for narrow band and swept spectrum analyses to evaluate the DDS generated square waves, especially the effects due to jitter in the frequency domain.

6.2.1 Narrow Band Analysis

Figs. 6.3 and 6.4 show the narrow band spectral comparisons between VCO and DDS generated square wave switching timing waveforms at 62 kHz and 80 kHz respectively, which are approximately the upper and lower bounds of the operating range, described in Section 3.5. By inspection, it can be seen that the DDS generated waveforms have slightly raised noise floors, as well as sidebands around the fundamental frequency, that are determined by the DDS frequency, f_D, and tuning word, M.

$$f_{mod} = \frac{f_D}{M} \tag{6.1}$$

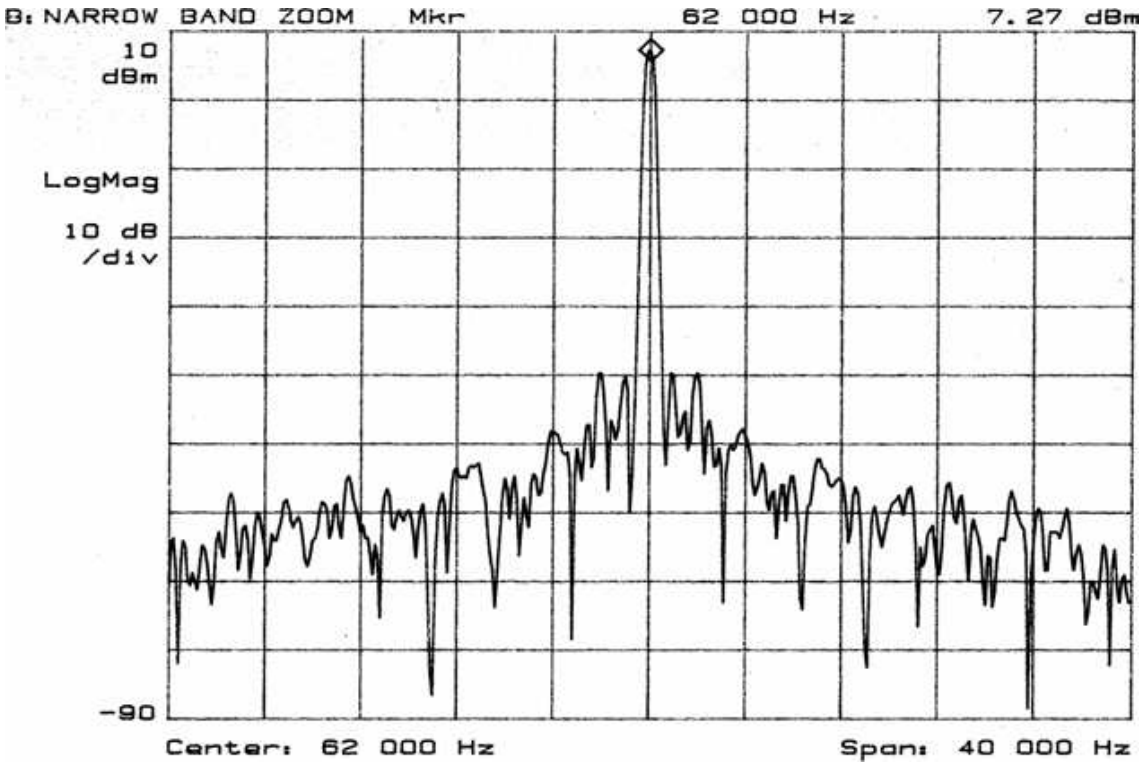
The never-ending Main Loop described in the control algorithm in Section 5.3.1 takes 31 instructions to produce a DDS sample, while the ISR takes 50 instructions to complete. Therefore, the equivalent overhead exhibited in the DDS execution is

$$overhead = 31 + 50 \times \frac{200 \times 10^3}{75 \times 10^6} \approx 31.13 \tag{6.2}$$

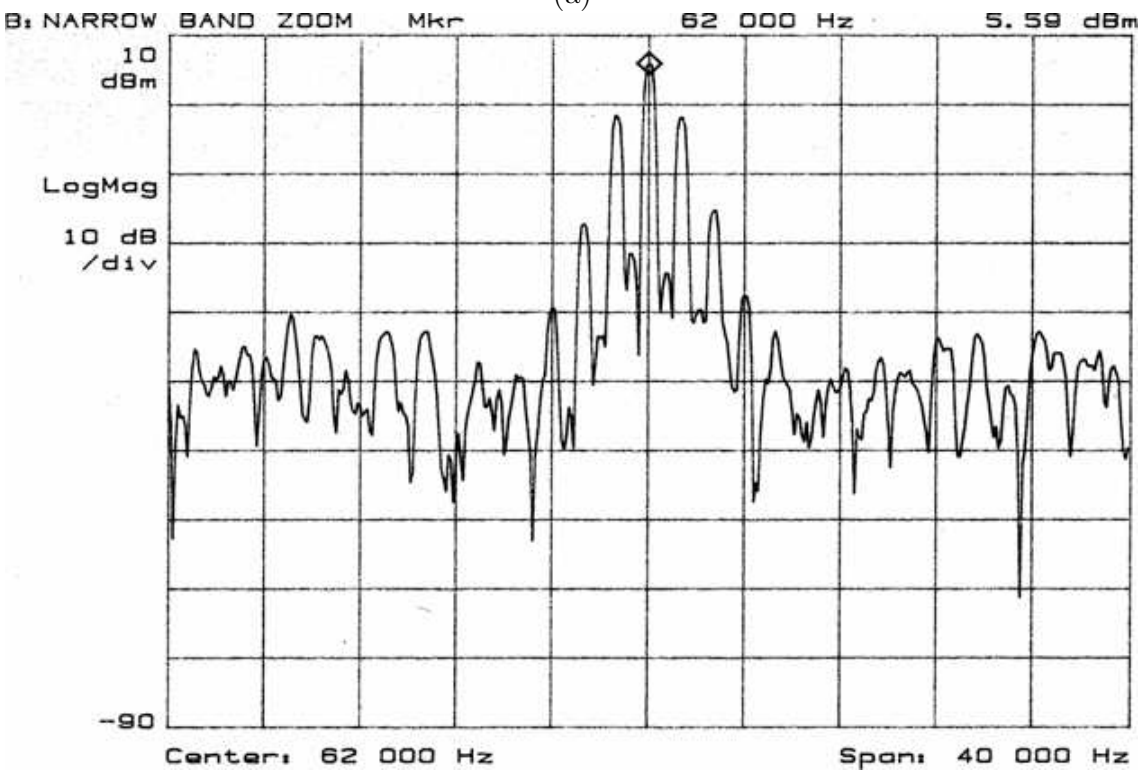
by scaling the overhead in 200 kHz ISR with the 75 MHz clock frequency. As a result, the equivalent DDS frequency is calculated using Eq. 4.3 to be

$$f_D = \frac{75 \times 10^6}{31.13} \approx 2.409 \text{ MHz} \tag{6.3}$$

So the 62 kHz DDS square wave in Fig. 6.3*b*, with $M = 1687$, has sidebands at integer multiples of 2.409 MHz/1687 ≈1.428 kHz from the fundamental frequency. Similarly, the sidebands for the 80 kHz DDS square wave in Fig. 6.4*b* are 2.409 MHz/2106 ≈1.144 kHz apart for $M = 2106$. In both cases, the noise floors of the DDS waveforms seem to have risen by around 20 dBm from the VCO generated waveforms, contributed in no small part by the long overhead of the ISR.

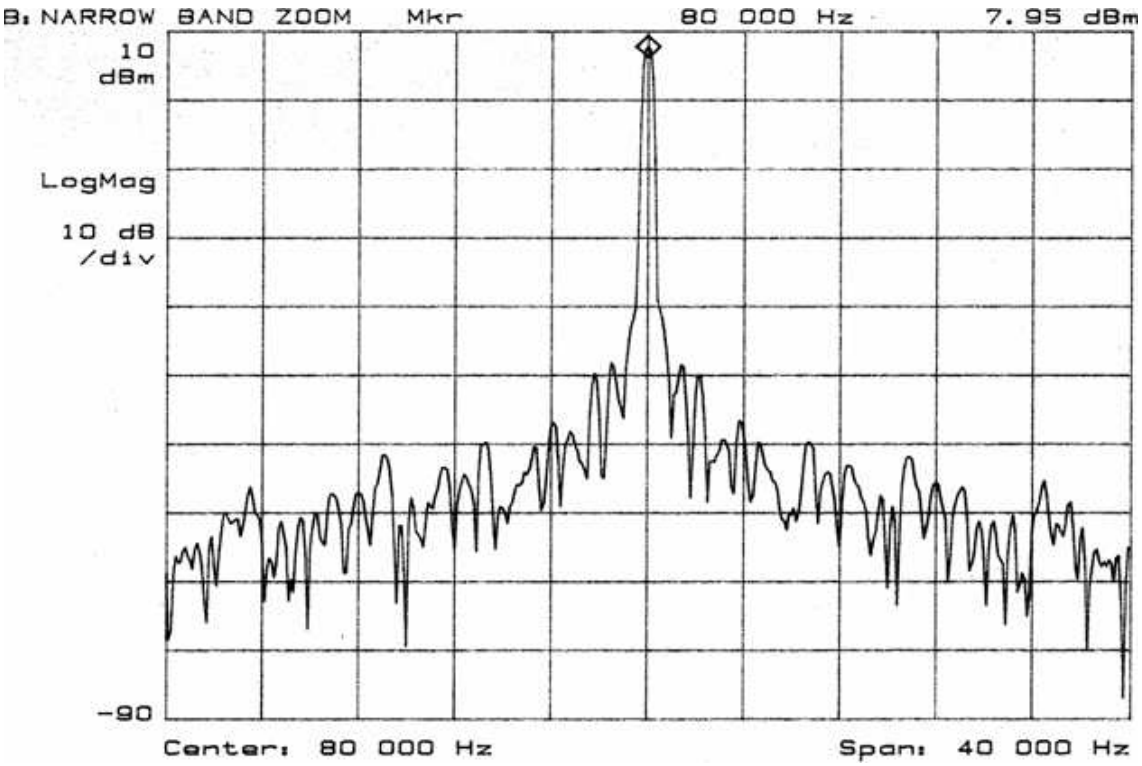


(a)

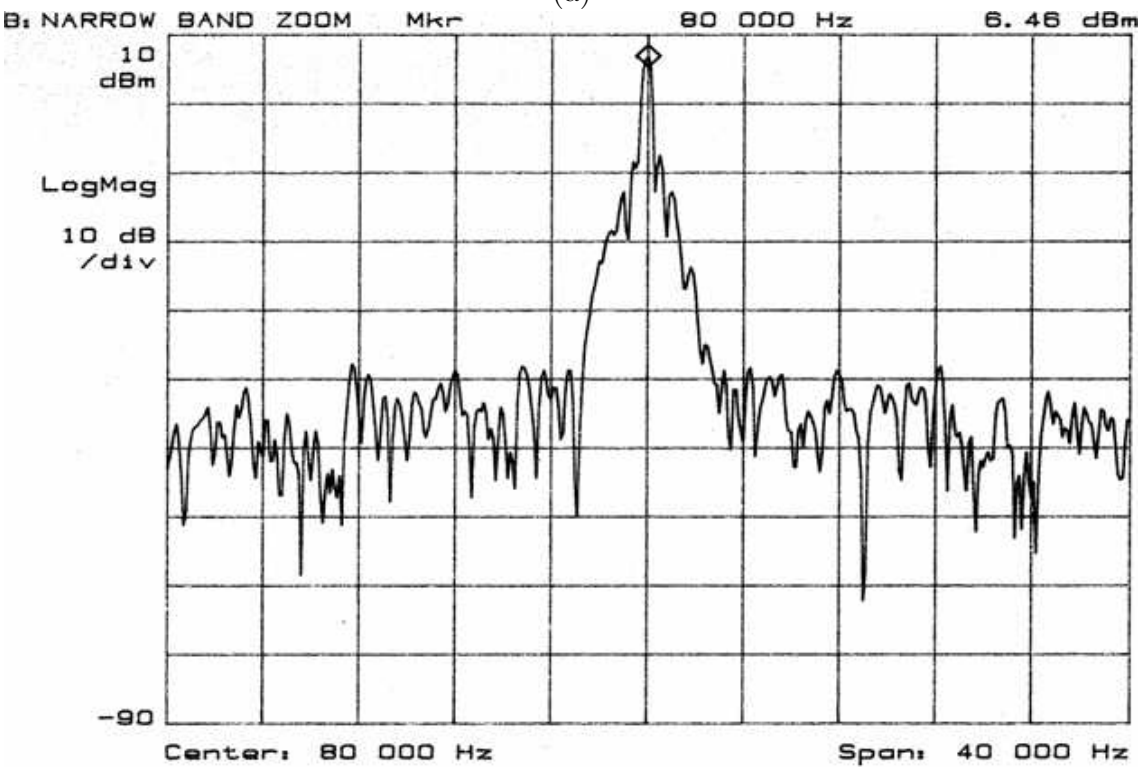


(b)

Figure 6.3 Narrow band frequency spectra of 62 kHz square waves produced by (a) VCO, and (b) DDS.



(a)



(b)

Figure 6.4 Narrow band frequency spectra of 80 kHz square waves produced by (a) VCO, and (b) DDS.

6.2.2 Swept Spectrum Analysis

Figs. 6.5 and 6.6 present the swept spectral differences between VCO generated square waves and the DDS generated square waves at 62 kHz and 80 kHz. The figures cover the range from the fundamental frequency up to the 5th harmonic to check whether the spectra are as expected for square waves, ie. odd harmonics are bigger than the nearest even harmonics.

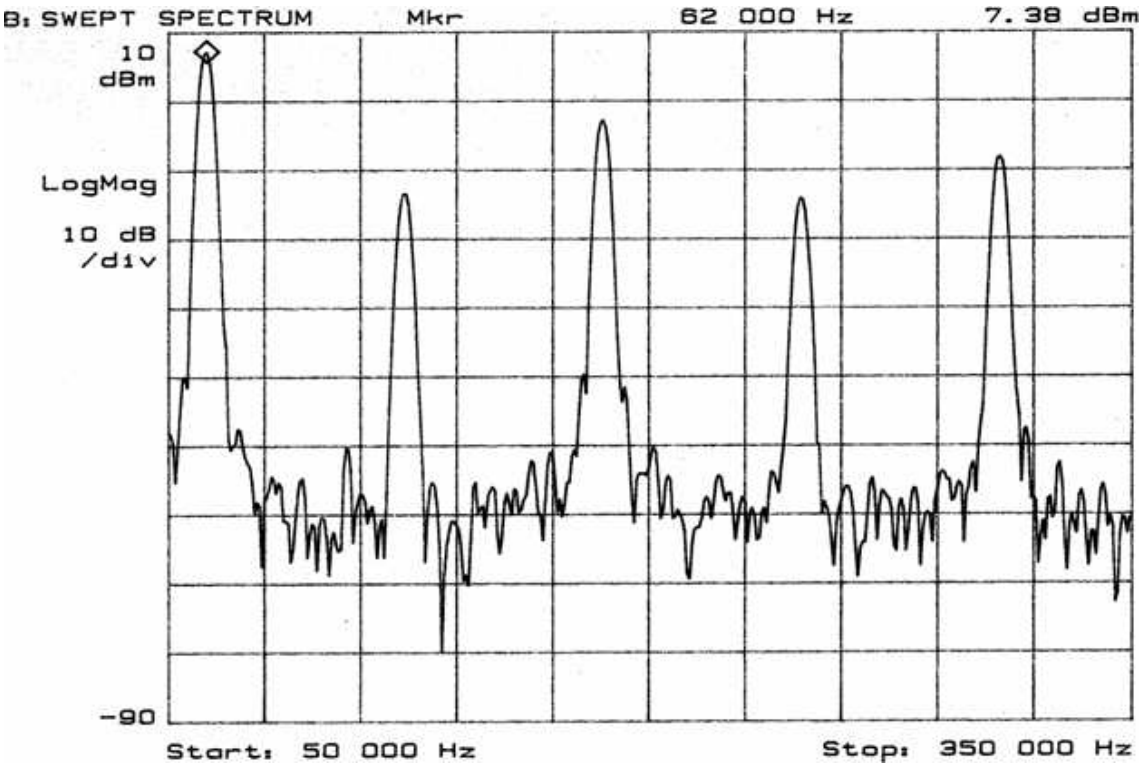
As expected, both VCO and DDS generated signals have square wave-like spectra, but the DDS generated signals suffer from the contamination of various noise signals that are sometimes as large as the even harmonics. These noise signals may mostly be caused by jitter that exhibits in DDS the algorithm, as shown previously in Section 6.1. On the bright side, the magnitudes of the odd harmonics for the DDS signals are similar to the VCO counterparts despite having a raised noise floor, therefore the DDS can produce adequate switching waveforms for the MOSFETs.

6.3 TIME DOMAIN ANALYSIS OF CHANGING LOADS

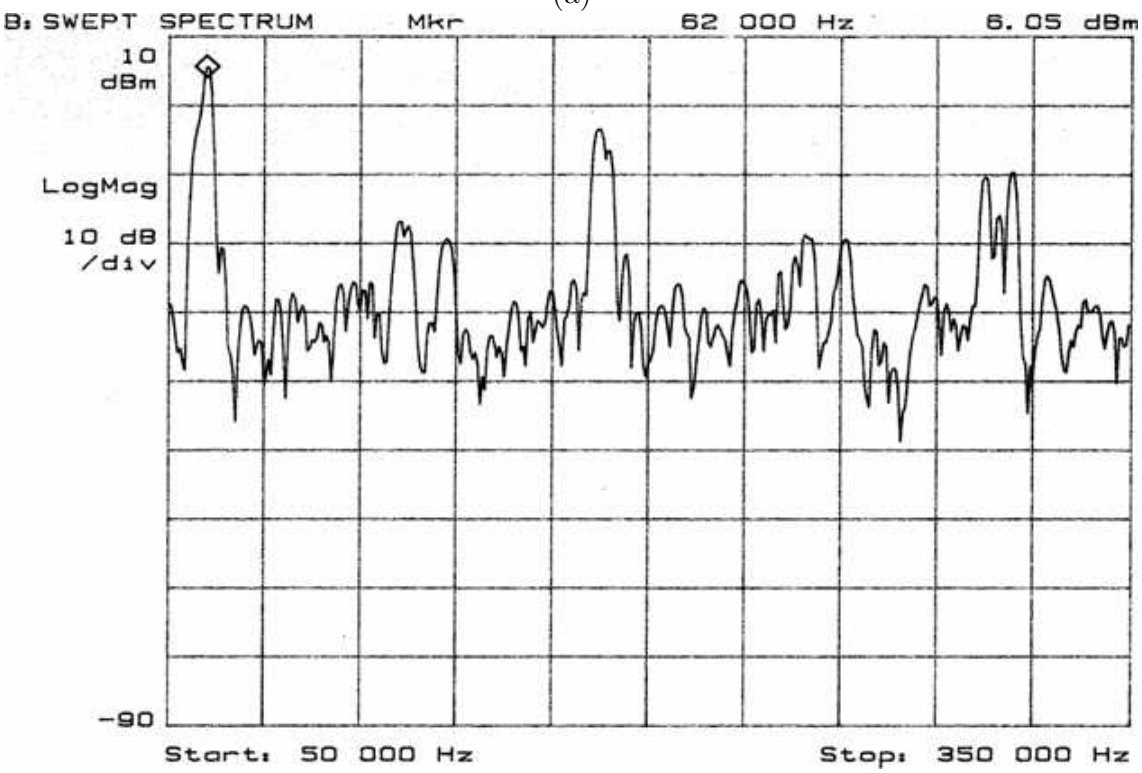
In order to prove that the CL controllers provide adequate regulation to the output voltage, tests to monitor the output voltage transients during load changes are performed with an input voltage of $50V$, which is within the specified input voltage range for all loads, as shown in Section 3.5.

Fig. 6.7 shows the output voltage transients when there is a sudden change in the output current from $6A$ to $2A$. During the transition, the loaded Q_s of the SLR converter reduces. Since the SLR converter is operating beyond resonance, a reduction in Q_s increases the output voltage at the same switching frequency. Therefore, the controller increases the switching frequency to regulate the output voltage back to normal. For both the analogue and digital controllers, it takes around $2.5ms$ for the output voltage to settle to within $0.1V$ of steady-state output.

Fig. 6.8 shows the voltage transients for a step change in output current from $2A$ to $6A$. As the current increases, the loaded Q_s of the SLR converter increases, causing a drop in output voltage. As a result, the feedback compensation reduces the switching frequency

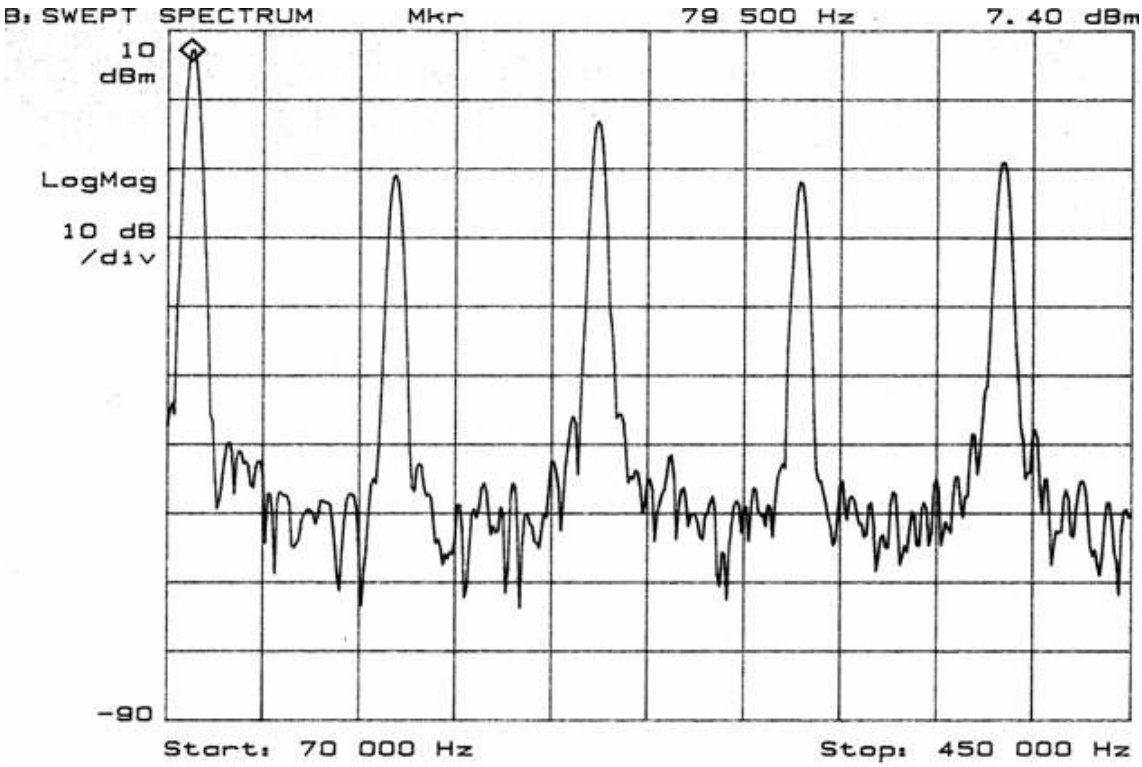


(a)

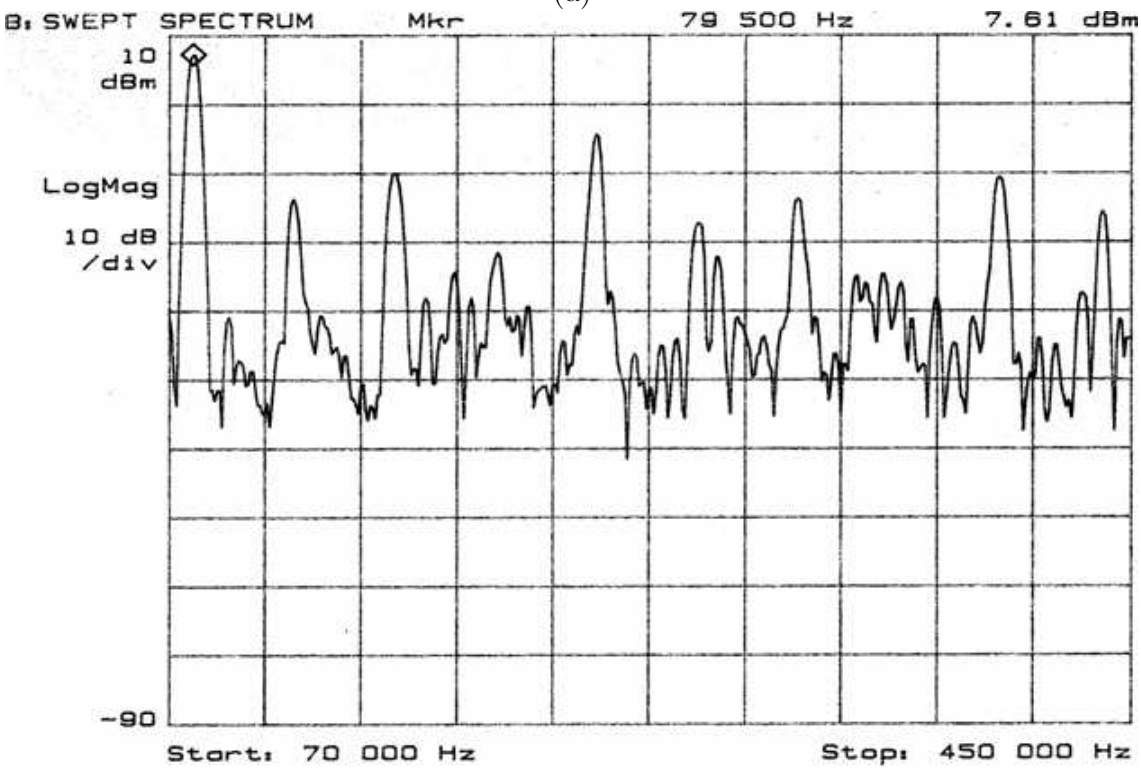


(b)

Figure 6.5 Swept frequency spectra of 62 kHz square waves produced by (a) VCO, and (b) DDS.



(a)



(b)

Figure 6.6 Swept frequency spectra of 80 kHz square waves produced by (a) VCO, and (b) DDS.

to increase the output voltage to the desired level. For both controllers, the settling time of the output voltage is around $1.5ms$.

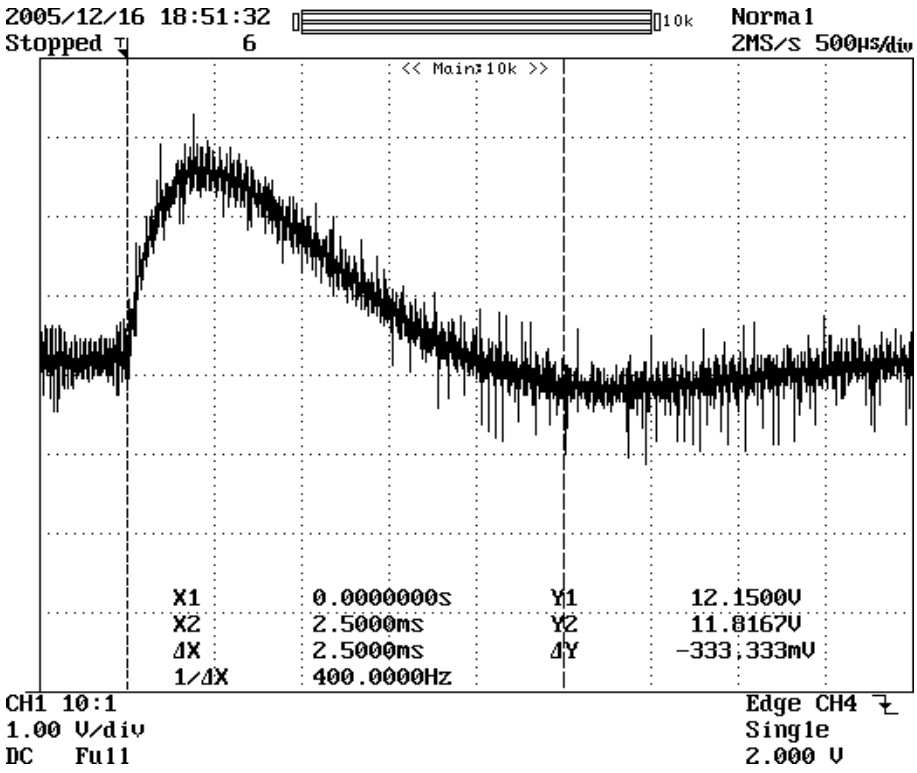
A closer inspection of the voltage transients for the digital controller show that even though the output voltage settles to a reasonable level in both cases, it still exhibits some ripple. Therefore, inspections of the voltage transients in both digital cases are taken over a longer period of time, and shown in Fig 6.9. The results show that for the load change of $6A$ to $2A$, it takes around $5ms$ to settle completely. However, it takes around $6ms$ to settle to steady-state, when the load changes from $2A$ to $6A$, with the latter being a bit more unpredictable. This longer settling time may be caused by the effects of jitter in DDS square waves, making it harder to dampen the output transitions. Unpredictability of the $2A$ to $6A$ case may be due to the higher Q_s of the system, making it more susceptible to frequency variations.

The fact that both controllers perform similarly is expected, because the digital compensation is based on the transfer function of the analogue version, and therefore behaves accordingly. However, the jitter in the DDS square waves may be the cause behind the fact that digital controllers takes a little longer to completely settle down to steady-state.

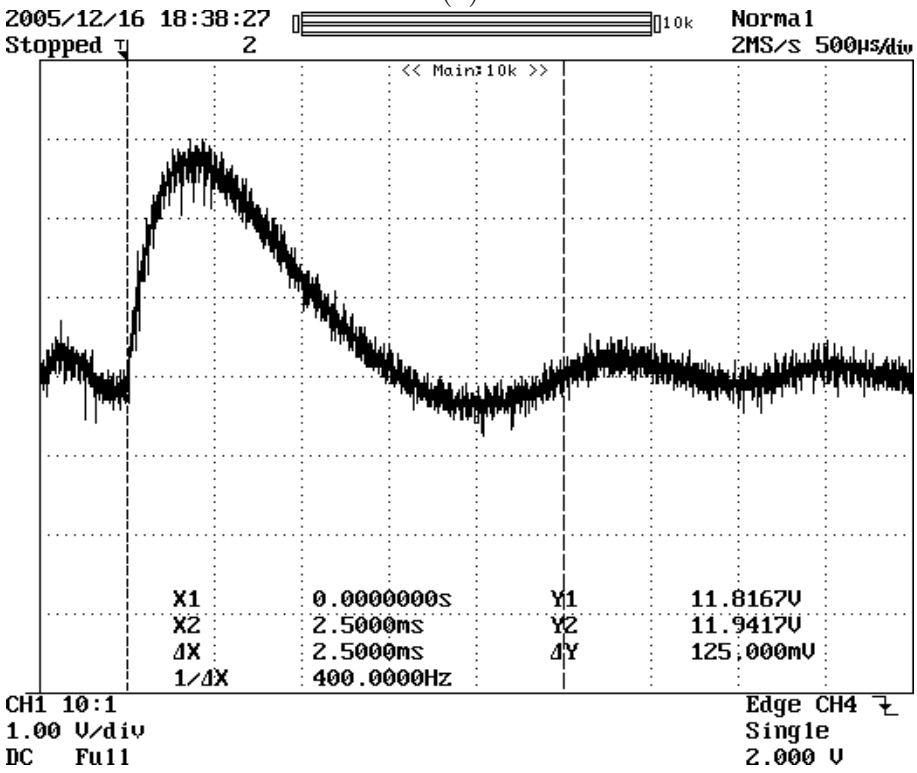
6.4 TIME DOMAIN ANALYSIS OF CHANGING INPUT VOLTAGE

Further experimentation to investigate the effects of input voltage change on output voltage regulation is done to test the stability of the CL SLR systems. In this test, the input voltage is stepped up from $50V$ to $60V$ and then back down again. This change in input voltage just about covers the whole operating input voltage range described in Section 3.5.

The experiment is performed by replacing the input supply with a constant $30V$ DC source in series with a programmable power supply capable of switching between $20V$ and $30V$. The programmable power supply used is *IT6822*, from ITECH, that sources up to $32V$ and $3A$. Tests on the *IT6822* show that both its rise time and fall time for a change of $10V$ are around $600ms$, as expected for realistic power supply changes, which is relatively large compare to the response times for the controllers shown in Section 6.3, all below $10ms$. Therefore, a preliminary assumption is that the change in input voltage is too slow to make the output voltage transients visible.

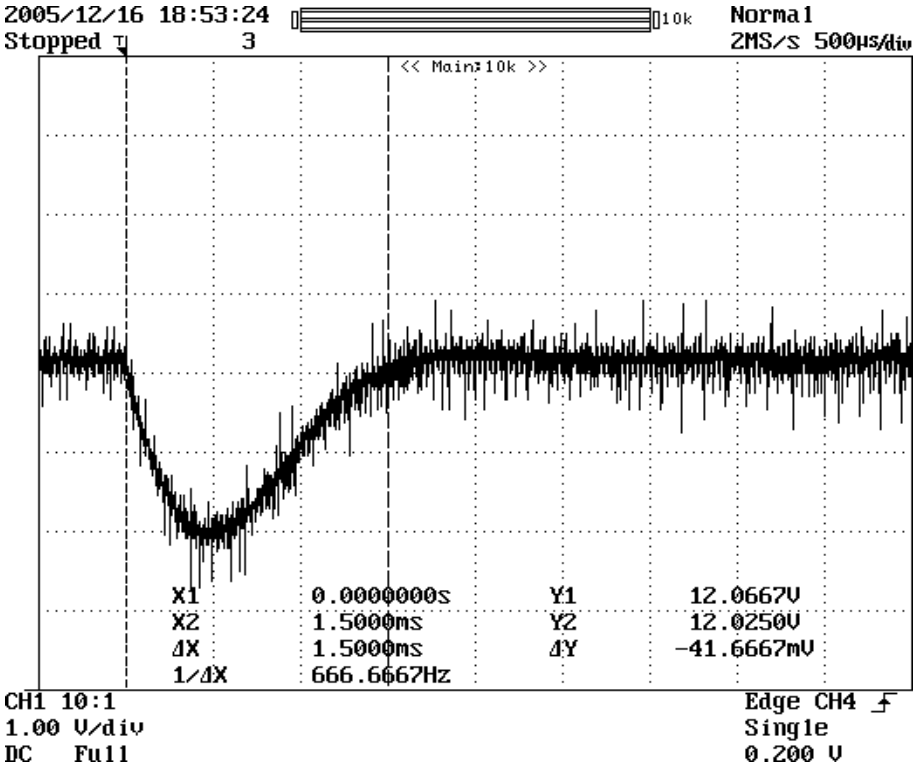


(a)

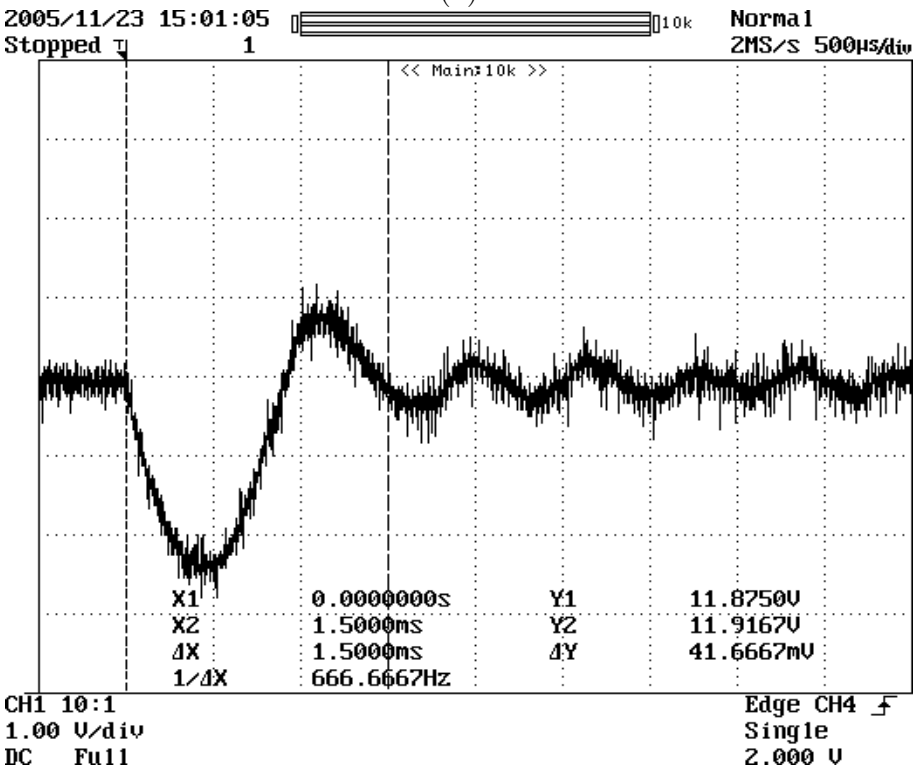


(b)

Figure 6.7 SLR converter output voltage transients when load current changes from $6A$ to $2A$ for (a) analogue control, and (b) digital control.

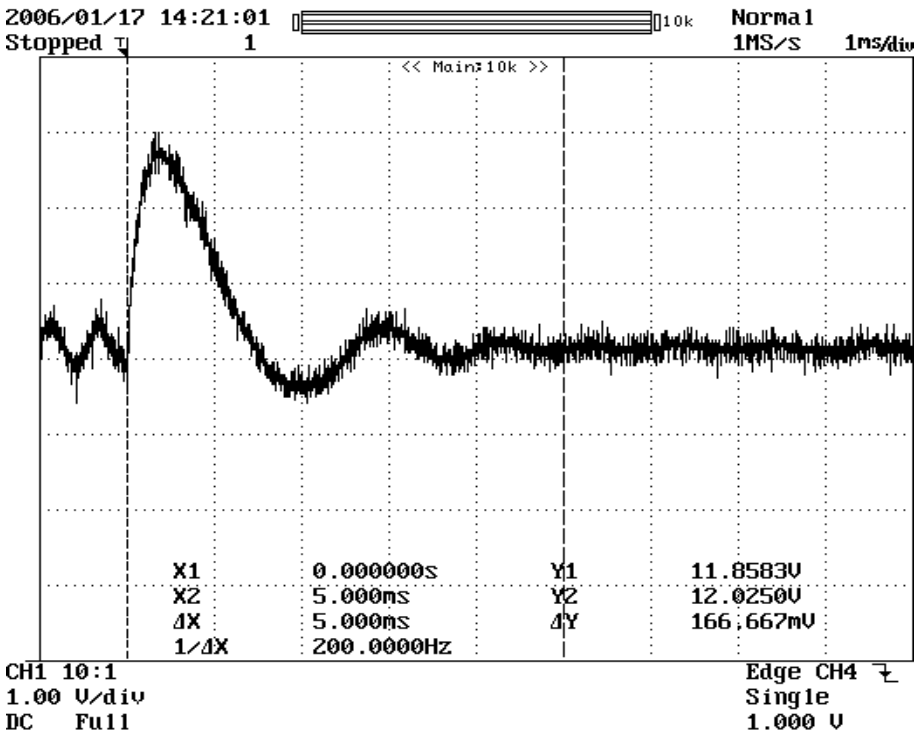


(a)

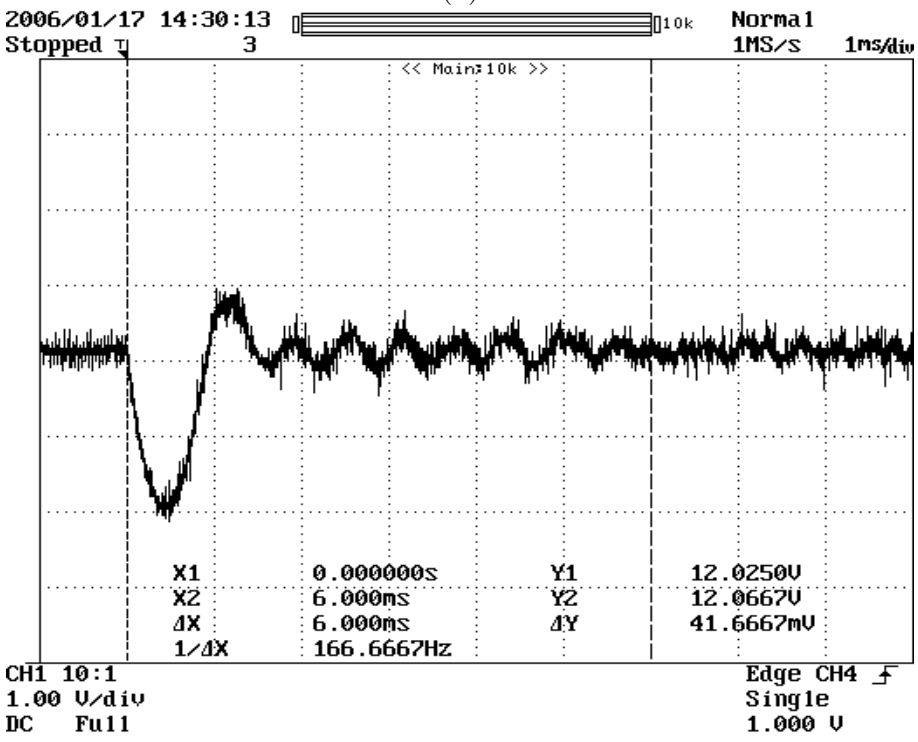


(b)

Figure 6.8 SLR converter output voltage transients when load current changes from $2A$ to $6A$ for (a) analogue control, and (b) digital control.



(a)



(b)

Figure 6.9 SLR converter output voltage transients to steady-state for digital control, with load current changes from (a) $6A$ to $2A$, and (b) $2A$ to $6A$.

Fig. 6.10 shows the changes to the output voltage with respect to a rise in input voltage for both controllers. Since the rectifier diodes are snubber-less, the output ripple caused by the reverse recovery of diodes increases as the input voltage rises. This effect is clearly shown in the analogue controller, as the peak-to-peak ripple voltage rises to $\approx 1.5V$. However, in the digitally controlled system, the output voltage ripple stays almost constant at $\approx 0.7V$ throughout the input voltage change, emphasizing the improved noise immunity advantage described in Section 4.1.1.

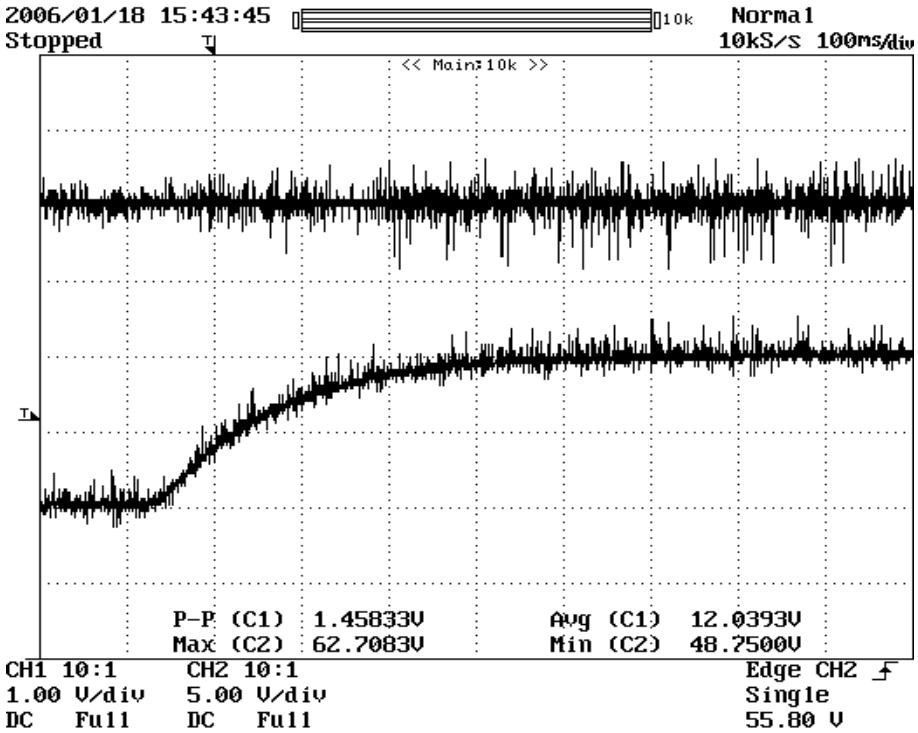
Fig. 6.11 shows the output voltage changes when the input voltage falls from $60V$ to $50V$. Similar to Fig. 6.10, the analogue controlled system started with greater voltage ripple, then the ripple voltage reduces when the supply voltage drops to around $50V$. On the other hand, the digital controller maintains its output voltage ripple during the change in input voltage.

It can be concluded that the digital controller perform better than the analogue controller under noisier operating conditions.

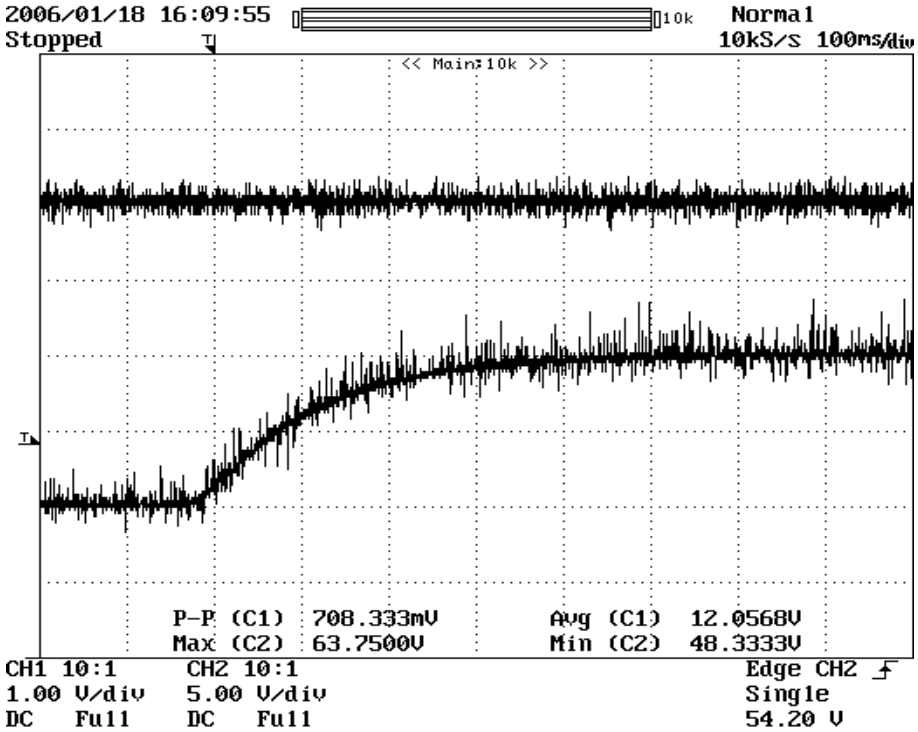
6.5 SUMMARY

The evaluation of the digital control has been presented in the form of time domain and frequency spectral analyses of the switching timing waveforms, and the time domain analyses of output voltage transients with changes in load and input voltage.

The time domain analysis of switching timing waveforms shows that digitally generated square wave signals exhibit jitter, shown as variations in the pulse-widths of adjacent square pulses. This effect is apparent at both 62 kHz and 80 kHz switching signals. The spectral analyses further underline the existence of jitter as the DDS generated signals have a raised noise floor of around 20 dBm, as well as sidebands around the fundamental frequency that cause degradation of the switching signals. Swept spectra of the switching signals cover the frequency range as high as the 5th harmonic of the fundamental frequency. It seems that being the spectra of square waves, both analogue and digital spectra have odd harmonics larger than the adjacent even harmonics, while the digital

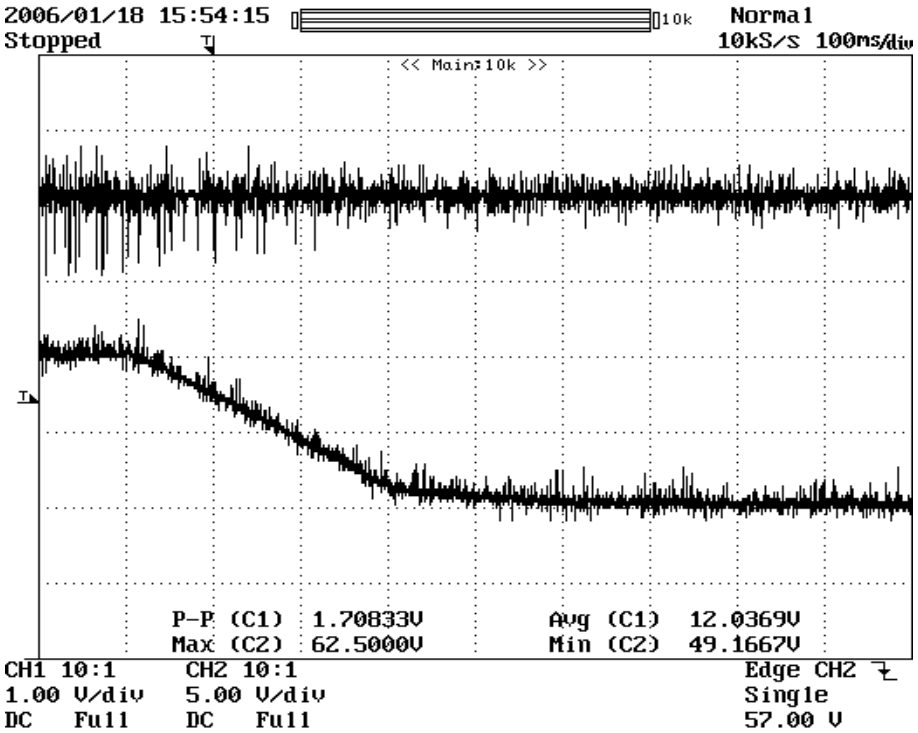


(a)

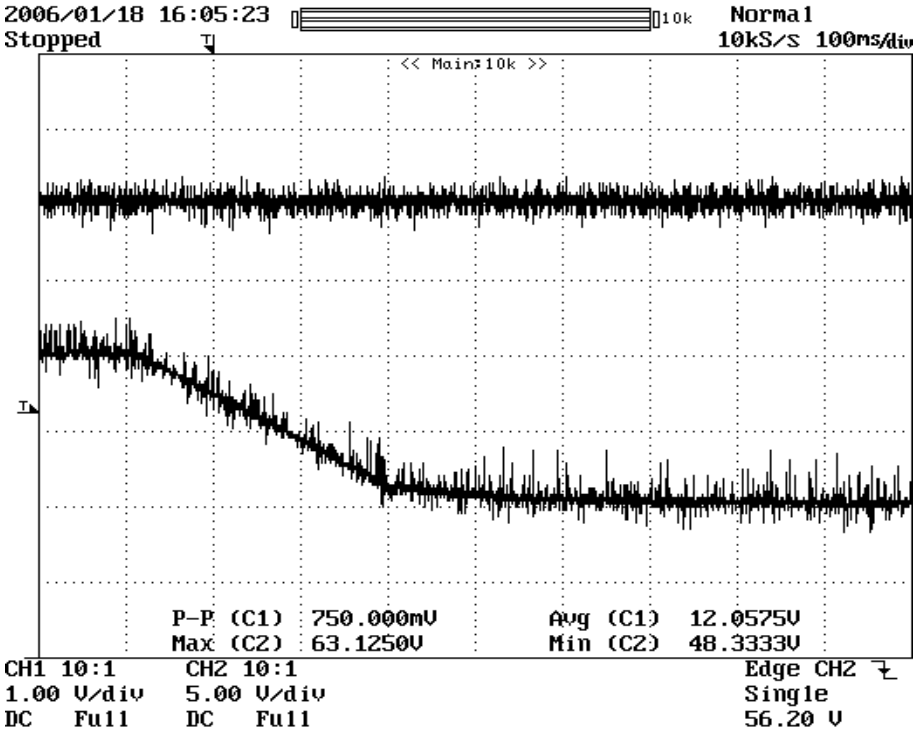


(b)

Figure 6.10 Top trace: output voltage, bottom trace: input voltage of the SLR converter. SLR converter output voltage transients when input voltage changes from $50V$ to $60V$ for (a) analogue control, and (b) digital control.



(a)



(b)

Figure 6.11 Top trace: output voltage, bottom trace: input voltage of the SLR converter. SLR converter output voltage transients when input voltage changes from $60V$ to $50V$ for (a) analogue control, and (b) digital control.

spectra have more unexpected harmonics and a raised noise floor.

The time domain analysis of the transients of output voltage in response to load changes shows both controllers take almost equally long to settle to a reasonable level. When the load current changes from $6A$ to $2A$, it takes both controllers around $2.5ms$ to regulate output voltage. When the load current changes from $2A$ to $6A$, the settling time for the output voltage is around $1.5ms$ for both controllers. But the voltage transients of the digitally controlled system do not completely die out until much later than the time quoted above. This unpredictable damping effect may be caused by the jitter of the switching signals.

Lastly, the time domain analysis for regulating outputs with respect to input voltage changes show that the SLR converter operates at higher noise conditions when the input voltage is high, causing the ripple voltage magnitude to increase for the analogue controlled system. But the same cannot be said about the digitally controlled SLR converter, as the output ripple stays almost constant throughout the input voltage change. Therefore, the digital controller has greater noise immunity than the analogue controller.

Chapter 7

CONCLUDING REMARKS

An SLR converter has been built with both analogue and digital controllers. The analogue controller used is a UC3863N chip that has a built-in error amplifier for feedback compensation as well as an internal VCO for waveform generation. The digital controller is done within a TMS320F2812 DSP that implements both the tasks of feedback compensation and switching signal generation in software. The digital compensator is applied as the discrete form of the analogue compensator designed earlier, while the generation of switching signal is done using DDS algorithm.

The results used for evaluation of the digital controller are the time domain and frequency spectral analyses of the switching waveforms, and the time domain output voltage transients during load and input voltage changes. The time domain waveforms of the switching signals show the DDS generated square waves have jitter that varies the pulse-widths of adjacent square pulses. This signal degradation is also evident in spectral analyses, where the DDS signals have sidebands around the fundamental frequency, as well as a raised noise floor compared to the analogue spectra. These effects are products of the *timer resolution* issue of DDS, where the amplitude transitions are delayed whenever the tuning word does not divide completely into the phase accumulator. The only way to counter that is to use a controller with higher clock and higher instruction throughput to improve the resolution of its timer. The effects of jitter are again visible in the time domain analyses of output voltage transients. Even though the settling times of the transient voltage are comparable for both controllers, unpredictable damping effects of the jitter cause the digital case to take longer to settle to steady-state. But the digital controller is less susceptible to noise and can keep the output voltage ripple small at different input voltages.

Overall, the major challenge of designing a digital controller that generates linearly varying high frequency switching signals has been overcome by implementing DDS algorithm on a fast DSP. Even though the limited parallel processing capability of the DSP resulted in large amounts of overheads in processing both compensation and waveform generation algorithms, jitter did not cause instability to the SLR converter. For future research, it may be interesting to use two controllers, one low-cost microprocessor for digital compensation, and one Field Programmable Gate Array (FPGA) for waveform generation with DDS. The use of two processors eliminates the DDS idle time during ISRs when calculating digital compensation, and the parallel processing ability of FPGA minimises overhead of DDS algorithms. The result may produce a digital controller with better timer resolution. But, the industrial applications of digital controllers are still largely dependent on the costs of the materials, therefore, the transition from analogue control to digital control may still be an economic decision rather than an engineering one.

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APPENDIX A

The half-power point or the bandwidth of the LCR filter is determined by the frequency when the magnitude of series impedance LC is equal to R. n is the factor that the half-power frequency is to the resonant frequency, $\omega_0 = 2\pi \times 60$ kHz is the resonant frequency, $L = 39.789\mu H$ and $C = 176.84nF$.

$$\begin{aligned}
\left| jn\omega_0 L + \frac{1}{jn\omega_0 C} \right| &= R \\
\left| j\left(n\omega_0 L - \frac{1}{n\omega_0 C} \right) \right| &= R \\
\sqrt{\left(n\omega_0 L - \frac{1}{n\omega_0 C} \right)^2} &= R \\
\left(\frac{n^2\omega_0^2 LC - 1}{n\omega_0 C} \right)^2 &= R^2 \\
\left(\frac{n^2 - 1}{0.0667n} \right)^2 &= R^2
\end{aligned}$$

$n > 1$ because operating above resonance,

$$\begin{aligned}
\frac{n^2 - 1}{0.0667n} &= R \\
n^2 - 1 &= R0.0667n \\
n^2 - R0.0667n - 1 &= 0
\end{aligned}$$

for $R = 6\Omega$,

$$\begin{aligned}
n &= \frac{0.4 + \sqrt{0.4^2 + 4}}{2} \\
&\approx 1.22
\end{aligned}$$

for $R = 1.5\Omega$,

$$\begin{aligned} n &= \frac{0.1 + \sqrt{0.1^2 + 4}}{2} \\ &\approx 1.05 \end{aligned}$$

Therefore, when $R = 6\Omega$, the half-power frequency is $1.22\omega_0$, while the parameter is $1.05\omega_0$ when $R = 1.5\Omega$.

APPENDIX B

This section shows the MATLAB codes used in the modelling of both analogue and digital controllers.

approx.m This file is used to calculate both the uncompensated and compensated transfer functions of the SLR converter at various operating conditions. The analogue compensator is then digitised to model the digitally compensated SLR converter.

```
%SLR components
Lr = 41.63e-6;
Cr = 180e-9;
Cf = 220e-6;
vo = 12;                    %output voltage
R = 6                       %load resistance
vg = 29.13/2                %input voltage
Q = sqrt(Lr/Cr)/R           %loaded Q
f0 = 1/(2*pi*sqrt(Lr*Cr))   %resonant frequency
w0 = 2*pi*f0
fs = 62e3                   %switching frequency
ws = 2*pi*fs
ff = fs/f0

%Approximation of control to output transfer function
%=A/((1+s/wfs)*(1+s/(w0s*Q0s)+s^2/w0s^2))
%refer to V. Vorpoerian, "Approxiamte small-signal analysis of the series
%and the parallel resonant converters," IEEE Transactions on Power Power
%Electronics, vol. 4, no. 1, pp.15-24, January 1989.
M = vo/vg
```

```
gamma = pi*f0/fs
h = -2/gamma
A0 = -2;
A = A0/M
ks = 1 + 1/((Q*gamma/2*cot(gamma/2))^2*(1-h/(M*Q)));
wfs = ks/(R*Cf)
w0s = ws - w0
Q0s = Q/ks
s = tf('s')
sys1 = A/((1+s/wfs)*(1+s/(w0s*Q0s)+s^2/w0s^2))

%Sensor design
R = 2.2e3;           %resister in LP filter
C = 6.8e-9;          %filter capacitor
sense = 1/(1+s*R*C)  %transfer function of sensor
sys1 = sys1*sense    %OL of SLR + sensor
figure(1)
bode(sys1)           %bode plot of OL of uncompensated SLR

%Compensator design
fc = 6e3                %crossover frequency of compensator
mag = 10                %original gain at crossover frequency
R1 = 1e3                %input resistor
G = 1/10^(mag/20)       %required attenuation at crossover frequency
C1 = 100e-9             %feedback resistor
sysn = (1+1/(s*R1*C1))  %compensator transfer function
figure(2)
bode(sysn)              %bode plot of compensator

%Compensated converter analysis
convo = sys1*sysn  %transfer function of OL compensated SLR
figure(3)
margin(convo)      %bode plot of OL compensated SLR
```

```
%Digitising feedback compensator
T = 5e-6;                              %sampling period of 5us
sysd = c2d(sysn,T)                     %digitise the analogue compensator
num = [1 -0.9375];
den = [1 -1];
sysd = tf([1 -0.9375],[1 -1],5e-6)     %tf of digital compensator
sysc = d2c(sysd)
sysd = sysc*sys1                       %tf of digitally compensated SLR
figure(4)
margin(sysd)                           %plot of digitally compensated SLR
```

APPENDIX C

This section shows the C codes used to program the TMS320F2812 DSP to perform digital control.

control.c This file consists of an infinite loop that performs DDS waveform generation, and an ISR that measures the ADC value and calculates digital compensation.

```
#include <DSP28_Device.h>
#include <ADCcalibrationDriver.h>

interrupt void ADC_ISR(void);

//allocate calibration driver variables:
ADC_CALIBRATION_DRIVER_VARS adc;

//initialize frequency parameters for this program:
#define CPU_FREQ  75E6    //CPU frequency
#define PWM_FREQ  200E3   //the frequency for ADC interrupt
#define PWM_PRD  CPU_FREQ/PWM_FREQ

//DDS constants
#define MIN_M 1600              //minimum tuning word (fs around 60kHz)
#define MAX_M 2200              //maximum tuning word (fs around 80kHz)
#define VREF 152                //ADC value for measurement of 12V

//initialise global variables for digital compensator
int16 voltage;                  //measured vo
int16 x_last = 0;               //error, vo - vref, last state
```

```
int16 x_now = 0;                //error, vo - vref, current state
int16 y_last = 0;               //compensator output, last state
int16 m = MAX_M;                //tuning word M
Uint16 deadtime = 0;

int main(void)                  //main loop
{
  Uint16 phase = 0;             //initialise phase accumulators

  //initialize System Control registers, PLL, WatchDog:
  InitSysCtrl();

  //initialize PIE module:
  InitPieCtrl();
  EALLOW;                       //enable access to protected registers
  PieVectTable.ADCINT = &ADC_ISR;
  EDIS;                         //disable access to protected registers
  PieCtrlRegs.PIEIER1.bit.INTx6 = 1;  //enable PIE INT1.6 = ADCINT

  //initialize ADC:
  ADCcalibrationInitAdc();

  //initialize Calibration Driver Variables:
  ADCcalibrationDriverInit(&adc);

  //initialize Event Manager:
  InitEv();
  EvaRegs.T1PR = PWM_PRD;   //setup period register
  EvaRegs.T1CMPR = PWM_PRD; //setup T1 compare value for 0% duty cycle

  //enable core interrupts:
  IER |= M_INT1; //ADC Interrupt

  //enable global interrupts and real-time mode:
```

```
  EINT;                       //enable global interrupt INTM
  ERTM;                       //enable global realtime interrupt DBGM

  EALLOW;
  GpioMuxRegs.GPAMUX.all=0x0000;     //GPIOA as digital I/O
  GpioMuxRegs.GPADIR.all=0xFFFF;     //GPIOA as outputs
  GpioMuxRegs.GPAQUAL.all=0x0000;    //input qualifier disabled
  GpioDataRegs.GPACLEAR.all=0xFFFF;  //GPIOA cleared

  GpioMuxRegs.GPBMUX.all=0x0000;     //GPIOB as digital I/O
  GpioMuxRegs.GPBDIR.all=0x0000;     //GPIOB as inputs
  GpioMuxRegs.GPBQUAL.all=0x0000;    //input qualifier disabled

  GpioMuxRegs.GPDMUX.all=0x0000;     //GPIOD as digital I/O
  GpioMuxRegs.GPDDIR.all=0xFFFF;     //GPIOD as outputs
  GpioMuxRegs.GPDQUAL.all=0x0000;    //input qualifier disabled
  GpioDataRegs.GPDSET.all=0xFFFF;    //GPIOD set

  GpioMuxRegs.GPFMUX.all=0x0000;     //GPIOF as digital I/O
  GpioMuxRegs.GPFDIR.all=0xFFFF;     //GPIOF as outputs
  GpioDataRegs.GPFCLEAR.all=0xFFFF;  //GPIOF cleared
  EDIS;

  //power up external ADC
  while (deadtime < 20)
    {
       deadtime++;
    }
  deadtime = 0;

  //start conversion
  GpioDataRegs.GPDCLEAR.bit.GPIOD6 = 1;
  GpioDataRegs.GPDSET.bit.GPIOD6 = 1;
```

```
  for (;;)                    //loop forever
  {
    phase = phase + m;        //accumulate phase and ignore overflow

    if (phase < 32768)        //check phase
    {
      GpioDataRegs.GPFCLEAR.bit.GPIOF4 = 1;
      while (deadtime < 2)    //implement deadtime
      {
        deadtime++;
      }
      deadtime = 0;
      GpioDataRegs.GPFSET.bit.GPIOF5 = 1;
    }
    else
    {
      GpioDataRegs.GPFCLEAR.bit.GPIOF5 = 1;
      while (deadtime < 2)    //implement deadtime
      {
        deadtime++;
      }
      deadtime = 0;
      GpioDataRegs.GPFSET.bit.GPIOF4 = 1;
    }
  }
}

interrupt void ADC_ISR(void)   //interrupt service routine
{
    //reinitialize interrupt for next ADC sequence:
    AdcRegs.ADCTRL2.bit.RST_SEQ1 = 1;       //reset SEQ1
    AdcRegs.ADCST.bit.INT_SEQ1_CLR = 1;     //clear INT SEQ1 bit
    PieCtrlRegs.PIEACK.all = PIEACK_GROUP1; //acknowledge interrupt
```

```
    //ADC read operations
    GpioDataRegs.GPDCLEAR.bit.GPIOD0 = 1;
    GpioDataRegs.GPDCLEAR.bit.GPIOD5 = 1;    //extra instruction to
    GpioDataRegs.GPDCLEAR.bit.GPIOD5 = 1;    //synchronise ADC output
    voltage = GpioDataRegs.GPBDAT.all - 65280;

    //GpioDataRegs.GPADAT.all = voltage;    //show adc voltage on LEDs
    GpioDataRegs.GPDSET.bit.GPIOD5 = 1;
    GpioDataRegs.GPDSET.bit.GPIOD0 = 1;

    //digital compensation, y[k] = x[k] - 0.9411*x[k-1] + y[k-1]
    x_last = x_now;                          //update previous error
    x_now = voltage - VREF;                  //update current error
    y_last = m;                              //update previous output
    m = x_now - x_last*15/16 + y_last;       //update tuning word

    //make sure the tuning word is within the boundary
    if (m < MIN_M)
    m = MIN_M;
    if (m > MAX_M)
    m = MAX_M;

    //start ADC conversion again
    GpioDataRegs.GPDCLEAR.bit.GPIOD6 = 1;
    GpioDataRegs.GPDSET.bit.GPIOD6 = 1;
    return;
}
```