Class-B Balanced Single-Ended Dual-Fed Distributed Power Amplifier

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Abstract:

The distributed amplifier approach allows the output powers of several FETs to be combined without the need for multi-way power combiners. In this paper we demonstrate that a balanced amplifier employing two single-ended dual-fed distributed amplifiers can operate effectively under class-B operation. Class-B operation and dual-feeding allow distributed amplification with significantly improved efficiencies compared to conventional distributed power amplifiers. The FETs are spaced 180 degrees to allow all FETs operate into identical optimum loadlines. The configuration uses all FET output power and has good port match.

1. Introduction

Parallel power combining methods can be used to combine the output powers of N FETs. Because of the difficulty in realising compact planar N-way power combiners, typical FET power amplifiers use corporate (tree) power dividers assembled from either branch line or Lange couplers. Although such 2-way dividers are easy to design, the size of the resulting power dividing and combining networks is large and increases with increasing number of FETs and restricted N to a maximum of four.

Distributed amplification offers an alternative method to combine FET output power without the need for multi-way power combiners. However, the conventional distributed amplifier (DA) suffers from low efficiency as up to half of the FET output power is wasted in the idle drain line termination [1]. The presence of both forward and reverse travelling waves on the drain line results in uneven sub-optimal utilisation of the FETs [1][2]. Further the DA topology is not directly amenable to class-B operation.

In this paper we present a class-B balanced amplifier that comprises two single-ended dual-fed distributed amplifiers. Class-B operation and dual-feeding allows significantly improved efficiency compared to conventional distributed amplifiers. The balanced configuration ensures good port match. Only two hybrids

are required regardless of the number of FETs combined. The bulk of the power combining is done by way of wave superposition on the drain lines.

2. Dual-Fed Distributed Amplifier

The dual-fed distributed amplifier approach (DFDA) [3] can be used to improve the efficiency by combining the waves appearing at both ends of the drain line. Figure 1 depicts a DFDA employing 4 FETs equally spaced, a hybrid to feed both ends of the gate line, and a hybrid to combine waves appearing at both ends of the drain line.

Figure 1: Circuit diagram of a 4-FET dual-fed distributed amplifier.

When 180° hybrids are used to feed both the gate and drain lines, both the forward and reverse gain are combined in-phase [4]. For an even number of FETs, the FET drain voltages and currents are equal when the FETs are spaced 180° at the centre frequency [5]. With equal drain voltages and currents, the FETs have equal output power [1] and operate into identical loadlines allowing them all to be optimum [5].

The DFDA however suffers from severe mismatch at its input and output ports. Analysis of the DFDA with an even number of FETs spaced 180° and uses 180° hybrids, reveals that the midpoints along the gate and drain lines may be short-circuited to earth without disturbing the operation of the FETs at the centre frequency [6]. The result is a pair of isolated amplifiers, called single-ended dual-fed distributed amplifiers (SE-DFDA) [7]. Replacing the 180° hybrids with 90° hybrids results in a balanced amplifier with inherently matched ports [6][7]. Figure 2 depicts a balanced amplifier comprised of two 2-FET SE-DFDAs whose FETs are spaced 180° . The gate and drain line short-circuit terminations allow ease of FET biasing. Like the DFDA, the circuit structure of the SE-DFDA is uniform and does not require tapering of the gate and drain lines, as has been previously proposed to improve the efficiency of conventional DAs [8].

Figure 2: Circuit diagram of a 4-FET balanced single-ended dual-fed distributed amplifier.

3. Class-B Operation of the SE-DFDA

Figure 3 shows an idealised FET i/v characteristic that shows the salient features:

- (i) V_{Dmin} - boundary between the triode and saturation regions,
- (ii) V_{Dmax} - upper boundary of FET saturation before onset of drain breakdown,
- (iii) I_{Dmax} - maximum allowable drain current often dictated by the maximum gate voltage before the onset of gate conduction,
- (iv) Optimum class-B and class-A load trajectories,
- (v) Drain bias voltage V_{DD} .

It can be seen from Figure 3 that the optimum load resistance for class-A operation is $(V_{Dmax} - V_{Dmin})/I_{Dmax}$.

Figure 3: Ideal FET output i/v characteristic with optimum class-A (dashed line) and class-B (thick line) load trajectories.

Under class-B, the FET gate is biased so that it conducts for half a cycle, and hence the drain current is a half-wave rectified wave-form (with peak I_{Dmax}) that contains dc, fundamental and even harmonic components. So that the drain voltage contains only dc and fundamental components, the FET drain terminals must be short-circuited at the even harmonics. With reference to Figure 2, the short-circuit terminations of the drain line transform to short-circuits at the FET drains at even harmonics and open-circuits at the fundamental and odd harmonics. Although odd harmonics are not short-circuited, they are not overwhelming for a well-designed GaAs power FET under class-B operation. It can be shown that the optimum class B load resistance at the fundamental is the same as the optimum class-A load resistance. Hence we can use same optimum drain line characteristic impedance as the class-A case [5]:

$$Z_{O_D} = \frac{V_{Dmax} - V_{Dmin}}{n I_{Dmax}} \quad (1)$$

where n is the number of FETs in a single SE-DFDA. This expression considers the effect of all voltage waves on the drain line and the FET output i/v characteristics [5]. For both classes, it is apparent from Figure 3 that the drain bias voltage is $(V_{Dmin} + V_{Dmax})/2$.

4. Design and Simulation

To test and demonstrate this approach, a class-B balanced amplifier employing two 2-FET SE-DFDAs was designed for operation at 1.8 GHz. Fujitsu FLK012WF packaged power GaAs FETs were used. Based on the FET data sheets, V_{Dmin} , V_{Dmax} and I_{Dmax} are 1V, 10V and 60mA respectively. Using (1), the optimum drain line characteristic impedance is $75\ \Omega$. The optimum drain bias voltage is 5.5 V and the gate bias voltage was set to -1.9 V (being slightly above the threshold voltage). Under this condition, the theoretical load power (P_L) under full class-B drive is 270 mW (24.3 dBm), the theoretical dc power (P_{dc}) is 420 mW, and hence the theoretical drain efficiency (P_L / P_{dc}) is 64 %. By choosing the gate line characteristic impedance to be $30\ \Omega$, the effects of loading by the FET input are minimal at 1.8 GHz and yet the corresponding microstripline width is not too wide. The branch-line hybrids were matched to $50\ \Omega$ at all ports, hence quarter-wave transformers were used to couple them to the gate and drain lines. The driven ends of the gate and drain lines were extended by 10° and 40° at 1.8 GHz respectively to ensure circuit stability with class-A biasing.

During circuit simulation, a Statz-Raytheon FET model fitted to data sheet i/v characteristics and s -parameters was used to represent the FET. Figure 4 shows the simulated output power and efficiency versus input power at 1.8GHz. It can be seen that the output power at the 1dB gain compression point is 24.8dBm, and the dc and power added efficiency are 61.4 % and 49.8 % respectively. The small-signal gain is about 8 dB. Figure 5 shows good input and output match over a broad range of frequencies. Figure 6 shows the simulated FET load trajectories at the internal drain current source at various frequencies. The trajectories show that the load trajectories are nearly identical and are close to ideal class-B trajectories over a broad range of frequencies. The looping is mainly due to FET output parasitics.

5. Conclusion

We have demonstrated that a single-ended dual-fed distributed amplifier can operate effectively under class-B conditions. Distributed amplification using the single-ended distributed amplifier approach offers a viable method of combining FET output power without the need for multi-way power combiners. Dual-feeding allows

collection of all FET output power and optimal use of the i/v characteristics of all FETs. The single-ended distributed amplifier is straightforward to design and uses uniform gate and drain transmission lines. A balanced amplifier employing two single-ended distributed amplifiers offers good input and output match.

Figure 4: Simulated output power and efficiency at 1.8 GHz.

Figure 5: Simulated small-signal input and output reflection coefficients.

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Figure 6: Simulated FET load trajectories at internal drain current source.