Gate Bias Control and Harmonic Load Modulation for a Doherty Amplifier

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ABSTRACT

Linearity and efficiency are both critical parameters for radio frequency transmitter applications. In theory, a Doherty amplifier is a linear amplifier that is significantly more efficient than comparable conventional linear amplifiers. It comprises two amplifiers, connected at their outputs by a quarter-wave transformer. The main amplifier is always on, while the peaking amplifier is off during low power levels. Load modulation of the main amplifier occurs when the peaking amplifier is on due to the quarter-wave transformer, ensuring the main amplifier never enters saturation. This results in an efficiency characteristic that increases with respect to input power at twice the normal rate at low power levels, and plateaus to a high value at high power levels. However, in much of the research that has been done to-date, less-than-ideal results have been achieved (although efficiency was better than a conventional amplifier). It was decided to investigate the cause of the discrepancy between theoretical and practical results, and devise a method to counteract the problem.

It was discovered that the main cause of the discrepancy was non-ideal transistor gate-voltage to drain-current characteristics. The implementation of a gate bias control scheme based upon measured transistor transfer characteristics, and the desired main and peaking amplifier output currents, resulted in a robust method to ensure near-ideal results. A prototype amplifier was constructed to test the control scheme, and theoretical, simulated and measured results were well matched. The amplifier had a region of high efficiency in the high power levels (over 34% for the last 6 dB of input power), and the gain was nearly constant with respect to input power (between 4 and 5 dB over the dynamic range).

Furthermore, it was decided to investigate the role harmonics play within the Doherty amplifier. A classical implementation shunts unwanted harmonics to ground within the main and peaking amplifiers. However, odd harmonics generated by the peaking amplifier can be used to operate the main amplifier like a class F amplifier. This means its supply voltage can be lowered, without the amplifier entering saturation, and the efficiency of the Doherty amplifier can be increased without a detrimental effect on the its linearity. A prototype amplifier was constructed to test this theory, and gave good results, with better efficiency than that of a conventional amplifier, and a constant gain with respect to input power (between 6.4 dB and 6.5 dB over the dynamic range).

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PREFACE

The following papers were prepared during the course of this work:

K. W. Eccleston, K. J. I. Smith, P. T. Gough, and S. I. Mann,"Harmonic load modulation in Doherty amplifiers," *Electronics Lett.*, vol. 44, no. 2, pp. 128-129, Jan. 2008

K. J. I. Smith, K. W. Eccleston, P. T. Gough, and S. I. Mann, "The effect of FET soft turn-on on a Doherty amplifier," *Microwave and Opt. Tech. Letters*, vol. 50, no. 7, pp. 1861-1864, Jul. 2008

K. J. I. Smith, K. W. Eccleston, P. T. Gough, and S. I. Mann, "A theoretical basis for Doherty amplifier bias control based on drain current characteristics," *Microwave and Opt. Tech. Letters*, vol. 51, no. 9, pp 2152-2156, Sep. 2009

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Chapter 1

INTRODUCTION

1.1 INTRODUCTION

This Chapter gives background information into why Doherty amplifiers are desirable (Sections 1.2 to 1.4), briefly discusses the objectives of this research (Section 1.5), discusses the scope of the work done (Section 1.6), outlines the original contributions made in the course of this research (Section 1.7), and gives an overview of the structure of this thesis (Section 1.8).

1.2 BACKGROUND

In the modern environment, radio frequency (RF) technology is more pervasive than ever. Two of the most prevalent applications are land mobile radio and cell phones. Land mobile radios have been around since the 1920s [1], and are still used in many fleets of vehicles, including taxis, buses, trucks, and emergency response vehicles. Cell phones are being used with increasing frequency, especially since the advent of the affordable smart phone, which allows a user to email, txt, call, pxt, and browse the internet, from any location where they get reception.

No matter what era or which application, it is always desirable to have high efficiency. In modern RF applications, the power amplifier tends to use the largest portion of the power supplied to the system, meaning its efficiency has the largest impact on the efficiency of the whole system. High DC-to-RF conversion efficiency reduces both power supply and RF power transistor cooling requirements. In mobile applications, high efficiency leads to reduced battery size and prolonged battery life. In base station applications, high efficiency leads to reduced power demand, both directly and indirectly (through lower cooling requirements). As base stations are often situated in remote locations that are difficult to access and electrify, any decrease in power requirements is highly desirable.

Linearity of the transmitter is critical for digital modulation schemes. Conventional linear amplifiers (e.g. class A) have increasing efficiency with increasing input power,

reaching maximum efficiency at maximum input power (see Appendix B). This results in low average efficiency when using modulation schemes that modulate the carrier amplitude, such as quadrature-amplitude modulation (QAM). Such schemes rarely operate at maximum input power, as shown in Figure 1.1, which gives the voltage distribution of a 16-QAM band-limited signal. It should be noted that if unlimited bandwidth is available, QAM has a finite number of amplitude states (in the case of 16-QAM, there are three). However, with limited bandwidth (such as in Figure 1.1), there is significant variation within each of these amplitude states.

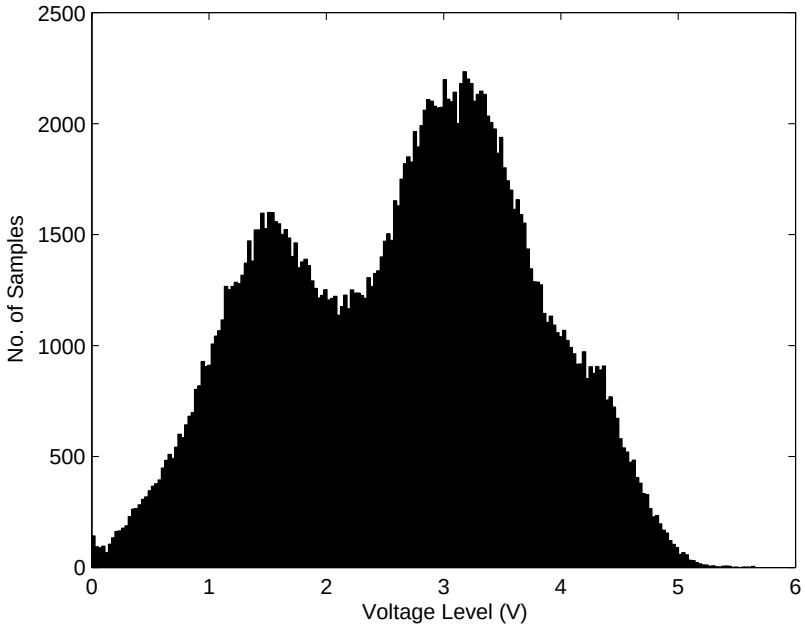


Figure 1.1: Distribution of the voltage for a 16-QAM signal

Since both efficiency and linearity are critical parameters for power amplifiers, there have been several circuit configurations proposed to maintain the linearity of the amplifier, while increasing the efficiency in the mid-power range. These circuits are more complex than conventional power amplifier circuits, but have the potential to significantly improve its performance when modulation schemes such as QAM are used. The three main enhancement techniques are Doherty amplifiers, envelope elimination and restoration (EER), and linear amplification using non-linear components (LINC).

1.3 COMPARISON OF EFFICIENCY ENHANCEMENT TECHNIQUES

There have been several efficiency enhancement techniques proposed for power amplifiers, but the three main ones (Doherty amplifiers, envelope elimination and restoration, and linear amplification using non-linear components) have been around for decades.

Doherty amplifiers [2], and outphasing or Chireix amplifiers [3] (from which stemmed the term LINC) were invented in the '30s. EER was invented by Kahn in the early '50s [4]. An overview of these techniques is given in the following sections.

1.3.1 Doherty Amplifiers

A Doherty amplifier comprises two amplifiers (one main, one peaking), connected by a quarter-wave transformer at the output (see Figure 1.2). The amplifier has two distinct regimes of operation - low power and high power. The switch-over point is at half of the maximum input voltage, or 6 dB below maximum input power (these are equivalent). During the low power regime, the peaking amplifier is biased off, and does not draw any power from the supply. The impedance of the quarter-wave transformer connecting the main amplifier to the load resistance is chosen such that, in this regime, the main amplifier sees twice its optimum load impedance. This means that as the input power increases, the output power (and efficiency) increase at double the normal rate. During the high power regime, the peaking amplifier turns on, and starts to contribute to the output power of the Doherty amplifier. Its output causes the main amplifier's load impedance to decrease (due to the quarter-wave transformer), meaning the main amplifier's output current continues to increase with increasing input power, but its output voltage stays constant and saturation does not occur. The main amplifier is normally biased in class AB or class B, while the peaking amplifier is usually biased in class C (as it has automatic threshold behaviour).

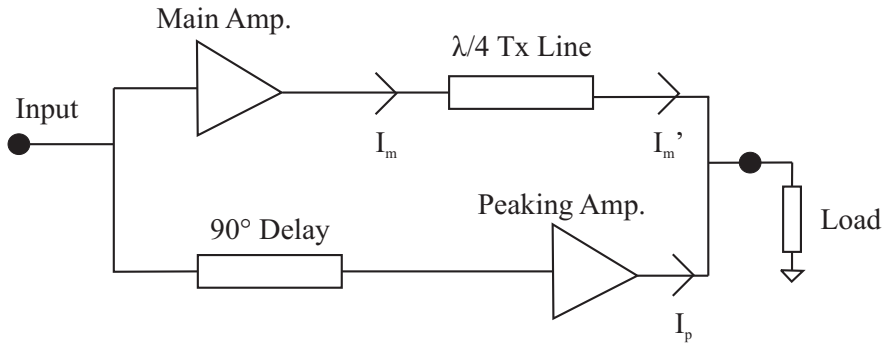


Figure 1.2: Doherty amplifier circuit design

As well as the components discussed above, a 90° delay is inserted at the input to the peaking amplifier, to ensure the output currents of the main and peaking amplifier arrive at the load resistance in phase. This is often portrayed as being another quarter-wave impedance transformer, but the delay can be created using any convenient method. There has been a large amount of research carried out in the last decade on Doherty amplifiers, with numerous variations on the original circuit proposed to generate high efficiency and linearity, while maintaining a simple circuit design.

1.3.2 Envelope Elimination and Restoration

The envelope elimination and restoration (EER) method of improving amplifier efficiency is a relatively simple concept; the input signal passes through a limiter before being amplified, which gives the signal a constant amplitude, but retains any phase modulation information. The amplifier can then be non-linear, designed to operate in saturation, and designed to have maximum efficiency at this value of input power (which it will see for all values of input power). In order to restore any amplitude modulation information to the signal, the envelope of the signal is measured (before the limiter), and this information is used to modulate the DC supply of the amplifier (see Figure 1.3).

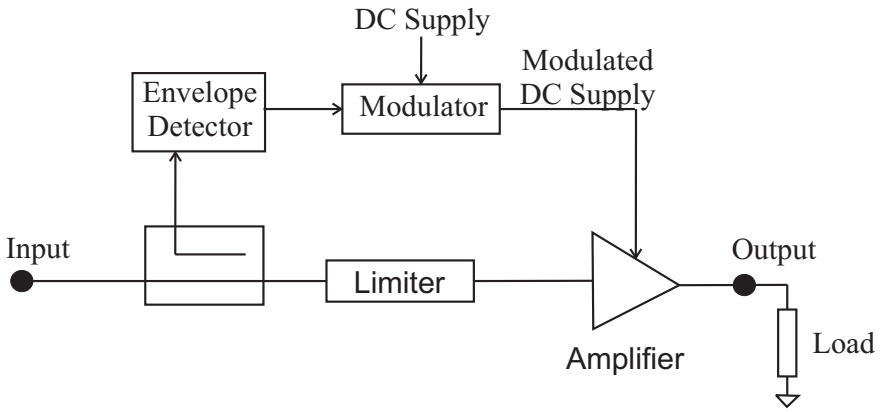


Figure 1.3: Envelope elimination and restoration circuit design

EER is theoretically the most efficient of the techniques available, as the amplifier is held at its maximum efficiency for all values of input power [5]. However, there are a number of challenges to be overcome before this technique can reach its full potential. The most significant is that a high efficiency power converter needs to be realised, otherwise any improvements in amplifier efficiency are countered by low power converter efficiency. It is worth noting that variations on EER have also been proposed, such as envelope tracking, where the amplifier's supply is decreased to give higher efficiency when the input power is low, but the amplifier itself is linear, and maintains the amplitude and phase modulation information in the signal. This obviously gives a lower average efficiency than EER, but is also simpler to implement.

1.3.3 Linear Amplification using Non-linear Components

Linear amplification using non-linear components (LINC, also known as outphasing or Chireix) is the most complex of the three efficiency-enhancing techniques discussed. It is similar to the Doherty amplifier, in that it uses two amplifiers whose outputs are summed, but neither of the amplifiers need to be linear. Instead, the two amplifiers are fed signals with different time-varying phases. This phase modulation creates an

output signal with the desired amplitude modulation, due to the trigonometric identity

$$\cos(A) + \cos(B) = 2\cos\left(\frac{A+B}{2}\right)\cos\left(\frac{A-B}{2}\right)$$

The input signals to the two amplifiers are chosen with phases equal to $\omega t + \cos^{-1}(V_{in})$ and $\omega t - \cos^{-1}(V_{in})$, where V_{in} is the amplitude of the input signal [6]. This results in an output signal with phase $\cos(\omega t)$, and amplitude $2GV_{in}$ (where G is the gain of the amplifier). In order for this technique to result in a high efficiency amplifier, the load of the two amplifiers needs to be modulated as well. The load resistance of the LINC amplifier is thus connected between the outputs of its two amplifiers, with a shunt capacitance and inductance to tune out drain reactances at a particular amplitude [5]. High efficiency results around this point, meaning a high average efficiency can be obtained for any signal with a known peak-to-average power ratio.

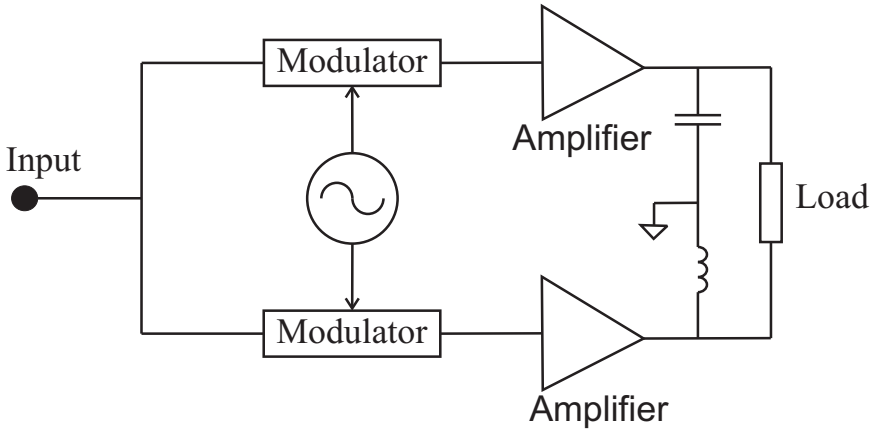


Figure 1.4: Circuit design for linear amplification using non-linear components

The complexity of implementing this technique has decreased due to the ubiquitous use of DSPs in modern applications. However, it is still a technique that has high overheads associated with it (such as generating the desired input signals). Furthermore, the load of the amplifier is not grounded, which in itself creates difficulties. Nonetheless, the ability to choose the point of maximum efficiency is attractive and, in an ideal implementation, it has a high efficiency characteristic over a broad dynamic range [6].

1.4 THE DOHERTY AMPLIFIER

Of the three techniques discussed in Section 1.3, the Doherty amplifier is the simplest circuit, although EER and LINC can potentially attain a larger dynamic range of high efficiency [5]. The simplicity of the circuit means that any difficulties with the operation of the amplifier have a small number of potential causes. The ideal Doherty amplifier

output characteristics are given in Figure 1.5, which shows that it is a linear amplifier (i.e. gain does not vary with input power), and that the efficiency characteristic is significantly better than the most efficient of the conventional linear amplifiers (class B). The exemplifying feature of the Doherty amplifier is its efficiency characteristic, where you get high (nearly constant) efficiency over a 6 dB range. Furthermore, the amplifier is linear throughout the dynamic range. For these reasons there has been a lot of interest in the Doherty amplifier over the past decade. It should be noted that the gain of the amplifier is dependent on the transistor size, where the size of the transistor is its maximum output current (which is proportional to the gate width in the case of a FET and the area of the emitter in the case of a BJT) . On the other hand, the efficiency characteristic is ideally independent of the transistor size.

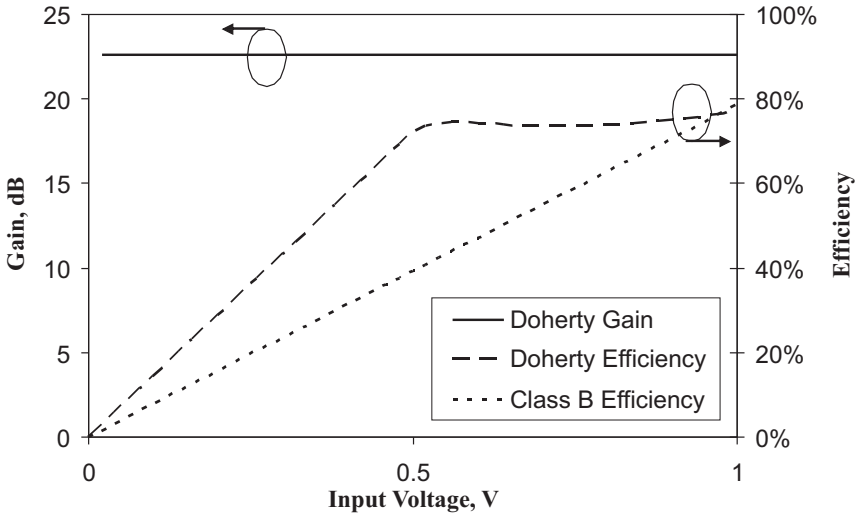


Figure 1.5: Efficiency and gain of an ideal Doherty amplifier and efficiency of a conventional class B amplifier

Unfortunately, a large portion of the research done on Doherty amplifiers has shown less-than-ideal results. Almost all the research carried out has achieved an improvement in efficiency compared with a conventional amplifier, but this has often been at the cost of linearity. More significantly, the efficiency improvement has been distinctly lower than that predicted by theory, and is often a continuously increasing characteristic, rather than a characteristic with a region of high efficiency in the high power region. On occasion, near-theoretical output characteristics have been reported but with little or no discussion on the design techniques used.

At the outset of the research conducted for this thesis, it was intended to investigate Doherty amplifier configurations with multiple peaking amplifiers. In the course of this research, and as a baseline for comparison, a standard Doherty amplifier was designed and constructed using unequal transistor sizes (see Section 2.4). The circuit was simple, comprising: two amplifiers, a quarter-wave transformer, and a branch-line coupler.

The transistor sizes were chosen to give near-ideal output current characteristics (see Chapter 4), and the amplifiers were designed to operate into their optimum load of 150 Ω (which necessitated the use of quarter-wave transformers at the amplifier outputs to match to the 50 Ω load at the output). The prototype amplifier is shown in Figure 1.6.

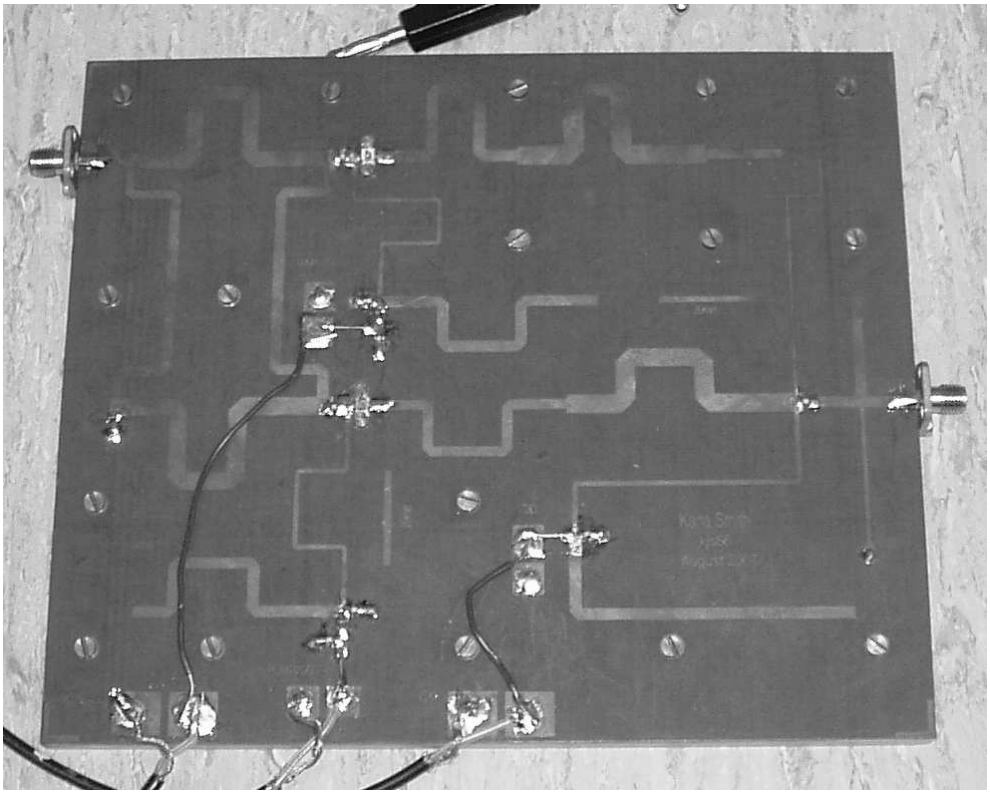


Figure 1.6: Photo of the first prototype Doherty amplifier, using unequal transistor sizes

The simulated output characteristics[1] of this amplifier showed near-theoretical Doherty amplifier behaviour, and the S-parameters of the prototype were a close match to the simulated S-parameters. However, large signal testing of the amplifier showed that there was a large discrepancy between the simulated results and the measured results. As mentioned, this is a fairly wide-spread problem, so the research focus shifted to addressing this issue. Three important points were learnt from this exercise:

1. Minor differences in FET model parameters were exacerbated by the Doherty circuit configuration.

2. The FET output conductance was an issue for the Doherty circuit.

3. The Doherty amplifier's performance was sensitive to the gate bias of both the main and peaking amplifiers.

[1]The simulations were done using the harmonic balance method in AWR Microwave Office [7] (see Appendix A)

The first and third points indicated that a gate bias control system that was based upon the gate-voltage to drain-current transfer characteristics of the transistors had the potential to guarantee Doherty operation, regardless of the transistor parameters. The output conductance of the FETs is both rate-dependent and finite, even in class C, but is treated as a constant in the circuit simulator. Although this simplification doesn't cause problems for class A amplifiers, it is questionable for class B and class C (see Appendix C for further details). As the prototype design utilised quarter-wave transformers at the output of the main and peaking amplifiers to match the 50 Ω load to a more-optimal value of 150 Ω, the FET output conductance was conversely transformed to a low value at the output of the Doherty amplifier, thereby reducing efficiency. It was decided that future prototypes would be designed such that the main and peaking amplifiers operated directly into 50 Ω loads, which would simplify the circuit by removing the need for these quarter-wave impedance transformers, and would also ameliorate the problems caused by the output conductance.

1.5 RESEARCH OBJECTIVE

Doherty amplifiers are a potentially elegant solution to the problem of low average efficiency power amplifiers, due to modulation schemes having a high peak-to-average power ratio. However, modern implementations of the Doherty amplifier often have output characteristics that are significantly worse than those predicted by theory (although they improve on a conventional amplifier). This is not always the case, leading to the conclusion that Doherty output characteristics are achievable. As such, it was desired to determine:

- What is the cause of the difference between the theoretical Doherty amplifier characteristics and those achieved in a practical implementation?
- How can this difference be eliminated, so that near-theoretical characteristics are achieved, regardless of transistor parametric variation?
- What role do harmonics play in the Doherty amplifier, and can they be used to advantage?

1.6 SCOPE

The scope of this research involved a number of different factors - the specific transistors used, frequency of operation, simulation set-up, and test set-up. These were chosen for a variety of different reasons (outlined in the following paragraphs), and were used throughout this body of work.

The Eudyna FLK017WF[2] transistor was chosen, as it has successfully been used in previous work [8, 9], and a model was available for use in simulations. Furthermore, it is a K-band device, which was operated at a lower frequency, meaning that parasitics aren't a limiting factor (although they are included in simulations). The Eudyna FLC057WG[2] was chosen as it was the transistor (within the same range of devices) that was closest to giving the desired ratio between the main and peaking amplifier transistors (see Section 2.4.1 and Appendix C).

The design frequency was chosen to be 770 MHz. A frequency under 1 GHz meant that transistor parasitics would be minimal, while the specific frequency was proposed by Tait Electronics Ltd (the sponsor for this work). However, it is difficult to match the input of the transistor at this frequency. Any matching at the input would be very narrow band, and wouldn't necessarily be at the same centre frequency as the rest of the amplifier due to manufacturers' tolerances. As such, the inputs of the transistors have been treated as an open circuit, and the outputs have been treated as current sources, resulting in lower gain.

The simulations were carried out using harmonic balance simulations in AWR Microwave Office [7]. These are used to solve for the large signal steady state response. See Appendix A for further details on the software.

The test set-up was as follows. A signal generator was connected to the input of the prototype board. Power supply and gate bias were connected to the board from digital power supplies (via digital multimeters where desired). The output power was measured by a power meter. It should be noted that in each case, only the Doherty amplifier was realised on the prototype board. Any bias control was carried out manually. A digital controller was not used, although one could be realised as part of a complete system which includes a Doherty amplifier.

1.7 ORIGINAL CONTRIBUTIONS

This thesis discusses several original contributions that were made to the body of work concerning Doherty amplifiers. These were:

- Investigation of the effect of transistor soft turn-on and non-identical maximum transistor drain currents on the output characteristics of a Doherty amplifier
- Creation of a gate bias control strategy that would ensure Doherty output characteristics with equal transistor sizes and equal transistor input power, regardless of transistor non-idealities (specifically, soft turn-on and non-identical maximum drain currents)

[2] http://www.us.eudyna.com/e/index.html

- Improvement of the efficiency of a Doherty amplifier that uses unequal transistor sizes, by strategically using harmonics.

1.8 OVERVIEW OF THESIS

A unified analysis of the Doherty amplifier using ideal transistors is given in Chapter 2 as a basic background on the subject. It covers both the design equations of a Doherty amplifier, and techniques to achieve Doherty output characteristics with ideal transistors. It also discusses the amplifier output characteristics achieved if the circuit is constructed with equal input power, equal transistor sizes and no bias control (i.e. if no techniques are used to increase the peaking amplifier's output current). The theory and analysis of Doherty amplifiers is given before the literature review, as it gives necessary background to the discussion.

Chapter 3 examines the existing literature on the topic of Doherty amplifiers. A more detailed examination of the research question and direction is presented in Chapter 4, along with an analysis of the problems caused in a Doherty amplifier by transistor non-linearities and parametric variation. Chapter 5 discusses a novel gate bias control method whereby near-theoretical Doherty amplifier output characteristics can be achieved regardless of transistor parameters and non-linearities. Chapter 6 discusses a method to improve the efficiency of a Doherty amplifier by using harmonic load modulation. Finally, Chapter 7 summarises the work done for this thesis, and recommends some directions further research could take.

Chapter 2

UNIFIED DOHERTY AMPLIFIER ANALYSIS USING IDEAL TRANSISTORS

2.1 INTRODUCTION

As mentioned in Chapter 1, a Doherty amplifier [2] has the potential for high efficiency over a wide range of input powers. A classical Doherty amplifier comprises two amplifiers, connected at their outputs by a quarter-wave transformer, as shown in Figure 2.1. The quarter-wave transformer has a key role to play in the operation of a Doherty amplifier, which will become clear later in the chapter. The 90° delay ensures that the signals of the main and the peaking amplifiers arrive at the load in phase. The main amplifier operates continuously, while the peaking amplifier only operates at high power levels, as indicated by the ideal fundamental current characteristics shown in Figure 2.2. The quarter-wave transmission line provides impedance transformation for the main amplifier - meaning as the peaking amplifier's output power increases, the impedance seen by the main amplifier will decrease. This is known as active load-pulling, which ensures the main amplifier operates at maximum output voltage, but does not saturate.

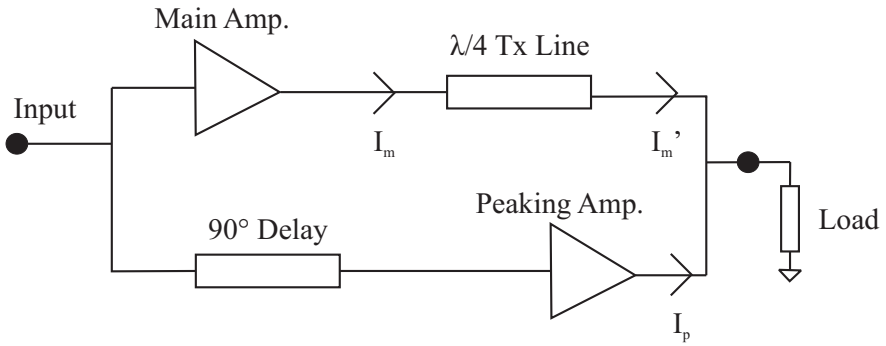


Figure 2.1: Doherty amplifier circuit design

The main amplifier is normally biased in class AB or class B, while class C is often used for the peaking amplifier, as it can automatically turn on and off at the appropriate power level [10, 11]. For the purposes of this investigation, it is assumed

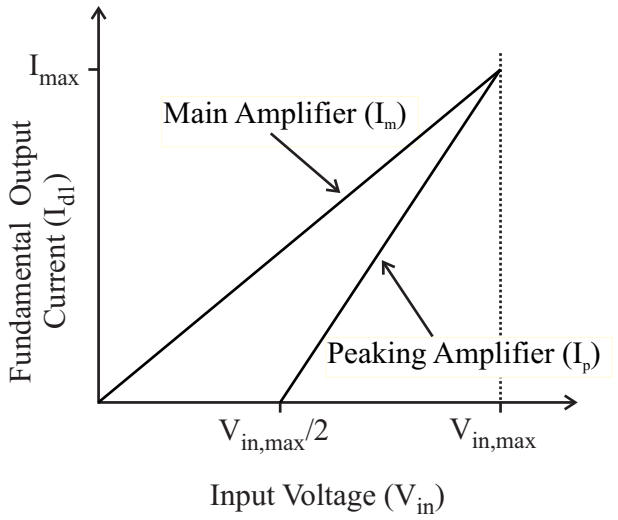


Figure 2.2: Desired fundamental current characteristics of the main and peaking amplifiers

the main amplifier is biased in class B, as this gives better efficiency than a class AB amplifier, while still being a linear amplifier (which is required, as shown in Section 2.2.1). As such, in order to analyse a practical Doherty amplifier, an understanding of class B and class C amplifiers is beneficial. This analysis is given in Appendix B for completeness.

Section 2.2 gives a basic analysis of a Doherty amplifier, where it is assumed that the desired fundamental output current characteristics are achieved, without details on how this occurs. Section 2.3 discusses the Doherty amplifier used in the theoretical analyses of the following sections, including a circuit layout, and a description of an ideal transistor. Section 2.4 analyses Doherty amplifiers which attempt to closely mimic the desired fundamental output current characteristics, while Section 2.5 covers the simplest implementation of the Doherty amplifier circuit, whose fundamental current characteristics only loosely approximate those described in Doherty's paper [2].

2.2 BASIC ANALYSIS OF AN IDEAL DOHERTY AMPLIFIER

2.2.1 Main and Peaking Amplifier Output Equations

If the outputs of the main and peaking amplifiers are represented as ideal current sources, a Doherty amplifier can be represented as shown in Figure 2.3, where the amplitudes of i_m and i_p as a function of the input voltage, V_{in}, are as shown in Figure 2.2. From the peaking amplifier characteristic, it can be seen that the operation of a Doherty amplifier can be separated into two regions:

1. The low power region, where $V_{in} \leq V_{in,max}/2$, and the peaking amplifier is off.

2. The high power region, where $V_{in,max}/2 < V_{in} \leq V_{in,max}$, and both amplifiers are on.

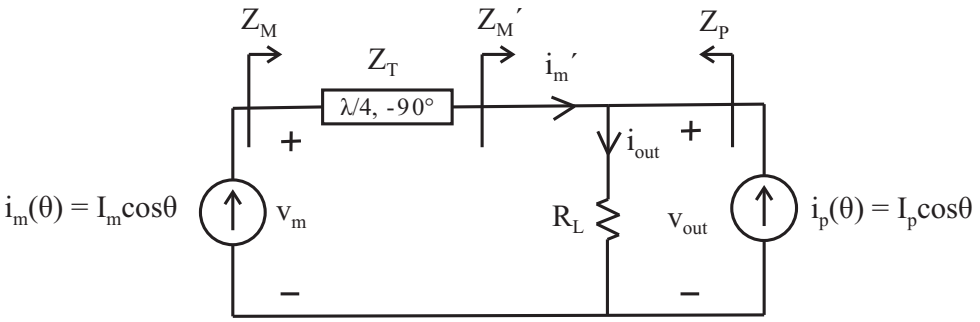


Figure 2.3: Equivalent Doherty amplifier circuit

From Figure 2.3, several equations can immediately be written:

$$V_{out} = I'_m Z'_M \tag{2.1}$$
$$= I_{out} R_L \tag{2.2}$$
$$I_{out} = I'_m + I_p \tag{2.3}$$

If the $\lambda/4$ transmission line is assumed to be ideal, (and hence lossless,) then

$$Z_T^2 = Z_M Z'_M \tag{2.4}$$

Using ABCD parameters to represent the $\lambda/4$ transmission line, the voltage and current on the main amplifier side of the transmission line, in terms of that at the load side, are

$$\begin{bmatrix} V_m \\ I_m \end{bmatrix} = \begin{bmatrix} 0 & jZ_T \\ j/Z_T & 0 \end{bmatrix} \begin{bmatrix} V_{out} \\ I'_m \end{bmatrix}$$

$$V_m = jZ_T I'_m \tag{2.5}$$
$$I_m = \frac{j}{Z_T} V_{out} \tag{2.6}$$

From (2.6) it can be seen that the output voltage is constrained to be directly proportional to the output current of the main amplifier. This means that if the main amplifier output current is directly proportional to V_{in}, as shown in Figure 2.2, the Doherty amplifier's output is also directly proportional to V_{in}.

2.2.2 Optimum Values of R_L and Z_T

To ensure high efficiency, R_L and Z_T are chosen such that both amplifiers reach maximum efficiency at maximum input voltage ($V_{in,max}$). As a reference point, $R_{L,B}$ is defined as the optimal value of load resistance if the main amplifier was operated as a stand alone class B amplifier.

Several boundary conditions can be established to help determine the optimum values of R_L and Z_T. Firstly, as discussed in Appendix B, to get maximum efficiency from the amplifiers at maximum input voltage,

$$V_m = V_{out} = V_{DD} \qquad \text{when } V_{in} = V_{in,max} \tag{2.7}$$

where V_{DD} is the amplifier supply voltage. Secondly, from Figure 2.2 it can be seen that

$$I_m = I_p = I_{max} \qquad \text{when } V_{in} = V_{in,max} \tag{2.8}$$

Finally, since both amplifiers will contribute equally to the output power at maximum input voltage,

$$I'_m = I_p = I_{max} \qquad \text{when } V_{in} = V_{in,max} \tag{2.9}$$

Substituting (2.9) into (2.3) gives

$$I_{out} = 2I_{max} \qquad \text{when } V_{in} = V_{in,max} \tag{2.10}$$

The load resistance, R_L of the amplifier can now be found in terms of $R_{L,B}$, using (2.7), (2.10) and (B.9):

$$\begin{aligned} R_L &= \frac{V_{out}}{I_{out}} \\ &= \frac{V_{DD}}{2I_{max}} && \text{when } V_{in} = V_{in,max} \\ &= \frac{R_{L,B}}{2} && \text{when } V_{in} = V_{in,max} \end{aligned} \tag{2.11}$$

Using (2.1), (2.7), and (2.9) gives

$$\begin{aligned} Z'_m &= \frac{V_{out}}{I'_m} \\ &= \frac{V_{DD}}{I_{max}} && \text{when } V_{in} = V_{in,max} \\ &= R_{L,B} && \text{when } V_{in} = V_{in,max} \end{aligned} \tag{2.12}$$

By definition, Z_M is the ratio of V_m to I_m:

$$\begin{aligned} Z_m &= \frac{V_m}{I_m} \\ &= \frac{V_{DD}}{I_{max}} && \text{when } V_{in} = V_{in,max} \\ &= R_{L,B} && \text{when } V_{in} = V_{in,max} \end{aligned} \tag{2.13}$$

Substituting (2.12) and (2.13) into (2.4) gives the optimum value of Z_T:

$$Z_T = R_{L,B} \tag{2.14}$$

$$= 2R_L \tag{2.15}$$

Equations (2.11) and (2.14) are important design equations for designing a Doherty amplifier.

2.2.3 Voltage Characteristics

Using the equations from Sections 2.2.1 and 2.2.2, the output voltage characteristics for the two amplifiers can de determined. In the low power region, the main amplifier's voltage can be determined easily, as it has a constant load of $2R_{L,B}$, and reaches a maximum of V_{DD} at $V_{in} = V_{in,max}/2$.

From (2.6), it is seen that the peaking amplifier's output voltage, (which is the output voltage of the Doherty amplifier,) is proportional to the main amplifier's output current, I_m. As I_m increases linearly with respect to V_{in}, the peaking amplifier's output voltage also increases linearly with V_{in}, reaching a maximum of V_{DD} at $V_{in} = V_{in,max}$.

Starting with (2.5), then using (2.14), (2.3), (2.2), (2.11) and (2.6), the main amplifier's output voltage can be obtained in terms of I_m and I_p:

$$V_m = R_{L,B}\left(2I_m - jI_p\right) \tag{2.16}$$

From Figure 2.2, equations for I_m and I_p can be determined (noting that I_p lags I_m by 90°):

$$I_m = \frac{I_{max}}{V_{in,max}} V_{in} \tag{2.17}$$

$$jI_p = \frac{2I_{max}}{V_{in,max}} V_{in} - I_{max} \qquad \text{when } V_{in,max}/2 \le V_{in} < V_{in,max} \tag{2.18}$$

Substituting these into (2.16), and using the equations developed in Appendix B, gives

$$\begin{aligned} V_m &= R_{L,B} I_{max} && \text{when } V_{in,max}/2 \le V_{in} < V_{in,max} \\ &= V_{DD} && \text{when } V_{in,max}/2 \le V_{in} < V_{in,max} \end{aligned}$$

This means that throughout the high power regime, the main amplifier's output voltage is held at a constant V_{DD}. However, its output power is increasing as its output current continues to increase with increasing input voltage. The resulting voltage transfer characteristic is shown in Figure 2.4 along with the desired current transfer characteristic. It should be noted that V_{out} is directly proportional to V_{in} (via (2.6) and (2.17)), meaning the Doherty amplifier is linear.

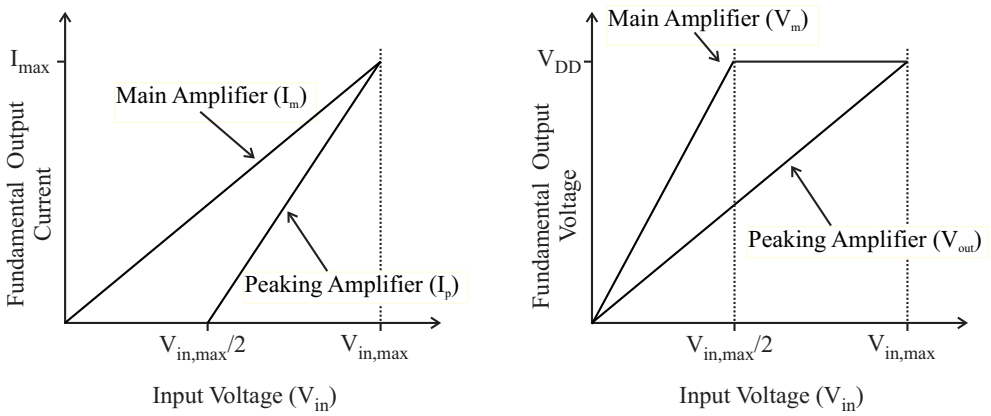


Figure 2.4: Main and peaking amplifier current and voltage characteristics

Dividing the voltage of the main amplifier by its current at each value of V_{in} gives the main amplifier's load impedance, Z_m, which is shown in Figure 2.5. During the low power regime, the main amplifier's load impedance is twice that of a comparable class B amplifier, meaning the amplifier reaches peak efficiency at half of maximum input voltage. However, once the peaking amplifier turns on, the main amplifier's load impedance decreases, from $2R_{L,B}$ to $R_{L,B}$ (since V_m is constant and I_m continues to increase). This impedance change is critical to the operation of the Doherty amplifier, as it ensures that the main amplifier's output voltage stays under V_{DD}, and saturation doesn't occur.

Figure 2.6 shows the loadline of the main amplifier with four different input voltage values - the two threshold values of $V_{in} = V_{in,max}/2$ and $V_{in} = V_{in,max}$, and examples of the loadlines in the low power regime and the high power regime. It can be seen that in the low power regime the load of the main amplifier is constant. However, during the high power regime the load of the main amplifier changes with increasing input voltage, and it is the output voltage of the amplifier that is constant. It should be noted that the x-axis shows the output voltage, not the fundamental output voltage, which is why the amplifier reaches $2I_{max}$ at maximum input voltage.

The amplifier's efficiency characteristic is dependent on the method used to implement the peaking amplifier. However, regardless of the implementation, in the low power regime the peaking amplifier is off, and it doesn't draw any power from the supply. In the high power regime the main amplifier has maximum voltage swing. These two facts contribute to the amplifier achieving high efficiency throughout the dynamic

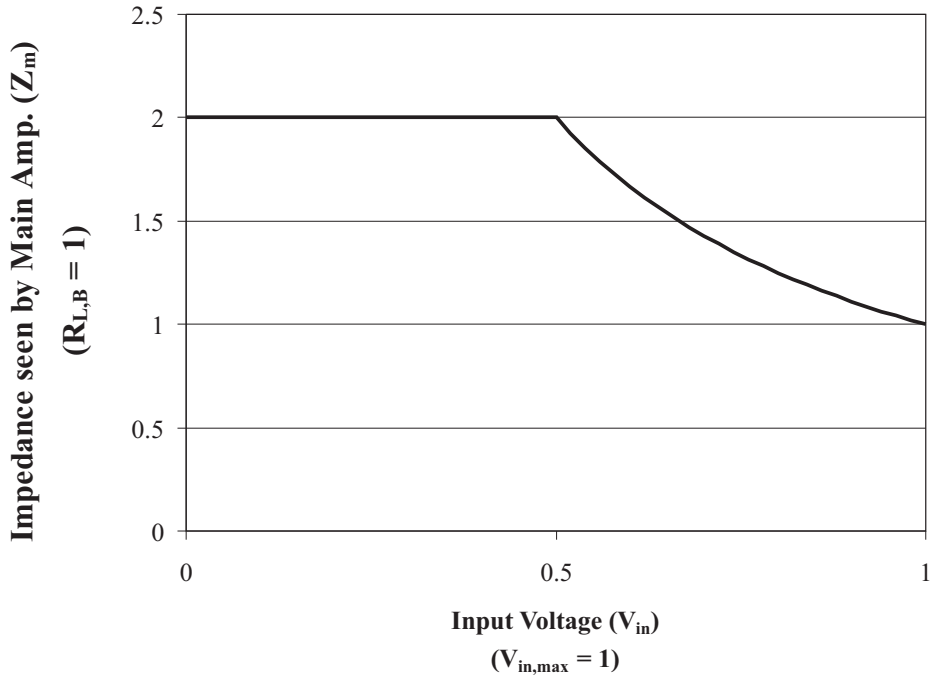


Figure 2.5: Load modulation of the impedance seen by the main amplifier

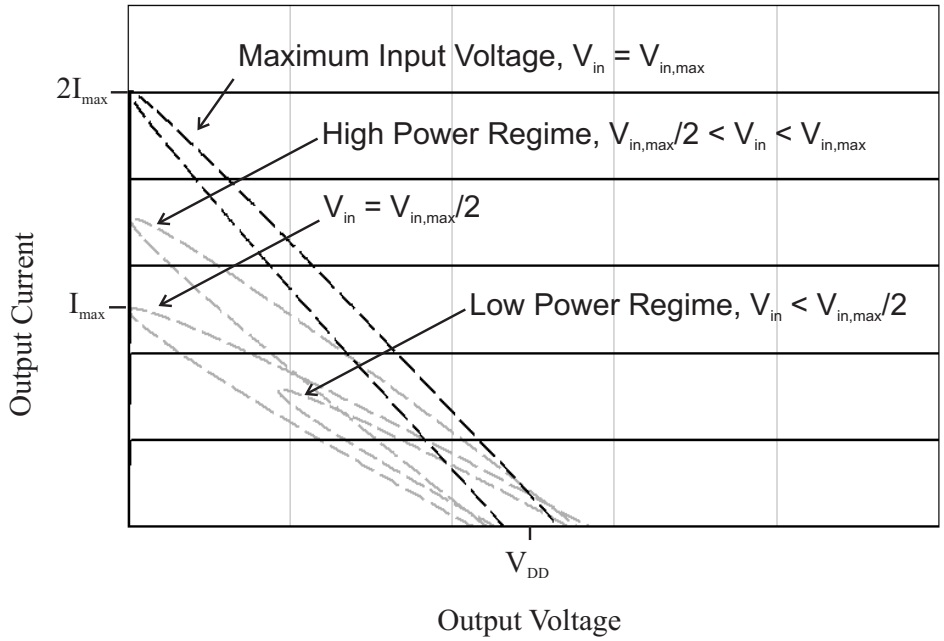


Figure 2.6: The loadline of the main amplifier for four different input voltages

power range. Section 2.4 discusses the various methods of implementing a Doherty amplifier, and gives output power, gain and efficiency characteristics for each case.

2.2.4 Doherty Amplifier Output Power, Gain and Efficiency

The equations for the output power, gain and efficiency of a Doherty amplifier using ideal transistors are simple, but are outlined below for completeness. They were used in the following sections to determine the output characteristics of the different Doherty amplifiers. The output power is

$$P_{out}(W) = \frac{\left(V_{out}/\sqrt{2}\right)^2}{R_L}$$

with a maximum of

$$P_{out,max}(W) = \frac{\left(V_{DD}/\sqrt{2}\right)^2}{R_L} \tag{2.19}$$

The gain is $P_{out,max}(dBm) - P_{av,max}(dBm)$, where the available power can be calculated using the thevenin resistance of the source (R_{TH}) and

$$P_{av,max}(W) = 2\frac{\left(V_T/\sqrt{2}\right)^2}{4R_{TH}}$$

The efficiency of the amplifier is

$$\eta = \frac{P_{out}(W)}{P_{DC}(W)}$$

where $P_{DC}(W) = V_{DD}(I_{d0,m} + I_{d0,p})$, and $I_{d0,m}$ and $I_{d0,p}$ are the DC currents drawn by the main and peaking amplifiers respectively. This gives a maximum efficiency of $\pi/4$ (as for a class B amplifier).

2.3 BASIC DOHERTY AMPLIFIER OPERATION

The circuit used for the Doherty amplifier analyses undertaken in the following sections is given in Figure 2.7. The inductors and their respective capacitors are chosen to resonate the input and the output of each transistor. Both amplifiers generate harmonics, and it is assumed that the output resonators will shunt these to ground. The output currents of the main and peaking amplifiers are therefore assumed to be sinusoidal, and are combined at the load, becoming the output current of the Doherty amplifier, as described in Section 2.2.

Ideal components are assumed; an ideal transistor being a voltage-dependent current source, with no charge storage or parasitics present. The gate voltage (V_{GS}) to

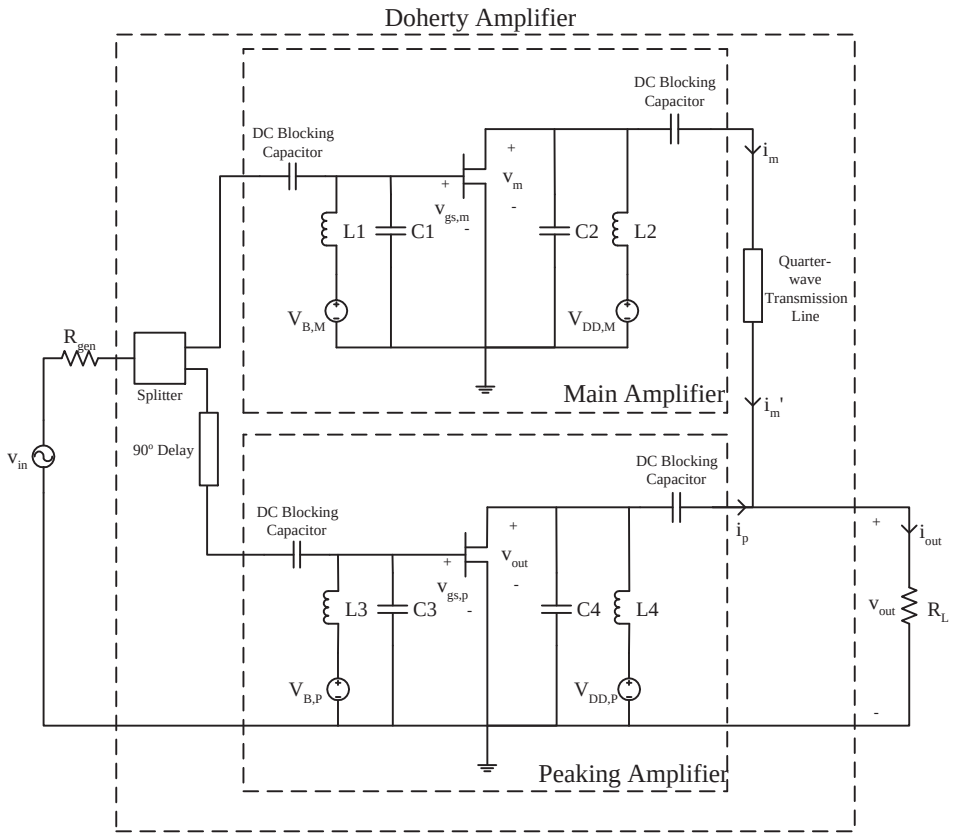


Figure 2.7: Circuit layout for a Doherty amplifier

drain current (I_d) transfer characteristic used is

$$I_d = \begin{cases} 0 & V_{GS} < V_T \\ I_{DSS}(1 - \frac{V_{GS}}{V_T}) & V_T < V_{GS} < 0,\ 0 < V_{DS} < V_{d,max} \\ I_{DSS} & V_{GS} > 0 \end{cases} \tag{2.20}$$

and is shown in Figure 2.8; V_T is the threshold voltage, (which is negative, and below which the transistor is off,) I_{DSS} is the maximum drain current, V_{DS} is the drain-to-source voltage, and $V_{d,max}$ is its maximum allowable value. It should be noted that a practical transistor's characteristic departs from this linear model, as the transitions between the three different stages are smooth curves. The ideal drain current to drain voltage characteristic is shown in Figure 2.9. Again, a practical transistor departs from this model; most significantly, it has a knee voltage, below which is the transistor's triode region, where the drain current lines decrease to 0 (at $V_{DS} = 0$). However, the linear model is often used by those who analyse power amplifiers [6, 11–14], because it leads to tractable solutions and usually provides reasonably accurate results.

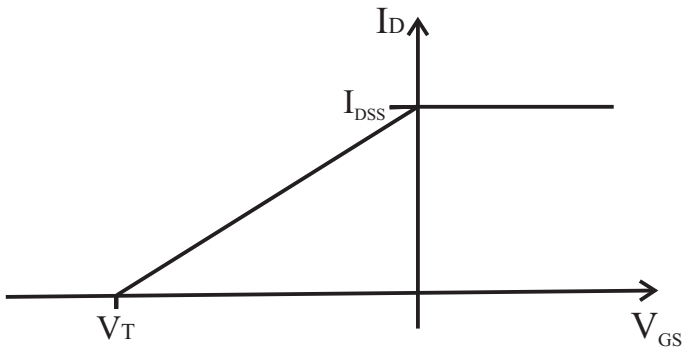


Figure 2.8: Ideal gate voltage to drain current transfer characteristic

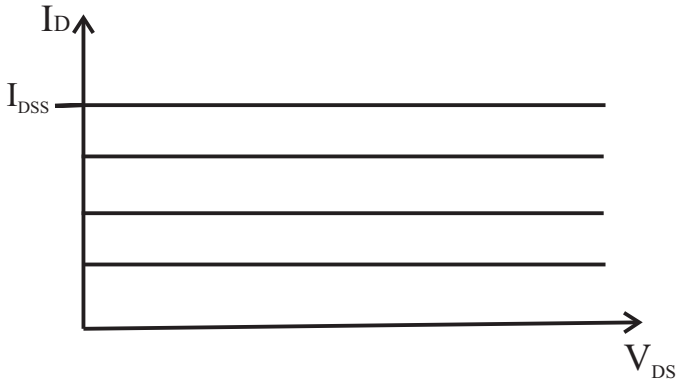


Figure 2.9: Ideal drain current to drain voltage characteristic for varying values of gate voltage

2.4 ACHIEVING THE PEAKING AMPLIFIER CURRENT CHARACTERISTIC

There are several different ways to achieve the desired current characteristics (see Figure 2.2) for Doherty operation. If ideal transistors are used for the analysis, the main amplifier's characteristic can easily be achieved by biasing at class B. The peaking amplifier is usually biased in class C to obtain automatic turn-on. However, a given transistor, when operated under class C, has a lower maximum output power than when operated under class B. This needs to be reconciled in the design of the Doherty amplifier, to ensure the two amplifiers have identical maximum output currents (see Figure 2.2). The three main methods of accomplishing this are discussed in Section 2.4.1, and the resulting output characteristics (output power, gain and efficiency) are compared in Section 2.4.2.

2.4.1 Discussion of Techniques

The three main methods of increasing the output of the peaking amplifier are: 1) bias control of the peaking amplifier, 2) a larger transistor in the peaking amplifier,

and 3) larger portion of input power fed to the peaking amplifier. It is also possible to achieve the desired peaking amplifier output current characteristic by biasing the peaking amplifier in class B, and preceding it by a variable attenuator whose setting is dependent on V_{in}. However, this is a more complicated proposition than the other methods, and is not further discussed.

Bias control of the peaking amplifier is potentially the most accurate of the options. The peaking amplifier can be biased in deep class C during the low power region, whilst in the high power region, an appropriate bias can be chosen to give the desired output current for any input power. Moreover, there is a gradual transition from class C to class B, as shown in Figure 2.10. Assuming ideal transistors with $V_T = -1$ (see Section 2.3), the required biases of the main and peaking amplifiers are shown in Figure 2.10. The method for calculating the appropriate bias values for the peaking amplifier is discussed in Chapter 5.

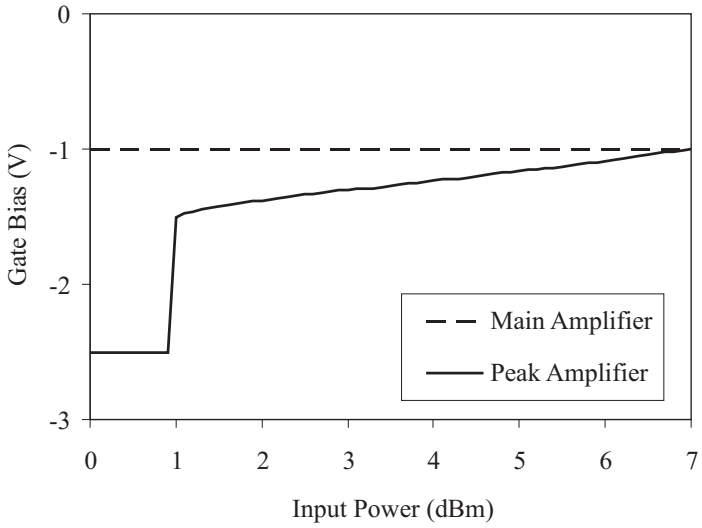


Figure 2.10: Bias control of an ideal transistor

Alternatively, the peaking amplifier's output can be increased by using a larger transistor (compared to that used in the main amplifier). In this case the peaking amplifier has a fixed bias of $1.5V_T$, which will ensure it turns on at half of maximum input voltage. In order for the two amplifiers to have identical maximum fundamental output currents, the peaking amplifier needs to be 2.55 times larger than the peaking amplifier (see Section B.3.7), where the size of the transistor is its maximum output current. The maximum input voltage of the Doherty amplifier will still be V_T, as the main amplifier is still biased in class B.

Finally, the input power to the Doherty amplifier can be split unequally between the main and peaking amplifiers, with the peaking amplifier receiving twice as much input voltage as the main amplifier. With this technique, the peaking amplifier needs a

fixed bias of $2V_T$ in order to turn on at half of maximum input voltage. This results in the peaking amplifier's maximum output current being twice that of the main amplifier. As the peaking amplifier is biased in class C, its maximum fundamental output current will be less than that of the main amplifier, which is biased in class B (see Appendix B). Increasing the peaking amplifier's input voltage, or shifting its bias point, can ensure that the two amplifiers have identical maximum fundamental output currents; however, this means the peaking amplifier will not turn on at $V_{in,max}/2$. It is not possible to achieve both identical maximum fundamental output currents, and correct turn-on, with this technique.

2.4.2 Comparison of Output Characteristics

Harmonic balance simulations of a Doherty amplifier were conducted using AWR Microwave Office [7], as described in Appendix A. Ideal components were used to confirm the validity of the characteristics predicted by the equations developed in Section 2.2. The ideal FETs were represented by a Statz model [15] (as described in Appendix C) with b = 1000, β = 100, V_T = -1 V and the parasitics set to 0. This results in I_{DSS} = 100 mA. In the case of unequal transistor sizes, the maximum drain current of the peaking FET was 255 mA which was obtained by setting β = 255. V_{DD} was set to 5 V.

The fundamental output currents and voltages for each case can be calculated using (B.8), (B.25), (2.16), (2.6). Both unequal transistor sizes and unequal input power change the shape of the main amplifier's voltage characteristic. Due to this change in shape, either the load of the amplifier needs to be reduced, or V_{DD} needs to be increased, to ensure saturation does not occur. The former approach has been taken to generate Figure 2.11. The load resistances used were: 50 Ω for bias control, 46 Ω for unequal transistor sizes, and 41 Ω for unequal input power. It can be seen that slight changes in the fundamental output current characteristic of the peaking amplifier impact on the fundamental output voltage characteristics of both amplifiers. Note that the main amplifier's fundamental output current is identical for each case.

The resulting output power and gain characteristics are shown in Figures 2.12 and 2.13. It can be seen that the simulated and calculated results are closely aligned. Furthermore, it can be seen that these methods to achieve Doherty output current characteristics all result in an amplifier with a nearly constant gain characteristic with respect to input power, implying linear amplification. There are slight differences in the amount of gain achieved by each method, with the bias control method's gain being the highest, and the unequal input power method's gain being the lowest.

Lastly, the efficiency of each of the methods was both calculated and simulated, and is shown in Figure 2.14. The differences between the methods are more pronounced in the efficiency graph although they all reach a similar maximum efficiency, and they

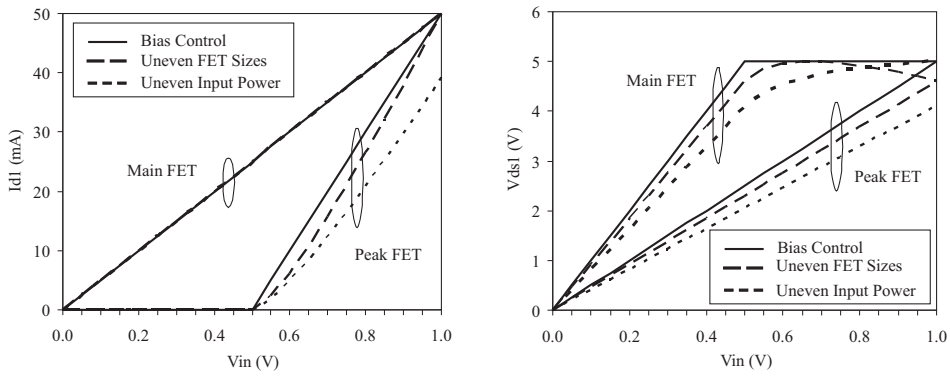


Figure 2.11: Fundamental outputs of the main and peaking amplifier using various techniques to increase the peaking amplifier's output current

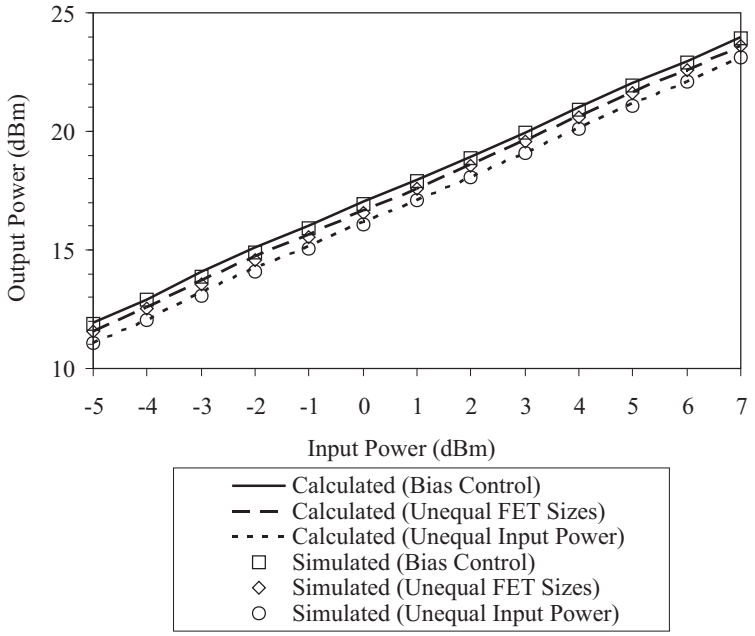


Figure 2.12: Doherty amplifier output power using various techniques to increase the peaking amplifier's output current

achieve high efficiency over a similar 6 dB dynamic range. The bias control method, which gives the ideal fundamental current and voltage characteristics, unsurprisingly gives the best efficiency characteristic. The differences in efficiency in the low power region are due to the different load impedances used (required to ensure saturation of the main amplifier does not occur). All three of the methods give a very good efficiency characteristic, with a significant increase in efficiency over a conventional parallel class B amplifier. A parallel class B was chosen for comparison, as it has the same maximum output power as a Doherty amplifier for a given transistor size, and it is the most efficient of the conventional linear amplifiers.

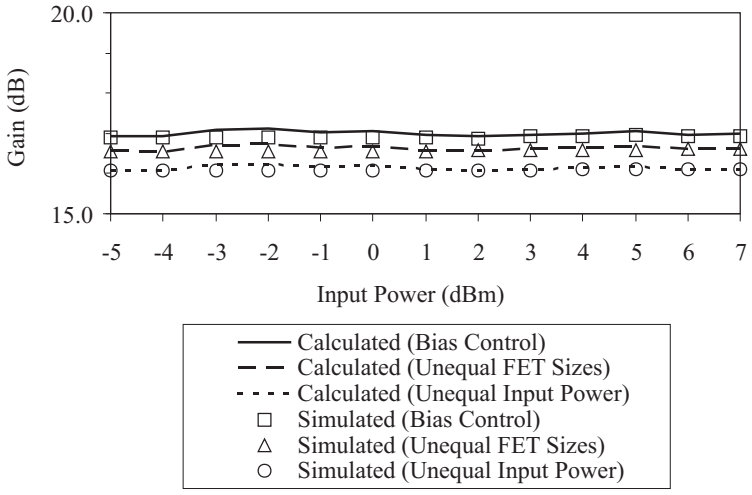


Figure 2.13: Doherty amplifier gain using various techniques to increase the peaking amplifier's output current

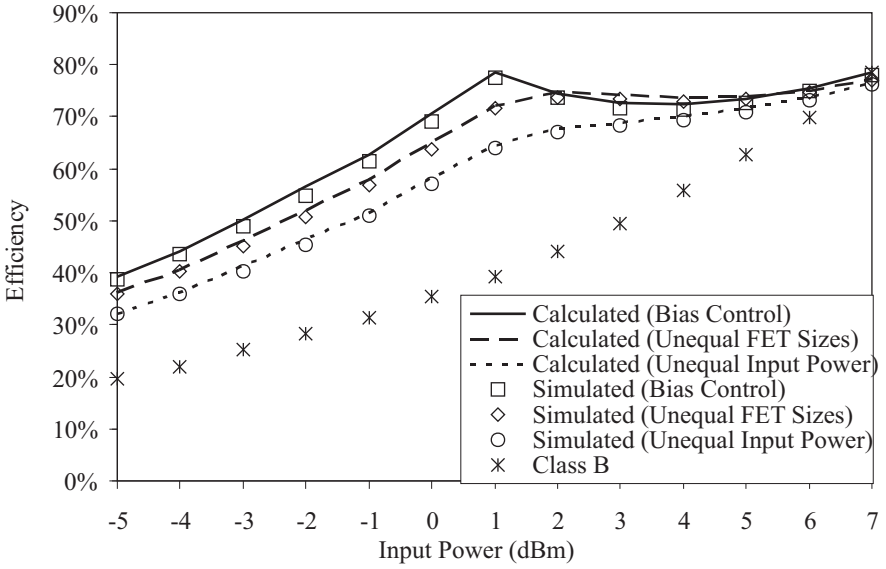


Figure 2.14: Doherty amplifier efficiency using various techniques to increase the peaking amplifier's output current

2.5 FIXED BIAS, EQUAL TRANSISTOR SIZES, AND EQUAL INPUT POWER

It is possible to use the Doherty amplifier circuit without attempting to accurately recreate the Doherty fundamental current characteristics (Cripps calls this a Doherty Lite [6]). The circuit is often implemented with a fixed bias, equal transistor sizes, and equal input power split - i.e. without compensation for the lower output of the class

C peaking amplifier. This is a simpler circuit to realise, and using class B bias for the main amplifier and class C bias for the peaking amplifier, the Doherty characteristics can be approximated. In fact, the main amplifier's fundamental current characteristic will be identical, but the peaking amplifier's maximum fundamental output current will be significantly lower than that required for true Doherty operation. It is interesting to see what effect this has on the amplifier's behaviour.

Using (B.8), (B.25), (2.16), (2.6), the current and voltage characteristics given by this implementation were calculated, and are shown in Figure 2.15. As discussed in Section 2.4.2, the modification of the shape of the voltage characteristic means the load of the Doherty amplifier needs to be reduced to ensure saturation does not occur. The load used was 31 Ω.

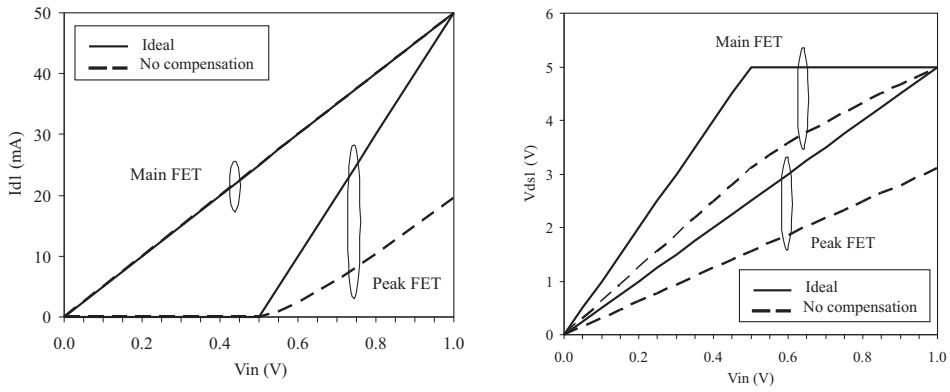


Figure 2.15: Main and peaking amplifier current and voltage characteristics with fixed bias, equal transistor sizes and equal input power split

As expected, the peaking amplifier's fundamental output current is significantly lower than the ideal characteristic. This means the load modulation of the main amplifier will be less than optimum, and as such the main amplifier's fundamental drain voltage characteristic is almost linearly increasing with input voltage. The decreased load means the effects of not achieving the peaking amplifier's fundamental output current characteristic are present even when the peaking amplifier is off.

The effect on the output power and gain is shown in Figures 2.16 and 2.17. As in Section 2.4.2, a simulation was conducted using AWR Microwave Office [7], as described in Appendix A. Ideal components were used to confirm the theoretical characteristics. The ideal FETs were represented by a Statz model [15] (as described in Appendix C) with $b = 1000$, $\beta = 100$, V_T = -1 V and the parasitics set to 0. This results in I_{DSS} = 100 mA. V_{DD} was set to 5 V. The figures show good agreement between the calculated and simulated results. The amplifier still shows a nearly constant gain characteristic with respect to input power, but the output power and gain have both dropped from the ideal characteristics.

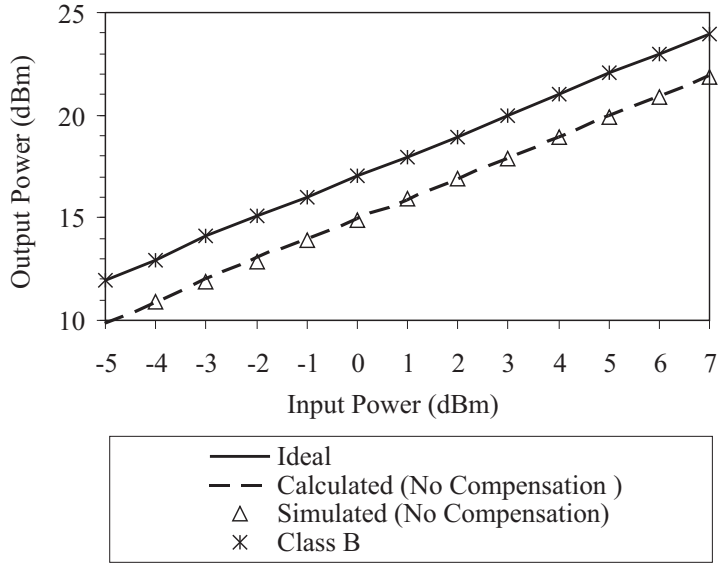


Figure 2.16: Doherty amplifier output power with fixed bias, equal transistor sizes and equal input power split

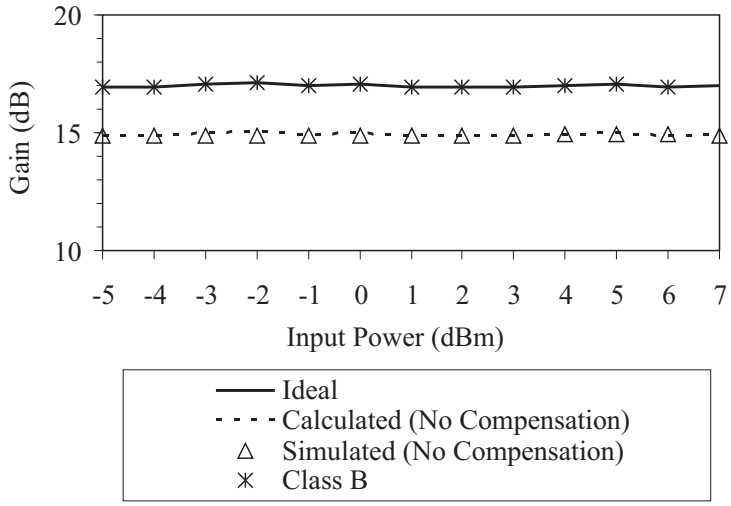


Figure 2.17: Doherty amplifier gain with fixed bias, equal transistor sizes and equal input power split

Using this implementation, the efficiency characteristic of the Doherty amplifier is significantly altered, as shown in Figure 2.18. It is still more efficient than a conventional parallel class B amplifier, but compares very unfavourably to the ideal Doherty efficiency characteristic. Again, the calculated characteristic closely matches simulations.

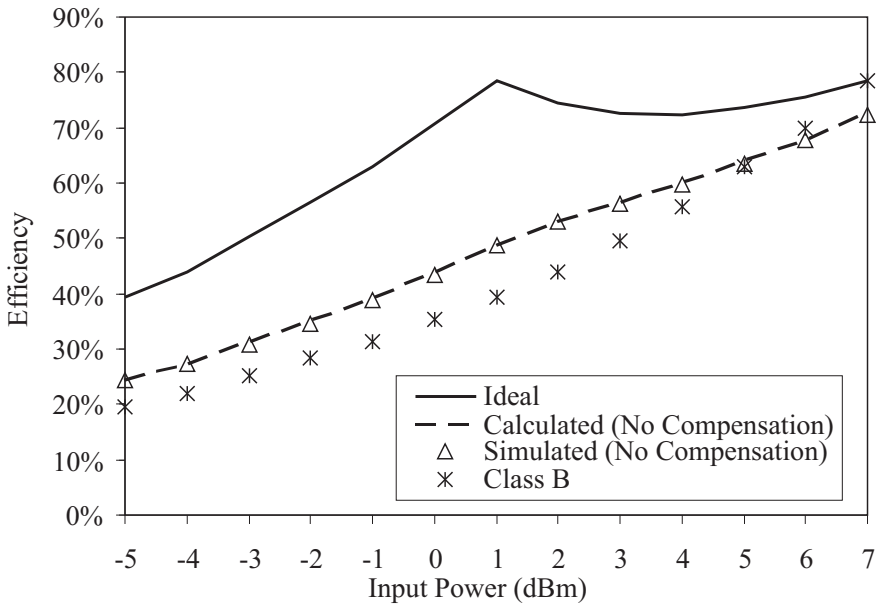


Figure 2.18: Doherty amplifier efficiency with fixed bias, equal transistor sizes and equal input power split

Chapter 3

DOHERTY AMPLIFIER LITERATURE REVIEW

3.1 INTRODUCTION

In recent years there has been a lot of interest shown in Doherty amplifiers. A large quantity of this research has been aimed at improving the linearity of a Doherty circuit in order to meet the requirements of various modulation schemes (e.g. WCDMA). Miniaturisation of the circuit has also been a high priority, to enable its use in mobile devices. Of more interest for this project has been the work done to improve the performance of a Doherty amplifier, since theory, simulations and results frequently have significant discrepancies.

This literature review has been split into three sections - Section 3.2 covers the work done to date to achieve classical Doherty operation (where the outputs of the main and peaking amplifiers approximate the ideal characteristics shown in Figure 2.2), Section 3.3 discusses the work done on improving the efficiency and/or linearity of the Doherty amplifier, and Section 3.4 gives an overview of related work that has been done on Doherty amplifiers.

3.2 ACHIEVING CLASSICAL DOHERTY OPERATION

As discussed in Section 2.4, to achieve classical Doherty operation using transistors requires a modification to the basic circuit. There are several different ways of achieving the desired fundamental output current characteristics (see Figure 2.2); the most popular are bias control, unequal transistor sizes, and unequal transistor input power. These are discussed in Sections 3.2.1 to 3.2.3.

It is worth noting that a significant portion of the research carried out does not address standard Doherty operation, but uses a fixed bias, with equal devices sizes and equal input power. This form of a Doherty circuit gives an improvement over a class B amplifier, and is a simpler implementation, making it an attractive alternative (see Section 2.5). However, it should not be confused with a classical Doherty where the maximum fundamental output currents of the two amplifiers are designed to be equal.

Separately from the issue of achieving higher peaking amplifier output current, there has been research that suggests offset lines (sometimes called peaking compensation lines) are needed at the output of each amplifier to ensure Doherty operation is achieved. This is further discussed in Section 3.2.4.

3.2.1 Bias Control

Bias control of the peaking amplifier has been used extensively to improve the performance of Doherty amplifiers. The approach normally taken is to have the bias of the peaking amplifier vary according to the envelope of the input signal. However, there has been research done on bias switching (utilising two bias points), and on varying the bias of the main amplifier as well as that of the peaking amplifier.

Bias switching of the peaking amplifier has been used in a few cases [16–18] rather than a more complicated control strategy. This approach shows a good improvement in efficiency and linearity (compared with a fixed bias amplifier), although only utilising two bias points doesn't give classical Doherty operation at all input powers, and so the results aren't as good as a classical Doherty amplifier. Two of the papers also implemented other modifications - [16] combined bias control with an extended Doherty amplifier (see Section 3.4.2) and unequal transistor sizes, while [18] implemented a power supply control circuit.

More complex bias control strategies have been implemented using both analogue and digital circuits. Various analogue circuits have been designed to deliver an adaptive peaking amplifier bias based on the envelope of the input signal [19–24]. In general, the output of the adaptive bias circuit was tuned by modifying component values based on experimental data [19] or simulated results [20–23]. Lee et al. [24] do not state how they determined their optimal gate bias control circuit, or its output values. With the exception of [21, 22, 24] standard Doherty operation seems to have been obtained by using bias control, with a region of high efficiency appearing, and linearity remaining relatively good. Chen et al. [21] and Liu et al. [22] combine bias control with unequal transistor sizes in a CMOS circuit, which may have resulted in a non-optimum bias control circuit. Lee et al. [24] implement controls on the DC supply voltages, (as well as the peaking amplifier gate bias,) which affects the efficiency of the amplifier. Furthermore, they were aiming for optimum linearity, which they achieved at the cost of efficiency, making it difficult to determine if Doherty operation was occurring or not.

Bias control has also been applied to the main amplifier [20, 23]. Cha et al. [20] determined the optimum biases of both amplifiers by iteratively simulating the circuit using envelope simulation. It is interesting to note that the shape of the peaking amplifier bias control when plotted against input power is close to an exponential function, whereas the bias control shape for ideal transistors (see Figure 2.10) is almost linear. They compare their results to a Doherty amplifier with fixed bias (see Section

2.5), and unsurprisingly get an improvement in both efficiency and linearity. Their efficiency characteristic has a region of high efficiency, as expected for a Doherty amplifier. They don't have any results showing AM-AM distortion, which could be used as an indication of whether linear amplification was occurring or not. However, they do show the adjacent channel leakage ratio (ACLR), which is better than that of a class AB and a fixed-bias Doherty amplifier at high output power levels, but worse at low output power.

Nam et al. [23] are mainly concerned with miniaturisation, and use four amplifiers - main driver and power amplifiers and peaking driver and power amplifiers. They bias control both peaking amplifiers, and the main power amplifier (but not the main driver amplifier). They also implement a DC/DC converter on the power supply to further improve efficiency. They get poorer linearity than a class AB amplifier, but a similar level as a fixed bias Doherty amplifier. The efficiency is significantly better than both of these, with a region of high efficiency at high output power.

Digital dynamic bias control strategies utilising digital signal processing have also been implemented with success [25–27]. In all cases, the bias control scheme was determined from experimental data, although [25, 26] were optimising for constant gain with respect to input power, while [27] optimised intermodulation distortion cancellation between the main and peaking amplifiers.

The remainder of the papers that used bias control with a standard Doherty circuit either implement it off-circuit, or do not discuss the implementation. Lees et al. [28] use a piece-wise linear peaking amplifier bias control to create classical Doherty operation. They then investigate the effect of varying the relative phase and magnitude of the input signals sent to the main and peaking amplifiers. Ferwalt et al. [29] use HBTs with base control on both the main and peaking amplifier to improve efficiency and obtain Doherty operation, with very good efficiency results (linearity is not discussed). Kang et al. [30] have a similar circuit setup to Nam et al. [23], with four amplifiers on a CMOS circuit. In this case however, they adjust the gate biases of the driver amplifiers solely to achieve unequal power input to the power amplifiers.

Finally, two papers look at implementing bias control in conjunction with multiple peaking amplifiers [31, 32]. Srirattana et al. [31] manually adjusts the bias of their second peaking amplifier, to ensure it reaches class B operation, while Lee et al. [32] implemented an analogue circuit to control the bias of both their peaking amplifiers, as well as the DC supply voltage. In the former case, the adjustment resulted in an improvement in both efficiency and linearity, while in the latter case linearity was was increased, but efficiency was slightly lower.

3.2.2 Unequal Transistor Sizes

Having a larger transistor in the peaking amplifier (determined by its maximum output current) compared with the main amplifier is not something that has been implemented frequently, and has usually been accompanied by research into other areas. This is perhaps due to the difficulty in getting devices that have the exact ratio required (when using discrete devices) [13, 31]. As the work on this topic is generally combined with other Doherty-related research, it is hard to determine exactly how effective using unequal transistor sizes is for achieving classical Doherty operation.

Liu et al. [17] analysed the effect of different classes of operation for the peaking amplifier, as well as an adaptive bias. Their results showed that with the peaking amplifier biased in class C, the amplifier had the expected efficiency shape, but the linearity suffered when the peaking amplifier turned on, indicating that the peaking amplifier's device size may have been incorrect. They then implemented an adaptive bias, which maintained the high efficiency, while improving the linearity.

The other work done on this topic has incorporated various other techniques - extended Doherty [13, 16], multiple peaking transistors [31, 33], bias switching [16] and unequal transistor input power [34].

3.2.3 Unequal Transistor Input Power

Feeding more input power to the peaking amplifier than to the main amplifier was first proposed by Kim et al. [14], which has a comprehensive theoretical analysis of the proposal. Their theory indicates that a ratio of 1:2.4 (main:peak) was optimal to get identical maximum fundamental output currents from the two transistors. However, they do not discuss how the peaking amplifier was to be biased to achieve automatic turn-on at the correct point with this ratio. They implement the unequal input power by installing a fixed attenuator at the input to the main amplifier, and get a significant improvement in efficiency and linearity compared with a class AB amplifier.

Unequal transistor input power has also been applied to Doherty amplifiers with bias circuit optimisation [35], unequal transistor sizes [34], multiple peaking transistors [33, 36], and an inverted Doherty structure (see Section 3.3.2). This is implemented either by dividing the power unequally at the input to the Doherty circuit, or by having separate inputs for each amplifier, with the amplitudes controlled outside the circuit. To achieve unequal input power, the self biasing effect of the peaking amplifier can be used, thereby eliminating the need for an input power divider or hybrid coupler [37].

3.2.4 Offset Lines

Offset lines (sometimes called peaking compensation lines) are transmission lines placed at the output of both the main and peaking amplifiers (after output matching). Re-

search has been done suggesting they are necessary for classical Doherty operation [38, 39]. Their purpose is to ensure that the amplifiers have the required output impedances for Doherty operation over the full dynamic range (e.g. at low power, the peaking amplifier's output impedance should be both high and resistive). The requirement for offset lines seems dependent on the type of transistor used, as amplifiers have been realised that do not require offset lines to achieve Doherty operation [13, 23, 31].

However, they have been used to good effect in a large amount of research, covering multiple topics - unequal input power [14], bias control [19, 20, 40], miniaturisation [30, 41, 42], multiple peaking amplifiers [32, 36, 43–45], linearisation [10, 46], utilising class F [47–49], and other, miscellaneous topics [50–53]. Steinbeiser et al. [54] take the use of offset lines one step further, by adjusting the lengths of the offset lines after building the prototype amplifier, based upon measured results. Their amplifier was not a classical Doherty, as it used a fixed bias, equal transistor sizes, and equal input power. Nonetheless, they achieved good results, indicating a good design strategy.

3.3 IMPROVING DOHERTY AMPLIFIER EFFICIENCY AND/OR LINEARITY

3.3.1 Class F Operation

There have been a couple of investigations into the use of class F [55] amplifiers for the Doherty amplifier, (instead of classes AB/B/C). Suzuki et al. [56, 57] built a Doherty amplifier comprising two class F amplifiers (where even harmonic impedances are low, and odd harmonic impedances are high), which they then linearised using feedforward and predistortion. Unfortunately they do not compare their results to a classical Doherty amplifier, making it hard to determine if using class F gives a better performance. Similarly, Goto et al. [58] proposed a Doherty amplifier that utilised class F for the main amplifier, but inverse class F (where even harmonic impedances are high, and odd harmonic impedances are low) for the peaking amplifier. Again, a comparison to a classical Doherty was not performed, and while the amplifier has a region of high efficiency, its linearity is poor in the high power region.

More recently, inverse class F amplifiers have been used for both the main and peaking amplifiers [47–49], by placing a harmonic control circuit at the outputs of the transistors. This shapes the loadlines of both amplifiers, resulting in a quasi-L shape for the main amplifier. This allows the DC supply voltage to be decreased without the amplifier going into saturation (which would result in a decrease in fundamental output power). As a result, the efficiency of the amplifier is improved compared with a standard Doherty. There is a degradation in linearity, but this was rectified by the application of digital predistortion to the circuit.

3.3.2 Inverted Doherty

Another interesting modification to the standard Doherty circuit is the inverted Doherty amplifier, where the $\lambda/4$ transformer is placed after the peaking amplifier rather than after the main amplifier. Ogama et al. originally proposed this to achieve the desired load modulation effect with high power transistors, which have relatively low output impedances [59]. Ahn et al. have documented a method for choosing whether an inverted or a normal Doherty amplifier would give better results, depending on the angle of the output reflection coefficient [51]. Their results are lacking the region of high efficiency that characterises standard Doherty operation, but they implement a fixed-bias Doherty amplifier with equal transistor sizes, and equal input power, so this is to be expected.

The inverted Doherty structure has not been directly compared to a standard structure in any of the papers using it, making it difficult to tell whether or not anything was gained [51,59–62]. Nonetheless, results have been obtained that are consistent with Doherty operation [59, 61–63], making it a viable alternative.

3.3.3 Bias Optimisation

The effect of different fixed bias points on the Doherty amplifier has been investigated in multiple papers. The first work done on this implemented two different bias conditions for the main amplifier - class AB or class B, with the peaking amplifier biased in class C [38,64]. In this case, the Doherty with a class B main amplifier had better efficiency, but worse linearity compared with the Doherty with a class AB main amplifier. Sirois et al. [65] also varied the bias of the main amplifier (from class B to class AB), and demonstrated that this has a significant effect on linearity of the Doherty, while having a minimal effect on its efficiency. Cho et al. [10, 46] and Takayama et al. [66] both investigate changing the peaking amplifier's bias, and show that it has a major effect on the efficiency of the Doherty amplifier.

The most common method of bias optimisation is to choose the biases of the main and peaking amplifiers such that their 3rd order intermodulation distortion (IMD3) cancels. This is possible because the main amplifier is usually biased in class AB, while the peaking amplifier is biased in class C, and these produce opposite signed IMD3 [43]. This technique has been applied in a variety of circumstances [14,36,40,43,50,63,67,68], but has not been directly compared to a Doherty without IMD3 cancellation, making it difficult to tell exactly what effect it has.

Moon et al. [27] have expanded upon this idea, by modifying the bias depending on the input power, to ensure IMD3 cancellation throughout the dynamic range. They compare their performance with that of a fixed bias Doherty amplifier, and get an improvement in linearity at high power levels, while efficiency is essentially unchanged.

3.3.4 External Linearisation Techniques

There has been a lot of research done on improving the linearity of the Doherty amplifier through adding external circuitry. A few different techniques have been implemented: - i) digital predistortion [25, 57, 65, 69–77], ii) analogue predistortion [11, 59, 78], iii) feedforward [10, 56, 59, 79] and iv) post-distortion linearisation [42]. In virtually all cases, the linearity of the amplifier was significantly improved, showing that the Doherty amplifier lends itself well to linearisation techniques. In all cases, the improvement in linearity is at the cost of efficiency. The extent to which this happens is dependent on the technique used.

3.3.5 Miscellaneous

There have been several techniques implemented in a Doherty amplifier structure that do not fall into any of the above classifications. These are discussed in the following paragraphs - using class E amplifiers, optimising the device size ratio, using metamaterials, and using a defected ground structure.

Similarly to the work done utilising Class F amplifiers (see Section 3.3.1), Class E amplifiers have been used to improve the efficiency of the Doherty amplifier, with third order intermodulation cancellation implemented to improve linearity (see Section 3.3.3) [80]. The efficiency is significantly improved compared to a Doherty with a class A main amplifier (but still class E peaking amplifier). They did not compare the linearity to a Doherty without class E main and peaking amplifiers.

Elmala et al. [81] implement a Doherty using 90-nm CMOS, which gives them the option to optimise the size of the transistors to reduce AM-PM distortion. In theory, as discussed in Section 2.4, the optimum ratio is 1:2.55 (main:peak) to achieve identical maximum fundamental output currents. They simulated the AM-PM phase error for ratios 1:1.3 to 1:2, and hence determined the optimum ratio to be 1:1.6. The resulting amplifier has good linearity, and good efficiency (considering the ratio is too low for standard Doherty operation).

Ji et al. [82] use a composite right/left-handed transmission line to improve the linearity of their fixed-bias Doherty amplifier with equal device sizes and equal input power. These transmission lines can be designed to have a specific phase response at two arbitrary frequencies, which was used to modify the design of the $\lambda/4$ transmission line that connects the outputs of the two amplifiers. They designed it to have a 90° phase shift at the fundamental (as is conventional), and a 360° phase shift at the second harmonic, resulting in its cancellation. They get a significant improvement in third order intermodulation distortion compared with a Doherty using a standard transmission line. They do not compare their efficiency results to another type of amplifier (Doherty or conventional), meaning it cannot be determined if the effect on

efficiency was detrimental.

Choi et al. [60] use a defected ground structure under the $\lambda/4$ transmission line connecting the main and peaking amplifier outputs, and under the peaking amplifier's offset line. By doing this they can terminate higher-order harmonics in a compact way. Their implementation is a fixed-bias Doherty amplifier with equal transistor sizes and equal input power. They also construct a Doherty amplifier without defected ground structure for comparison. Both amplifier's have some nonlinear amplification in the high power region (as indicated by the gain characteristic), but the defected ground structure Doherty has an improvement in efficiency as well as a lower adjacent channel leakage ratio (ACLR).

3.4 RELATED RESEARCH

There has been a lot of other research on Doherty amplifiers that is not directly related to achieving classical Doherty operation or to improving the linearity or efficiency of a Doherty circuit. These are briefly summarised in the following sections for completeness.

3.4.1 Miniaturisation/ High Power/ High Frequency

In order to make the Doherty amplifier suitable for commercial applications, research has been conducted into making the circuit smaller (e.g. for handsets) [16, 22, 23, 30, 37, 41, 78, 81, 83–90]. This has largely been successful, although generally a fixed-bias Doherty amplifier with equal transistor sizes and equal input power was used, which gives lower efficiency and linearity than a classical Doherty as discussed in Section 2.5. Park et al. [41] compare their results to a non-compact Doherty amplifier, and shows that miniaturisation of the amplifier is possible without sacrificing efficiency and linearity. Jung et al. [85] came up with a series-type Doherty (as opposed to the standard parallel architecture) to decrease circuit size and Koo et al. [78] continued this work. This architecture shows similar results to a classical Doherty amplifier, with relatively good linearity, and a region of high efficiency at high power levels. It is also more compact, as no input hybrid coupler is required.

Some applications require high output power or operate at high frequencies. A large number of papers implement a Doherty amplifier at high power levels [46, 51, 53, 91–97], although the amplifier usually has fixed-bias, equal transistor sizes and equal input powers, meaning classical Doherty operation is not achieved. Nonetheless, the results indicate that the Doherty circuit works at high power levels. Similarly, [42, 83, 98, 99] implement a Doherty circuit at high frequencies, and show that the circuit can be used under those conditions.

3.4.2 Extended Doherty

It is also frequently desired to have region of high efficiency extend over more than 6 dB. This is accomplished either by adding extra peaking amplifiers [12] (sometimes referred to as a N-way Doherty amplifier [43]), or by shifting the point at which the peaking amplifier turns on. The former method results in a more complicated amplifier structure, but in theory adds a second efficiency peak, without modifying the efficiency characteristic in the last 6 dB of input power. Conversely, turning the peaking amplifier on earlier, (and loading the main amplifier higher to get maximum efficiency from it at the turn-on point,) maintains circuit simplicity, but results in a larger dip in efficiency in the high power region [12].

Both of these methods have been implemented in several different ways, with varying degrees of success. Again, they are usually implemented with fixed bias, equal transistor sizes, and equal input power. In practice, multiple peaking amplifiers [31, 32, 36, 40, 43, 49, 67, 91, 100] give an improvement in efficiency over a 2-way Doherty amplifier, but it is often not significant. Likewise, extended Doherty amplifiers [13, 16, 29, 34, 66, 89, 101, 102] usually show an improvement in efficiency at a lower output power (compared with a conventional amplifier, or a classical Doherty), but it is generally significantly less than that predicted by theory.

In [44,45], Cho et al. create an extended Doherty using multiple peaking amplifiers. In both cases they achieve a nice efficiency characteristic, with a region of high efficiency that starts at a lower power than in a classical Doherty. However, this came at the cost of linearity, with the gain being very dependent on input power once the high efficiency region is entered. This indicates that the main amplifier may be going into saturation.

Chapter 4

DOHERTY AMPLIFIER CHALLENGES

4.1 INTRODUCTION

Doherty amplifiers have the potential to be linear amplifiers with high average efficiency for modulation schemes that largely operate below maximum output power, as shown in Chapter 2. However in practical implementations, efficiency is often significantly lower than that predicted by theory with ideal transistors. Where this happens, there is either no region of high efficiency but instead a continuously increasing efficiency curve (albeit higher than a class AB or class B amplifier), or a high efficiency region is present, but the linearity of the amplifier decreases significantly in the high power region. Section 4.2 outlines the research questions that this thesis answers, while Sections 4.3 and 4.4 look at the effects of transistor non-idealities on the Doherty amplifier.

4.2 RESEARCH SUMMARY

4.2.1 Research Question

Doherty amplification is currently a very popular topic, as shown by the amount of recent research carried out (see Chapter 3). However, the majority of this research does not achieve characteristics similar to those predicted by theory (see Chapter 2). As the Doherty amplifier's theoretical output characteristics are quite impressive given the simplicity of the circuit, it was desirable to find out the cause of the difference.

Hence the research reported here has three facets:

- What is the cause of the difference between the theoretical Doherty amplifier characteristics and those achieved in a practical implementation?
- How can this difference be eliminated, so that near-theoretical characteristics are achieved, regardless of transistor parametric variation?
- What role do harmonics play in the Doherty amplifier, and can they be used to advantage?

4.2.2 Development of Research Direction

In the initial stages of the research process, it rapidly became apparent that there were widely varying definitions of a standard or classical Doherty amplifier. In a large number of papers, a Doherty amplifier with fixed-bias, equal transistor sizes (i.e. equal maximum output currents), and equal input power was referred to as a standard Doherty. The original paper [2] produces the desired output current characteristics by feeding unequal input power to the two amplifiers. It was decided that for the purposes of this thesis, a classical Doherty would be defined as one that attempted to approximate the desired current characteristics (see Figure 2.2).

Amplifiers that didn't compensate for the lower output of a class C amplifier accounted for a large quantity of the output characteristics that were significantly different from the theoretical (classical) characteristics. However, the papers that did compensate for a lower peaking amplifier output current still had large discrepancies between reality and theory in the majority of cases. Where good linearity was combined with a region of high efficiency, it was usually obtained by carrying out multiple simulations or measurements, and tuning the circuit or its input signal(s) based on these, rather than from an analytical basis. Srirattana et al. [31] suggested that the Doherty efficiency characteristic was not achievable due to transistor soft turn-on but this claim had not been investigated. This was the starting point for research reported in this thesis into the effect of transistor non-idealities on the Doherty amplifier output characteristics (discussed in Sections 4.3 and 4.4).

The investigation into transistor non-idealities showed that the Doherty amplifier circuit was sensitive to both soft turn-on and unequal maximum fundamental output currents. The theoretical analysis with ideal components indicated that bias control of the peaking amplifier was the best way to achieve the desired fundamental output currents (see Section 2.4). It is also the only method that can easily compensate for soft turn-on of the amplifiers, or for unequal maximum output currents. As the existing research into bias control (see Section 3.2.1) had not looked at the optimum bias from an analytical point of view, it was decided to approach it from this direction, using the Statz transistor model (see Appendix C). The results from this work are discussed in Chapter 5.

Finally, during the design of the Doherty amplifier, the method used for harmonic terminations was scrutinised. The drain supply (V_{DD}) was fed to the transistors via a quarter-wave transmission line terminated with a capacitor, which acts as a trap for even harmonics. As the peaking amplifier is biased in class C, it was initially presumed that a third-harmonic trap was required on its output. However, closer examination of the Doherty circuit revealed that this was not the case, and the odd harmonics produced by the peaking amplifier can be shunted to ground via the quarter-wave transmission line on the main amplifier's drain supply. In doing so, class F operation in the main

amplifier is obtained, which increases the efficiency of the Doherty amplifier. This elegant and novel method is the subject of Chapter 6.

4.3 THE EFFECT OF TRANSISTOR SOFT TURN-ON

4.3.1 Theoretical Analysis

In order to answer the first research question, the most basic non-ideality was introduced to the Doherty amplifier - soft turn-on. To maintain generality, unequal transistor sizes were considered, with a larger peaking amplifier transistor to ensure the fundamental output currents of the two amplifiers were identical at maximum input power as described in Section B.3.7.

To perform a theoretical analysis to gauge the effect of soft turn-on (and to ensure the effects of any other non-idealities were excluded), as well as to ensure tractability, a number of assumptions were made. It was assumed that the transistors had no triode region, no charge-storage and no parasitics. In practise, the triode region and resistive parasitics will predominantly scale down the efficiency and the charge-storage and reactive parasitics will impact on matching circuit design. The FET drain current (I_d) was related to the gate voltage (V_{gs}) by the following drain current transfer characteristic

$$I_d = \begin{cases} 0 & \text{when } V_{gs} < V_T \\ I_{DSS}\left(1 - \frac{V_{gs}}{V_T}\right)^x & \text{when } V_T \leq V_{gs} < 0 \\ I_{DSS} & \text{when } V_{gs} \geq 0 \end{cases} \tag{4.1}$$

where x is a positive-valued parameter, I_{DSS} is the saturation current of the transistor, and V_T is the threshold voltage. When x is 1, the drain current has a linear transfer characteristic, and when x is 2 it is a square-law transfer characteristic. These cases represent bounds of a range of different transfer characteristics with the linear case exemplifying abrupt turn-on (the ideal case), while the square-law case exemplifies an extreme case of soft turn-on.

The analysis considered the case of the main amplifier biased in class B, and the peaking amplifier in class C. To counteract the low gain of the class C peaking amplifier (see Section 2.4), the peaking amplifier device size was 2.55 times and 5.3 times that of the main amplifier FET for the linear and square-law drain current transfer characteristics respectively, so as to give identical fundamental output currents at maximum input power (see Section B.3.7 for calculation of transistor size ratios).

As in Section 2.4, the following values for the transistors/amplifiers were chosen: I_{DSS} = 100 mA (main amplifier only), V_T = -1 V, and V_{DD} = 5 V. The maximum drain current for the peaking amplifier was 255 mA for the linear case, and 530 mA for the square-law case. The main amplifier was biased at -1 V, and the peaking amplifier

was biased at -1.5 V, so it would turn on and off automatically at half of maximum input voltage. The amplifiers' theoretical fundamental output currents were calculated (using (B.8), (B.25), (B.37) and (B.38)), as shown in Figure 4.2. The fundamental output currents of the amplifiers using square-law transistors never reaches 50 mA due to the shape of the drain current waveform. With a non-linear transfer characteristic, it is no longer half of a sinusoidal signal, but instead is shaped like a bell-curve. This results in a lower fundamental output current.

To ensure that $V_m \leq V_{DD}$, so that saturation doesn't occur, (2.16) can be rearranged to give an upper bound of the load resistance, R_L:

$$R_L \leq \frac{V_{DD}}{2I_m - jI_p} \tag{4.2}$$

The load resistance for the linear and square-law cases was 46 Ω and 58 Ω respectively, as the output current characteristics are different for each case, giving different point of maximum voltage. It should be noted that unequal transistor sizing does not result in the ideal peaking amplifier output current characteristic (see Section 2.4.2), which means even the linear case does not have a 50 Ω load. The fundamental drain output voltages were calculated according to (2.16), (2.6), and are shown in Figure 4.3. The main amplifier's load impedance over the dynamic range is shown in Figure 4.4, while the resulting theoretical efficiency and gain of the Doherty amplifier were calculated using the equations in Section 2.2.4, and are shown in Figure 4.5.

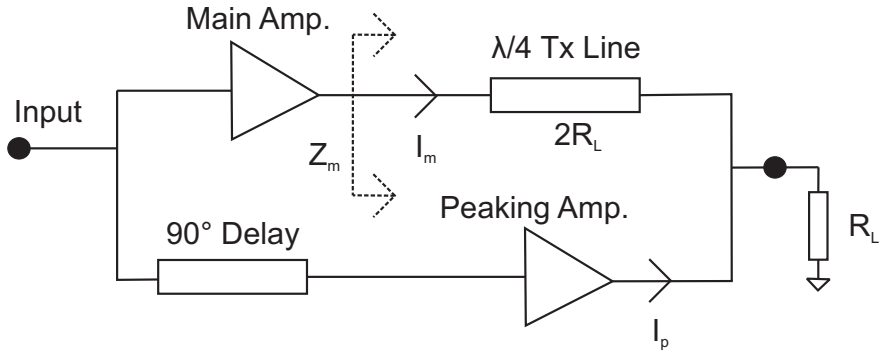


Figure 4.1: Doherty amplifier circuit design with unequal transistor sizes (1:2.55 for $x = 1$ and 1:5.3 for $x = 2$)

It is clear that the main amplifier's load is identical for both the linear and square-law cases in the low power regime, and at maximum power, as expected. However, there is significant variation between the two in the high power regime, with the square-law characteristic resulting in insufficient load modulation. It can also be seen that the change from a linear to a square-law transfer characteristic has a significant effect on the output characteristics throughout the dynamic range. With a linear transfer characteristic ($x = 1$), the amplifier behaves according to the original Doherty proposal [2]

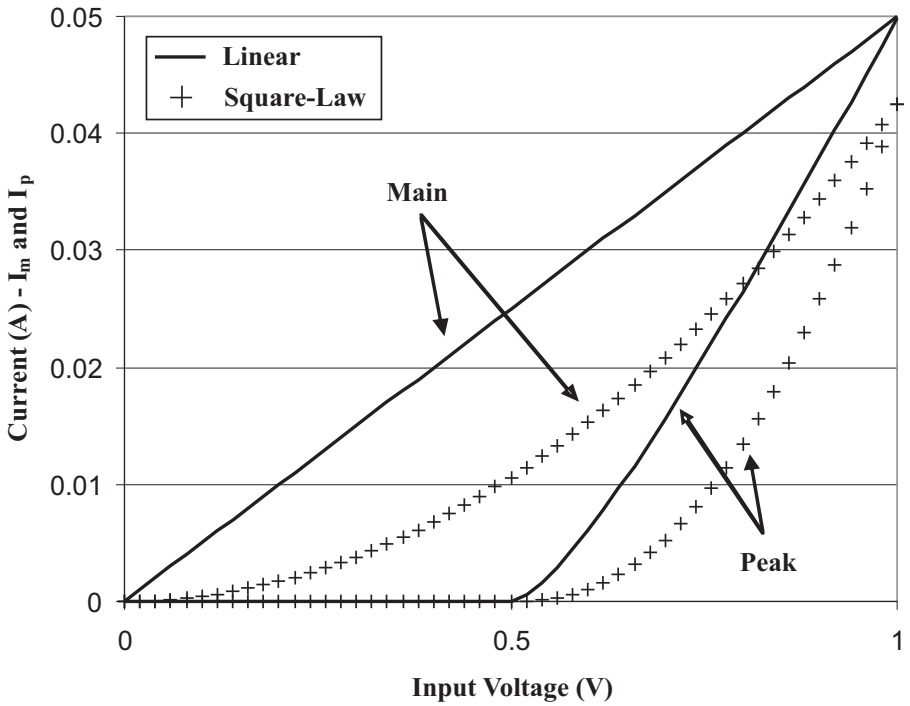


Figure 4.2: Theoretical fundamental output currents with linear and square-law drain current transfer characteristic

- constant gain, global improvement in the efficiency, as well as an extended high efficiency region. However, with a square-law transfer characteristic ($x = 2$), the amplifier is highly non-linear (level-dependent gain), and only offers an improvement in efficiency at high input levels.

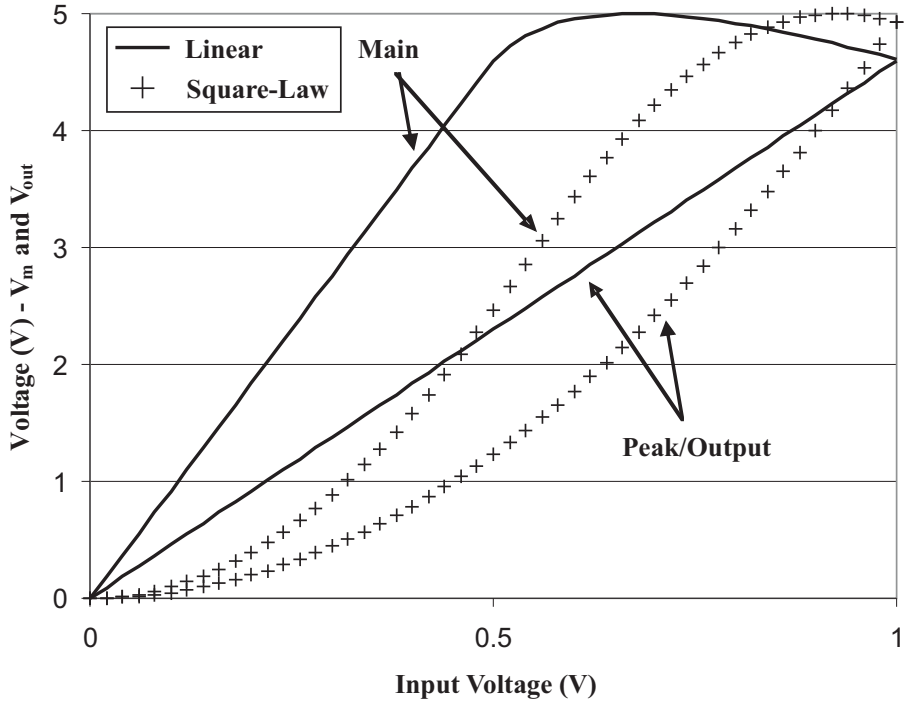


Figure 4.3: Theoretical fundamental output voltages with linear and square-law drain current transfer characteristic

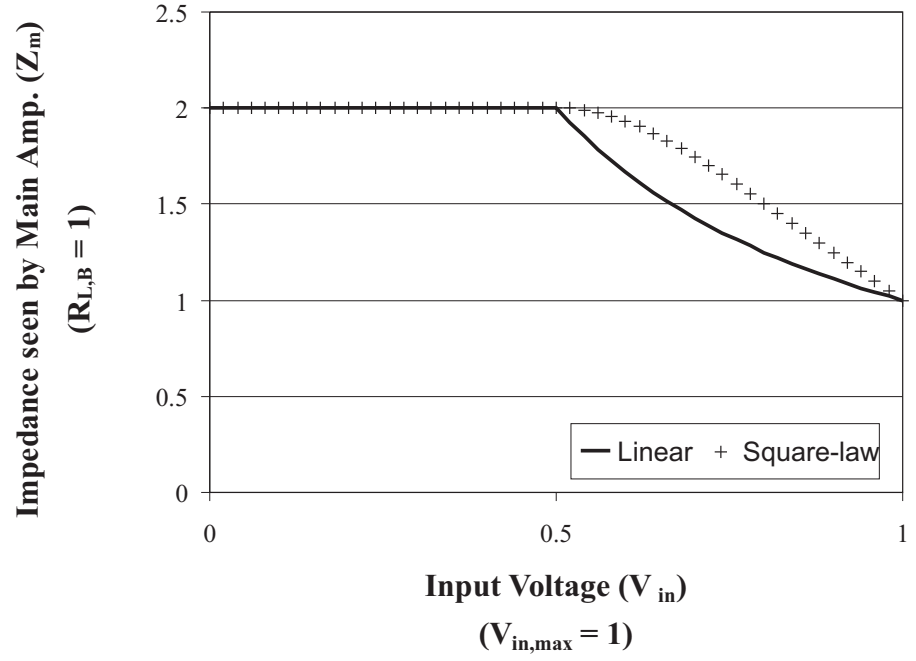


Figure 4.4: Theoretical load modulation of the Doherty amplifier with linear and square-law drain current transfer characteristic

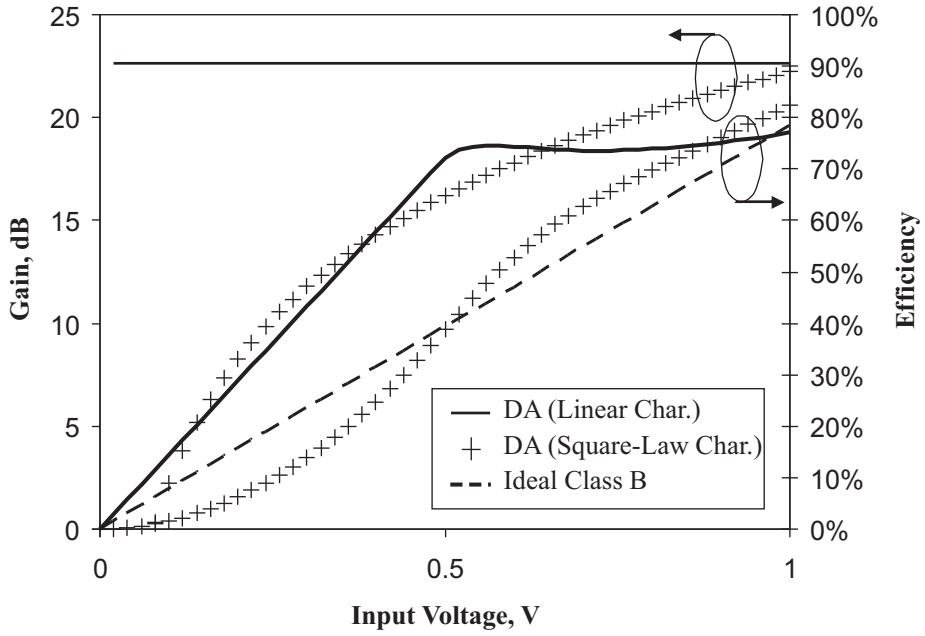


Figure 4.5: Theoretical gain and efficiency of the Doherty amplifier with linear and square-law drain current transfer characteristic

4.3.2 Simulation Results

Harmonic balance simulations of a Doherty amplifier were conducted using AWR Microwave Office [7], as described in Appendix A. The FETs were represented by a Statz model [15] (as described in Appendix C) with values of b and β given in Table 4.1. The Statz model conveniently has this direct mechanism to change the softness of the transistor's pinch-off so that it can be adjusted over a range from linear to square-law. Apart from the gate-voltage to drain-current transfer characteristic, other assumptions concerning the transistor were the same as in the theoretical analysis, with the threshold voltage, V_T, equal to -1 V, no knee voltage ($\alpha = 30$), and no parasitics present.

In order to vary the softness of the drain current transfer function, the Statz model parameter b was varied between 1000 (hard turn-on) and 0 (square-law characteristic). To make the results comparable, β was calculated at each value of b (using (C.1)), in order to give the same maximum output current in all cases (see Figure 4.6). The specific values used for the various cases of soft turn-on are given in Table 4.1. The load resistance of the amplifier was modified in each case to give the highest maximum efficiency without saturating. Correspondingly, the impedance of the quarter-wave transformer (see Figure 4.1) was equal to $2R_L$. These values are also given in Table 4.1.

The effect of this on the efficiency and gain is shown in Figures 4.7 and 4.8 respectively. It can be seen that the simulation results closely match the theoretical results

b	β A/V^2	Peak FET Size Multiplication factor	R_L Ω	Z_T Ω
1000	100.1	2.55	45	90
5	0.6	3.1	46.5	93
2	0.3	3.6	49	98
0.5	0.15	4.4	53	106
0	0.1	5.3	57	114

Table 4.1: The parameters used for determining the effect of soft turn-on

for the linear and square law cases, and it confirms that transistor soft turn-on has a significant effect on the efficiency of a Doherty amplifier. The best performance was obtained for a linear drain current transfer characteristic. However, as the turn-on gets closer to a square-law characteristic, the efficiency characteristic becomes closer to that of an ideal class B amplifier, and the linearity gets significantly worse.

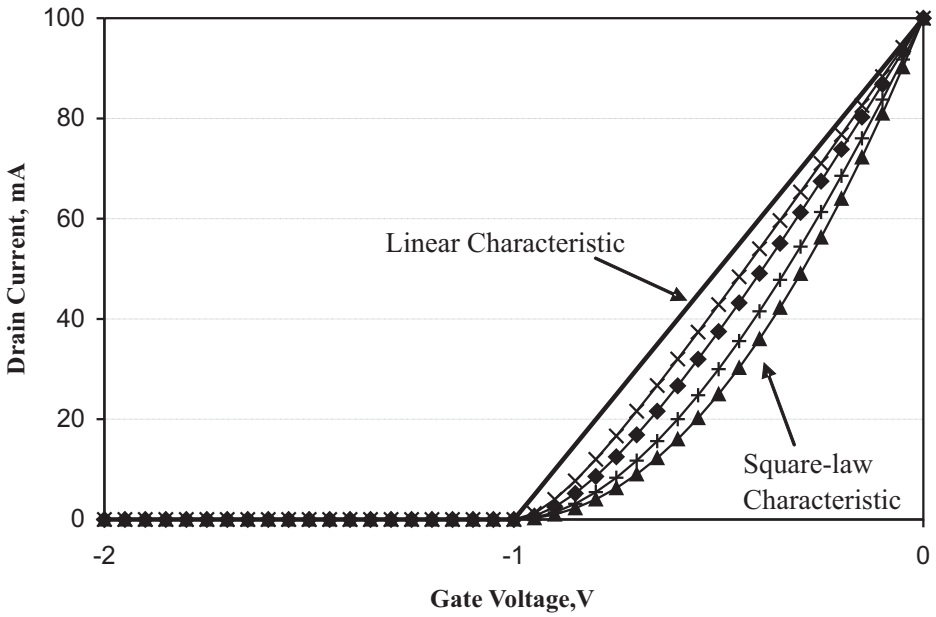


Figure 4.6: Simulated drain current transfer characteristics with varying degrees of soft turn-on

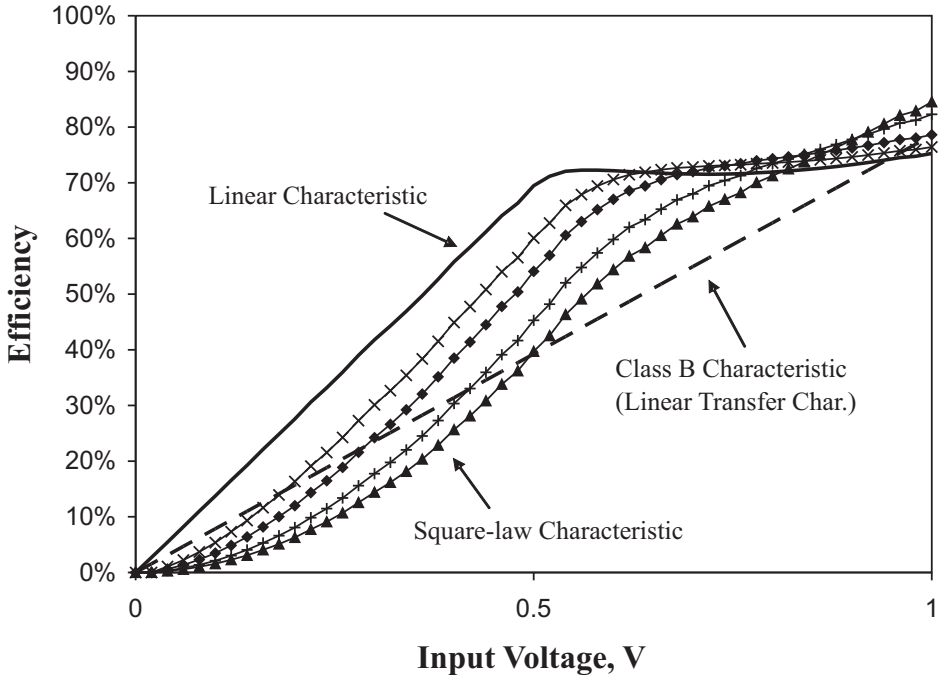


Figure 4.7: Simulated efficiency characteristics with varying degrees of soft turn-on

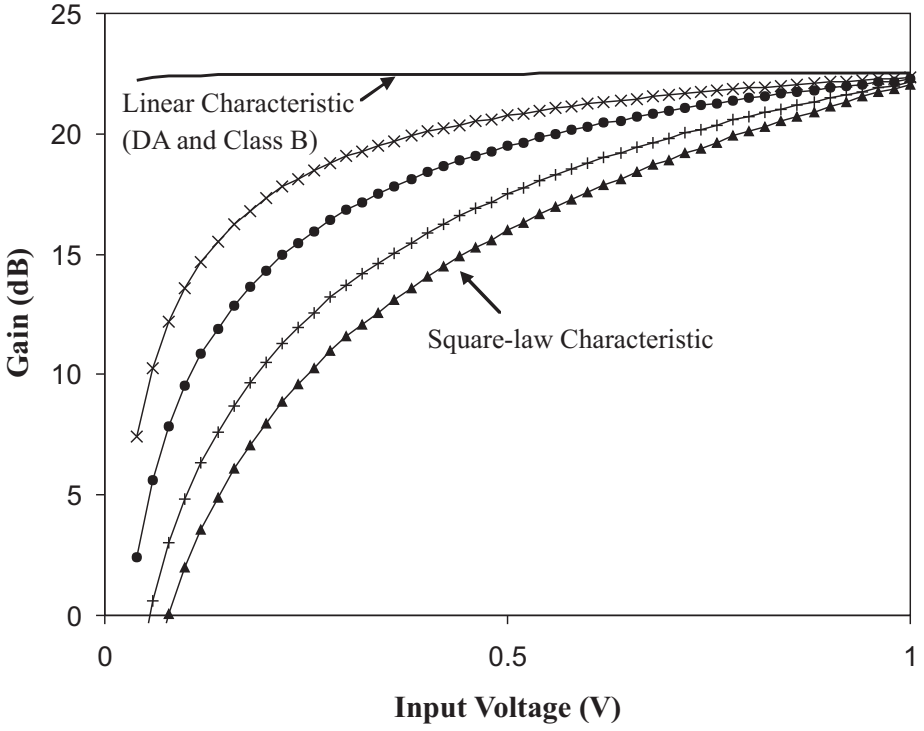


Figure 4.8: Simulated gain characteristics with varying degrees of soft turn-on

4.3.3 Conclusion

Transistor soft turn-on is one of the mechanisms which causes practical Doherty amplifiers to have output characteristics that deviate from the ideal. The soft-turn on of the transistors has a significant detrimental effect on the overall amplifier characteristics, decreasing the average efficiency and increasing the dependance of the gain on the input power (implying nonlinear amplification). The linear transfer characteristic normally used for theoretical analysis gives an upper bound for the output characteristics, while the square-law characteristic gives a lower bound. As such, in order to have a Doherty amplifier with near-ideal output characteristics it is important to either have a transistor with a near-ideal drain current transfer characteristic, or to have a mechanism that corrects for transistor soft turn-on.

4.4 THE EFFECT OF UNEQUAL MAXIMUM DRAIN CURRENTS

There are two potential causes of unequal maximum output currents - 1) the ideal device size ratio of 1:2.55 is not available (where discrete devices are used), and 2) even if the ideal ratio is available, transistor parametric variation will mean there is likely to be some discrepancy anyway. Sections 2.4 and 2.5 indicate that if the peaking amplifier's maximum fundamental output current is significantly less than that of the main amplifier, the Doherty amplifier's output characteristics are significantly worse. However, if the Doherty amplifier is designed using one of the methods described in Section 2.4, then the difference between the main and peaking amplifiers' fundamental output current should be minor.

In order to discern the effect this has on the output of a Doherty amplifier, the ratio between the two devices was varied from 1:3 (main:peak) down to 1:1 (where 1:2.55 is the ideal ratio). A simulation was setup, with ideal transistors ($x = 1$) using a fixed bias ($V_{B,M}$ = -1 V, $V_{B,P}$ = -1.5 V). The parameters used were I_{DSS} = 100 mA (main amplifier only), V_T = -1 V, and V_{DD} = 5 V (as in Sections 2.4 and 4.3). Due to the change in the main amplifier voltage characteristic, this meant the load resistance varied from 47 Ω (1:3) to 31.1 Ω (1:1). The fundamental output currents and voltages were calculated according to(B.8), (B.25), (2.16), (2.6), and are shown in Figures 4.9 and 4.10. It can be seen that with a transistor size ratio of 1:2.55, the output currents and voltages approximate the ideal behaviour (see Figure 2.4), and as the ratio gets lower, they move further and further away. If the ratio is higher than ideal, both the peaking amplifier's output current and the main amplifier's output voltage are a significant departure from the ideal characteristics.

The efficiency and gain are shown in Figures 4.11 and 4.12 respectively. It can be seen that unequal maximum fundamental output currents do not cause a significant

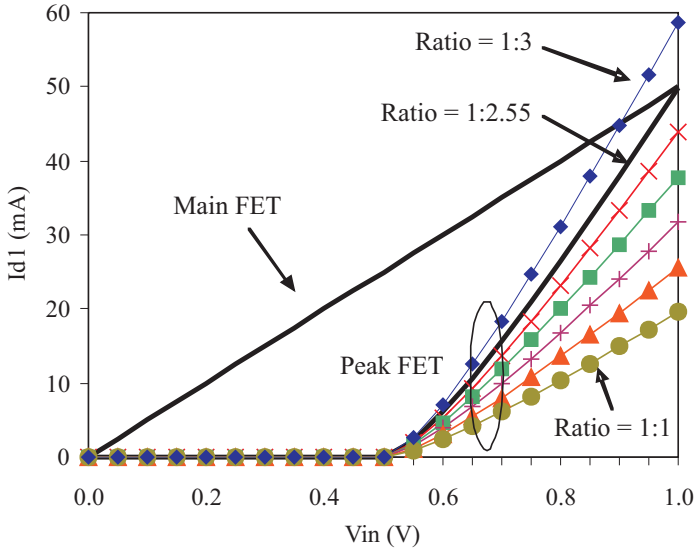


Figure 4.9: Theoretical fundamental output currents with unequal maximum fundamental output current

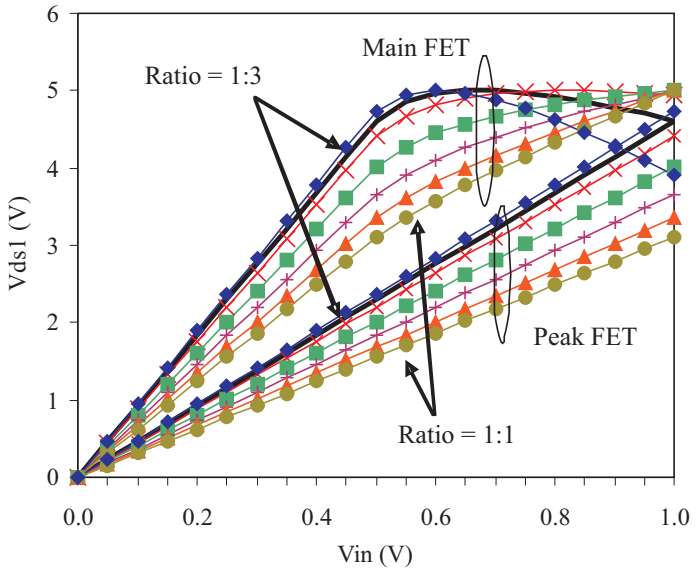


Figure 4.10: Theoretical fundamental output voltages with unequal maximum fundamental output current

departure from ideal Doherty output characteristics, unless the ratio drops below 1:2. When the ratio is approximately 1:2, the efficiency is still very similar to the ideal case, although the gain drops very slightly. When the ratio is 1:3, the efficiency characteristic is still very good, but the amplifier's gain is non-constant, implying nonlinear amplification. It should be noted that having a lower-than-ideal peaking amplifier maximum

output current does not cause the amplifier to become non-linear, it simply reduces both the gain and efficiency. The gain reduction is unavoidable, as the peaking amplifier's output power is necessarily lower if its output current is lower, and hence the output power of the whole amplifier is lower.

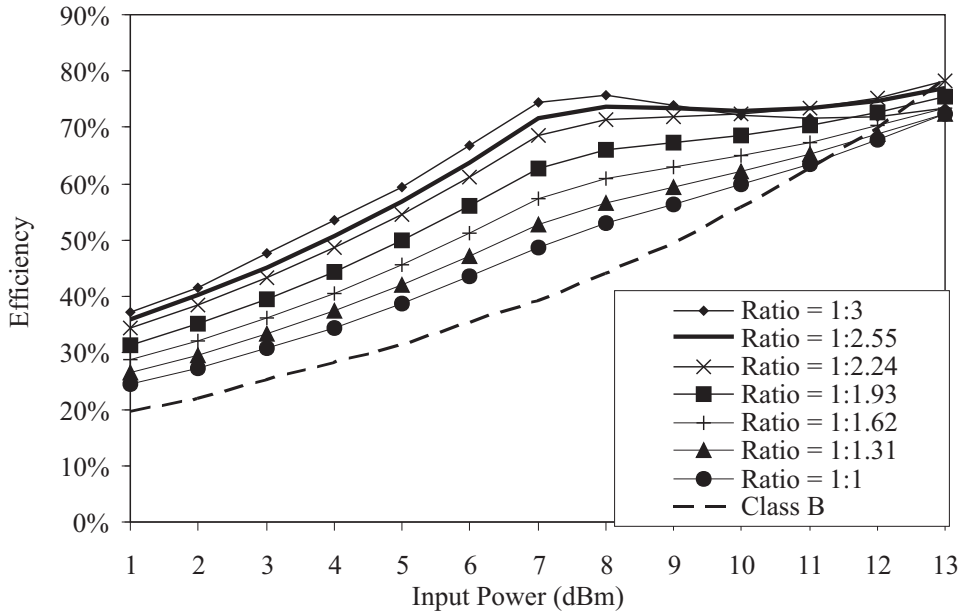


Figure 4.11: Simulated efficiency with unequal maximum fundamental output current

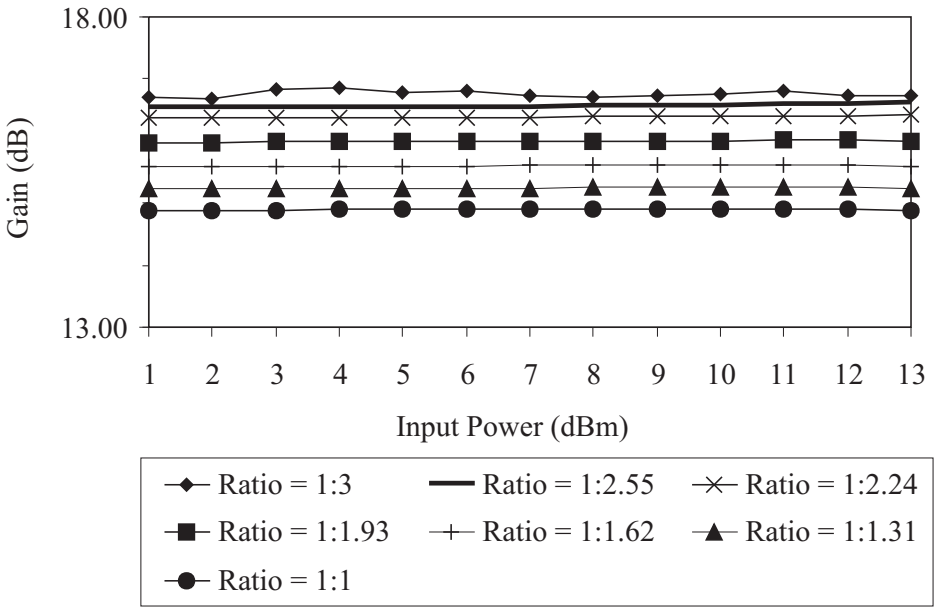


Figure 4.12: Simulated gain with unequal maximum fundamental output current

In conclusion, unequal maximum fundamental output currents can be a contributing factor to the discrepancies between ideal and practical Doherty amplifier output characteristics. If the Doherty amplifier is designed with this in mind, but parametric variation (or the unavailability of discrete devices with the correct ratio,) means there is a small departure from the ideal ratio, the decrease in efficiency is not dramatic. However, if the ratio drops under 1:2, then the efficiency starts to decrease significantly from the ideal case. In all cases, the gain of the amplifier is constant with respect to input power (implying linear amplification), but as the peaking amplifier's output current decreases, the gain of the Doherty amplifier also decreases, which is a direct result of the decrease in the peaking amplifier's output power. A number of papers implement a Doherty amplifier with a fixed bias, equal transistor sizes and equal input power, meaning the worst case given here (a ratio of 1:1) is their ideal output (given that the circuit components are all ideal). This type of Doherty amplifier was discussed from a theoretical point of view in Section 2.5.

Chapter 5

A THEORETICALLY BASED GATE BIAS CONTROL SCHEME

5.1 INTRODUCTION

Transistor soft turn-on can be a major problem in achieving a Doherty amplifier whose performance matches theory, as shown in Section 4.3. Variation in the maximum fundamental drain current of the two transistors also has a negative impact on results (see Section 4.4). Furthermore, as shown in Section 2.4.1, there is a small variation in results depending on which method is used to ensure the peaking amplifier's output approximates the ideal (see Figure 5.1). Out of the available methods, bias control gives the highest efficiency and gain, with similar linearity (as indicated by the flatness of the gain characteristic). It is also capable of overcoming the problems created by transistor soft turn-on and transistor parametric variation. The existing literature on the subject (see Section 3.2.1), has usually created a bias control scheme based on simulated or measured results. Given that two of the major contributors to non-ideal results are easily modelled using the Statz model [15] (see Appendix C), it was decided to create a gate bias control scheme based on theory to achieve the ideal current characteristics shown in Figure 5.1.

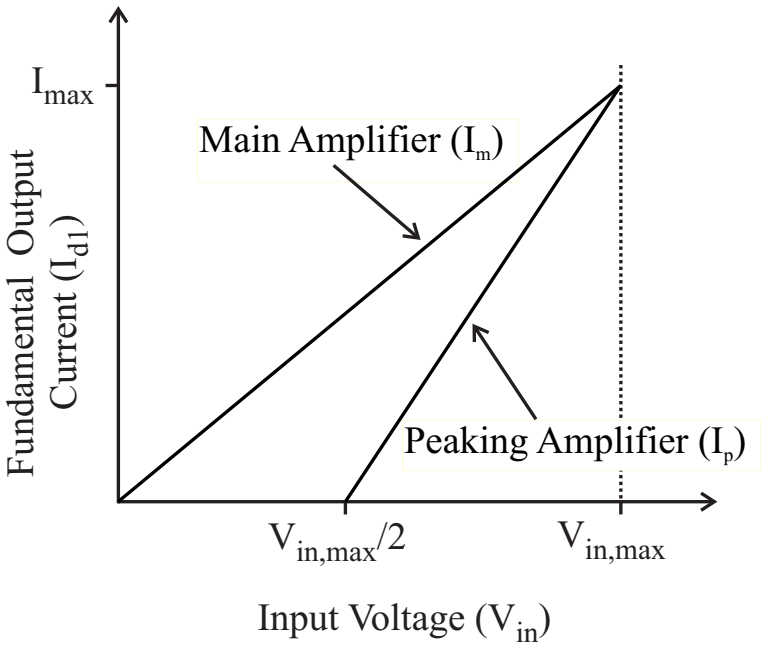


Figure 5.1: Ideal main and peaking amplifier transfer characteristics

5.2 GATE BIAS CONTROL STRATEGY

The proposed bias control strategy ensures that the main and peaking amplifiers closely mimic the desired fundamental output current characteristics (shown in Figure 5.1). Essentially, the main amplifier is operated in class B whilst the peaking amplifier is inactive for low power levels, and then rises from class C to class B as the input level increases from 6 dB below P_{max} to P_{max}. The input power is measured at the input of the amplifier, and a suitable gate bias voltage, V_B, is established for each FET so they achieve the desired fundamental output current (I_{d1}) as given in Figure 5.1.

In this work, the Statz model (see Appendix C) [15] was used for the FET drain current transfer characteristic, as it has a convenient mechanism to adjust the softness of the transistor's turn-on. The equation for the Statz model saturation drain current is:

$$I_d(V_{gs}) = \frac{\beta(V_{gs} - V_T)^2}{1 + b(V_{gs} - V_T)} \tag{5.1}$$

where I_d is the instantaneous drain current, V_T is the threshold voltage, β and b are parameters, and V_{gs} is the gate-to-source voltage, described by:

$$v_{gs}(t) = V_{in} \sin \omega t + V_B \tag{5.2}$$

where V_{in} is the input voltage and V_B is the gate bias voltage. For a given value of V_B

and V_{in}, the fundamental component of the output current, I_{d1}, is given by:

$$\begin{aligned} I_{d1} &= \frac{1}{\pi}\int_0^{2\pi} I_d(V_{in}\sin\omega t + V_B)\sin\theta\, d\theta \\ &= \frac{1}{\pi}\int_0^{2\pi} \frac{\beta(V_{in}\sin\theta + V_B - V_T)^2}{1 + b(V_{in}\sin\theta + V_B - V_T)}\sin\theta\, d\theta \end{aligned} \tag{5.3}$$

In this work, I_{d1} is known for a given value of V_{in} (see Figure 5.1), and V_B is to be determined. V_B is found by an iterative solution of (5.3) and therefore requires an initial guess. During the solution of (5.3), the trapezoid method with 10,000 points was used to numerically evaluate the integral. To obtain an initial guess, it was assumed that the drain current waveform is approximately a half-sinusoid, whose peak value, $I_{d,pk}$ is twice the fundamental component, I_{d1}. With this value of $I_{d,pk}$, the corresponding peak value of gate voltage, $V_{gs,pk}$, can be obtained by solving (5.1) with the aid of Figure 5.2, giving an initial guess of V_B:

$$V_B = V_T + \frac{2bI_{d1} + \sqrt{2b^2I_{d1}^2 + 8\beta I_{d1}}}{2\beta} - V_{in} \tag{5.4}$$

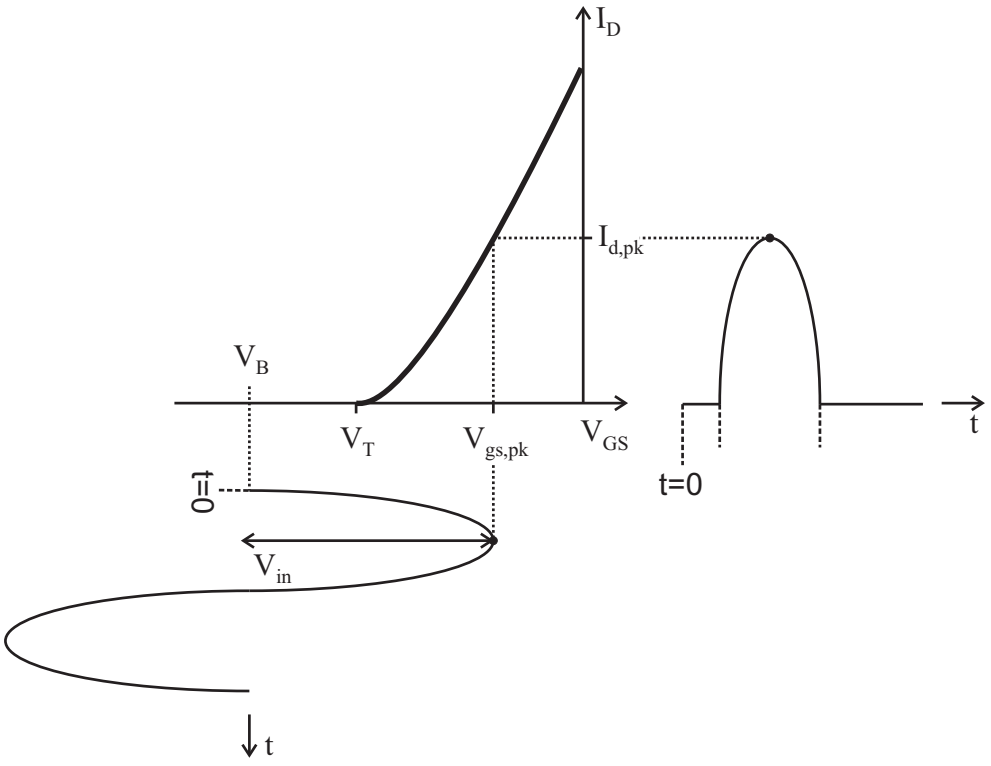


Figure 5.2: Graphical representation of the mapping of the gate voltage waveform to the drain current waveform

The gate bias control strategy for ideal transistors (with a threshold voltage, V_T, of -1 V) is shown in Figure 5.3. The peaking amplifier is initially biased at -2.5 V to

ensure it is off during the low power regime. During the high power regime, the peaking amplifier's bias continuously increases until it reaches class B at maximum input power ($V_{B,P} = -1\ V$). The main amplifier has a fixed class B bias of -1 V.

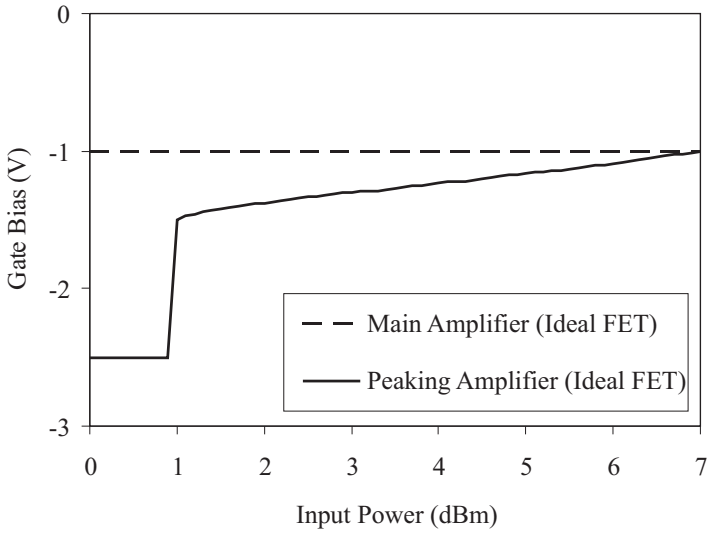


Figure 5.3: Gate bias control for ideal transistors

5.2.1 Simulations with an Ideal Circuit, and Non-Ideal FET Transfer Characteristics

To test the proposed bias control strategy, the FETs in the ideal circuit (used for the simulations in Chapters 2 and 4) were given various gate-voltage to drain-current transfer characteristics. So as not to complicate the test, an ideal circuit, being one with resistive non-linearities and no parasitic reactances was considered. Two degrees of soft turn-on were considered:

1. One based on data-sheet figures for a Eudyna FLK017WF, with $\beta = 0.195$, $V_T = -2$, $b = 6$ (which we denote a data-sheet transistor)

2. One based on a square-law characteristic, with $\beta = 0.015$, $V_T = -2$, $b = 0$ (which we denote a square-law transistor)

These values result in $I_{DSS} = 60mA$. To confirm that unequal values of I_{DSS} is also correctable by this bias control scheme, two cases were implemented without soft turn-on, but with unequal maximum drain currents. The simulations were carried out in AWR Microwave Office [7] as described in Appendix A.

Initially it was thought that gate bias control was only required on the peaking amplifier, with a fixed class B bias for the main amplifier (as this is the case for ideal transistors, as seen in Figure 5.3). In order to test this assumption, the performance

of the Doherty amplifier was determined, using data-sheet transistors, with gate bias control only applied to the peaking amplifier, and then gate bias control applied to both amplifiers. The resulting gain and efficiency is shown in Figure 5.4.

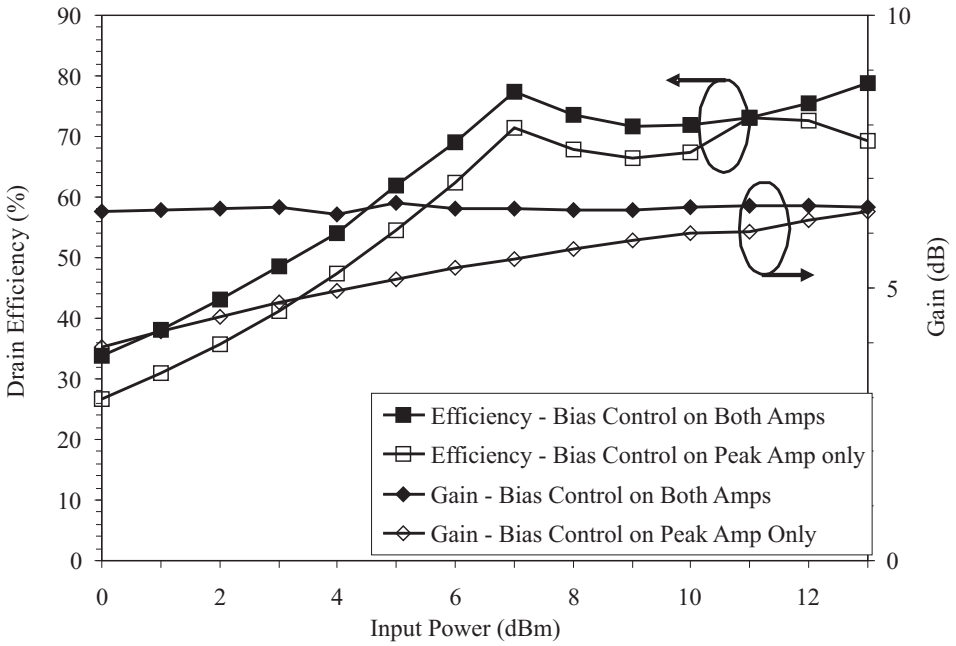


Figure 5.4: Simulated gain and efficiency of the Doherty amplifier with gate bias control performed only on the peaking amplifier or on both the main and peaking amplifiers

It can be seen that there is a minor difference in DC-to-RF efficiency, and a significant difference in the gain of the Doherty amplifier (with respect to input power) depending on whether the main amplifier gate bias is fixed or dynamically controlled. A constant gain characteristic (with respect to input power) implies linear amplification, and as such, is highly desirable. Thus, gate bias control is desirable on both the main and peaking amplifiers. With this in mind, all further simulations of a Doherty amplifier in this chapter utilise bias control on both main and peaking amplifiers. It should be noted that the gate bias control on the main and peaking amplifiers is different, with the main amplifier's bias being close to class B at all times, while the peaking amplifier's bias increases from class C up to class B.

To see whether this method can handle different FET transfer characteristics, simulations of two Doherty amplifiers were performed, one using only data-sheet transistors, and the other using only square-law transistors. The supply voltage (V_{DD}) was set to 3 V, as this is the optimum value for identical transistors with $I_{DSS} = 60mA$ (as determined by (2.16)). The efficiency, output power and gain are shown in Figures 5.5 to 5.7. The bias control for the main and peaking amplifiers in each case is different, as it is based in the transfer characteristics of the transistors used.

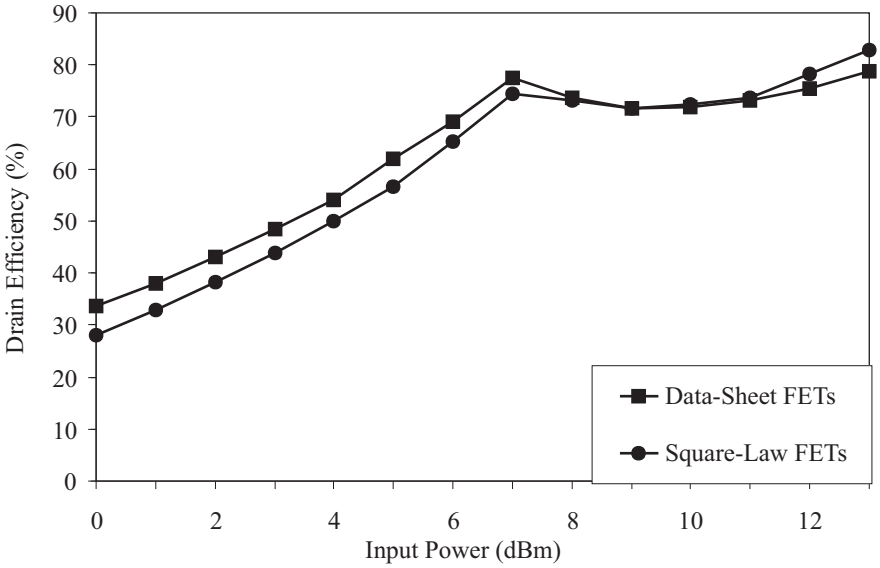


Figure 5.5: Simulated efficiency of the Doherty amplifier with FETs based on a data-sheet transfer characteristic or a square-law transfer characteristic

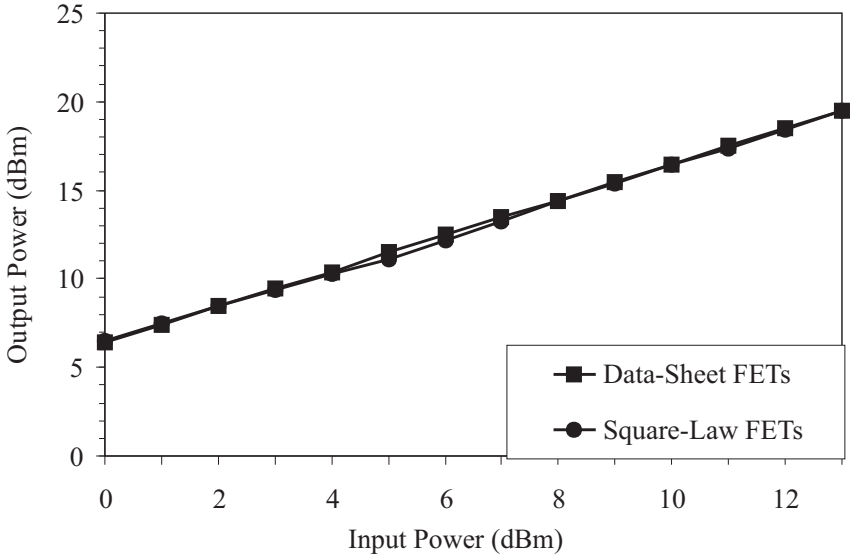


Figure 5.6: Simulated output power of the Doherty amplifier with FETs based on a data-sheet transfer characteristic or a square-law transfer characteristic

It can be seen that with bias control implemented, both cases give near-ideal Doherty characteristics, with a distinct region of high efficiency over the last 6 dB of input power, and a constant gain with respect to input power. These results confirm that the proposed bias control strategy can overcome the problems caused by soft turn-on for Doherty amplifiers.

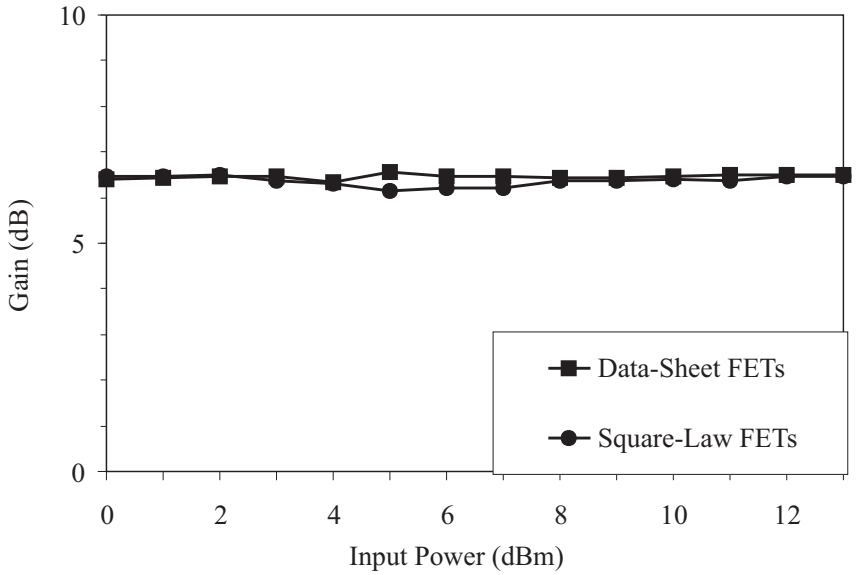


Figure 5.7: Simulated gain of the Doherty amplifier with FETs based on a data-sheet transfer characteristic or a square-law transfer characteristic

To confirm that gate bias control can also counteract the problems caused by unequal values of I_{DSS}, simulations were run with the maximum drain current of the peaking amplifier's FET (I_{DSS}) decreased by 10% (to 54 mA) and 20% (to 48 mA) successively (compared to the main amplifier's FET, which remained constant at 60 mA). This gave ratios of 1:0.9 and 1:0.8 (main FET I_{DSS}:peak FET I_{DSS}) respectively. The drain transfer characteristics are shown in Figure 5.8.

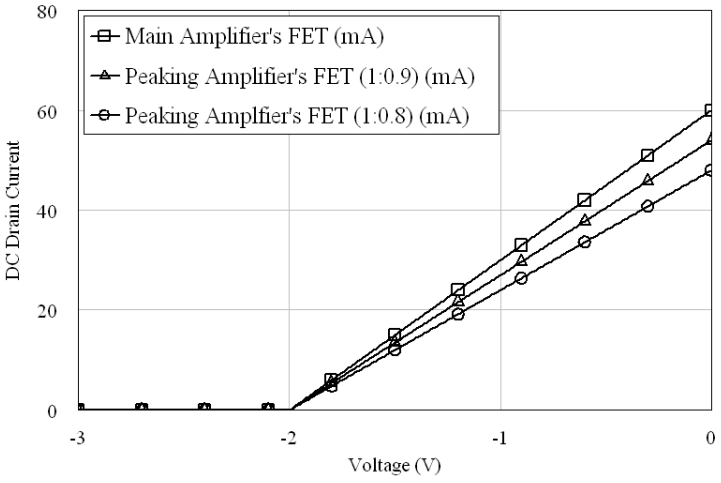


Figure 5.8: The gate-voltage to drain-current transfer characteristics of the FETs used to determine the effectiveness of the bias control strategy with unequal maximum drain currents

The gate bias control for each main and each peaking amplifier is different, with the main amplifiers' biases being close to class B at all times, while the peaking amplifiers' biases increases from class C up to class B. The differences between the bias control in each case are because the strategy is based on the transfer characteristics of the transistors, as well as the desired drain current characteristics. Even though the main amplifiers' transfer characteristic is the same in each case, the desired output current characteristics differ, as the bias control strategy ensures that the main and peaking amplifiers will have equal maximum fundamental output currents. This means the amplifier with the higher I_{DSS} should not be biased at class B at maximum output power, but should be biased in low class C.

Biasing one of the amplifiers in low class C at maximum input power means that the Doherty amplifier has a lower output power and gain, but also ensures that the amplifier has nearly constant gain with respect to input power (implying linear amplification), and that there is a region of high efficiency. Since the output power is lower, the supply voltage, V_{DD}, should also be lowered, as this can be done without putting the amplifier into saturation. As there is no triode region present in these transistors, V_{DD} is lowered by the same percentage as the maximum output current - i.e. it is set to 2.7 V and 2.4 V respectively (compared to 3 V when both amplifiers have $I_{DSS} = 60$ mA). The output characteristics of the amplifier are given in Figures 5.9 to 5.11.

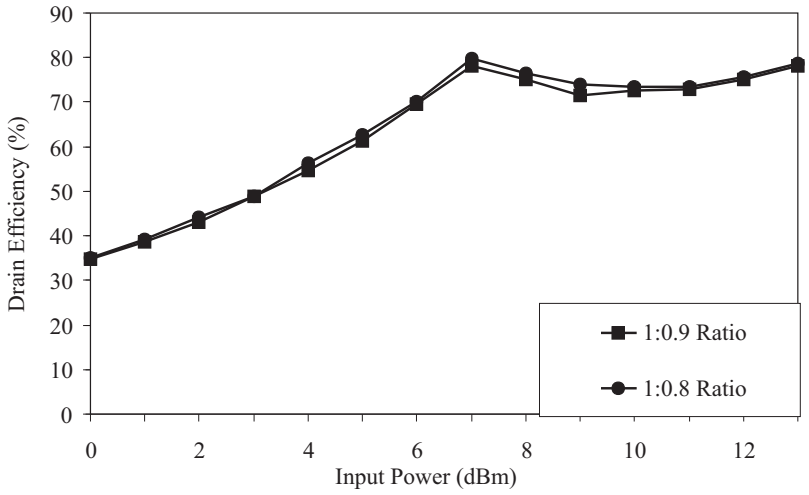


Figure 5.9: Simulated efficiency of the Doherty amplifier with FETs that have unequal maximum drain currents

It can be seen that the efficiency characteristic of the Doherty amplifier is consistent with the ideal case, as is the output power and gain. As expected the output power and gain of the amplifier decrease as the maximum drain current is decreased, but by choosing an appropriate supply voltage, the efficiency does not suffer.

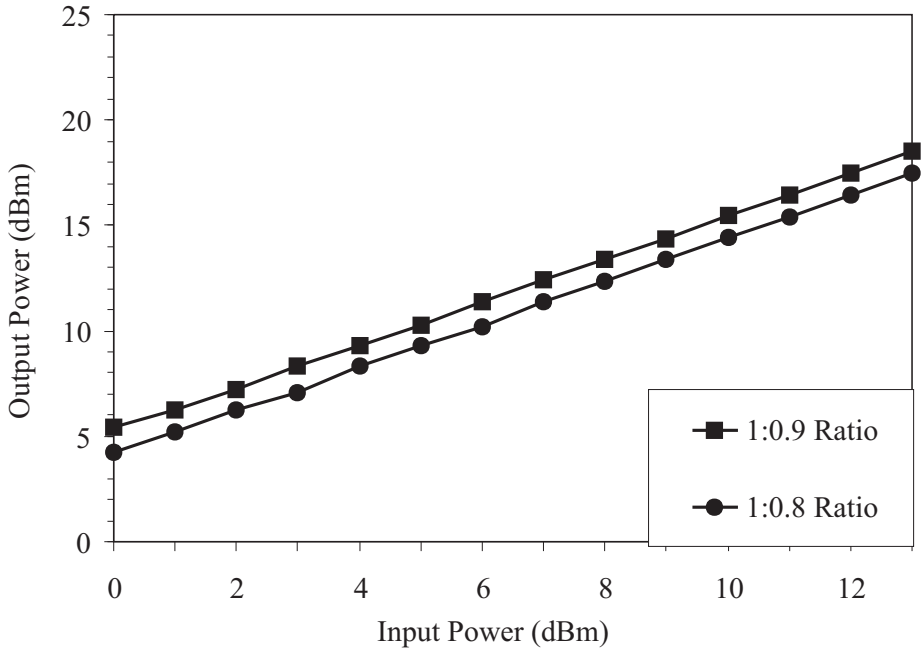


Figure 5.10: Simulated output power of the Doherty amplifier with FETs that have unequal maximum drain currents

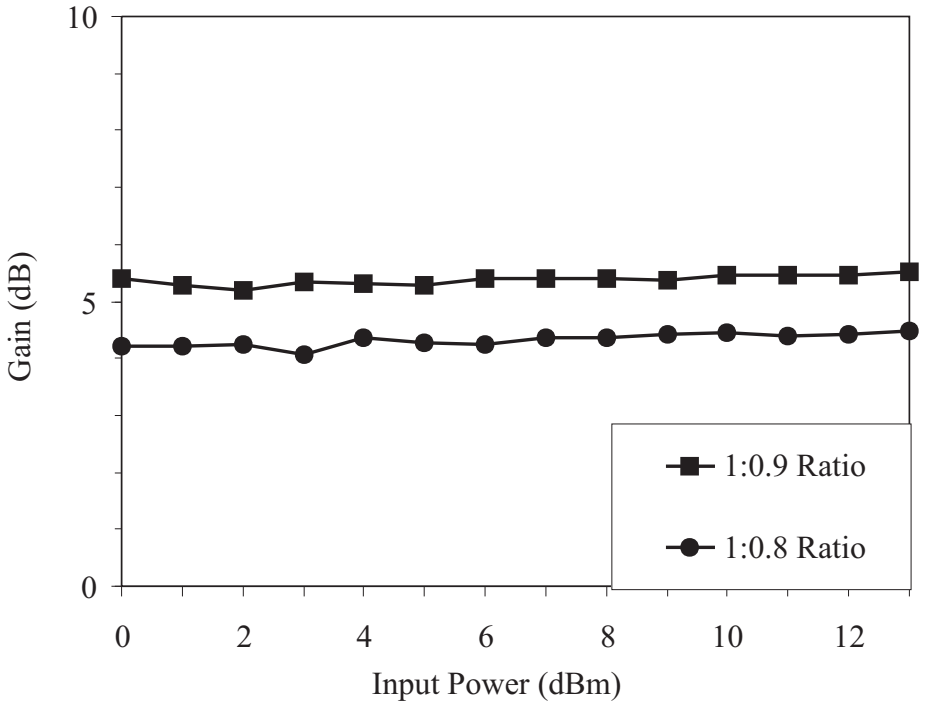


Figure 5.11: Simulated gain of the Doherty amplifier with FETs that have unequal maximum drain currents

5.3 IMPLEMENTATION

To test the algorithm described in Section 5.2 with a practical circuit, a 770 MHz Doherty amplifier was designed, employing two Eudyna FLK017WF GaAs FETs. These FETs have a maximum saturation drain current (I_{DSS}) of 60 mA, a pinch-off voltage (V_T) of -2 V, and a drain knee voltage (V_k) of 1 V. In theory (ignoring parasitic effects), this Doherty amplifier has a gain of 5.3 dB, a maximum output power of 18.3 dBm, and a maximum efficiency (η_{max}) of 65%. These theoretical values account for the triode region of the FETs and assume a 3.6 V supply and a 50 Ω load for the Doherty amplifier, which at maximum input power translates to 100 Ω for class B. The equations used for these calculations are given in Section 2.2.4, where to account for the triode region of the amplifier, V_{DD} is replaced by $V_{DD} - V_k$ in (2.19).

Harmonic balance simulations of a bias-controlled Doherty amplifier were conducted using AWR Microwave Office [7], as described in Appendix A. The FETs were represented by a nonlinear model based upon the Statz drain current and capacitance model [15], which includes chip and package parasitic effects (see Appendix C). A load resistance of 50 Ω was used (rather than a higher, more-optimal load), as this means the load presented to the transistors was significantly smaller than R_{ds}. Without impedance transformers, the uncertainty of R_{ds} for class B and class C operations is diminished (see Appendix C).

The FET output capacitances were absorbed into the quarter-wave transmission line between the main and peaking amplifiers according to [103]. The FETs used had an output capacitance of approximately 0.34 pF. This resulted in the 100 Ω ($2R_L$) quarter-wave transformer (see Figure 1.2) being replaced with a 80.5° microstrip line with an impedance of 101 Ω [103], and also meant the output capacitances did not need to be absorbed into a parallel resonator circuit. The amplifiers were designed to operate into a 100 Ω load ($2R_L$), meaning an external 50 Ω load could be coupled directly to the amplifier via 50 Ω microstrip. A basic circuit diagram is shown in Figure 5.12, while the complete one is given in Appendix D. The even harmonics generated by the amplifiers' outputs are shunted to ground via the quarter-wave transformers at their outputs. The odd harmonics generated by the peaking amplifier are shunted to ground via the quarter-wave transformer at the main amplifier's output.

Two combinations of transistors were simulated:

1. Both FETs based on data-sheet figures for the Eudyna FLK017WF
2. Changing the peaking transistor to a square law model FET with a lower maximum drain current ($\beta = 0.015, V_T = -2, b = 0$).

To obtain the gate bias control scheme, the effect of the parasitic source and drain resistances needs to be taken into account, as shown in Figure 5.13. Both of these

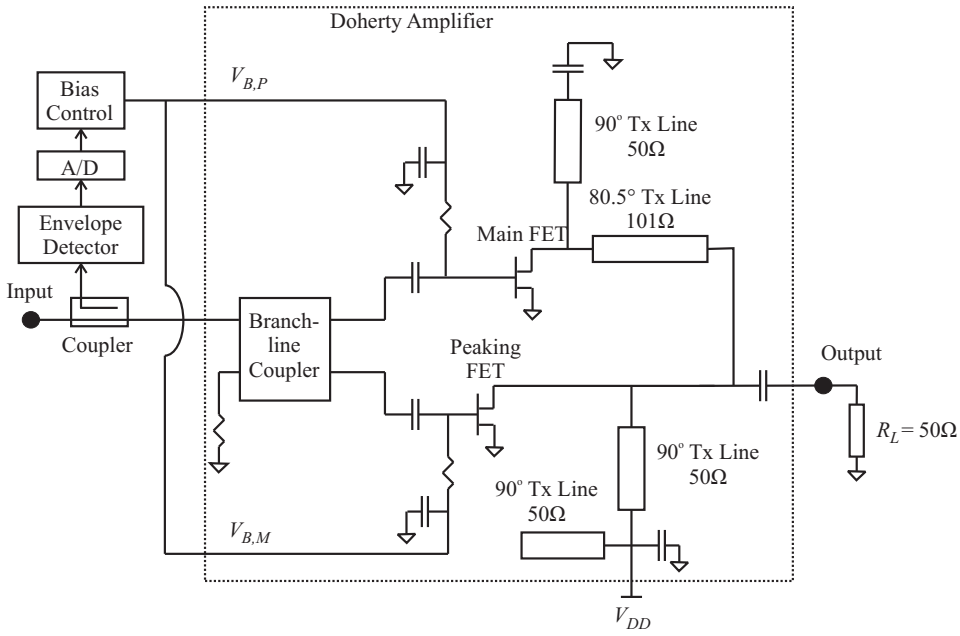


Figure 5.12: Doherty amplifier circuit diagram for gate bias control

models give the same drain-current to gate-voltage transfer characteristic. The Statz drain current model used to calculate the bias control strategy was fitted to the FET transfer characteristics at their external terminals ($\beta = 0.205$ for the data-sheet FET and $\beta = 0.014$ for the square law FET). Modifying β accounts for the internal resistances $R_s = 1.7\ \Omega$ and $R_d = 2\ \Omega$. The supply voltage (V_{DD}) was set to 3.6 V and 3.5 V respectively for the two combinations, and was chosen based upon the simulated maximum fundamental drain-to-source voltage of the main amplifier (which is always higher than that of the peaking amplifier - see Chapter 2). This was added to the knee voltage of the transistors (1 V) to get the supply voltage values.

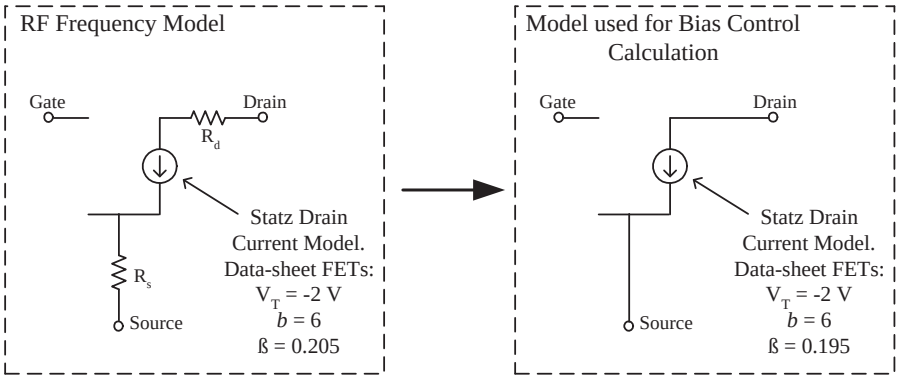


Figure 5.13: Transistor models used in simulation and in calculating the bias control strategy

The transistor transfer characteristics are shown in Figure 5.14. The data-sheet characteristic is the same as that used in the ideal circuit simulations (in Section 5.2.1),

but the square-law characteristic has been modified to cover the potential problems of both soft turn-on and unequal maximum drain currents. The gate bias control scheme is shown in Figure 5.15. In the low power regime, the peaking amplifier's gate bias voltage was set to -3.5 V to ensure that it remains off. Figure 5.16 shows the simulated fundamental output currents of both amplifiers, where two data-sheet FETs are used.

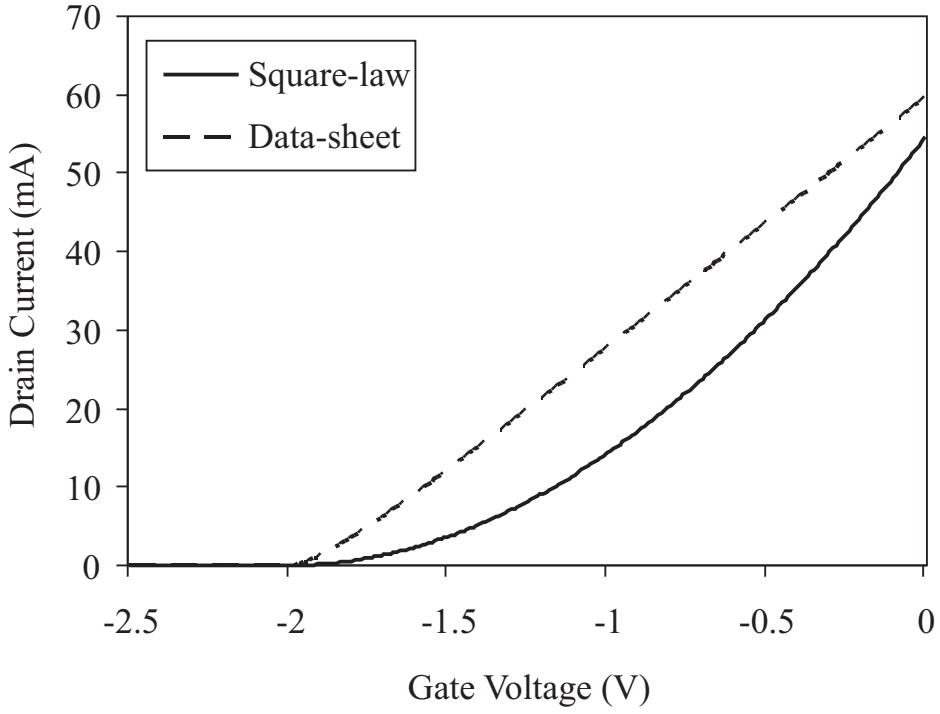


Figure 5.14: Transistor gate-voltage to drain-current transfer functions

It can be seen that the approximation given by (5.4) gives relatively good results, but the ideal Doherty characteristic is not quite achieved, even with the complete analysis, which refines the result (given by (5.3)). This is a result of a 0.8 dB imbalance between the input signals of the two FETs. This imbalance arises from coupler asymmetry being exacerbated by asymmetric loading by the FET inputs, which differ due to their different bias conditions. Conversely, in the analysis, it is assumed that the FETs are driven equally by voltage sources.

The simulated load impedance of the main amplifier is shown in Figure 5.17, compared with the ideal load modulation characteristic, and the load of the comparable class B amplifier. It can be seen that the bias control scheme gives near-ideal results.

The output characteristics of these amplifiers were compared to the same amplifiers with a fixed class B bias ($V_{B,M} = V_{B,P} =$ -2 V). This is used for the comparison, as it is a linear amplifier with the same maximum output power as the Doherty amplifier. It also means that any issues arising from the components used are common to both

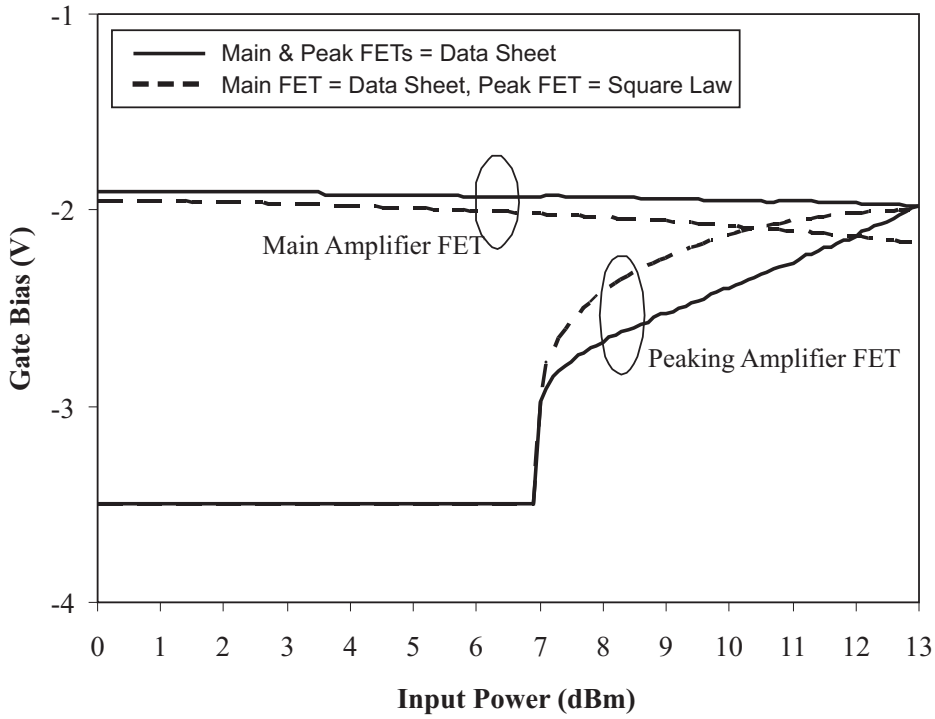


Figure 5.15: Gate bias control scheme for the two combinations of FETs used in simulations

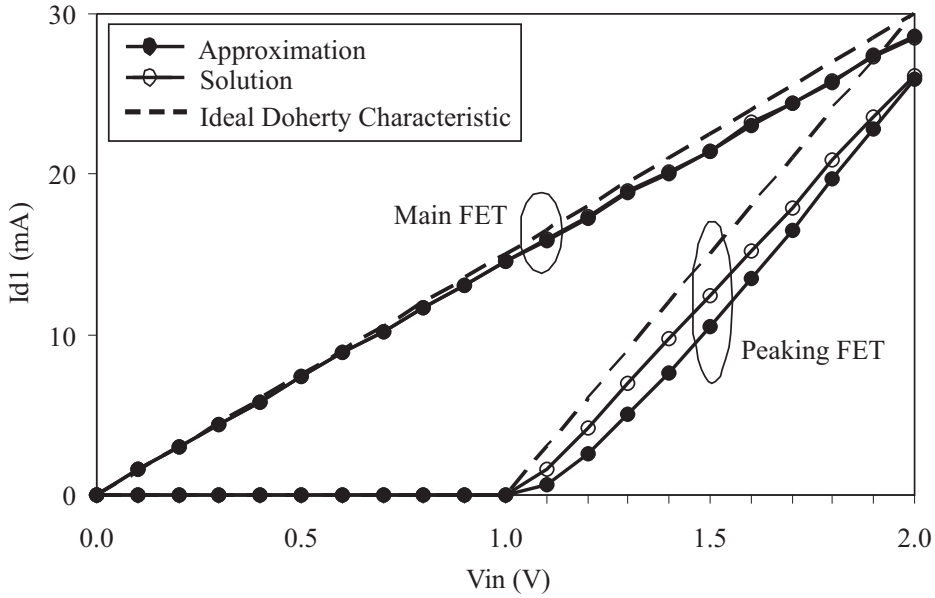


Figure 5.16: Fundamental drain currents using bias control on a Doherty amplifier with two data-sheet FETs

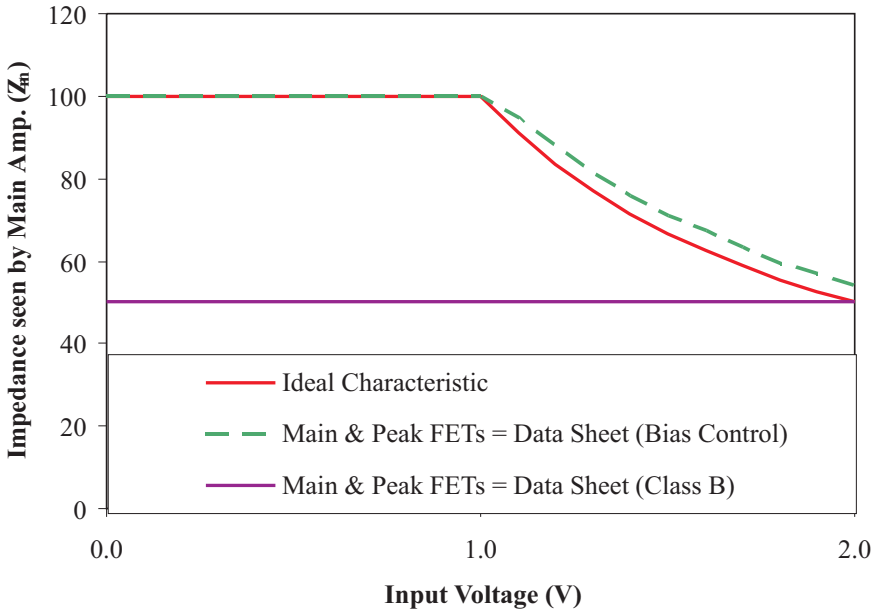


Figure 5.17: Load Modulation of the impedance seen by the main amplifier

amplifiers. Figure 5.18 shows that in both cases the efficiency is significantly better than the class B amplifier, except at the highest power levels. Most importantly, the shape of the efficiency curves are consistent with Doherty operation. The efficiency of the case with a square law peaking amplifier FET is slightly lower than that of the two data-sheet FETs as the supply voltage has not been optimised accurately enough.

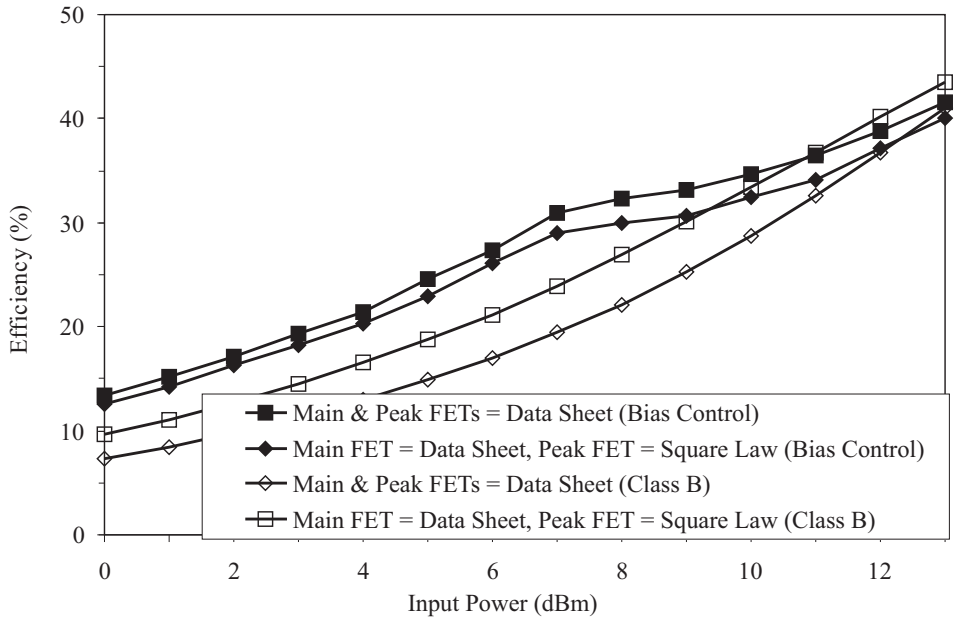


Figure 5.18: Simulated efficiency of the Doherty amplifier with bias control

The gain and output power of the Doherty and the class B amplifier are shown in Figures 5.20 and 5.19. It can be seen that linearity of the bias controlled Doherty amplifier is comparable to, or better than the class B amplifier's (as indicated by the flatness of the gain characteristic). The simulated gain with two data-sheet FETs averages 3.5 dB, and differs from the theoretical value (5.3 dB) due to FET drive imbalance, losses in the coupler and the FET parasitic gate resistance.

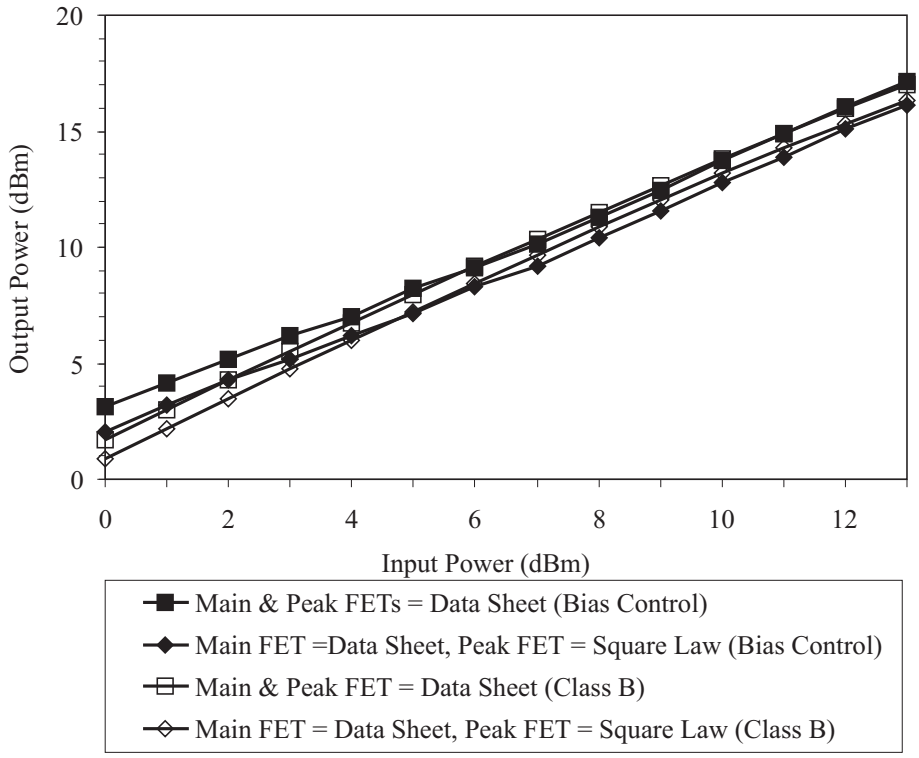


Figure 5.19: Simulated output power of the Doherty amplifier with bias control

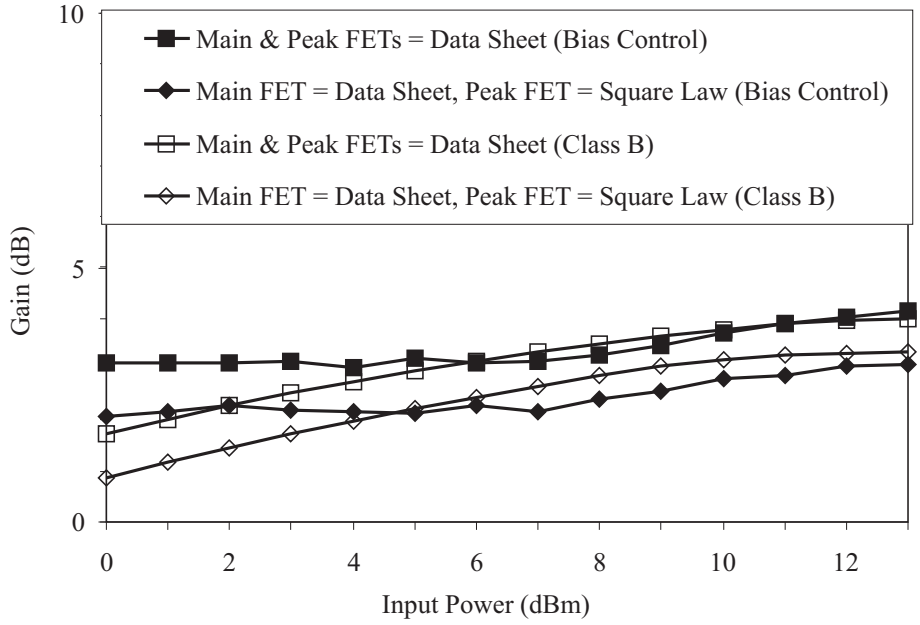


Figure 5.20: Simulated gain of the Doherty amplifier with bias control

5.4 EXPERIMENTAL RESULTS

An amplifier was built using microstrip lines and two Eudyna FLK017WF FETs on a 0.7874 mm (31 mil) substrate with a dielectic constant of 2.2 (see Figure 5.21). The S-parameters of the amplifier were measured under class AB conditions ($V_{B,M} = V_{B,P} = -0.7\ V$), and compared to those generated by simulations (using two data-sheet transistors, as described in Section 5.3) to ensure that the prototype amplifier was close to the design (see Appendix E). Figure 5.22 shows S_{21} for the amplifier around the designed centre frequency of 770 MHz. It can be seen that the centre frequency shifted to 800 MHz, due to the tolerance of the substrate dielectric constant. The maximum gain under this bias condition is 10.9 dB, but it should be noted that the gain of a class AB amplifier is higher than that of a class B or class C amplifier (as is used in a Doherty circuit).

The DC i/v characteristics of each FET were measured. The drain current model (5.1) was fitted to these measurements assuming a source and drain resistance of 1.7 Ω and 2 Ω respectively. The resulting model parameters ($\beta = 0.054$, $V_T = -2.3$, $b = 1$) were subsequently used in simulations to compare with experimental results (the two FETs had near identical transfer characteristics, as shown in Figure 5.23). For calculating the gate bias control scheme, a value of $\beta = 0.050$ was used, as this gives the same characteristic at the external terminals of the FET.

The bandwidth of the amplifier was also determined, both at maximum input power, and at half of maximum input power. The results are shown in Figure 5.24,

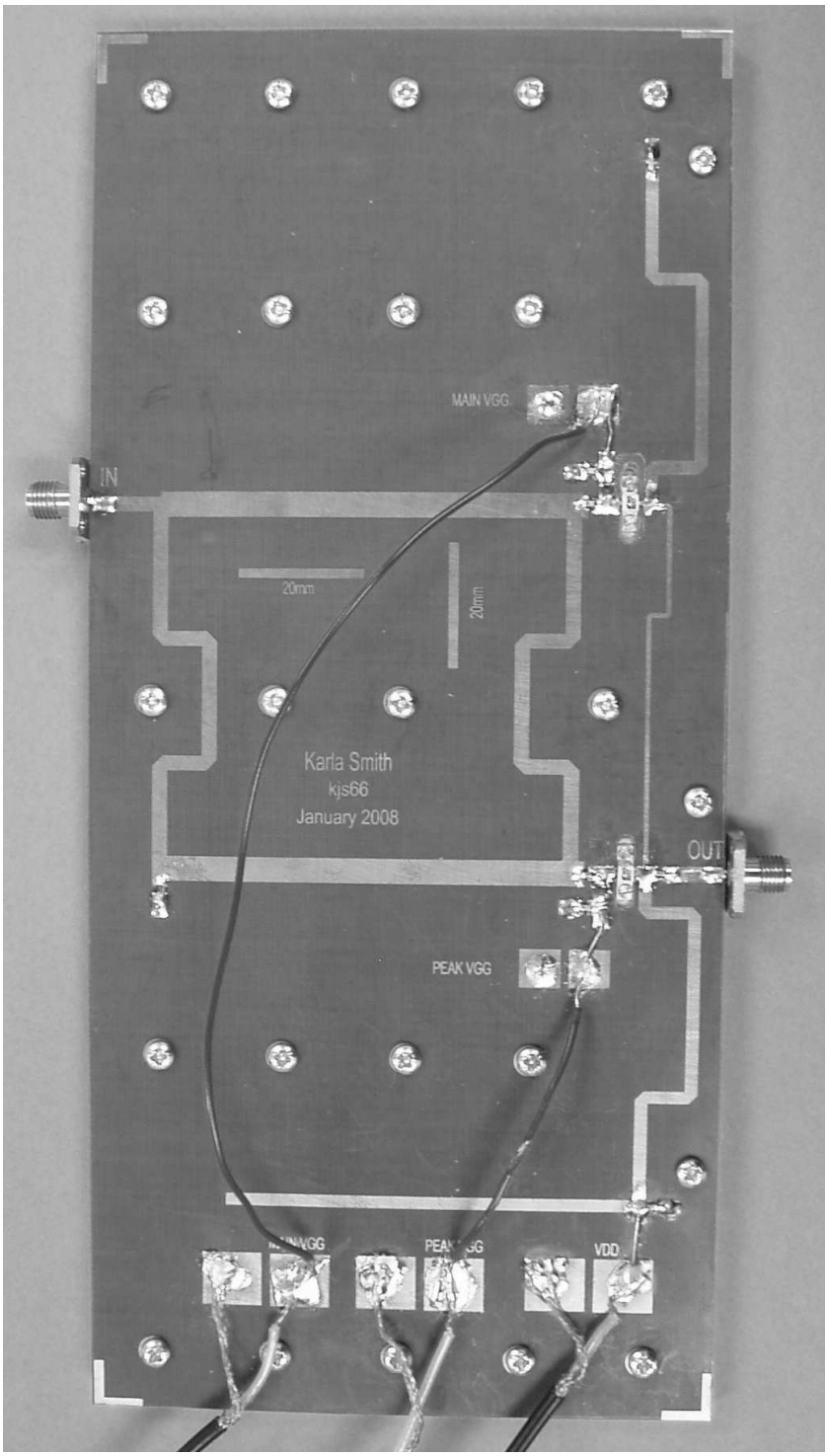


Figure 5.21: Photo of the prototype Doherty amplifier

and confirm that the centre frequency of the prototype amplifier is at 800 MHz. More importantly, the graph shows that the bandwidth of the amplifier is approximately 100 MHz, indicating it is not narrow-band.

The amplifier's performance was measured at its centre frequency of 800 MHz

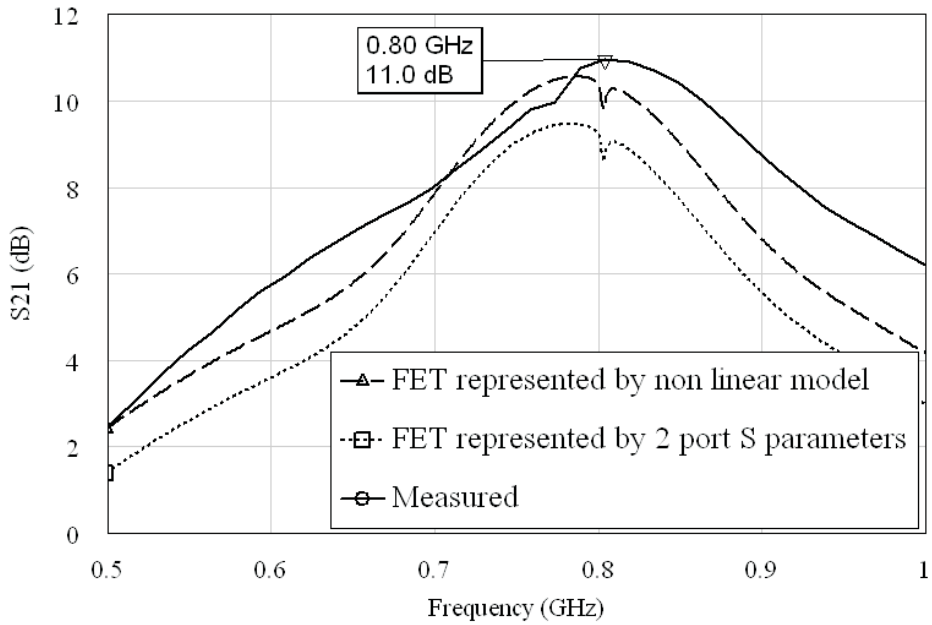


Figure 5.22: S_{21} of the prototype amplifier for gate bias control

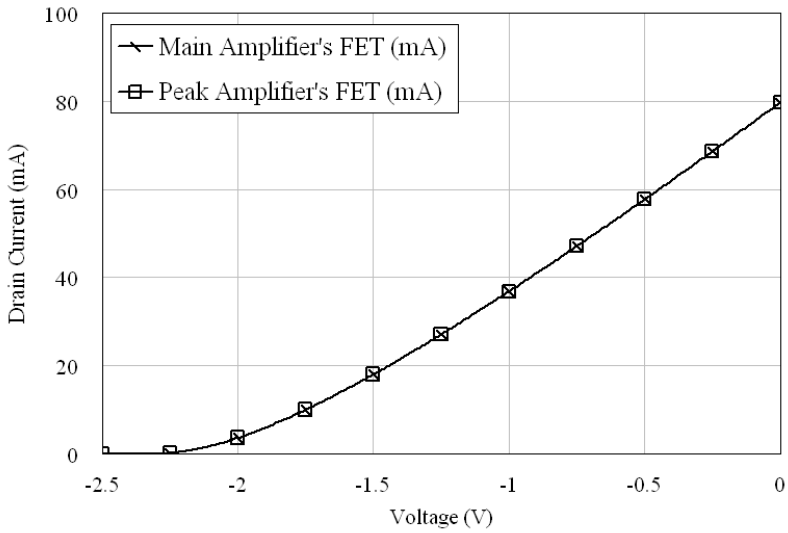


Figure 5.23: Gate-voltage to drain-current transfer characteristics of the FETs used in the prototype amplifier

with a CW signal, and a supply voltage (V_{DD}) of 4.3 V. It was compared to the same amplifier with a fixed class B bias on both FETs ($V_{B,M} = V_{B,P} = -2\ V$), as this results in a class B amplifier with the same maximum output power. Figures 5.25 and 5.26 show the measured efficiencies (DC-to-RF and PAE respectively), compared with the simulated efficiencies. The measured DC-to-RF efficiency is over 34% from 8 - 14 dBm input power.

The gain and output power are shown in Figure 5.27. It can be seen that with the

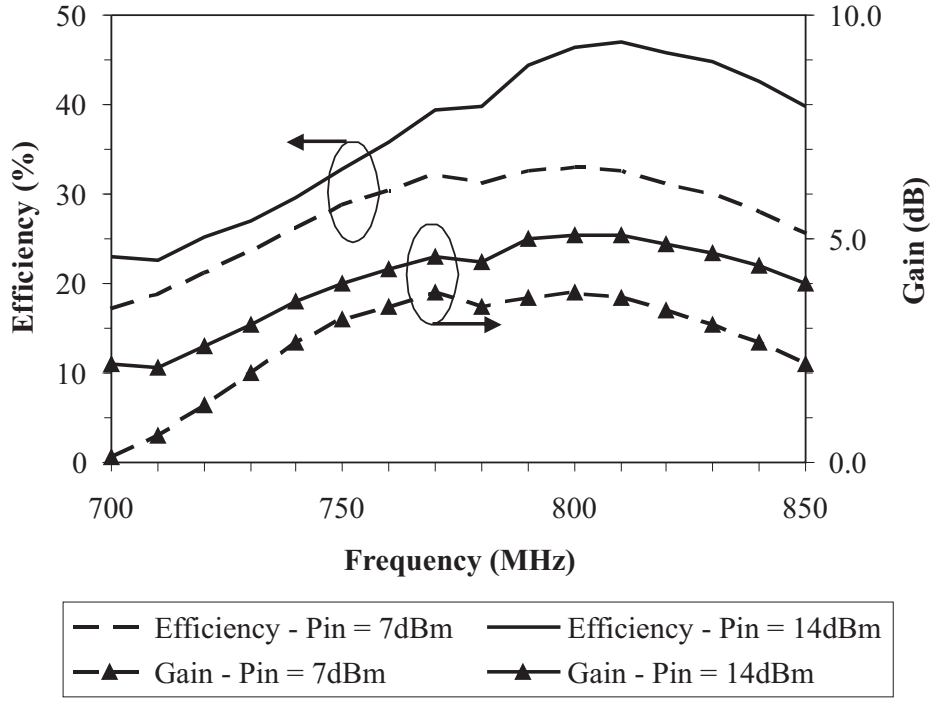


Figure 5.24: Measured Doherty amplifier bandwidth

gate bias control scheme, the amplifier has good linearity (as indicated by the constant gain with respect to input power), and is highly efficient. The output characteristics shown in these graphs have the qualities most desired in a Doherty amplifier (as predicted by theory) - a region of high efficiency, and a constant gain with respect to input power.

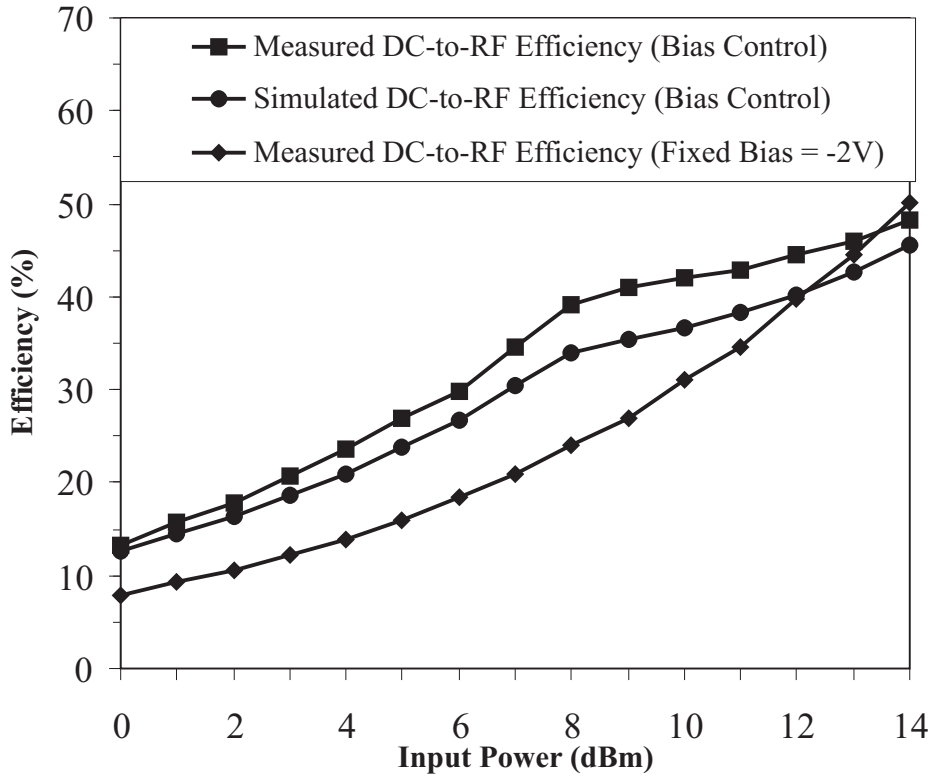


Figure 5.25: Measured Doherty amplifier DC-to-RF efficiency at the centre frequency

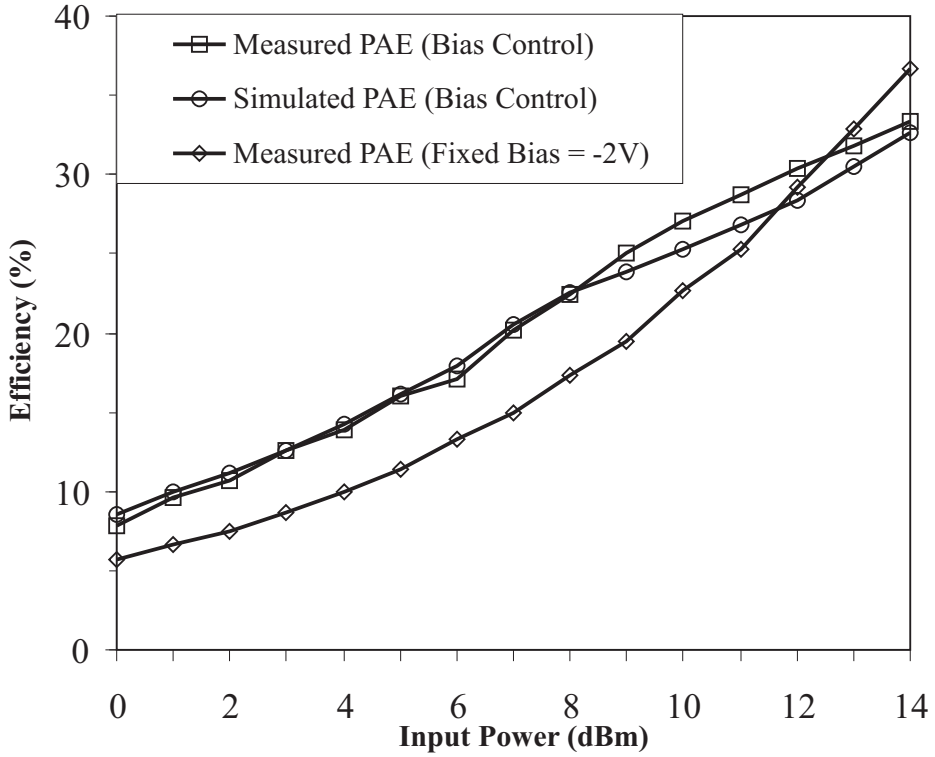


Figure 5.26: Measured Doherty amplifier power added efficiency at the centre frequency

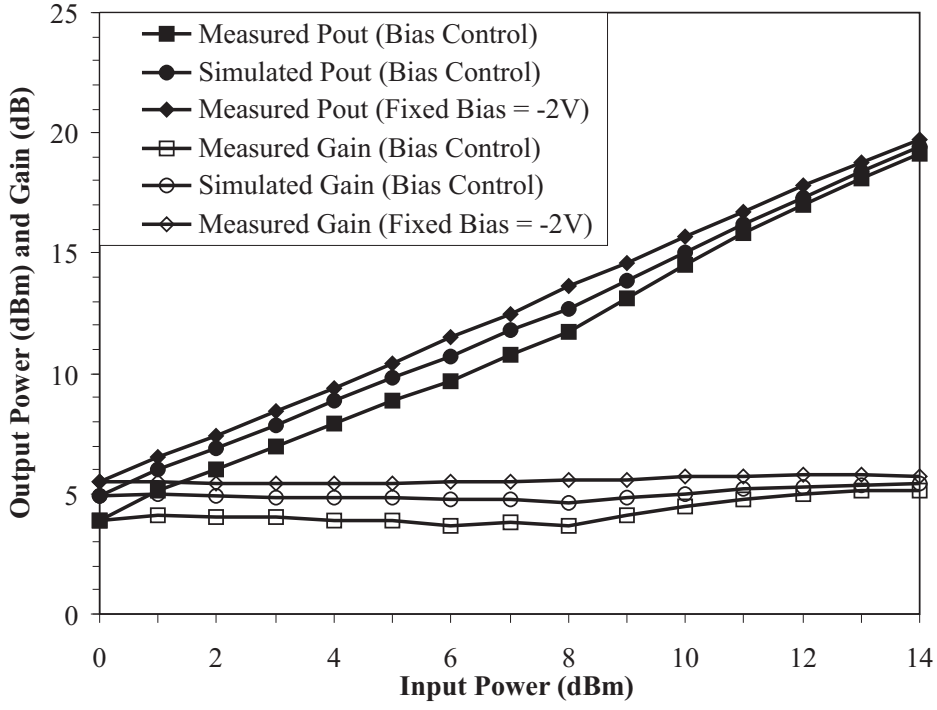


Figure 5.27: Measured Doherty amplifier output power and gain at the centre frequency

5.5 CONCLUSION

In conclusion, Doherty operation can be synthesised with a dynamic gate bias control scheme, based upon the measured drain current characteristics of the main and peaking transistors. Circuit simplicity is maintained by the use of two equal-sized (but not necessarily identical) transistors, and feeding the main and peaking amplifiers equal input power. This scheme can be applied to non-ideal transistors, and will still ensure Doherty operation in all cases. The method is sufficiently generic, allowing it to be applied to different transistor sizes (size being the maximum output current) and technologies, as it only requires the transistor to be modelled as a dependant current source. A Statz drain current model [15] was used in this work, but other models could be used.

The problems of both soft turn-on and unequal maximum drain currents were simulated using an ideal circuit, and the proposed bias control strategy was able to compensate for the performance issues that are present when these non-idealities occur in a Doherty amplifier. The same strategy was then implemented in a practical circuit, and theory, simulation and practical results all matched well in the prototype amplifier. The Doherty output characteristic of high efficiency over a range of input powers was achieved, as the prototype amplifier's DC-to-RF efficiency remained over 34% for the last 6 dB of input power (i.e. from 8 - 14 dBm). Associated with high efficiency was nearly constant gain of the amplifier with respect to input power (between 4 and 5 dB). Higher gain and output power could be obtained by using larger transistors.

Chapter 6

HARMONIC LOAD MODULATION

6.1 INTRODUCTION

In a classical Doherty amplifier implementation the main amplifier is usually biased in class B, and the peaking amplifier in class C; hence, inside the main amplifier even harmonics will be present, and inside the peaking amplifier both even and odd harmonics will be present. Unwanted harmonics are usually shunted to ground internally, and only the fundamental component is present at the amplifiers' outputs. The even harmonics of both amplifiers are easily shunted to ground via a quarter-wave transformer connecting the transistors' drains to their DC supplies, or via a resonant circuit. The former approach is usually preferred, and the peaking amplifier's third order harmonics are shunted to ground via a harmonic trap at the peaking amplifier's output, while the other odd harmonics are often ignored due to their relatively small amplitudes. However, the structure of the Doherty amplifier permits other possibilities for harmonic suppression within the wider circuit.

In this chapter, a structure is proposed that neatly and elegantly shunts the harmonics generated by both the main and peaking amplifiers to ground. This structure utilises the quarter-wave transformer linking the outputs of the two amplifiers, and the odd harmonics generated by the peaking amplifier, to decrease the amplitude of the main amplifier's drain voltage waveform. We call this harmonic load modulation. The main amplifier's supply voltage can be decreased without the amplifier going into saturation, and while retaining the amplitude of the fundamental component of the waveform. Essentially, the main amplifier is operated in class F [55], rather than class B, with the necessary harmonics being supplied by the peaking amplifier. This results in a higher efficiency characteristic for the Doherty amplifier, with little change to the linearity.

6.2 THEORY

The proposed structure for harmonic load modulation is shown in Figure 6.1. Compared to the classical Doherty circuit (see Figure 2.7), the resonant circuits at the out-

puts of each amplifier are replaced by quarter-wave transmission lines and decoupling capacitors. This configuration for the drain supply feed has inherent even harmonic suppression. It will be shown that odd harmonic suppression will also occur. Both amplifiers are operated with a fixed gate bias; the main amplifier is biased in class B, and the peaking amplifier in class C.

As discussed in Chapter 2, for the peaking amplifier to have the desired fundamental output current characteristic, some form of compensation is needed (as a class C bias results in a lower-than-desired output current). For this research, unequal transistor sizes have been used (size being the maximum output current), but unequal input power would also work. It should be noted that the gate bias control strategy proposed in Chapter 5 (using equal transistor sizes) cannot be used with harmonic load modulation, as the odd harmonics generated by the class C peaking amplifier are required. With equal transistor sizes, the gate bias control strategy changes the peaking amplifier's bias from class C up to class B. As such, at maximum input power, no odd harmonics are generated. However, the gate bias control strategy could be used in conjunction with unequal transistor sizes or unequal input power, if near-ideal output current characteristics are not achieved. This has not been done in this work.

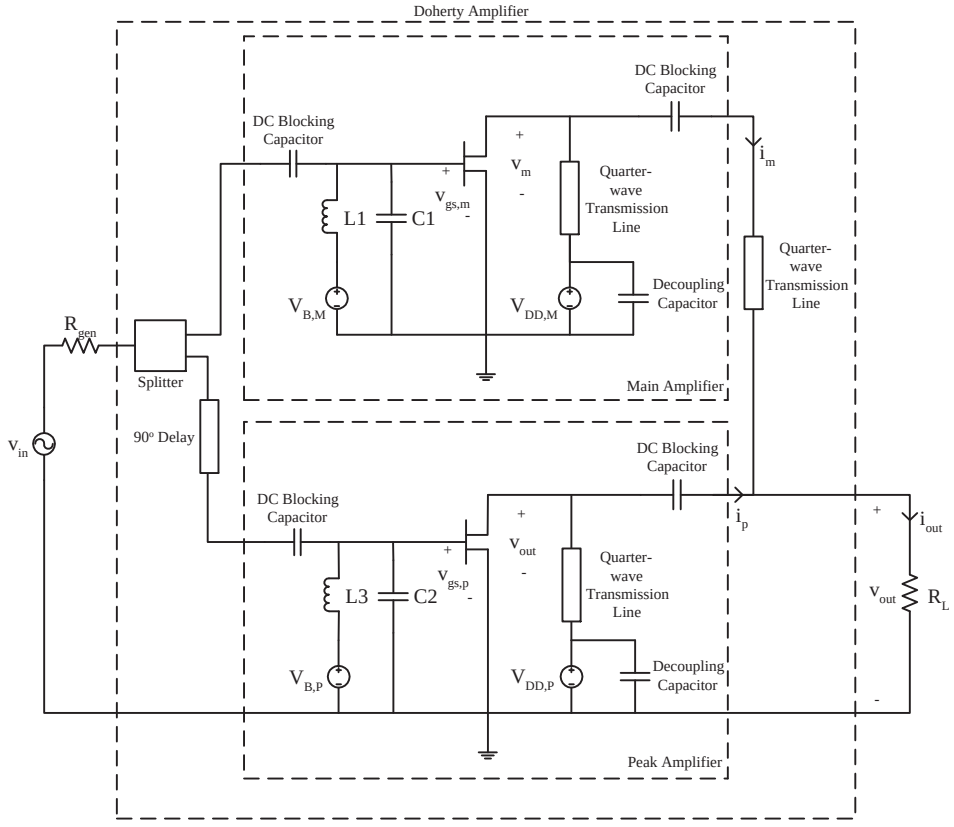


Figure 6.1: Doherty amplifier circuit diagram for harmonic load modulation

During the low power regime, the peaking amplifier is off, so no odd harmonics are generated. The harmonic load modulation circuit behaves the same as a standard Doherty circuit - the main amplifier sees a constant load of $2R_{L,B}$, and its output power and efficiency increase linearly until $V_{in,max}/2$. During the high power regime, the peaking amplifier turns on, and starts to generate both even and odd harmonics, as well as the fundamental. The fundamental is fed directly to the load, and causes load modulation for the main amplifier, in the conventional manner. The even harmonics are shunted to ground via the quarter-wave transmission line at the peaking amplifier's output. The odd harmonics generated by the peaking amplifier are shunted to ground via the quarter-wave transmission line at the main amplifier's output, meaning the load only sees the fundamental component of the waveform. The odd harmonic voltage standing waveforms along the quarter-wave transformer linking the two amplifiers are maximum at the drain of the main amplifier, meaning the main amplifier is load modulated at both the fundamental and the odd harmonics. These odd harmonics shape the drain voltage waveform of the main amplifier so it resembles a clipped sinusoidal wave (see Figure 6.2).

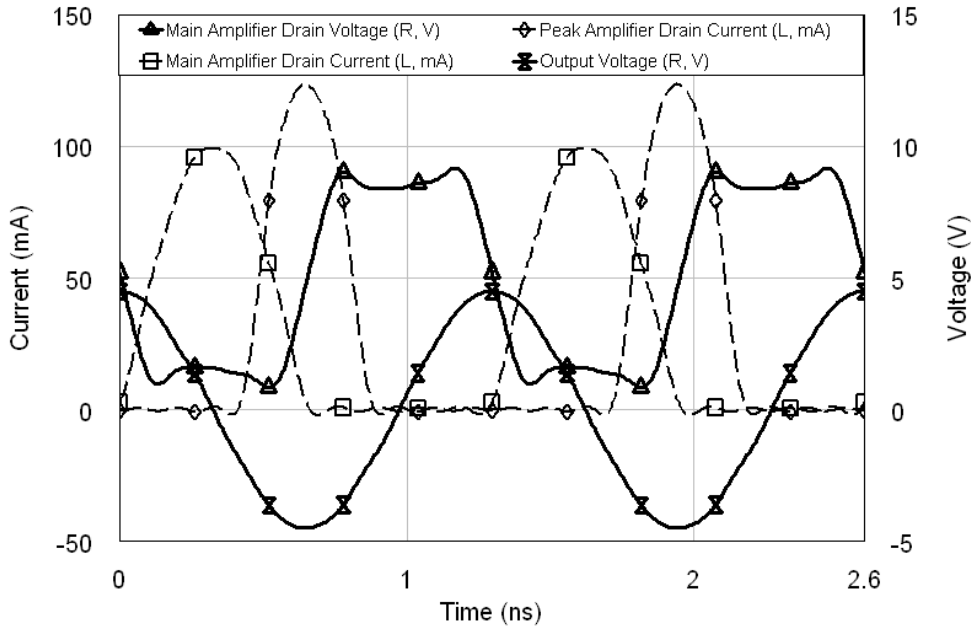


Figure 6.2: Simulated harmonic load modulation waveforms

The load lines generated by a standard Doherty amplifier and a harmonic load modulated Doherty amplifier are given in Figures 6.3 to 6.5. To generate these graphs (and Figure 6.2), harmonic balance simulations were conducted using AWR Microwave Office [7], as described in Appendix A. Ideal components were used in all cases, except for the transistors. These had a knee voltage of 1 V ($\alpha = 2$), but were otherwise ideal, with $b = 1000$, $\beta_m = 50$, $\beta_p = 127.5$, and $V_T = -2\ V$ (giving $I_{DSS,m} = 100\ mA$ and $I_{DSS,p} = 255\ mA$). Two classical Doherty loadlines are shown on each figure - one with

a standard main amplifier supply voltage, and one with the same main amplifier supply voltage as the harmonic load modulation circuit. The supply voltage for the peaking amplifiers, and the main amplifier in the standard Doherty amplifier was 5.5 V, while the supply voltage for the main amplifier in the harmonic load modulated amplifier, and the standard Doherty with a lower supply was 5 V. Figure 6.3 shows an example of the loadlines in the low power regime ($V_{in} < V_{in,max}/2$), Figure 6.4 shows the loadlines at half of maximum input voltage ($V_{in} = V_{in,max}/2$), and Figure 6.5 shows them at maximum input voltage ($V_{in} = V_{in,max}$).

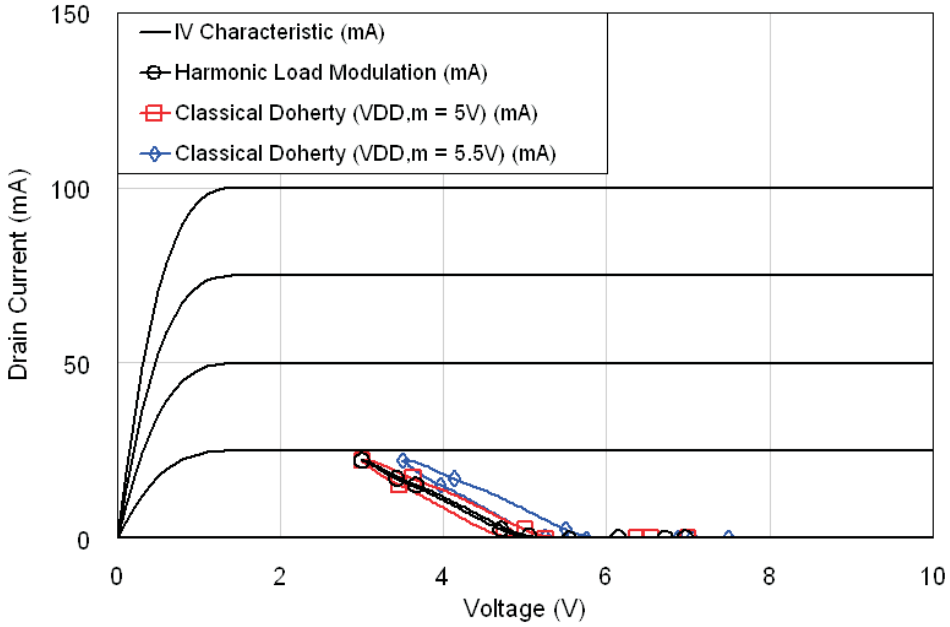


Figure 6.3: An example of main amplifier loadlines in the low power regime

It can be seen that during the low power regime the main amplifiers load is the same for each case, and as the power is increased to half of maximum input voltage, the load stays constant. At half of maximum input power the triode region is barely entered for both the harmonic load modulated Doherty amplifier and for the standard Doherty amplifier with a lower main amplifier supply. Due to the fact that this is not a hard boundary, this small entry into the triode region is not a significant problem. During the high power regime the harmonic load modulation of the main amplifier starts to take effect, and the loadline for the harmonic load modulated amplifier bends, forming an L-shape, avoiding the triode region. By comparison, the standard Doherty amplifier with the same main amplifier supply voltage as the harmonic load modulated amplifier has entered the triode region again, and has started to saturate.

The efficiency, output power and gain of the same three amplifiers are shown in Figures 6.6 and 6.7 respectively. It can be seen that the efficiency of the harmonic load modulated Doherty amplifier is higher than the other two amplifiers. Lowering the

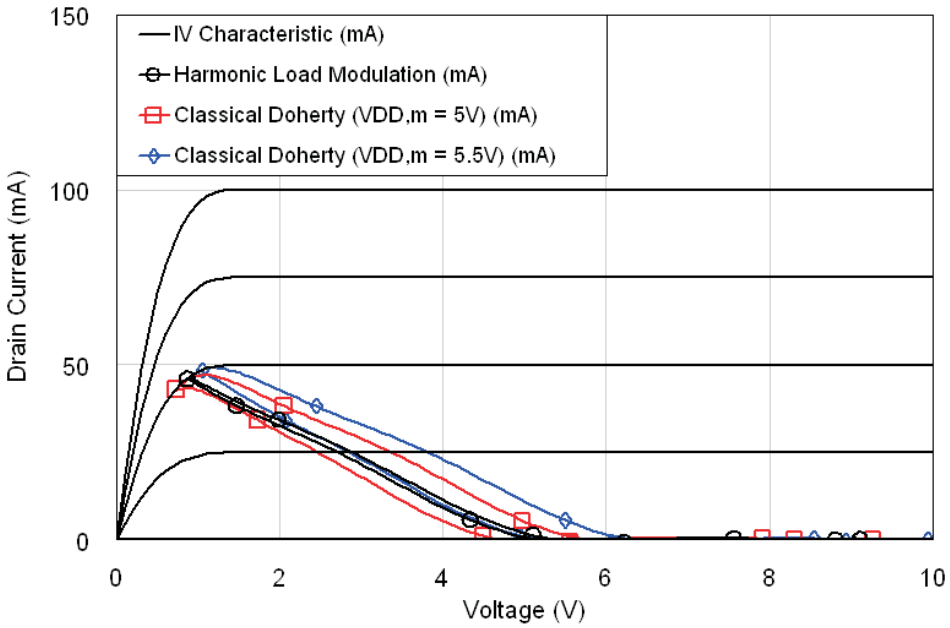


Figure 6.4: Main amplifier loadlines at half of maximum input voltage

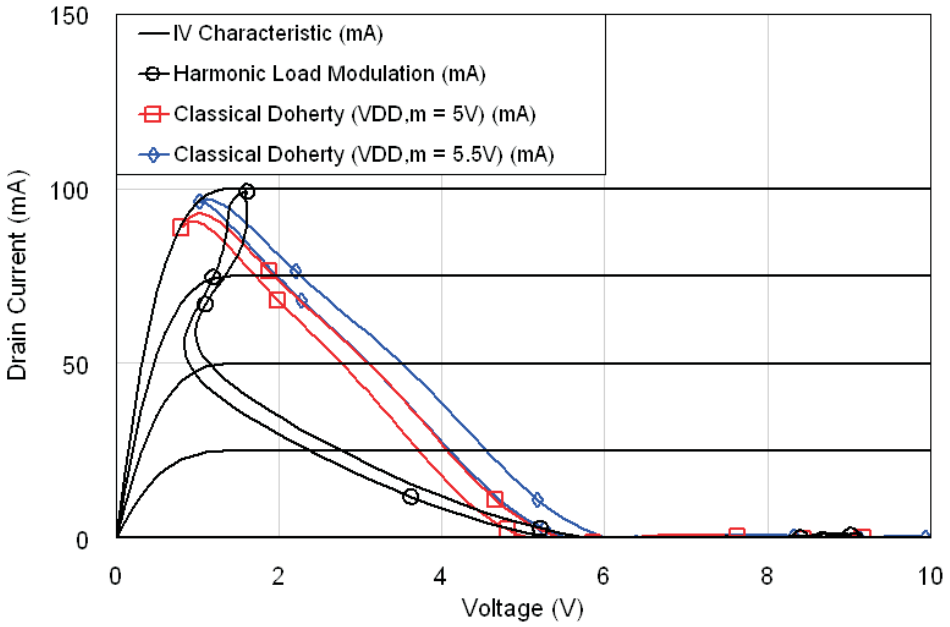


Figure 6.5: Main amplifier loadlines at maximum input voltage

supply of the main amplifier in the standard Doherty amplifier has increased its efficiency in the low power regime, but it decreases back to the standard curve in the high power regime. This is explained by the output power and gain characteristics, which show that the harmonic load modulated amplifier has almost maintained a constant gain with respect to input power when compared to a standard Doherty amplifier. By contrast, the standard Doherty amplifier with a lower main amplifier supply voltage

has a decrease in gain in the high power regime. This is because saturation is occurring when the amplifier's loadline enters the triode region. The gain of the harmonic load modulated Doherty amplifier does have a small dip in it at half of maximum input voltage ($P_{in,max} - 6\ dB$), which corresponds to the point at which it enters the triode region (see Figure 6.4), but it is a minimal decrease.

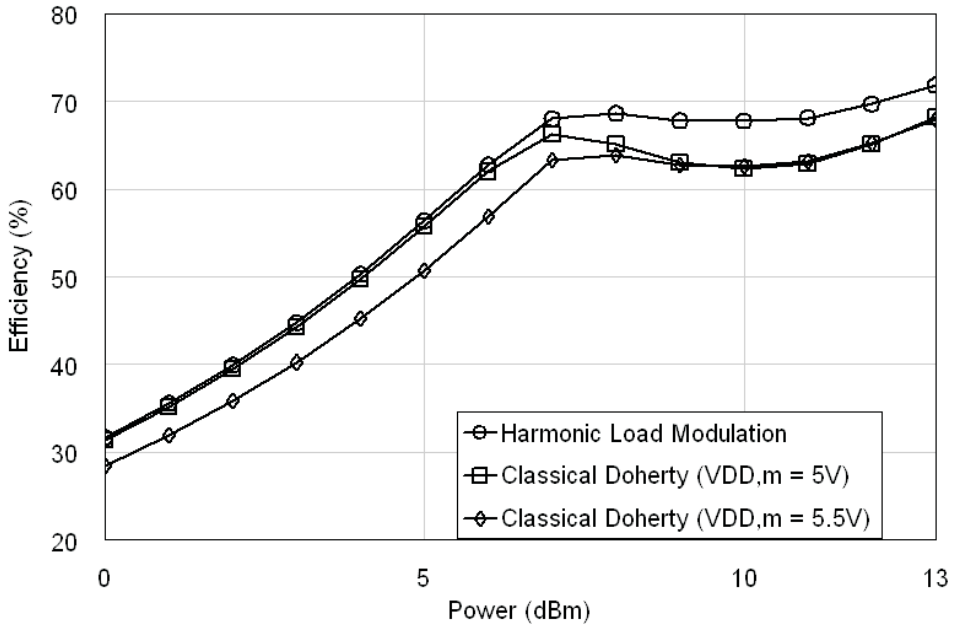


Figure 6.6: Efficiency of an ideal harmonic load modulated amplifier

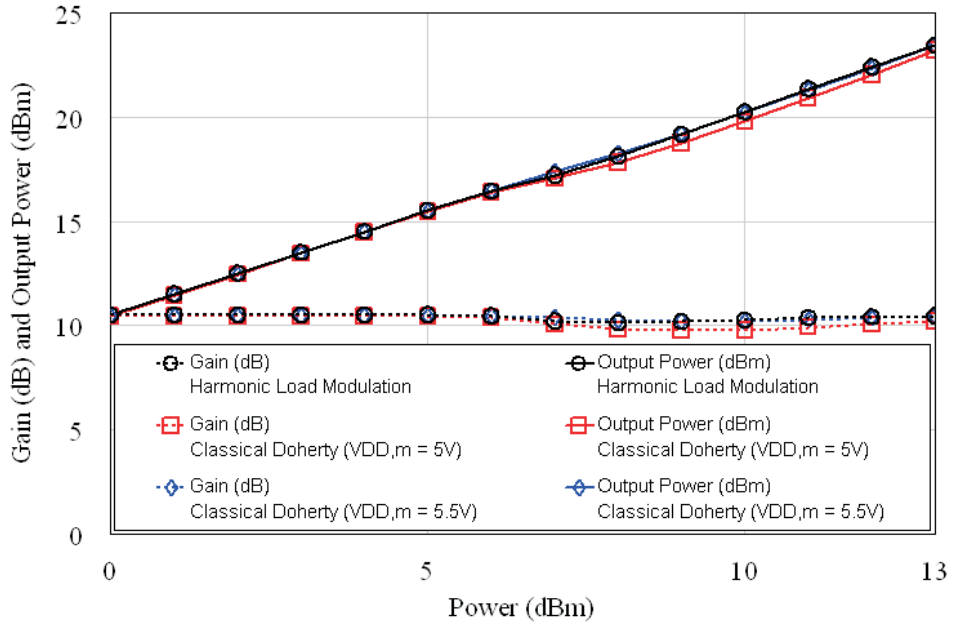


Figure 6.7: Output power and gain of an ideal harmonic load modulated amplifier

6.3 IMPLEMENTATION

To test the circuit layout described in Section 6.2, a 770 MHz harmonic load modulation amplifier was designed, employing a Eudyna FLK017WF for the main amplifier, and a Eudyna FLC057WG for the peaking amplifier. These two FETs both have a threshold voltage, V_T, of -2 V, and a drain knee voltage, V_k, of 1 V. The FLK017WF has a maximum saturation drain current of 60 mA, while the FLC057WG has a maximum saturation drain current of 200 mA (see Figure 6.8). The ratio between the two transistors is 1:3.3, which is higher than the ideal ratio of 1:2.55 (see Section B.3.7). However, the FLC057WG is the FET closest to the desired size which is in the same range of devices as the FLK017WF (which was chosen for the reasons outlined in Section 1.6). As shown in Section 4.4, this means the amplifier's output power and gain are likely to be less linear than a Doherty amplifier with the correct device size ratio.

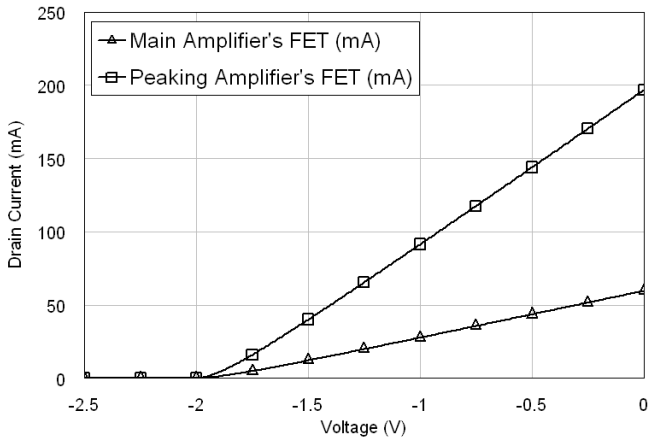


Figure 6.8: Gate-voltage to drain-current transfer functions of the FETs used in the harmonic load modulation amplifier

Harmonic balance simulations of a this amplifier were conducted using AWR Microwave Office [7], as described in Appendix A. The FETs were represented by a nonlinear model based upon the Statz drain current and capacitance model [15], which includes chip and package parasitic effects (see Appendix C). A load resistance of 50 Ω was used (rather than a higher, more-optimal load), as this meant the load presented to the transistors is significantly smaller than R_{ds}. Without impedance transformers, the uncertainty of R_{ds} for class B and class C operations is diminished (see Appendix C). A basic circuit diagram is shown in Figure 6.9, while the complete one is given in Appendix D.

As discussed in section 2.4.1, the main amplifier is biased in class B at $V_{B,M} = V_T = -2\ V$ and the peaking amplifier is biased in class C at $V_{B,P} = 1.5V_T = -3\ V$. The DC supply for the main amplifier is 3.5 V, while the peaking amplifier is supplied 4.5 V. Figure 6.10 shows the waveforms for the amplifier. It can be seen that the output

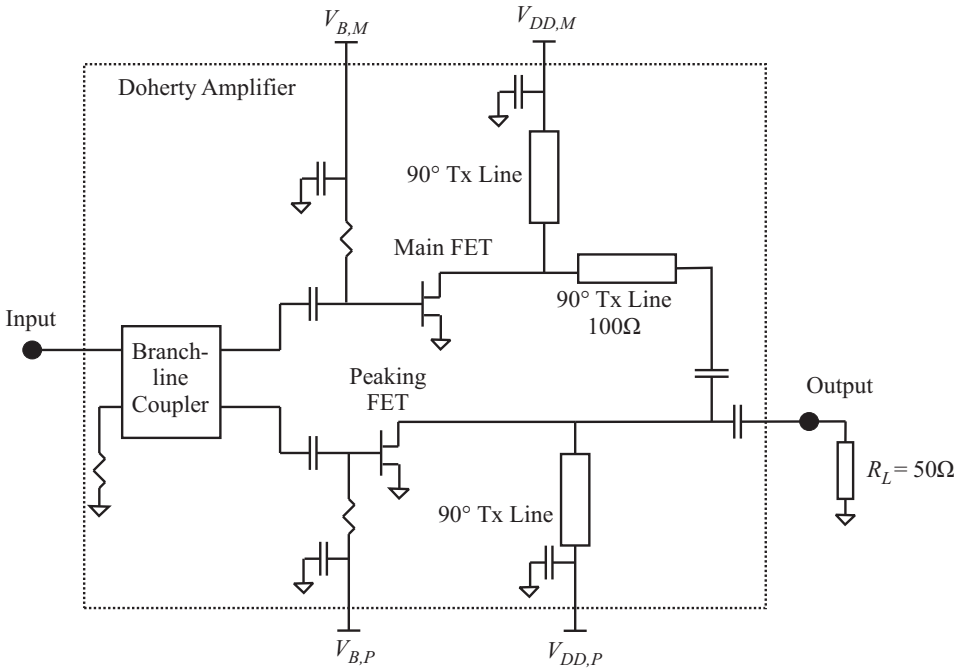


Figure 6.9: Harmonic load modulation amplifier circuit diagram

voltage waveform is still sinusoidal, while the main amplifier's drain voltage waveform resembles a clipped sine wave.

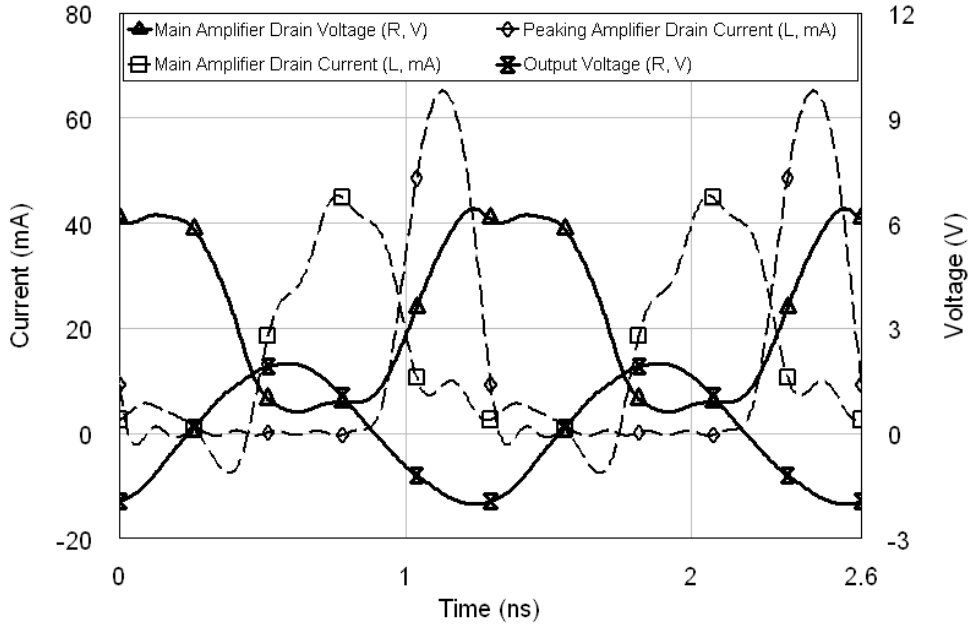


Figure 6.10: Simulated waveforms of a practical harmonic load modulation circuit

The correct operation of the harmonic load modulation amplifier was confirmed by the main amplifier's loadline, as shown in Figure 6.11. The L-shape of the loadline is not as pronounced as when an ideal circuit and ideal transistors are used (see Figure

6.5), but it is still clearly curved and avoids the triode region. For comparison, a standard Doherty amplifier was also simulated, using the same transistors; in one case both amplifiers are supplied the same voltage as the peaking amplifier in the harmonic load modulation amplifier (4.5 V), and in the other the main amplifier is supplied the same voltage as the main amplifier in the harmonic load modulation amplifier (3.5 V). As expected, the loadlines of these amplifiers are not curved.

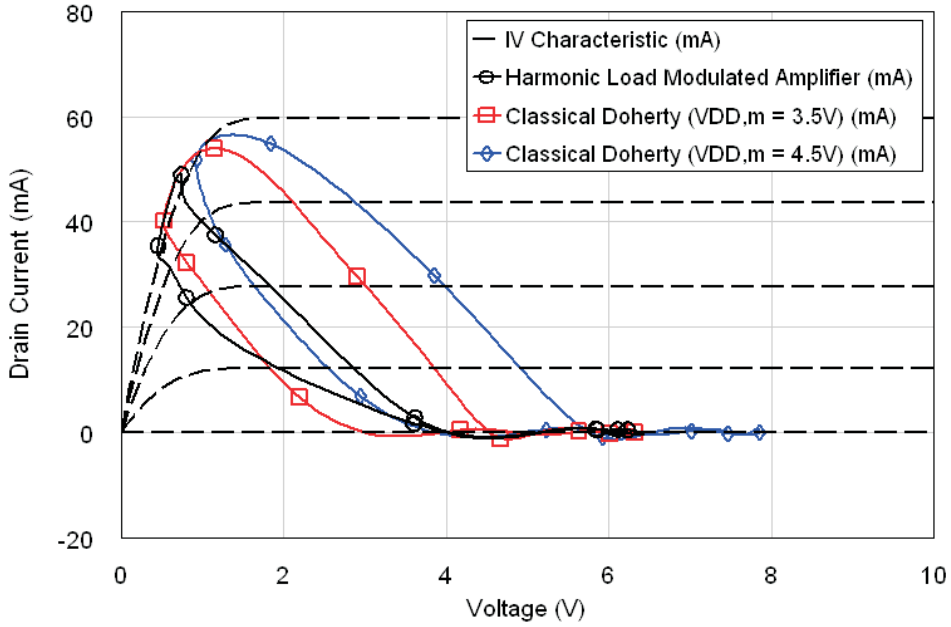


Figure 6.11: Simulated loadline for a practical harmonic load modulation amplifier

Figure 6.12 shows the harmonics in the output power (at maximum input power) of both the harmonic load modulation amplifier and the conventional Doherty amplifier ($V_{DD,m} = 4.5$V). It can be seen that the harmonics are being suppressed via quarter-wave transformers at the amplifiers' outputs, and that the fundamental component of the output power is the same in both cases, with very low levels of unwanted harmonics.

The output characteristics of the amplifier were simulated, and compared to the same conventional Doherty amplifier (see Figures 6.13 and 6.14). The efficiency of the harmonic load modulation amplifier is significantly better than that of the conventional Doherty amplifier, as expected. The gain and output power of both amplifiers are very similar, confirming the harmonic load modulated amplifier is not entering saturation, despite having a lower main amplifier supply voltage.

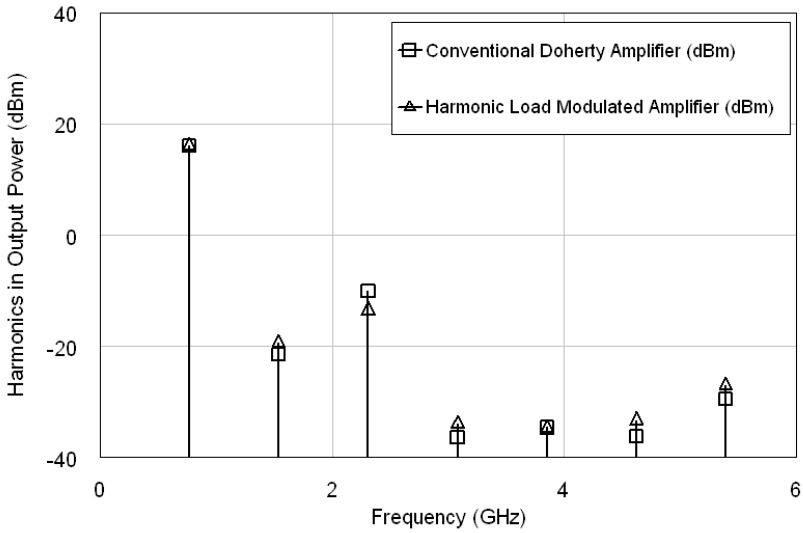


Figure 6.12: Simulated harmonic content of the output power in a practical harmonic load modulation amplifier

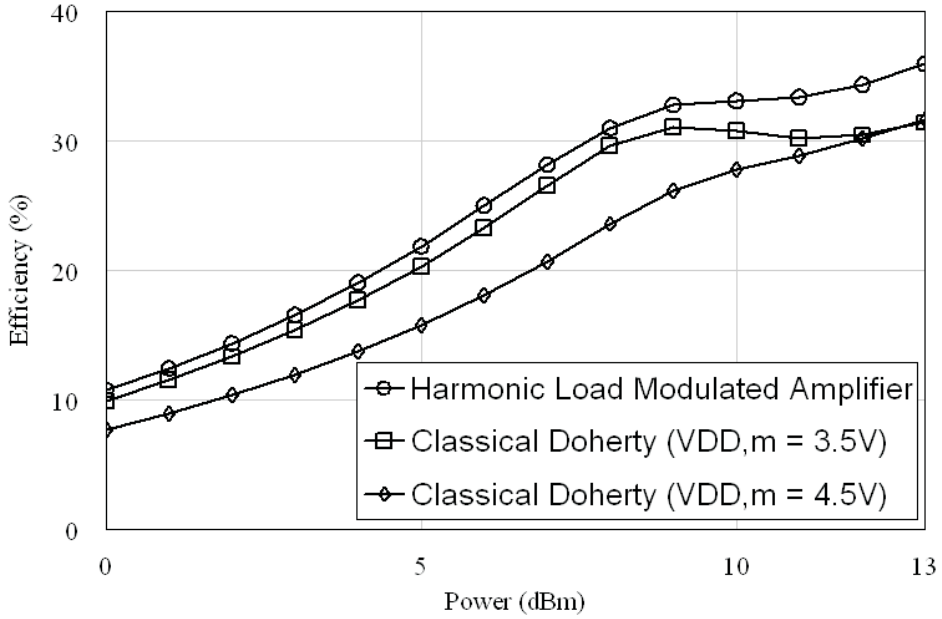


Figure 6.13: Simulated DC-to-RF efficiency of a practical harmonic load modulation circuit

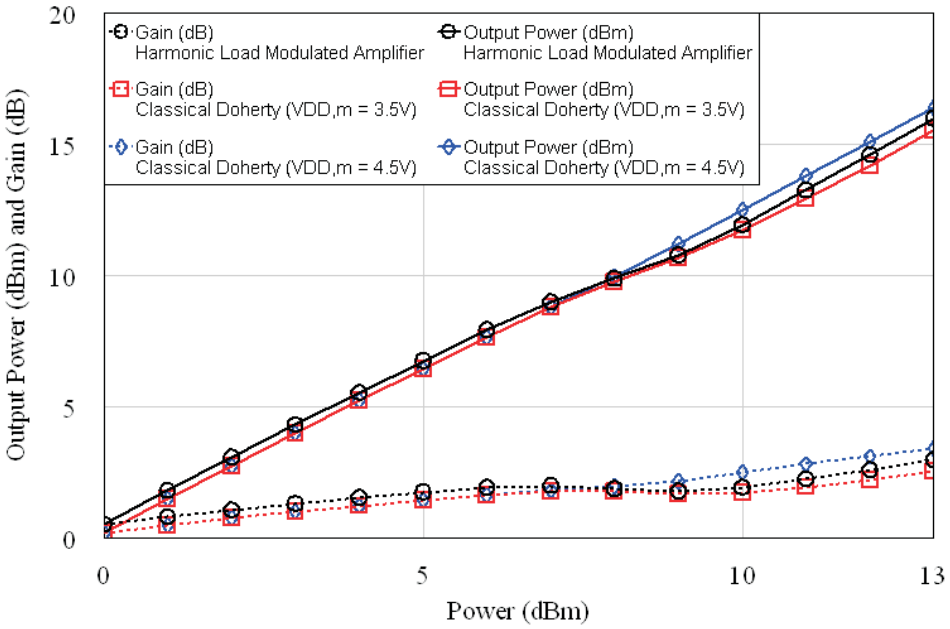


Figure 6.14: Simulated output power and gain of a practical harmonic load modulation circuit

6.4 EXPERIMENTAL RESULTS

An amplifier was built using microstrip lines and a Eudyna FLK017WF GaAs FET for the main amplifier, and a Eudyna FLC057WG FET for the peaking amplifier on a 0.7874 mm (31 mil) substrate with a dielectric constant of 2.2 (see Figure 6.15). The S-parameters of the amplifier were measured under class AB conditions ($V_{B,M} = V_{B,P} = -0.7\ V$), and compared to those generated by simulation (using two data-sheet transistors, as described in Section 6.3) to ensure that the prototype amplifier was close to the design (see Appendix E). Figure 6.16 shows S_{21} for the amplifier around the centre frequency of 770 MHz. The maximum gain under this bias condition is 13 dB, but it should be noted that the gain of a class AB amplifier is higher than that of a class B or class C amplifier (as is used in a Doherty circuit).

The DC i/v characteristics of each FET were measured, and the drain current model (5.1) was fitted to these measurements. The resulting model parameters ($\beta = 0.048$, $V_T = -2.4$, $b = 1$ for the main amplifier's FET and $\beta = 0.092$, $V_T = -2.6$, $b = 0.4$ for the peaking amplifier's FET) were subsequently used in simulations to compare with experimental results. The gate-voltage to drain-current transfer characteristics of the FETs is shown in Figure 6.17. It can be seen that parametric variation between the data-sheet information and the actual FETs used has resulted in earlier turn-on points than the data-sheet figure of -2 V, especially for the peaking amplifier's FET. Furthermore, the ratio between the maximum saturation drain currents of the two FETs is higher than predicted by data-sheet information, with $I_{DSS,m} = 82\ mA$ and $I_{DSS,p} = 305\ mA$, resulting in a ratio of 1:3.7.

The bandwidth of the amplifier was also determined, both at maximum input power, and at half of maximum input power. The results are shown in Figure 6.18, and confirm that the centre frequency of the prototype amplifier is at 770 MHz. More importantly, the graph shows that the bandwidth of the amplifier is approximately 100 MHz, indicating it is not narrow-band.

The amplifier's performance was measured at its centre frequency of 770 MHz with a CW signal, a main amplifier supply voltage ($V_{DD,m}$) of 3.5 V, and a peaking amplifier supply voltage ($V_{DD,p}$) of 4.5 V. The main amplifier was biased at -2 V, and the peaking amplifier at -3 V, as per the design, as it is intended that the harmonic load modulated amplifier need not involve measuring the FET transfer characteristics. Figure 6.19 shows the measured DC-to-RF efficiency compared with the simulated efficiencies. It should be noted that the maximum efficiencies are significantly higher than those simulated in Section 6.3. This is solely due to the differences in FET transfer characteristics between the data-sheet information and the FETs used for the prototype. The circuit design, the amplifier biases and the DC supply voltages are all the same for both sets of simulations.

It can be seen that the efficiency characteristic quickly increases at low power levels

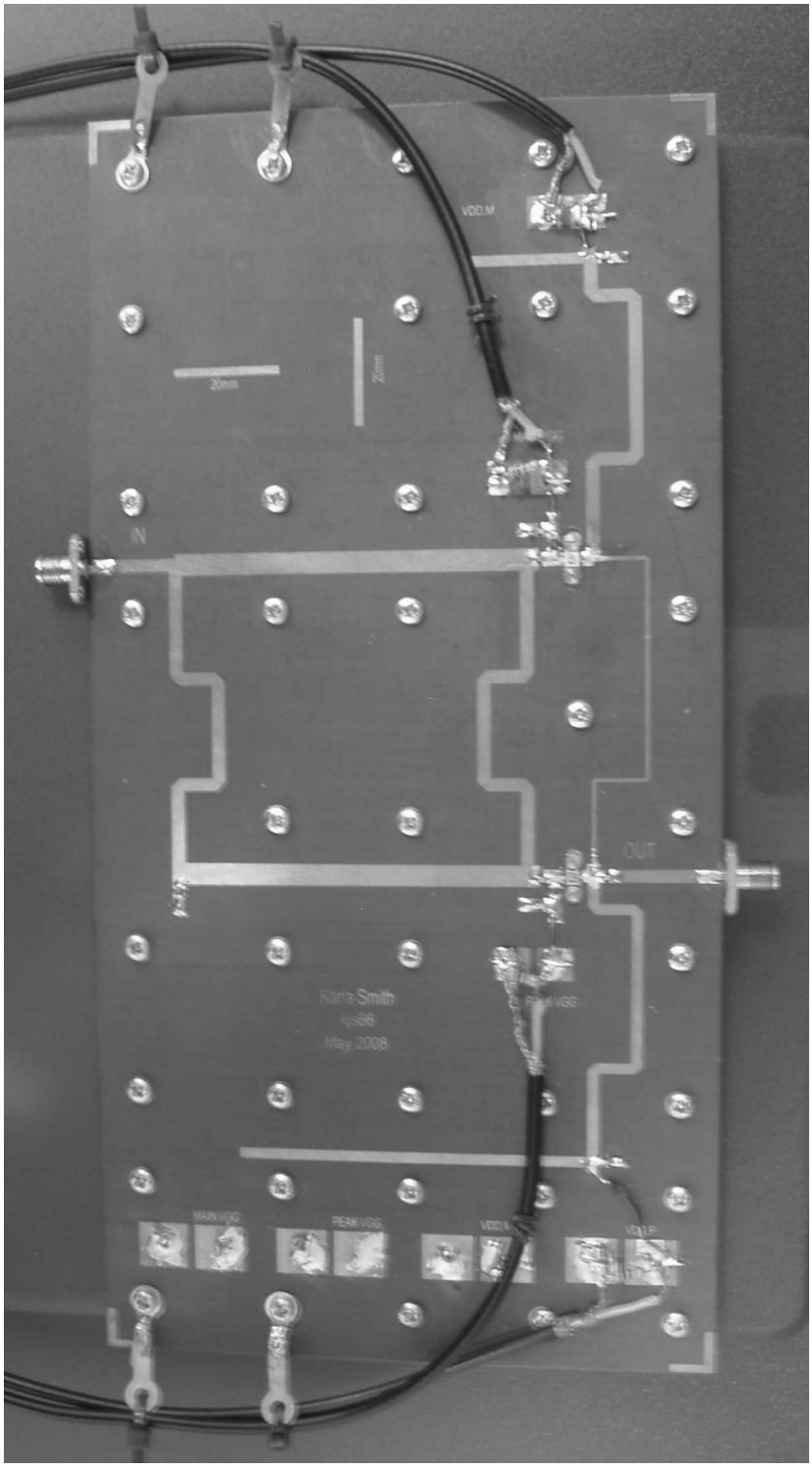


Figure 6.15: Photo of the prototype harmonic load modulation amplifier

and tries to plateau at high power levels (the efficiency characteristic for a conventional amplifier would be straighter). The simulation results are not as good as the measured results, which is caused by inaccuracies in the simulation model (described in detail in

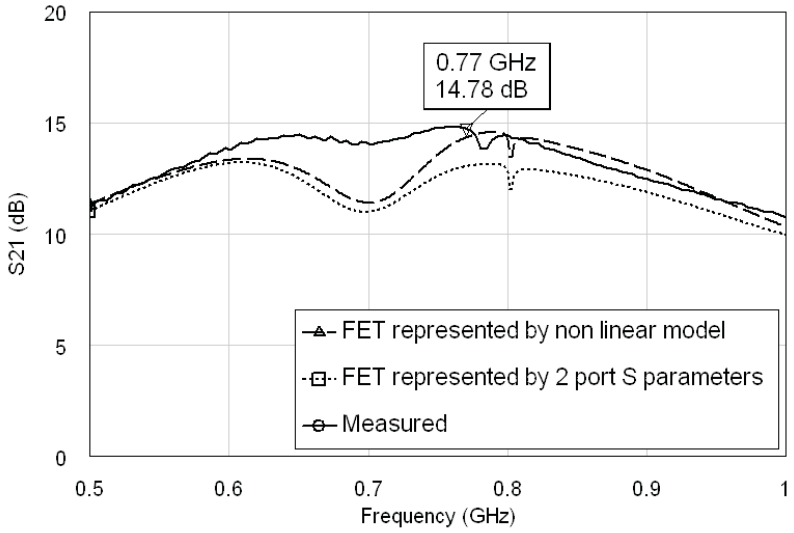


Figure 6.16: S_{21} of the prototype amplifier for harmonic load modulation

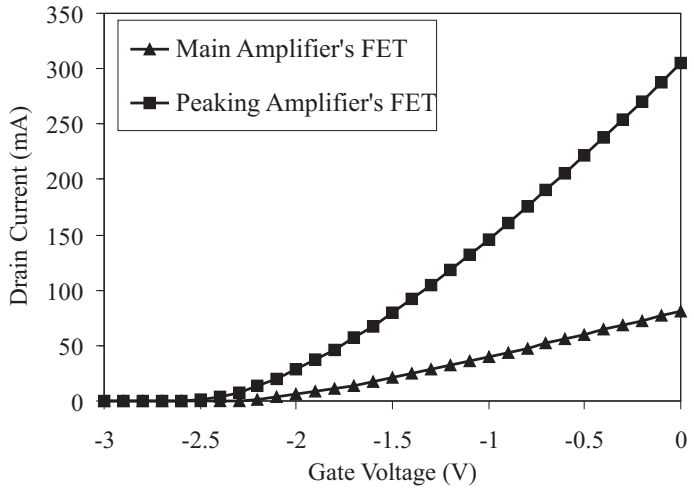


Figure 6.17: Gate-voltage to drain-current transfer characteristics of the FETs used in the prototype harmonic load modulation amplifier

Appendix C. The model used for this simulation has been fitted to the measured DC i/v characteristics. As shown in Chapter 4, the Doherty amplifier's output characteristics are sensitive to both soft turn-on and unequal maximum drain currents. Both of these are present in the prototype amplifier, and it is unsurprising that the efficiency characteristic is less-than-ideal. This is a common challenge for realising a Doherty amplifier, as discussed in Section 1.4.

The gain and output power of the prototype amplifier are shown in Figure 6.20. The amplifier has very constant gain with respect to input power (the gain is between 6.6 and 6.9 dB), indicating saturation is not occurring, despite the low main amplifier

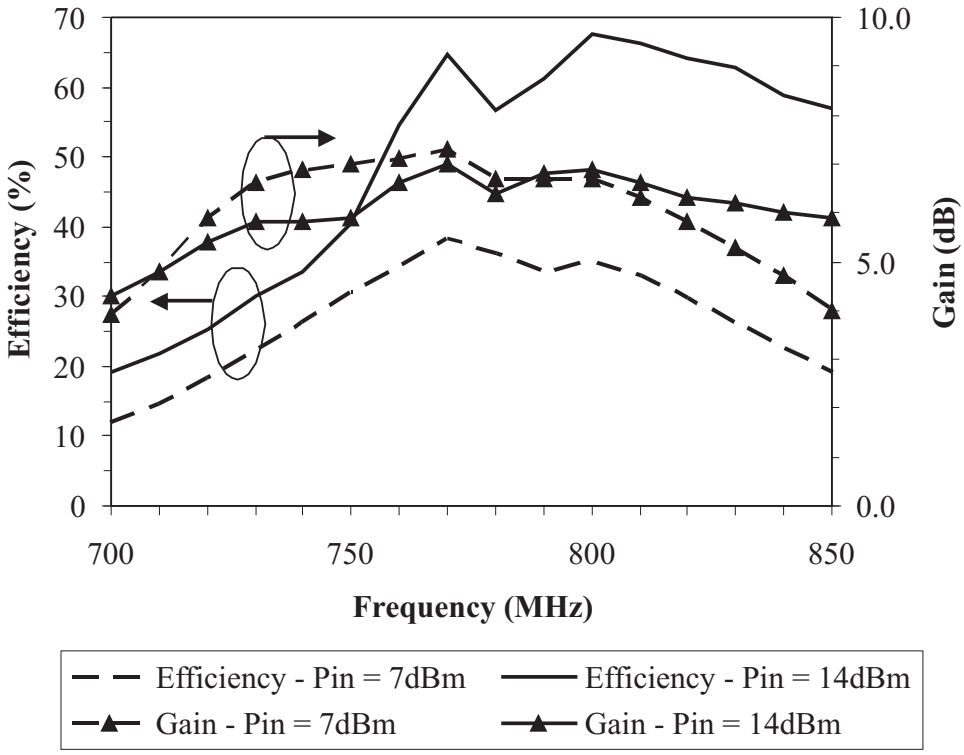


Figure 6.18: Measured harmonic load modulation amplifier bandwidth

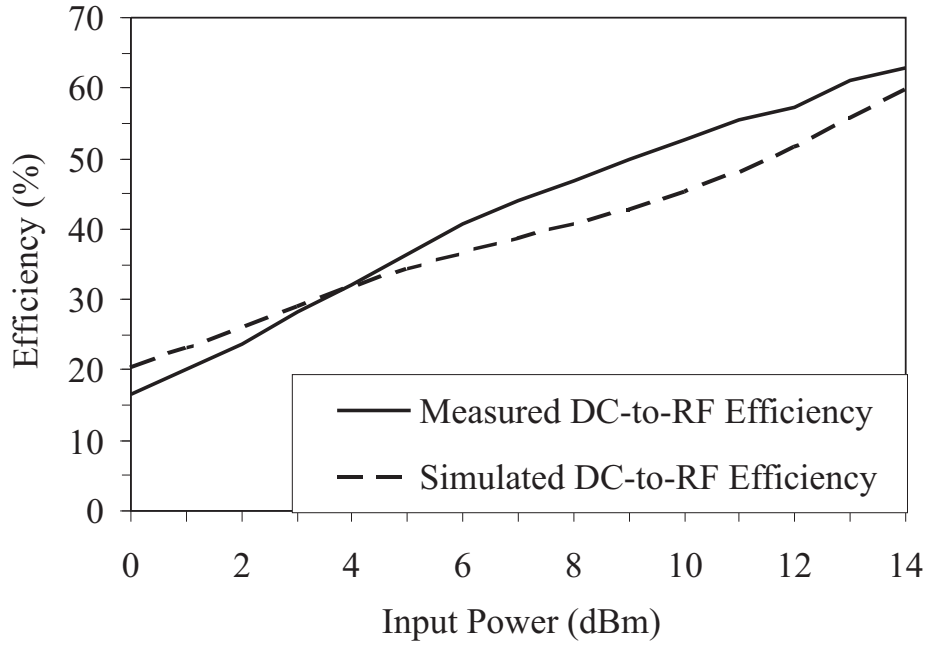


Figure 6.19: Measured harmonic load modulation amplifier DC-to-RF efficiency

supply voltage.

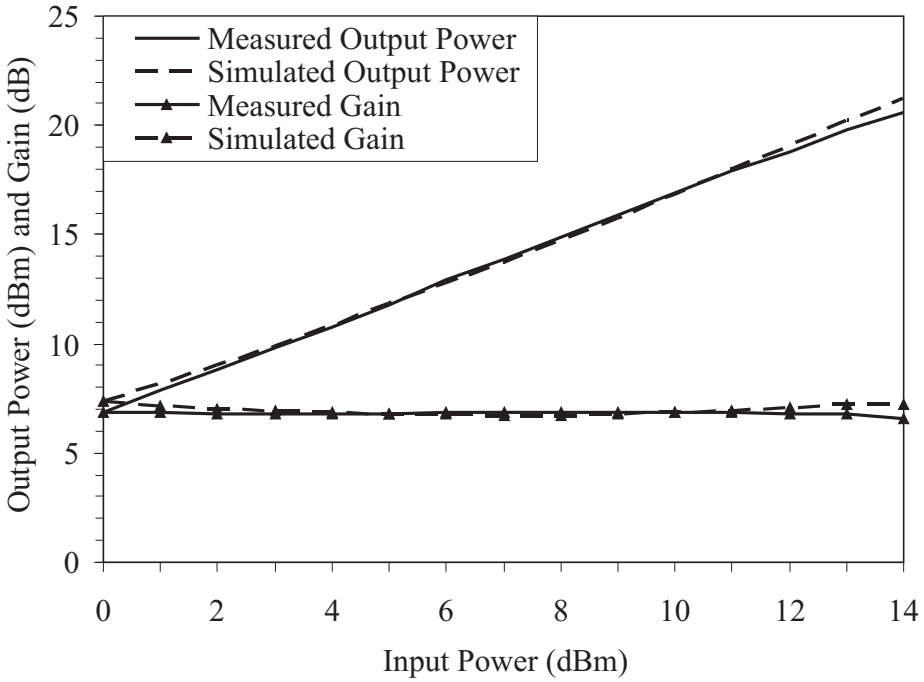


Figure 6.20: Measured harmonic load modulation amplifier output power and gain

The prototype amplifier was also measured with different values of main amplifier supply voltage - from 4.5 V down to 3 V. The efficiency results are shown in Figure 6.21, and show that the lower the main amplifier supply voltage is, the more efficient the amplifier is in the low power regime. In the high power regime, the efficiencies are very similar, regardless of the main amplifier's supply voltage.

The gain and output power of the amplifier are shown in Figures 6.22 and 6.23. It can be seen that regardless of the main amplifier's supply voltage, the gain of the amplifier is very flat, implying linear amplification. As the supply voltage decreases the gain also decreases. Hence, there is a trade-off between gain and efficiency when determining the optimum main amplifier supply voltage.

The output signal was connected to a spectrum analyser to measure the harmonics at different input power levels. The results are given in Table 6.1. It can be seen that the harmonic content of the amplifier's output power is similar for all values of the main amplifier's supply voltage. Where a dash is shown in the table, the result was below the noise floor of the spectrum analyser. The fundamental component of the output power decreases with decreasing main amplifier supply voltage, but this is consistent with the gain and output power results shown in Figures 6.22 and 6.23. The output power's 4th and higher harmonics were below the noise level of the spectrum analyser, so are not shown in the table.

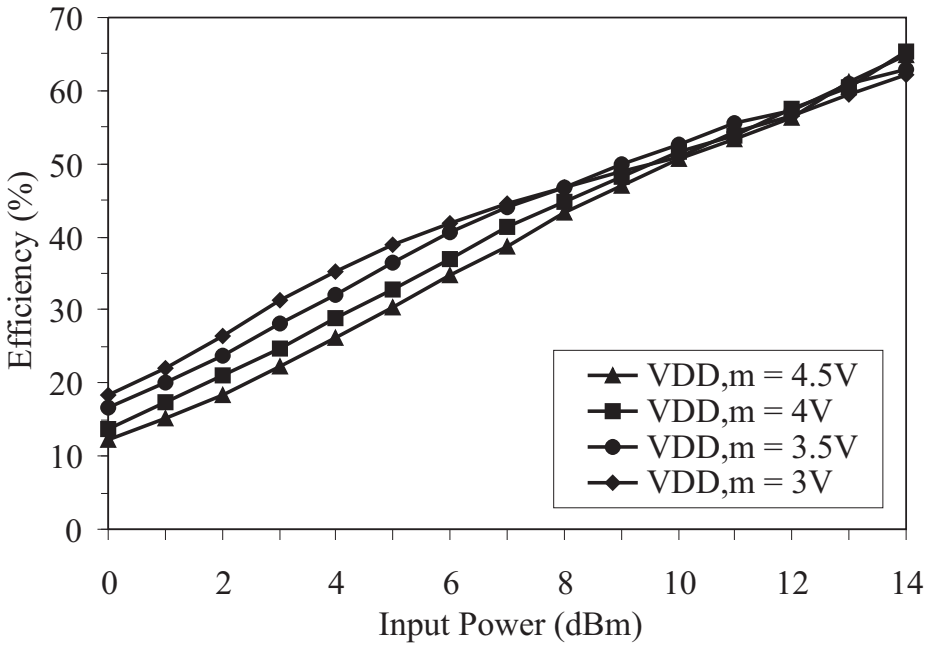


Figure 6.21: Measured harmonic load modulation amplifier DC-to-RF efficiencies with different main amplifier supply voltages

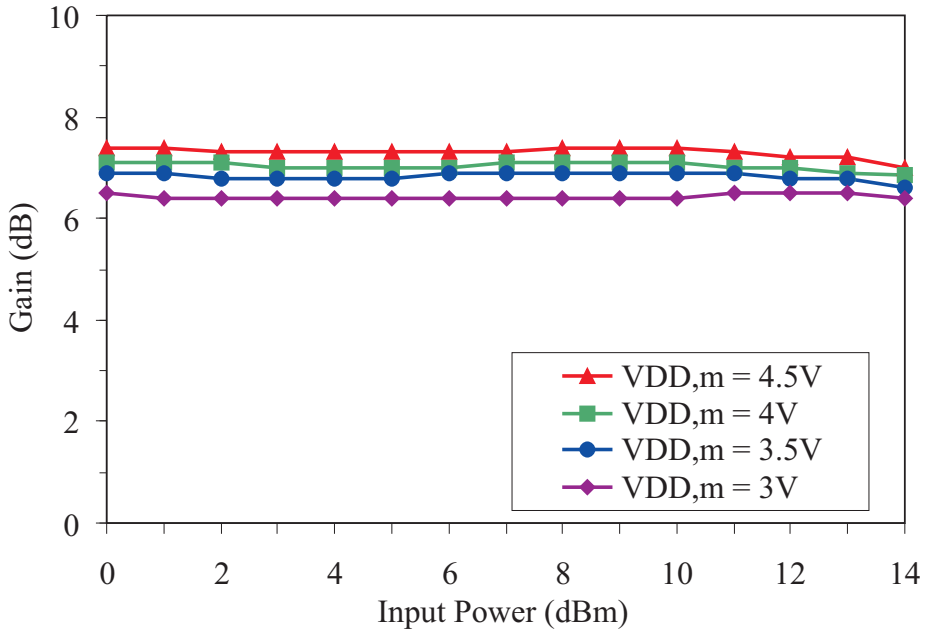


Figure 6.22: Measured harmonic load modulation amplifier gain with different main amplifier supply voltages

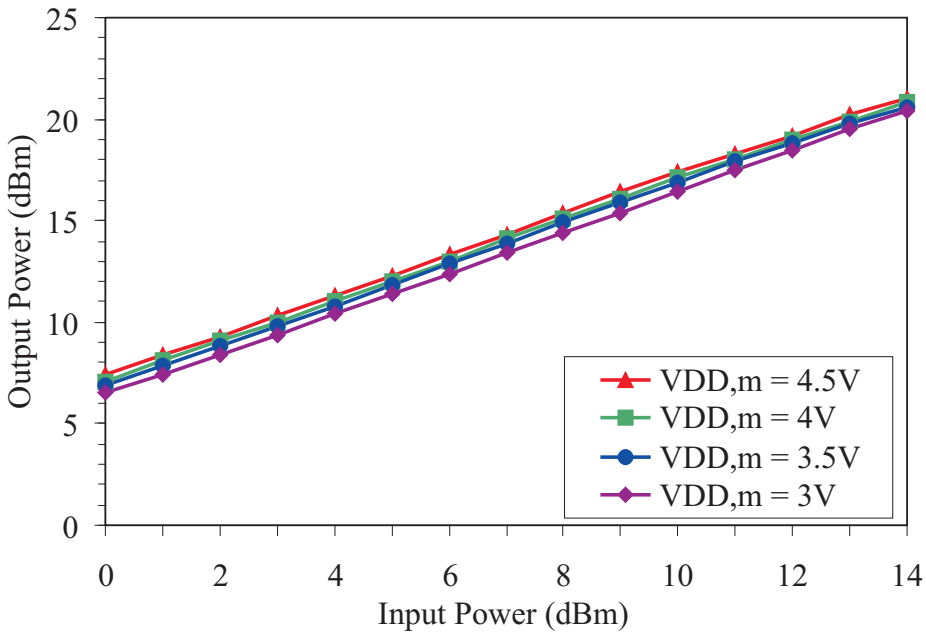


Figure 6.23: Measured harmonic load modulation amplifier output power with different main amplifier supply voltages

The results show that harmonic suppression is occurring within the amplifier. The output power increases linearly with respect to input power (see Figure 6.23), and has negligible levels of harmonics present (see Table 6.1), which indicates that the harmonic load modulation amplifier is not entering saturation as the main amplifier's supply voltage is decreased.

Input Power (dBm)	Fundamental (dBm)			
	$V_{DD,m} = 3\ V$	$V_{DD,m} = 3.5\ V$	$V_{DD,m} = 4\ V$	$V_{DD,m} = 4.5\ V$
0	-10.6	-10.3	-10.0	-9.7
5	-5.6	-5.6	-5.1	-4.8
10	-1.0	-0.7	-0.2	0.2
14	2.8	3.2	3.3	3.5
Input Power (dBm)	2nd Harmonic (dBm)			
	$V_{DD,m} = 3\ V$	$V_{DD,m} = 3.5\ V$	$V_{DD,m} = 4\ V$	$V_{DD,m} = 4.5\ V$
0	-	-	-	-
5	-38	-38	-38	-36
10	-24	-25	-25	-25
14	-17	-17	-18	-18
Input Power (dBm)	Third Harmonic (dBm)			
	$V_{DD,m} = 3\ V$	$V_{DD,m} = 3.5\ V$	$V_{DD,m} = 4\ V$	$V_{DD,m} = 4.5\ V$
0	-	-	-	-
5	-36	-38	-38	-39
10	-21	-22	-24	-25
14	-16	-16	-16	-17

Table 6.1: Measured harmonic content of the output power in the prototype harmonic load modulation amplifier

6.5 CONCLUSIONS

In conclusion, the harmonic load modulation circuit design improves the efficiency of a Doherty amplifier without compromising on the linearity. The odd harmonics generated by the peaking amplifier are shunted to ground by the quarter-wave transformer at the output of the main amplifier, which shapes the main amplifier's drain voltage waveform, and allows the main amplifier's supply voltage to be lowered. This is an elegant method to create class F behaviour in the main amplifier.

A harmonic load modulation amplifier was simulated using practical components, and high efficiency and linearity was observed. The same design was then implemented in a prototype amplifier, and simulation and practical results were well matched. The amplifier displayed high efficiency over the dynamic range, while maintaining good linearity. There is a trade-off between gain and efficiency in the harmonic load modulation circuit; as the main amplifier's supply voltage is decreased, the efficiency increases, but the gain decreases. At the lowest level of supply voltage (3 V), saturation is not present, as demonstrated by the constant gain with respect to input power (between 6.4 dB and 6.5 dB), and the low levels of unwanted harmonics in the output power. Higher gain and output power could be obtained by using large transistors.

Chapter 7

CONCLUSIONS AND RECOMMENDATIONS FOR FURTHER WORK

7.1 CONCLUSIONS

The power amplifier is one of the most important components of a radio frequency transmitter, as it consumes the most DC power. Conventional linear amplifiers have a low average efficiency for modulation schemes that modulate the carrier amplitude (e.g. QAM). The Doherty amplifier is theoretically a linear amplifier with high efficiency over a wide dynamic range. However, implementing a standard Doherty amplifier that demonstrates a region of high efficiency, as well as good linearity, is not a trivial task. A large amount of the research recently carried out on Doherty amplifiers has either a continuously increasing efficiency characteristic, or a gain characteristic that is highly dependant on the input power, implying nonlinear amplification.

There are several potential reasons for a proliferation of less-than-ideal results. A number of implementations do not implement a classical Doherty amplifier, but instead use equal transistor sizes (size being the maximum output current), equal input power and fixed biases. This means the peaking amplifier outputs approximately half of the current required for classical Doherty operation, and the efficiency and gain characteristics decrease as a result (see Section 2.5).

A basic prototype Doherty amplifier was constructed using unequal transistor sizes, which was intended to be a baseline comparison for further research (see Section 1.4). This amplifier highlighted the difficulty of achieving classical Doherty amplifier output characteristics, even when simulation results are near-ideal; specifically it illustrated the sensitivity of the Doherty amplifier to transistor parametric variation, gate biasing and the drain-to-source resistance, R_{ds}. To eliminate the latter problem, it was decided that further prototypes would operate the amplifiers directly into the 50 Ω load, rather than transforming the load impedance to a higher, more optimal value.

Even when the design of the Doherty amplifier attempts to replicate the ideal fundamental output current characteristics, transistor soft turn-on can be a contributing factor to decreases in efficiency and amplifier linearity, as discussed in Section 4.3. Fi-

nally, unequal maximum fundamental output currents can result from unavailability of appropriate transistor sizes when using discrete devices, or from transistor parametric variation. This also has a detrimental effect on the Doherty amplifier's output characteristics (see Section 4.4), resulting in decreased gain and efficiency when the peaking amplifier's output current is lower than the main amplifier's, and decreased amplifier linearity when it is higher.

Bias control can potentially compensate for the problems caused by transistor soft turn-on and unequal maximum output currents. A gate bias control strategy based upon the measured gate-voltage to drain-current transfer characteristics of the transistors in the Doherty amplifier, and the desired drain current characteristics for the main and peaking amplifier is discussed in Chapter 5. By appropriate biasing of the main and peaking amplifiers at any particular input power, the effects of soft turn-on and unequal maximum output currents can be eliminated. Doherty output characteristics can be assured, with high efficiency and good linearity, regardless of transistor parametric variation. The proposed strategy uses two equal-sized transistors for simplicity, and increases the bias of the peaking amplifier from class C to class B as the input power increases. A prototype amplifier was constructed, and tests showed good agreement between theory, simulation and measured results. The efficiency remained over 34% for the last 6 dB of input power (i.e. from 8 - 14 dBm), while the gain of the amplifier was reasonably flat (remaining between 4 and 5 dB).

The harmonics generated within a Doherty amplifier circuit (which uses unequal transistor sizes or unequal input power) can be used to reduce the main amplifier's peak drain voltage. The proposed circuit design is simple and novel, with the odd harmonics generated by the peaking amplifier being shunted to ground via a quarter-wave transformer at the output of the main amplifier. Essentially, the main amplifier is operated in class F mode, and its drain current waveform resembles a clipped sinusoid. The main amplifier's supply voltage can thus be decreased without saturation occurring, which results in a higher efficiency characteristic over the dynamic range, without a decrease in linearity. We call this harmonic load modulation (see Chapter 6). A practical implementation is feasible, as demonstrated by the prototype harmonic load modulation amplifier that was designed, simulated and constructed. The prototype amplifier exhibited good linearity and efficiency characteristics, although the efficiency was less-than-ideal. This could potentially be rectified by modifying the gate bias control strategy from Chapter 5 to work with unequal transistor sizes.

7.2 SUMMARY OF CONTRIBUTIONS

The effect of transistor soft turn-on on the output characteristics of a Doherty amplifier was investigated. It was discovered that transistor soft turn-on causes the Doherty amplifier to have decreased efficiency and linearity. The effect of unequal maximum

output currents was also researched, and it was shown that while this has less impact on the Doherty amplifier's output than transistor soft turn-on, it still can result in a decrease in efficiency and a decrease in gain and/or a decrease in amplifier linearity, depending on whether the peaking amplifier outputs too much or too little current compared to the ideal level.

A gate bias control strategy is proposed, based upon the measured gate-voltage to drain-current characteristics of the transistors used in a Doherty amplifier. The strategy controls the gate bias of both the main and peaking amplifier, and attempts to replicate the ideal output current characteristics of a Doherty amplifier. The strategy compensates for transistor soft turn-on and unequal maximum fundamental output currents, giving near-ideal Doherty output characteristics regardless of transistor parametric variation. A prototype amplifier was constructed, and demonstrated good agreement between theory, simulation and results, with high efficiency and linearity. The strategy is not dependent on the transistor type or model used in this work, and can easily be used for any transistor, as long as it can be modelled as a dependant current source.

During the design of the prototype amplifier for the gate bias control strategy, the role of the harmonics in a Doherty amplifier circuit was questioned. An elegant and novel solution to their removal from the output signal was conceived, which resulted in the main amplifier basically operating as a class F amplifier (see Chapter 6). This meant that its supply voltage could be decreased without the amplifier entering saturation. The output power and gain of the harmonic load modulation amplifier was very similar to that of a conventional Doherty amplifier, and the efficiency was increased over the whole dynamic range. A prototype amplifier was constructed, and demonstrated that the harmonic load modulation circuit design worked as per simulations, with good efficiency and linearity.

7.3 RECOMMENDATIONS FOR FURTHER WORK

There is still a significant amount of research to be done before the work in this thesis is ready for a commercial application, although the research done here has proved that the concepts are sound. The main areas to be investigated are:

1. Increasing the gain of the amplifiers by:
    - The use of impedance transformation between the output load of 50 Ω and the optimum load of the transistors
    - The use of larger transistors
    - Input matching

2. Improving the bias control strategy to take into account the difference between the input signals received by main and peaking amplifiers, and the theoretical input signals.

3. Implementing the bias control strategy in a digital controller, rather than a manual implementation.

4. Investigating an adaptive system, where the output levels of the amplifiers are continuously monitored and used to update the bias control strategy, to further improve the results, and to take into account any changes in the transistor transfer characteristics which may occur over time.

5. Improving the performance of the harmonic load modulation amplifier, perhaps by use of gate bias control, (combined with unequal transistor sizes or unequal input power) to account for unequal maximum output currents and transistor soft turn-on.

Appendix A

SIMULATION METHODOLOGY

A.1 CHOICE OF SIMULATION SOFTWARE

For microwave circuit simulations the large-signal steady-state solution is of interest. There are two common ways this can be determined: time domain analysis and mixed domain analysis. Time domain analysis (such as is used in SPICE) is not appropriate for the circuits used in this thesis, for two reasons. Firstly, microwave circuits have both small and large time-constants. The latter are due to bias and decoupling circuits, and result in long computation times if the circuit is analysed in the time domain. Secondly, time domain analysis inefficiently analyses non-linear elements (such as transmission lines), of which there are a significant number.

Mixed domain analysis partitions the circuit into linear and non-linear elements, performing frequency domain and time domain analysis on them respectively. This makes it efficient for the type of circuits used in this thesis. There are several software packages which perform this style of analysis. The simulations in this thesis were carried out using AWR Microwave Office (MWO) [7], which uses harmonic balance principles.

A.2 HARMONIC BALANCE PRINCIPLES

Harmonic balance determines the large-signal steady-state solution of the circuit for sinusoidal excitation. For a non-linear circuit, this solution is a Fourier series of the voltages and currents. The solution is determined by partitioning the circuit into linear and non-linear elements, with the former analysed in the frequency domain, and the later in the time domain. The two domains are bridged by the fast Fourier transform (FFT) and the inverse fast Fourier transform (IFFT). This is an efficient analysis method, as the 'best' domain is used for each circuit element.

The technique is iterative, with the Fourier coefficients being adjusted at each iteration until Kirchhoff's current law is satisfied. The Fourier series is truncated throughout the computations, as it is impossible to determine an infinite series of

Fourier coefficients. The degree of truncation is determined by the user, and is discussed further in section A.4.

In MWO, the results determined can be displayed in a range of ways, for example as a waveform or a spectrum. Attributes of the results can also easily be presented, such as the amplitude of a waveform, or the load power. In the later case they can be presented as a function of input power (i.e. multiple excitation levels are calculated).

A.3 VALIDITY FOR CLASS B AND CLASS C AMPLIFIERS

To demonstrate the validity of the harmonic balance technique and the simulation software for the circuits used in this thesis, ideal class B and class C amplifiers were simulated. Figures A.1 and A.2 show the waveforms for these amplifiers. In both cases 100 harmonics were used (well above the level required for accurate simulations, as discussed in section A.4). It can be seen that all the figures give results consistent with class B and class C amplifier operation, meaning the harmonic balance technique used in MWO is a valid choice for simulating Doherty amplifiers.

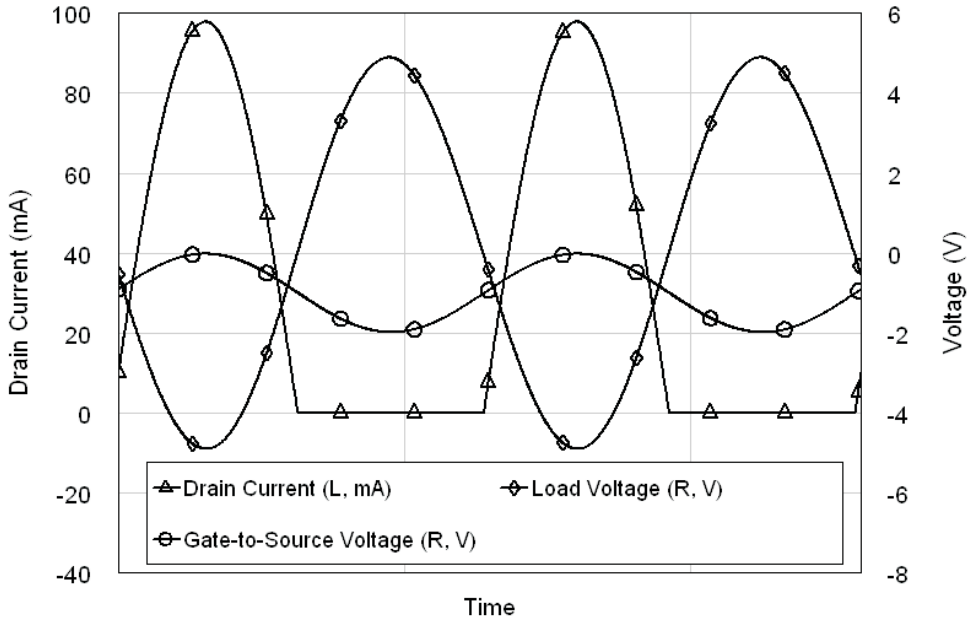


Figure A.1: Simulated waveforms for an ideal class B amplifier

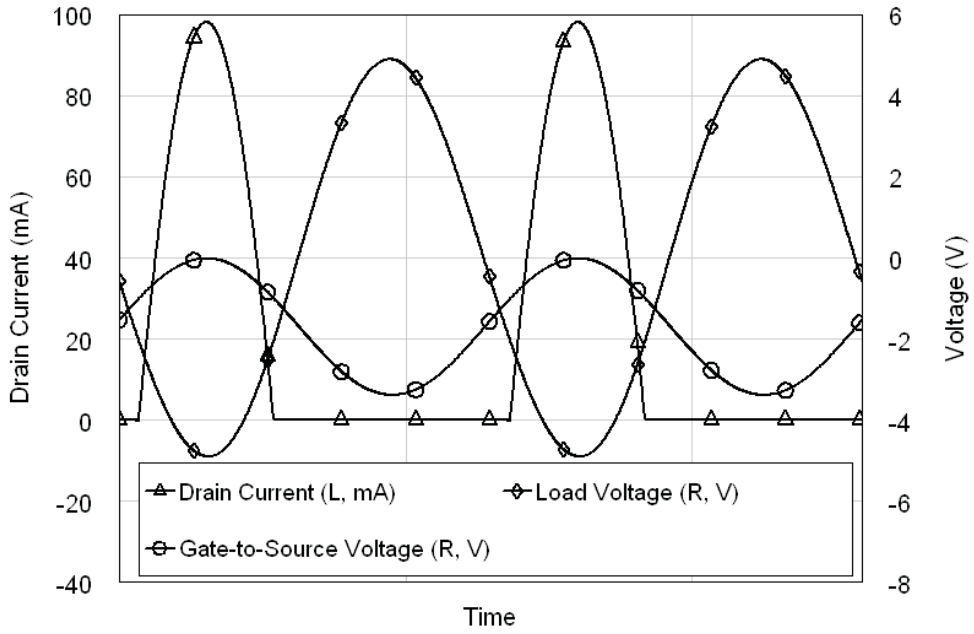


Figure A.2: Simulated waveforms for an ideal class C amplifier

A.4 NUMBER OF HARMONICS USED

Truncation of the Fourier coefficients is required in any calculation, as it is impossible to determine an infinite series. In MWO, the number of harmonics used in a simulation is chosen by the user. Truncation of these coefficients is feasible, since harmonics over the the 5th harmonic are generally negligible. The more harmonics used, the more accurate the results will be, but this is gained at the expense of computation time. The simulations in this thesis used nine harmonics, which gives good results for single-tone excitation (multi-tone excitation was not used at any time).

Figures A.3 to A.5 demonstrate the effect of decreasing the harmonics used in the computations. When compared to Figure A.2 (which used 100 harmonics), it can be seen that nine harmonics gives a good approximation, with only small discrepancies at the points where the transistor turns on. However, using six and two harmonics give decreasing degrees of accuracy.

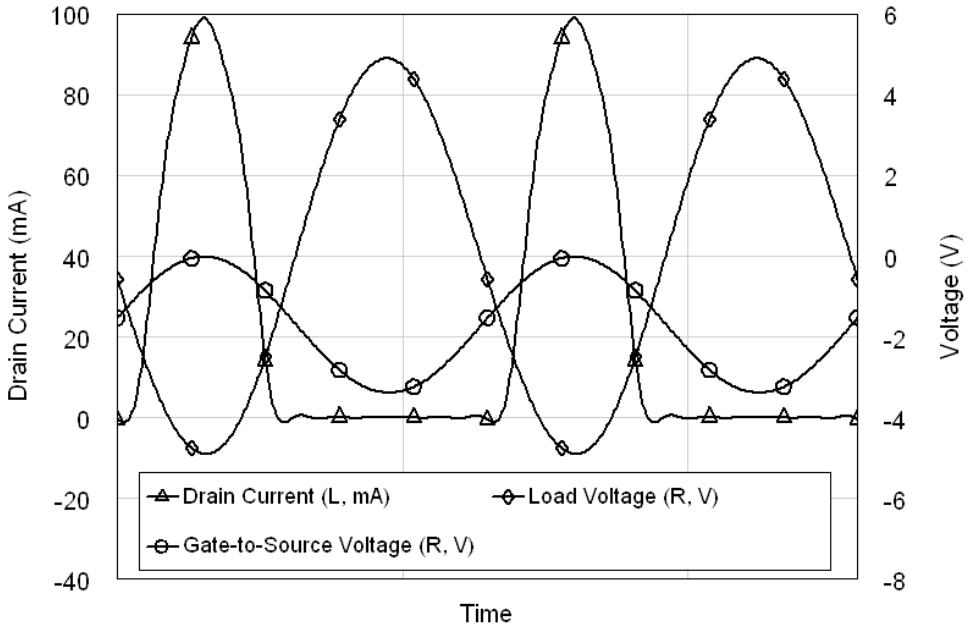


Figure A.3: Simulated waveforms for an ideal class C amplifier using nine harmonics

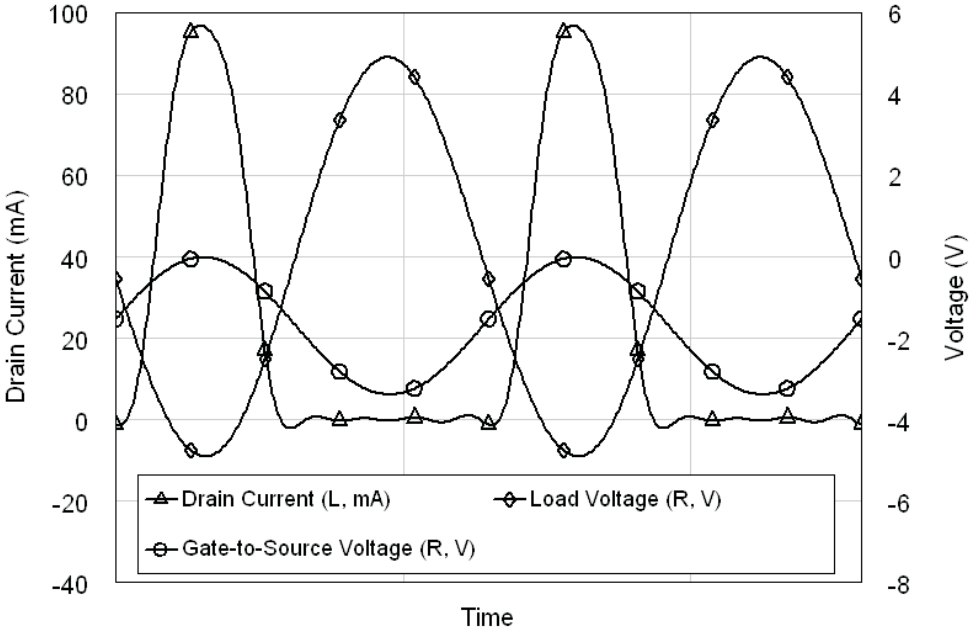


Figure A.4: Simulated waveforms for an ideal class C amplifier using six harmonics

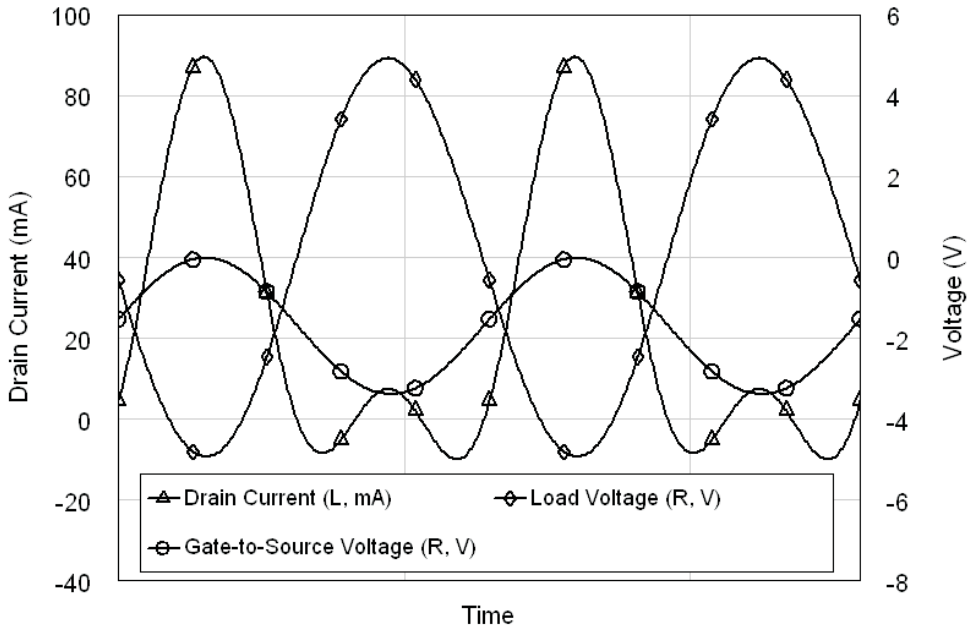


Figure A.5: Simulated waveforms for an ideal class C amplifier using two harmonics

Appendix B

CLASS B AND C AMPLIFIER ANALYSIS USING IDEAL TRANSISTORS

B.1 BASIC ANALYSIS INFORMATION

B.1.1 Class B and Class C Amplifier Circuit

The circuit layout used for the class B and class C analyses is given in Figure B.1. Ideal components are assumed; the transistor details are discussed in Section 2.3. The inductors and their respective capacitors are chosen such that

$$\omega_0 = \frac{1}{\sqrt{L_1 C_1}} = \frac{1}{\sqrt{L_2 C_2}}$$

i.e. they are resonant at the operating frequency, and all harmonics in the output waveforms are shunted to ground.

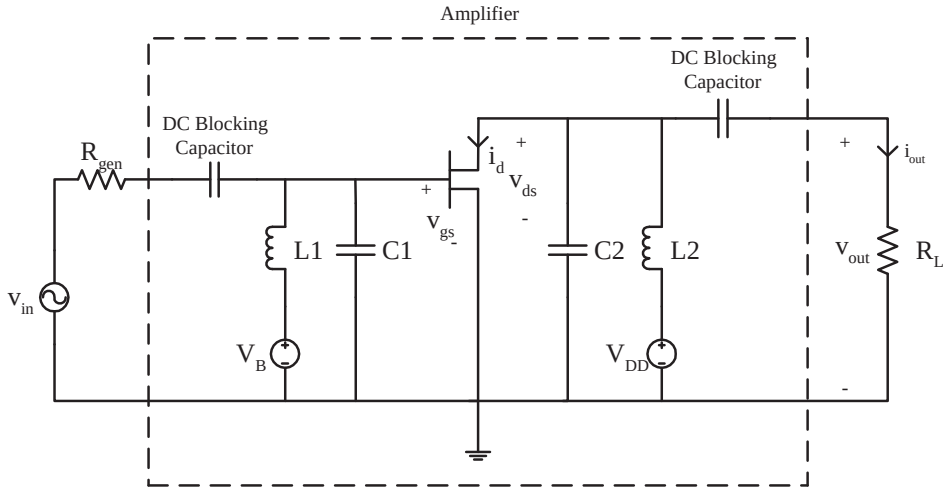


Figure B.1: Basic circuit diagram for class B and class C amplifiers

B.1.2 Fourier Analysis

Any periodic voltage or current waveform can be written in the expanded form,

$$x(t) = a_0 + \sum_{n=1}^{\infty} a_n \cos\left(n\frac{2\pi}{T}t\right) + \sum_{n=1}^{\infty} b_n sin\left(n\frac{2\pi}{T}t\right)$$

where T is the period of the waveform. For an even function,

$$a_o = \frac{2}{T}\int_0^{\frac{T}{2}} x(t)\,dt \tag{B.1}$$

$$a_n = \frac{4}{T}\int_0^{\frac{T}{2}} x(t)\cos\left(n\frac{2\pi}{T}t\right)\,dt \tag{B.2}$$

Writing in terms of θ ($\omega_0 = 2\pi/T$ and $\theta = \omega_0 t$),

$$x(t) = a_0 + \sum_{n=1}^{\infty} a_n \cos(n\theta) \tag{B.3}$$

B.2 CLASS B AMPLIFIER ANALYSIS

B.2.1 Waveforms

In a class B amplifier, the transistor is biased at the threshold voltage, V_T, meaning its drain current waveform is a half-wave rectified sinewave. A complete set of waveforms for the transistor is given in Figure B.2; their mathematical expressions are:

$$\begin{aligned} v_{gs}(\theta) &= V_{in}\cos\theta + V_T \\ v_{ds}(\theta) &= V_{DD} - V_{out}\cos\theta \\ v_{dg}(\theta) &= V_{DD} - (V_{out} + V_{in})\cos\theta - V_T \end{aligned} \tag{B.4}$$

$$i_d(\theta) = \begin{cases} I_{d,pk}\cos\theta & -\frac{\pi}{2} \le \theta \le \frac{\pi}{2} \\ 0 & \text{elsewhere} \end{cases}$$

$$I_{d,pk} = \frac{I_{DSS}V_{in}}{|V_T|} \qquad V_{in} \le |V_T|$$

At maximum input power, the peak value of the drain-to-gate voltage waveform, $v_{dg,pk}$, will be $2V_{DD} - 2V_T$ (from (B.4)). It should be noted that V_T is negative.

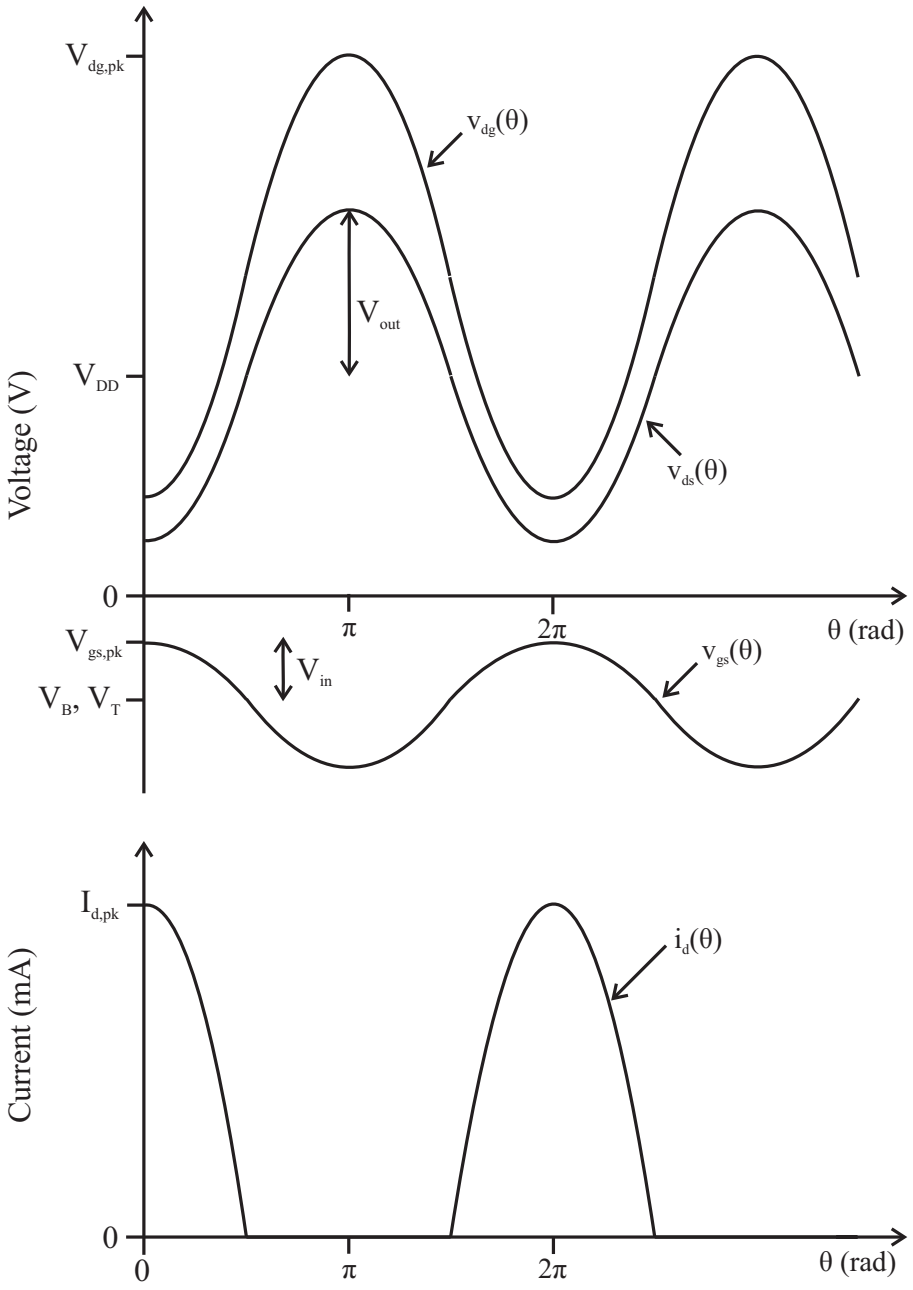


Figure B.2: Class B transistor waveforms

B.2.2 Fourier Analysis of Drain Current

Using Fourier series, as discussed in Section B.1.2, the DC and harmonic components of the drain current waveform can be determined. Applying (B.1) to $i_d(\theta)$, the DC component is

$$I_{d0} = \frac{I_{d,pk}}{\pi} \tag{B.5}$$

Applying (B.2) to $i_d(\theta)$, the harmonic components of the drain current are

$$I_{dn} = \frac{2I_{d,pk}}{\pi(1-n^2)} \cos\left(\frac{n\pi}{2}\right) \qquad n \geq 2 \tag{B.6}$$

and the fundamental is given by:

$$I_{d1} = \frac{I_{d,pk}}{2} \tag{B.7}$$

$$= \frac{I_{DSS}V_{in}}{2|V_T|} \tag{B.8}$$

Finally, the full expanded equation for $i_d(\theta)$ can be written, by substituting (B.5), (B.6), and (B.7) into (B.3);

$$i_d(\theta) = \frac{I_{d,pk}}{\pi} + \frac{I_{d,pk}}{2}\cos\theta + \frac{2I_{d,pk}}{3\pi}\cos 2\theta - \frac{2I_{d,pk}}{15\pi}\cos 4\theta + \cdots$$

From this result, it can be seen that there are no odd harmonics in the drain current waveform. As the only undesired harmonics are even, it is possible to use a $\lambda/4$ transmission line short-circuit stub to shunt them to ground, instead of the resonant circuit depicted in Figure B.1.

B.2.3 Optimum Load

In order to produce maximum efficiency, R_L is chosen such that the drain current and drain voltage swing will be maximised within the confines of the FET output characteristic. These are both achieved at maximum input power; the former when $V_{in} = |V_T|$, and the latter if $V_{out} = V_{DD}$ (see Figure B.2). It should be noted that it is necessary for $V_{DD} \leq V_{d,max}/2$, otherwise $v_{dg}(\theta)$ will exceed its maximum allowable value. As such, using (B.7), the optimal value of the load resistance is

$$R_{L,opt} = \frac{V_{d1,max}}{I_{d1,max}} = \frac{2V_{DD}}{I_{d,pk,max}} = \frac{2V_{DD}}{I_{DSS}} \tag{B.9}$$

Rearranging this to get an optimal supply voltage (given a set load resistance) gives

$$V_{DD} = \frac{I_{DSS}R_L}{2} \tag{B.10}$$

B.2.4 Output Power

As the undesired harmonics are shunted to ground by the output resonator, and the DC component of the drain current is blocked from reaching the load by a capacitor, the output current and voltage are sinusoidal with amplitudes

$$I_{out} = \frac{I_{d,pk}}{2} = \frac{I_{DSS}V_{in}}{2|V_T|}$$

$$V_{out} = \frac{I_{d,pk} R_L}{2} = \frac{I_{DSS} V_{in}}{2|V_T|} R_L$$

Using the equations for output current, the output power of the circuit is

$$\begin{aligned} P_{out} &= \frac{-I_{d1}^2}{2} R_L \\ &= \frac{I_{d,pk}^2 R_L}{8} \\ &= \frac{(I_{DSS} V_{in})^2 R_L}{8 V_T^2} \end{aligned} \tag{B.11}$$

Clearly, P_{out} is proportional to P_{in}. To ensure the amplifier stays within the linear region, $V_{in} \leq |V_T|$. Hence, the maximum output power is when V_{in} is at its maximum of $|V_T|$;

$$P_{out,max} = \frac{I_{DSS}^2 R_L}{8} \tag{B.12}$$

B.2.5 Efficiency

The efficiency of a class B amplifier can be calculated, once the DC power being fed into the circuit is determined. The DC power is

$$\begin{aligned} P_{DC} &= V_{DD} \cdot I_{d0} \\ &= \frac{V_{DD} I_{d,pk}}{\pi} \\ &= \frac{V_{DD} I_{DSS} V_{in}}{\pi |V_T|} \end{aligned} \tag{B.13}$$

Meaning that the P_{DC} is directly proportional to V_{in}. When $V_{in} = |V_T|$ it will be at its maximum of

$$P_{DC,max} = \frac{V_{DD} I_{DSS}}{\pi} \tag{B.14}$$

Using (B.11) and (B.13), the efficiency of the circuit is

$$\begin{aligned} \eta &= \frac{P_{out}}{P_{DC}} \\ &= \frac{\pi I_{d,pk} R_L}{8 V_{DD}} \\ &= \frac{\pi I_{DSS} V_{in} R_L}{8 V_{DD} |V_T|} \end{aligned} \tag{B.15}$$

Clearly, η is also proportional to V_{in}, and also has its maximum when $V_{in} = |V_T|$. This maximum is

$$\begin{aligned} \eta_{max} &= \frac{\pi}{4} \\ &= 78.5\% \end{aligned}$$

B.2.6 Comparison of Theoretical and Simulation Results

The output power, gain and efficiency characteristics of a specific class B amplifier are shown in Figure B.3 (V_T = -1 V, I_{DSS} = 100 mA). Two sets of values are shown - one from a simulation, the other calculated using (B.11) and (B.15), and the fact that $Gain = P_{out,dB} - P_{in,dB}$. These confirm that as long as $V_{in} \leq |V_T|$, the equations given are valid.

It can be seen that the gain is constant with respect to input power, meaning the amplifier is linear within the bounds given. As expected, the efficiency is proportional to input voltage, with a maximum value of 78.5%. However, once saturation is reached, the characteristics dramatically change.

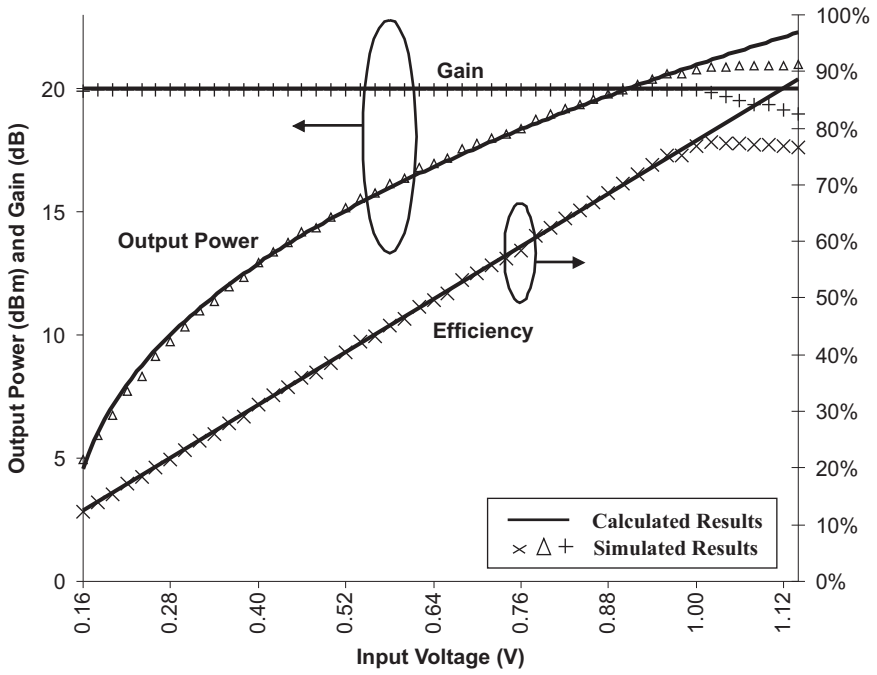


Figure B.3: Class B Gain, Output Power and Efficiency

B.3 CLASS C AMPLIFIER ANALYSIS

B.3.1 Waveforms

In a class C amplifier, the transistor is biased between its threshold voltage, V_T, and $2V_T$, meaning its drain current waveform is a series of peaks (less than half-wave). A complete set of waveforms for the transistor is given in Figure B.4; their mathematical

expressions are:

$$\begin{aligned} v_{gs}(\theta) &= V_{in}\cos\theta + V_B \\ v_{ds}(\theta) &= V_{DD} - V_{out}\cos\theta \\ v_{dg}(\theta) &= V_{DD} - (V_{out} + V_{in})\cos\theta - V_B \end{aligned} \tag{B.16}$$

$$i_d(\theta) = \begin{cases} I_{d,pk}\cos\theta & -\frac{\alpha}{2} \le \theta \le \frac{\alpha}{2} \\ 0 & \text{elsewhere} \end{cases}$$

$$I_{d,pk} = I_{DSS}\left(1 - \frac{V_{in} + V_B}{V_T}\right) \qquad V_{in} \le |V_B|$$

where α is the conduction angle. Equating (B.16) to V_T gives

$$\alpha = 2\cos^{-1}\left(\frac{V_T - V_B}{V_{in}}\right) \tag{B.17}$$

It should be noted that α changes as the input power of the amplifier changes. Also, the case of $\alpha = \pi$ (or 180°) is the special case of a class B amplifier.

At maximum input power, the peak value of the drain-to-gate voltage waveform, $v_{dg,pk}$, will be $2V_{DD} - 2V_B$ (from (B.16)). It should be noted that V_B is negative. This can be compared to the peak value in a class B amplifier, which is $2V_{DD} - 2V_T$. It can be seen that the class C amplifier has a larger drain-to-gate voltage amplitude than a class B amplifier. Hence, transistor breakdown is more likely to occur, which is one of the major disadvantages of a class C amplifier.

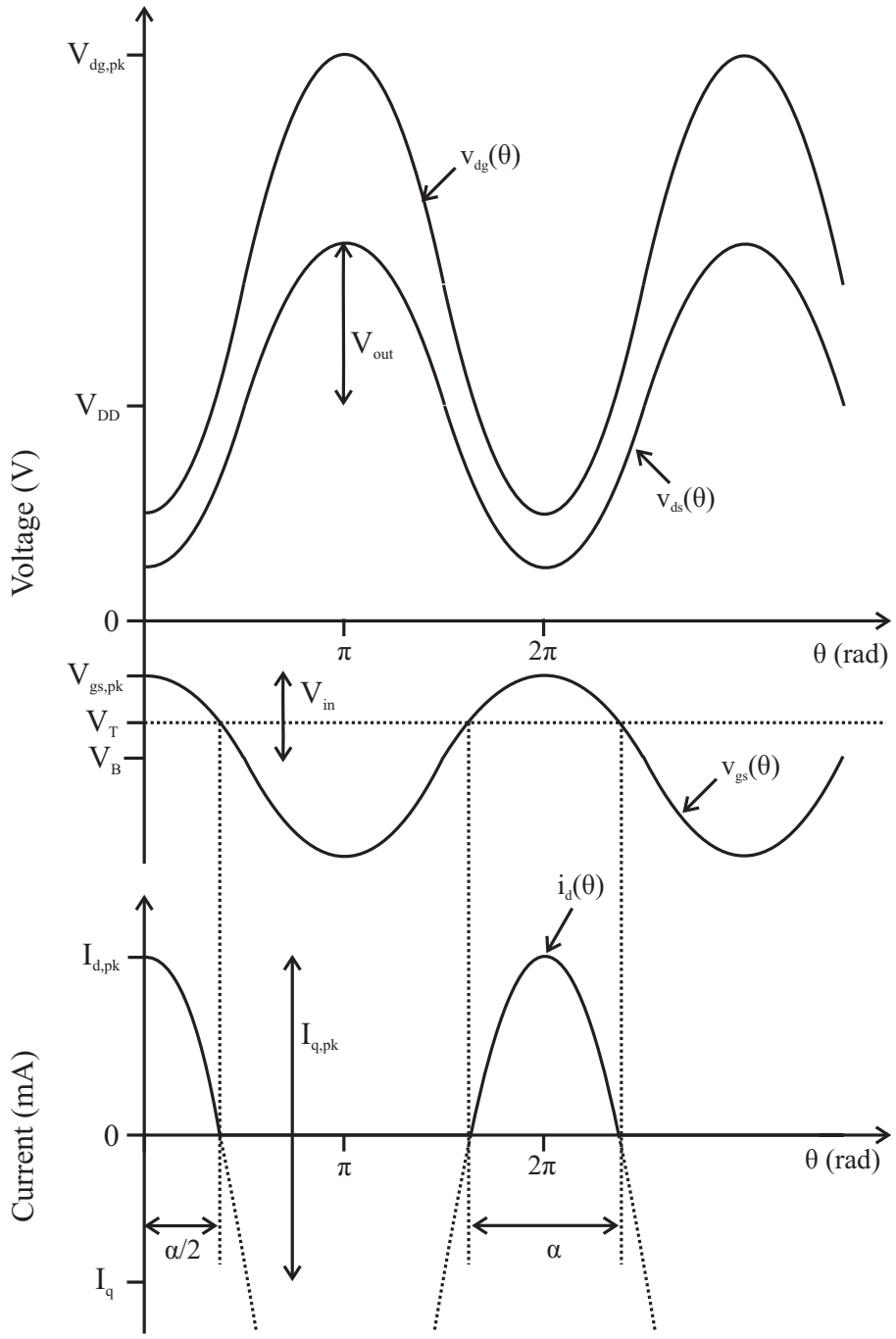


Figure B.4: Class C transistor waveforms

B.3.2 Fourier Analysis of Drain Current

In Figure B.4, it can be seen that $i_d(\theta)$ can be thought of as the positive portion of a sinusoidal wave centred on a quiescent point, I_q:

$$i_d(\theta) = \begin{cases} I_q + I_{q,pk}\cos\theta & -\frac{\alpha}{2} \leq \theta \leq \frac{\alpha}{2} \\ 0 & \text{elsewhere} \end{cases} \tag{B.18}$$

$$I_q = I_{d,pk} - I_{q,pk} \tag{B.19}$$

It is desirable to have the results of the Fourier analysis expressed in terms of $I_{d,pk}$. I_d goes to zero at $\theta = \pm\alpha/2$. Equating (B.18) to zero:

$$I_q = -I_{q,pk} \cos\frac{\alpha}{2} \tag{B.20}$$

Equating (B.19) and (B.20) gives

$$\begin{aligned} -I_{q,pk} \cos\frac{\alpha}{2} &= I_{d,pk} - I_{q,pk} \\ I_{q,pk} &= \frac{I_{d,pk}}{1 - \cos\frac{\alpha}{2}} \end{aligned} \tag{B.21}$$

Using Fourier series, as discussed in Section B.1.2, the DC and harmonic components of the drain current can be determined. Applying (B.1) to $i_d(\theta)$, the DC component is

$$I_{d0} = \frac{I_{d,pk}}{\pi}\left(\frac{\sin\frac{\alpha}{2} - \frac{\alpha}{2}\cos\frac{\alpha}{2}}{1 - \cos\frac{\alpha}{2}}\right) \tag{B.22}$$

Applying (B.2) to $i_d(\theta)$, the harmonics of the drain current are

$$I_{dn} = \frac{2I_{d,pk}}{n\pi\left(1 - n^2\right)}\left(\frac{n\sin\frac{\alpha}{2}\cos\frac{n\alpha}{2} - \cos\frac{\alpha}{2}\sin\frac{n\alpha}{2}}{1 - \cos\frac{\alpha}{2}}\right) \qquad n \geq 2 \tag{B.23}$$

and the fundamental is given by:

$$I_{d1} = \frac{I_{d,pk}}{2\pi}\left(\frac{\alpha - \sin\alpha}{1 - \cos\frac{\alpha}{2}}\right) \tag{B.24}$$

$$= \frac{I_{DSS}}{2\pi}\left(1 - \frac{V_{in} + V_B}{V_T}\right)\left(\frac{\alpha - \sin\alpha}{1 - \cos\frac{\alpha}{2}}\right) \tag{B.25}$$

Finally, the full equation for $i_d(\theta)$ can be written, by substituting (B.22), (B.23), and (B.24) into (B.3);

$$\begin{aligned} i_d(\theta) = {} & \frac{I_{d,pk}}{\pi}\left(\frac{\sin\frac{\alpha}{2} - \frac{\alpha}{2}\cos\frac{\alpha}{2}}{1 - \cos\frac{\alpha}{2}}\right) + \frac{I_{d,pk}}{2\pi}\left(\frac{\alpha - \sin\alpha}{1 - \cos\frac{\alpha}{2}}\right)\cos\theta \\ & + \frac{I_{d,pk}}{3\pi}\left(\frac{\cos\frac{\alpha}{2}\sin\alpha - 2\sin\frac{\alpha}{2}\cos\alpha}{1 - \cos\frac{\alpha}{2}}\right)\cos 2\theta \\ & + \frac{I_{d,pk}}{12\pi}\left(\frac{\cos\frac{\alpha}{2}\sin\frac{3\alpha}{2} - 3\sin\frac{\alpha}{2}\cos\frac{3\alpha}{2}}{1 - \cos\frac{\alpha}{2}}\right)\cos 3\theta + \cdots \end{aligned}$$

From this result it can be seen that unlike in a class B amplifier, there are both odd and even harmonics in the drain current waveform. As a side note, the equations derived above can also be used for class A, class AB, and class B amplifiers. Figure B.5 shows values for the different drain current components, up to $n = 4$.

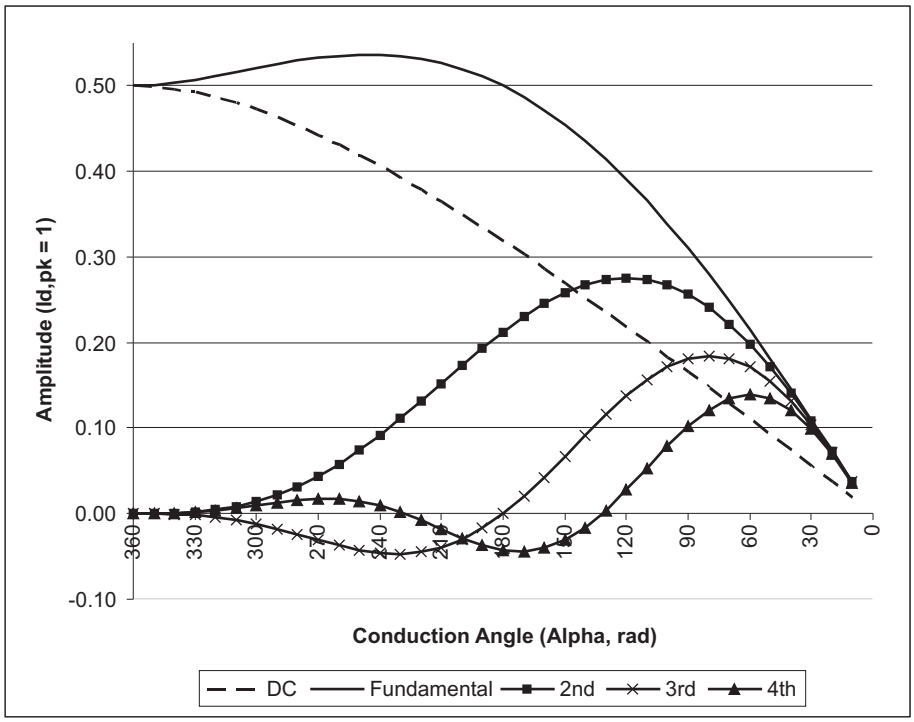


Figure B.5: Drain current components for class A, class AB, class B and class C amplifiers

B.3.3 Optimum Load

In order to produce maximum efficiency, R_L is chosen such that the drain current and drain voltage swing will be maximised within the confines of the FET output characteristic. These are both achieved at maximum input power; the former when $V_{in} = |V_T|$, and the latter if $V_{out} = V_{DD}$ (see Figure B.4). It should be noted that it is necessary for $V_{DD} \leq V_{d,max}/2$, otherwise $v_{dg}(\theta)$ will exceed its maximum allowable value. As such, using (B.24), the optimal value of the load resistance is

$$\begin{aligned} R_{L,opt} = \frac{V_{d1,max}}{I_{d1,max}} &= \frac{2\pi V_{DD}}{I_{d,pk}} \left(\frac{1 - \cos\frac{\alpha}{2}}{\alpha - \sin\alpha} \right) \\ &= = \frac{2\pi V_{DD} V_T}{I_{DSS}\left(V_T - 2V_B\right)} \left(\frac{1 - \cos\frac{\alpha}{2}}{\alpha - \sin\alpha} \right) \end{aligned} \tag{B.26}$$

Rearranging this to get an optimal supply voltage (given a set load resistance) gives

$$V_{DD} = \frac{R_L I_{DSS}\left(V_T - 2V_B\right)}{2\pi V_T} \left(\frac{\alpha - \sin\alpha}{1 - \cos\frac{\alpha}{2}} \right) \tag{B.27}$$

It can be seen, that unlike a class B amplifier, the optimum load and supply voltage are dependent on α. They are evaluated at maximum input power, and hence at the value of α at maximum input power.

B.3.4 Output Power

As the undesired harmonics are shunted to ground by the output resonator, and the DC component is blocked from reaching the load by a capacitor, the equations for the output current and voltage are sinusoidal with amplitudes:

$$I_{out} = \frac{-I_{d,pk}}{2\pi}\left(\frac{\alpha - \sin\alpha}{1-\cos\frac{\alpha}{2}}\right)$$

$$V_{out} = \frac{-I_{d,pk}R_L}{2\pi}\left(\frac{\alpha - \sin\alpha}{1-\cos\frac{\alpha}{2}}\right)$$

Using the equation for output current, the output power of the circuit is

$$\begin{aligned} P_{out} &= \frac{I_{d1}^2}{2}R_L \\ &= \frac{I_{d,pk}^2 R_L}{8\pi^2}\left(\frac{\alpha - \sin\alpha}{1-\cos\frac{\alpha}{2}}\right)^2 \end{aligned} \tag{B.28}$$

To ensure the amplifier stays within the linear region, $V_{in} \leq |V_B|$. Hence, the maximum output power will occur when $V_{in} = |V_B|$:

$$P_{out,max} = \frac{I_{DSS}^2 R_L}{8\pi^2}\left(\frac{\alpha - \sin\alpha}{1-\cos\frac{\alpha}{2}}\right)^2 \tag{B.29}$$

B.3.5 Efficiency

The efficiency of a class C amplifier can be calculated, once the DC power being fed into the circuit is determined. Using (B.22), the DC power is

$$\begin{aligned} P_{DC} &= V_{DD}\cdot I_{d0} \\ &= \frac{V_{DD}I_{d,pk}}{\pi}\left(\frac{\sin\frac{\alpha}{2} - \frac{\alpha}{2}\cos\frac{\alpha}{2}}{1-\cos\frac{\alpha}{2}}\right) \qquad \text{(B.30)} \\ &= \frac{V_{DD}I_{DSS}}{\pi}\left(1 - \frac{V_{in}+V_B}{V_T}\right)\left(\frac{\sin\frac{\alpha}{2} - \frac{\alpha}{2}\cos\frac{\alpha}{2}}{1-\cos\frac{\alpha}{2}}\right) \qquad \text{(B.31)} \end{aligned}$$

When $V_{in} = |V_B|$ the DC power will be at its maximum of

$$P_{DC,max} = \frac{V_{DD}I_{DSS}}{\pi}\left(\frac{\alpha - \sin\alpha}{1-\cos\frac{\alpha}{2}}\right)\left(\frac{\sin\frac{\alpha}{2} - \frac{\alpha}{2}\cos\frac{\alpha}{2}}{1-\cos\frac{\alpha}{2}}\right) \tag{B.32}$$

As such, using (B.28) and (B.30), the efficiency of the circuit is

$$\begin{aligned}\eta &= \frac{P_{out}}{P_{DC}} \\ &= \frac{I_{d,pk}R_L}{8\pi V_{DD}} \frac{(\alpha - \sin\alpha)^2}{\left(1-\cos\frac{\alpha}{2}\right)\left(\sin\frac{\alpha}{2} - \frac{\alpha}{2}\cos\frac{\alpha}{2}\right)} \\ &= \frac{I_{DSS}R_L}{8\pi V_{DD}} \left(1 - \frac{V_{in}+V_B}{V_T}\right) \frac{(\alpha - \sin\alpha)^2}{\left(1-\cos\frac{\alpha}{2}\right)\left(\sin\frac{\alpha}{2} - \frac{\alpha}{2}\cos\frac{\alpha}{2}\right)} \end{aligned} \tag{B.33}$$

The maximum efficiency also occurs when $V_{in} = |V_B|$, and is given by

$$\eta_{max} = \frac{I_{DSS}R_L}{8\pi V_{DD}} \frac{(\alpha - \sin\alpha)^2}{\left(1-\cos\frac{\alpha}{2}\right)\left(\sin\frac{\alpha}{2} - \frac{\alpha}{2}\cos\frac{\alpha}{2}\right)} \tag{B.34}$$

B.3.6 Comparison of Theoretical and Simulation Results

The gain, output power and efficiency characteristics of a specific class C amplifier are shown in Figure B.6 (V_T = -1 V, I_{DSS} = 100 mA and V_B = -1.7 V). Two sets of values are shown - one from a simulation, the other calculated using (B.28) and (B.33), and the fact that $Gain = P_{out,dB} - P_{in,dB}$. These confirm that as long as $V_{in} \leq |V_B|$, the equations given are valid. It can be seen that this amplifier isn't linear - the gain varies with V_{in}. However, the efficiency of the amplifier is higher than that for a class B amplifier. In the case shown in the figure, (at maximum power $\alpha \approx 131°$,) the maximum efficiency is approximately 85%. In theory, the maximum efficiency of a class C amplifier is 100%, although, as this happens when $\alpha = 0°$ (and hence $P_{out} = 0$), it is not particularly useful. It should also be noted that a class C amplifier provides less gain than a class B amplifier.

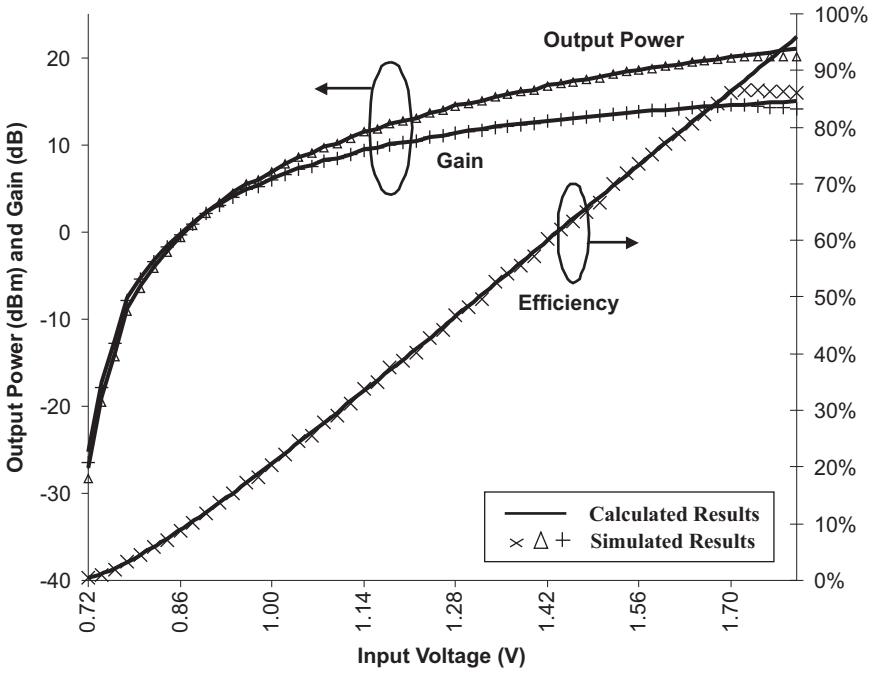


Figure B.6: Class C Gain, Output Power and Efficiency

B.3.7 Class C Amplifier Characteristics Relating to a Doherty Amplifier

The gate-voltage to drain-current characteristic of a class C amplifier is very important for a Doherty amplifier, as it is highly desirable to have equal maximum output currents, as shown in Section 4.4. The drain current of a class C amplifier is dependent on α, which according to (B.17), is dependent on the bias voltage, V_B (which is fixed), and the input voltage, V_{in} (which varies with input power). The bias of the peaking amplifier is different for each technique used to increase the output power of the peaking amplifier (see Section 2.4.1). The α characteristic of the peaking amplifier, using each technique, is shown in Figure B.7. It should be noted that the input voltage against which these graphs are plotted is for the Doherty amplifier, not for the peaking amplifier.

It can be seen that unequal transistor sizes and unequal input power split result in the same α characteristic, while the bias control technique results in a larger variance in α. This is because the first two techniques bias the peaking amplifier at a fixed point in class C, while with bias control the peaking amplifier's bias goes from class C up to class B. In all cases however, α varies over the range of input voltages.

The Doherty amplifier's ideal current characteristics have equal maximum fundamental drain currents for the main and peaking amplifier's transistors ($I_{m,max} = I_{p,max}$). The fundamental drain current of the main amplifier can be determined using

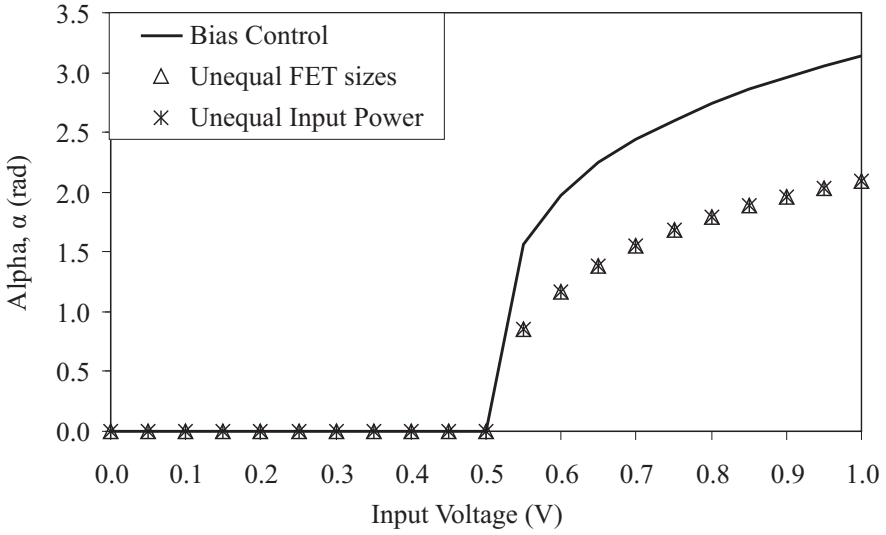


Figure B.7: Conduction angle, α, of the peaking amplifier in a Doherty amplifier

(B.8), and the fact that at maximum input voltage, $V_{in,m} = |V_T|$, giving

$$I_{m,max} = \frac{I_{DSS,m}}{2} \tag{B.35}$$

The maximum drain current of the peaking amplifier is dependent on α, which can be calculated by substituting $V_{B,P} = 1.5V_{B,M} = 1.5V_T$ and $V_{in,p} = -V_T$ into (B.17), giving $\alpha = 2.09$ rad (note that V_T is negative). Substituting these values into (B.25) gives

$$I_{p,max} = 2.45\frac{I_{DSS,p}}{4\pi} \tag{B.36}$$

Equating (B.35) and (B.36) (as it is desired to have equal maximum fundamental drain currents), and rearranging, gives

$$\frac{I_{DSS,p}}{I_{DSS,m}} = 2.55$$

A similar process can be followed to determine the ratio between the two transistors when a square law characteristic is assumed. In this case, the main and peaking amplifiers' fundamental drain currents are

$$I_{m1} = \frac{4I_{DSS,m}V_{in}^2}{3\pi V_T^2} \tag{B.37}$$

$$I_{p1} = \frac{2I_{DSS,p}(V_T - V_{in} - V_B)^2}{\pi V_T^2}\left(\frac{\frac{3}{4}\sin\frac{\alpha}{2} + \frac{1}{12}\sin\frac{3\alpha}{2} - \frac{\alpha}{2}\cos\frac{\alpha}{2}}{\left(1-\cos\frac{\alpha}{2}\right)^2}\right) \tag{B.38}$$

Once more using $V_{B,P} = 1.5V_{B,M} = 1.5V_T$ and $V_{in,p} = -V_T$, and $\alpha = 2.09$ rad, the

maximum drain currents can be determined,

$$I_{m,max} = \frac{4I_{DSS,m}}{3\pi} \tag{B.39}$$

$$I_{p,max} = 0.5\frac{I_{DSS,p}}{2\pi} \tag{B.40}$$

Equating these and rearranging gives

$$\frac{I_{DSS,p}}{I_{DSS,m}} = 5.3$$

The output current characteristics of the peaking amplifier, for all the different techniques, are shown in Figure B.8. It can be seen that they all approximate the ideal characteristic (in the case of bias control, the ideal characteristic is achieved), but there are slight differences, due to the differences in α and V_B. Using unequal input power it is not possible to achieve the ideal maximum fundamental peaking amplifier output current and to have the peaking amplifier turn on at the correct point. This is because the turn-on point is at half of maximum input voltage, but the fundamental output current of the peaking amplifier is less than half of the maximum output current.

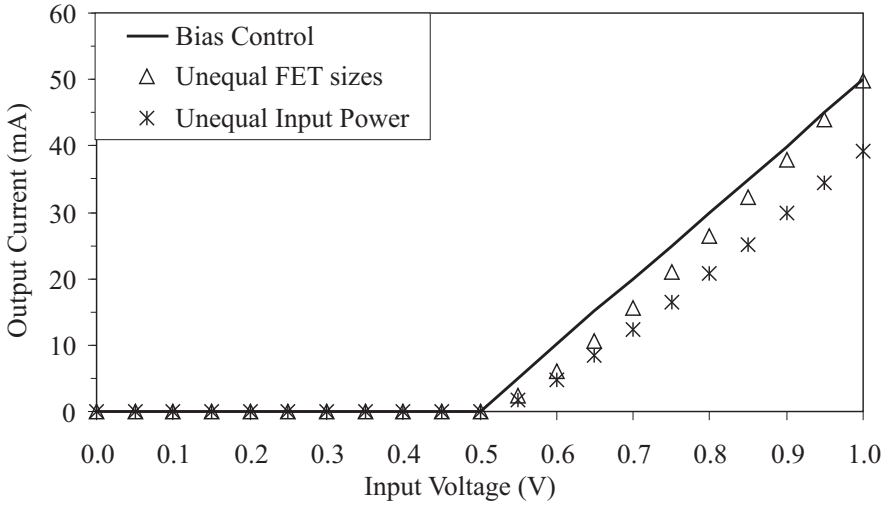


Figure B.8: Fundamental output current of the peaking amplifier in a Doherty amplifier

Appendix C

THE FET MODEL USED IN SIMULATION

The complete FET model includes chip and parasitic effects, and has a circuit diagram as shown in Figure C.1. This model is based on the Statz model [15], and is used for all the simulations carried out in this body of work. It should be noted that Statz defined a non-linear model for C_{gd}, but when the FET is operated above the knee voltage (as in this work), the capacitance is approximately constant. The diode between the gate and drain is used to model breakdown between the gate and drain, while the diode between the gate and source models the forward conduction current.

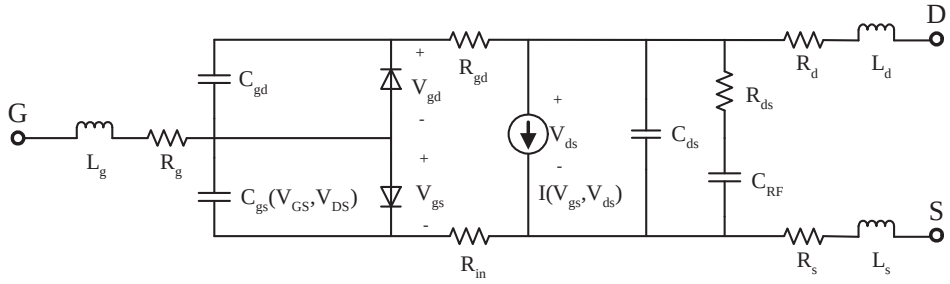


Figure C.1: The complete FET model circuit diagram used in simulations

The Statz model [15] has a convenient method for adjusting the drain current transfer characteristic, making it highly suitable for the work done in Sections 4.3 and 4.4. The Statz equation for the drain current is

$$I_d\left(V_{gs}\right) = \begin{cases} 0 & \text{when } V_{gs} < V_T \\ \frac{\beta(V_{gs}-V_T)^2}{1+b(V_{gs}-V_T)} & \text{when } V_T \leq V_{gs} < 0 \end{cases} \tag{C.1}$$

where I_d is the instantaneous drain current, V_T is the threshold voltage, β and b are parameters, and V_{gs} is the gate-to-source voltage. By varying b the softness of the transistor's turn-on can be modified, and, given a desired maximum drain current, β can easily be determined.

One of the concerns of a GaAs FET is rate dependent effects, a symptom of which is that the output conductance at RF and microwave frequencies is significantly higher

than indicated by the static i/v characteristics. A common way to account for this phenomena is to use a series RC network, comprising R_{ds} and C_{RF}. R_{ds} is chosen to achieve the required output conductance, and C_{RF} is very large (in the order of μF or more) [104]. In reality, the rate dependent behaviour cannot accurately be described by a simple RC network [105]. However, this simple RC network is commonly used (as shown in Figure C.1) for FET elements in microwave circuit simulators. This works well for class A and class AB amplifiers, but for class B and class C amplifiers where the FET is cut-off for a significant proportion of the cycle, this simple model can give rise to error. One recommendation for class B amplifiers is to set R_{ds} to a high value [106]. For class C amplifiers a yet higher value of R_{ds} would be expected. However, this is questionable, as for a significant portion of the cycle, the FET is conducting. Hence, a significant challenge in this type of amplifier, where the transistors operate over a wide range of biases and conduction angles, is determining the value of R_{ds} to be used when simulating practical GaAs transistors [106].

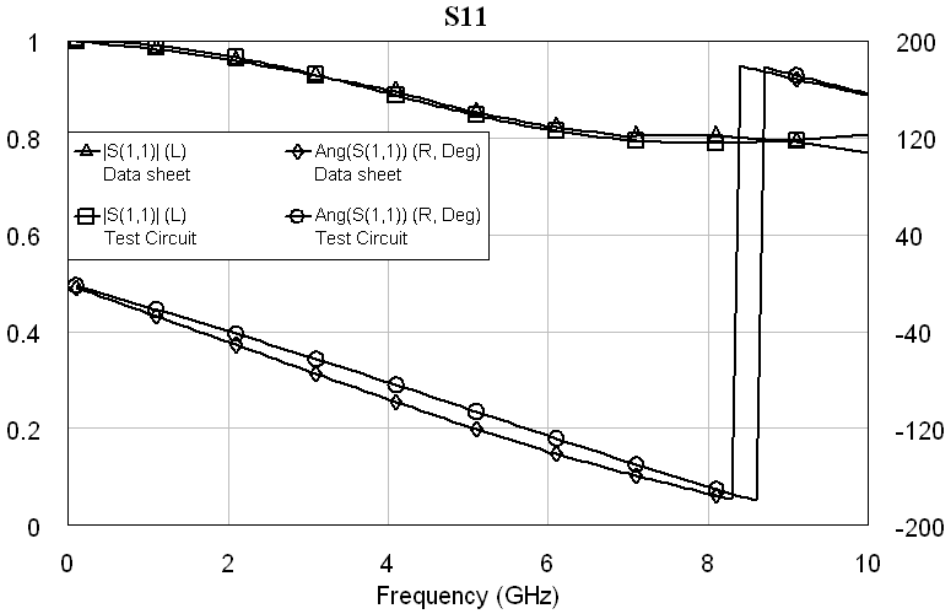
The Eudyna FLK017WF was the transistor used for the prototype amplifiers, as it has been used extensively in previous work [8, 9]; these parameter values were used for this work. A Eudyna FLC057WG was also used for the harmonic load modulation prototype. Based upon the DC IV characteristics, the FLC057WG has a size 3.3 times that of the FLK017WF. As such, its model parameters were determined by multiplying or dividing the FLK017WF parameters by 3.3 (where appropriate). The exception to this is the gate and drain inductances, which are divided by two (as the FLC057WG has twice as many gate and drain bond-wires), and the source inductance which is kept constant (in both FETs the source is bonded thorough the base of the transistor package). The parameters used are given in Table C.1. It should be noted that V_T and b are independent of transistor size, while β is proportional to it.

Parameter	FLK017WF	FLC057WG	Unit	Description
β	0.205	0.677	A/V^2	DC parameter relating to size
V_T	-2	-2	V	Threshold voltage
b	6	6		DC parameter relating to turn-on softness
α	2	2		Drain I/V knee parameter
λ	0	0		Output conductance parameter
τ	0.01	0.01	ns	Gate-drain time delay
V_{BR}	15	15	V	Gate junction breakdown voltage
IS	0.01	0.01	pA	Gate diode current parameter
N	1	1		Gate diode ideality factor
V_{BI}	0.85	0.85	V	Gate junction built-in voltage
FC	0.5	0.5		Gate depletion cap. linearisation parameter
R_{ds}	600	181	Ω	RF drain-source resistance
C_{RF}	1	3.3	μF	Cap. that determines R_{ds} break frequency
R_D	2	0.61	Ω	Drain resistance
R_G	0.6	0.18	Ω	Gate resistance, fixed part
R_S	1.7	0.52	Ω	Source resistance
R_{IN}	2.7	0.82	Ω	Intrinsic resistance
C_{GS0}	0.7	2.31	pF	Gate-source capacitance parameter
$\delta 1$	0.3	0.3		Capacitance parameter
$\delta 2$	0.2	0.2		Capacitance parameter
C_{DS}	0.34	1.122	pF	Drain-source capacitance
C_{GD}	0.021	0.069	pF	Gate-drain fixed capacitance
$TNOM$	26.85	26.85	°C	Temperature
R_{GD}	1	0.303	$m\Omega$	Gate-drain resistance
L_S	0.054	0.054	nH	Source inductance
L_G	0.6	0.3	nH	Gate inductance
L_D	0.4	0.2	nH	Drain inductance

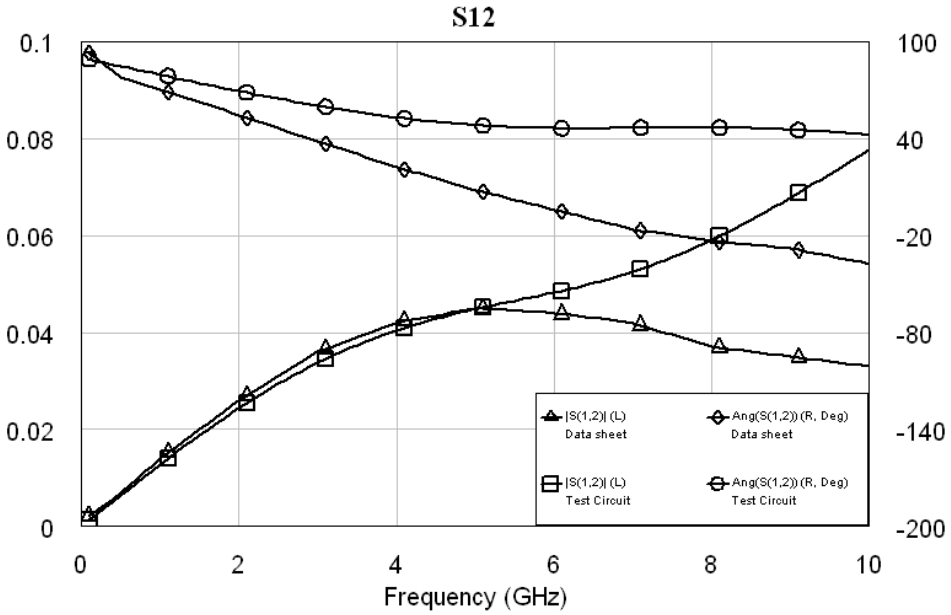
Table C.1: The Statz model parameters used

C.1 S-PARAMETERS

To confirm that the parameters given in Table C.1 accurately model the transistor, the data-sheet S-parameters were compared to those generated by simulation. The results for both transistors biased in class AB ($V_{B,M} = V_{B.P}$ = -0.7 V) are shown in Figures C.2a to C.3d. It can be seen that the S-parameters generated by the model (with parameter values given in Table C.1) are very close to the ones in the manufacturer's data file, although S_{12} deviates from the data-sheet values at high frequency levels. This indicates these parameters can be used in simulations with a high degree of confidence.

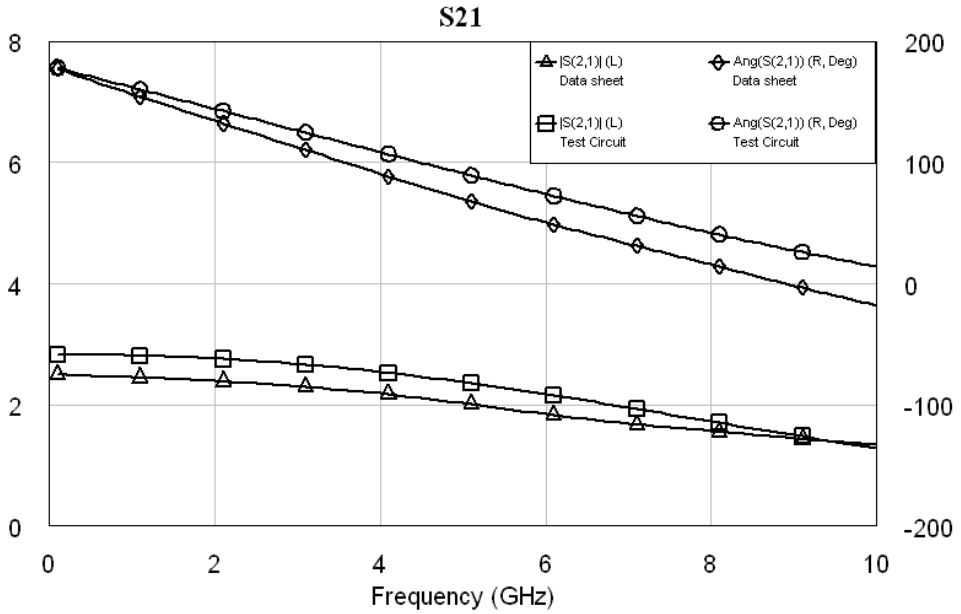


(a) S_{11} of the FLK017WF

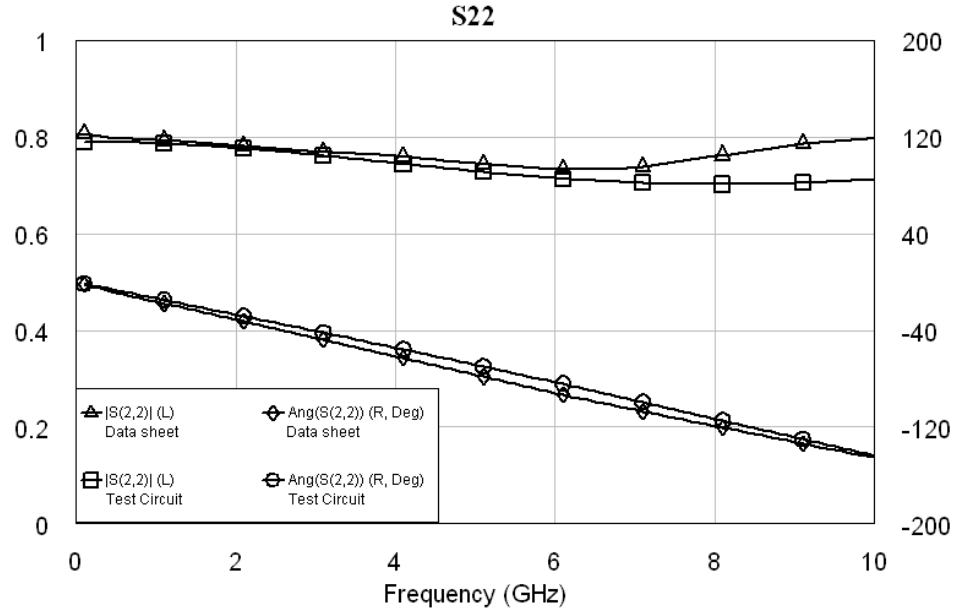


(b) S_{12} of the FLK017WF

Figure C.2: S-parameters of the FLK017WF

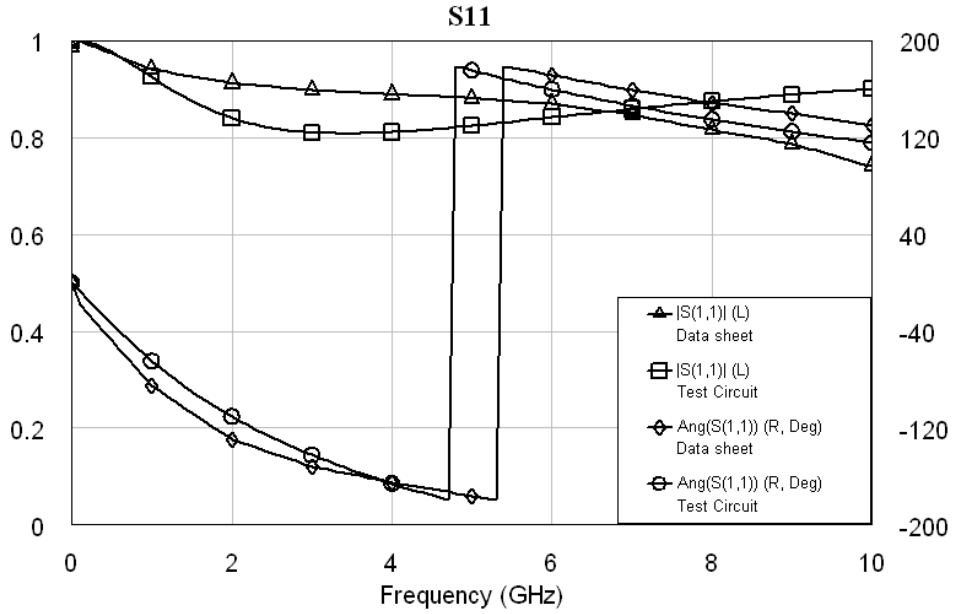


(c) S_{21} of the FLK017WF

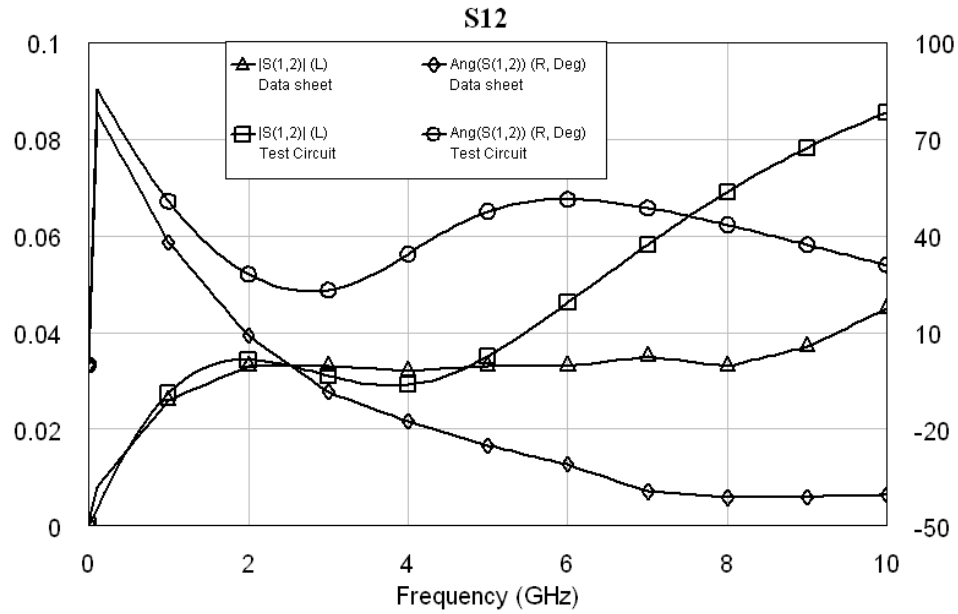


(d) S_{22} of the FLK017WF

Figure C.2: S-parameters of the FLK017WF

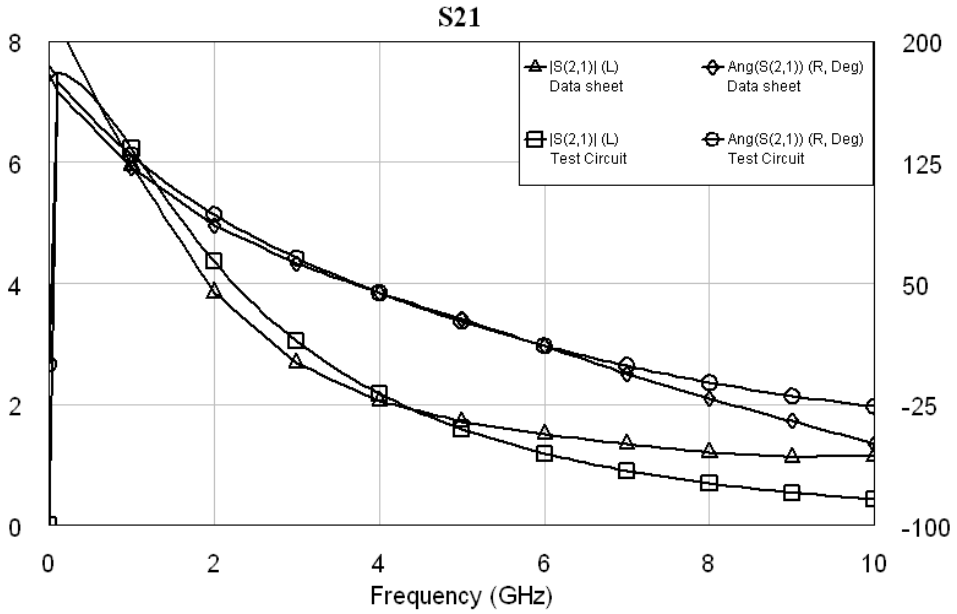


(a) S_{11} of the FLC057WG

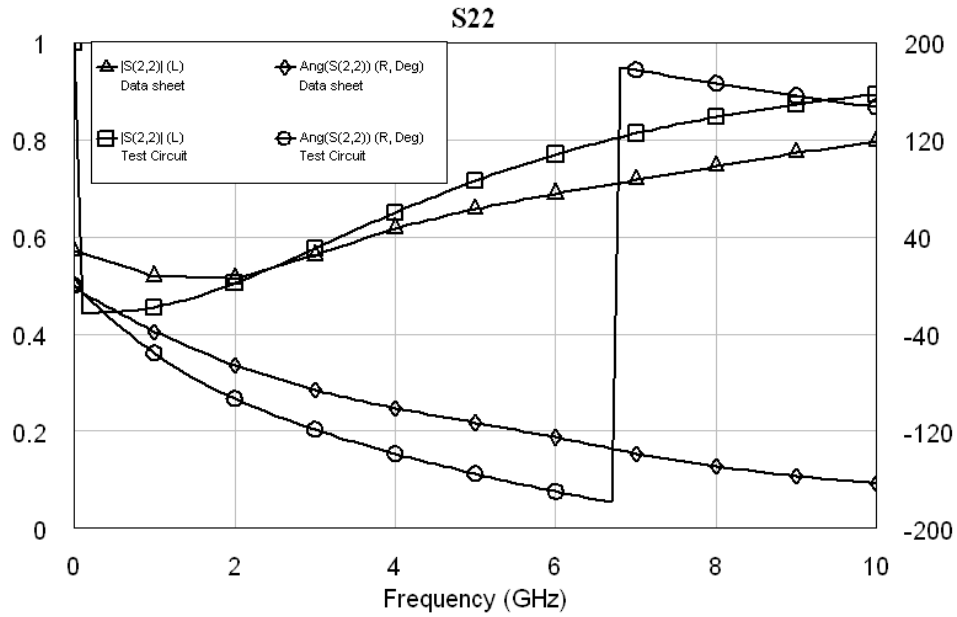


(b) S_{12} of the FLC057WG

Figure C.3: S-parameters of the FLC057WG



(c) S_{21} of the FLC057WG



(d) S_{22} of the FLC057WG

Figure C.3: S-parameters of the FLCK057WG

Appendix D

DETAILED CIRCUIT DIAGRAMS AND PROTOTYPE LAYOUTS

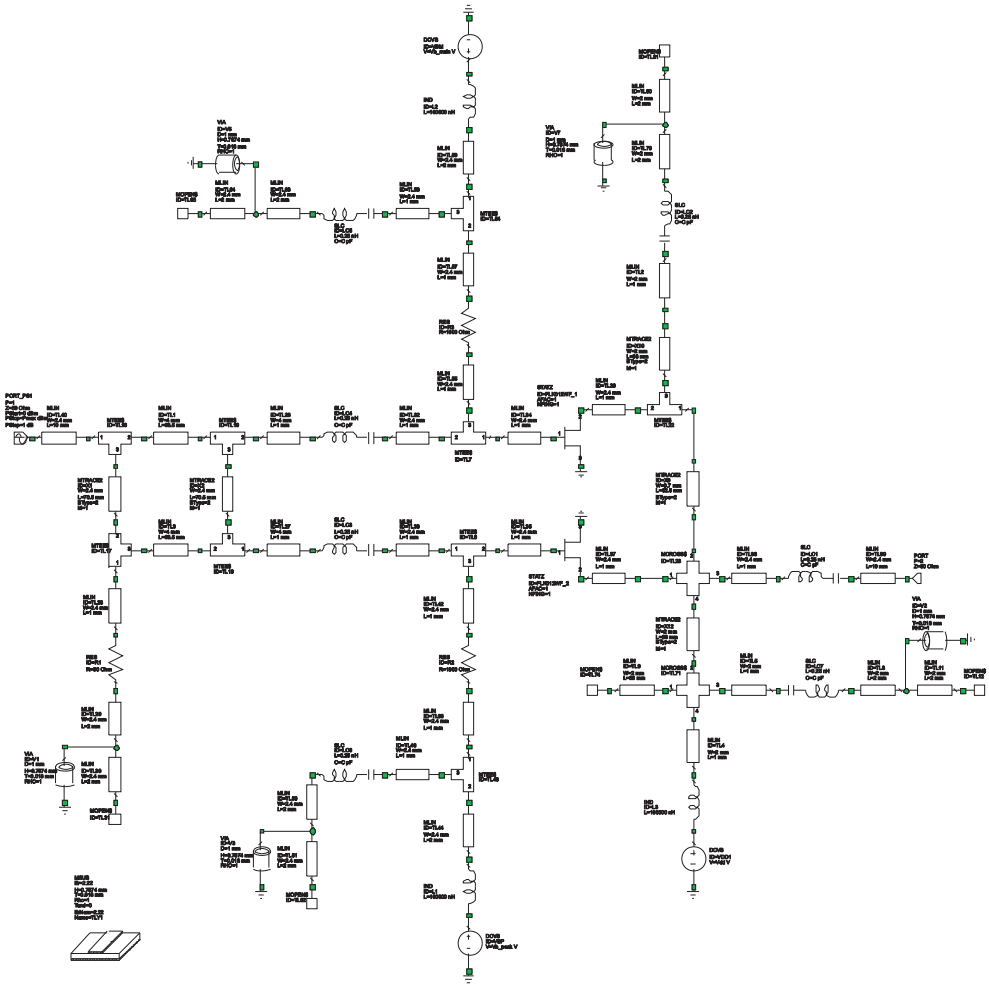


Figure D.1: Circuit diagram for the prototype used in the bias control research

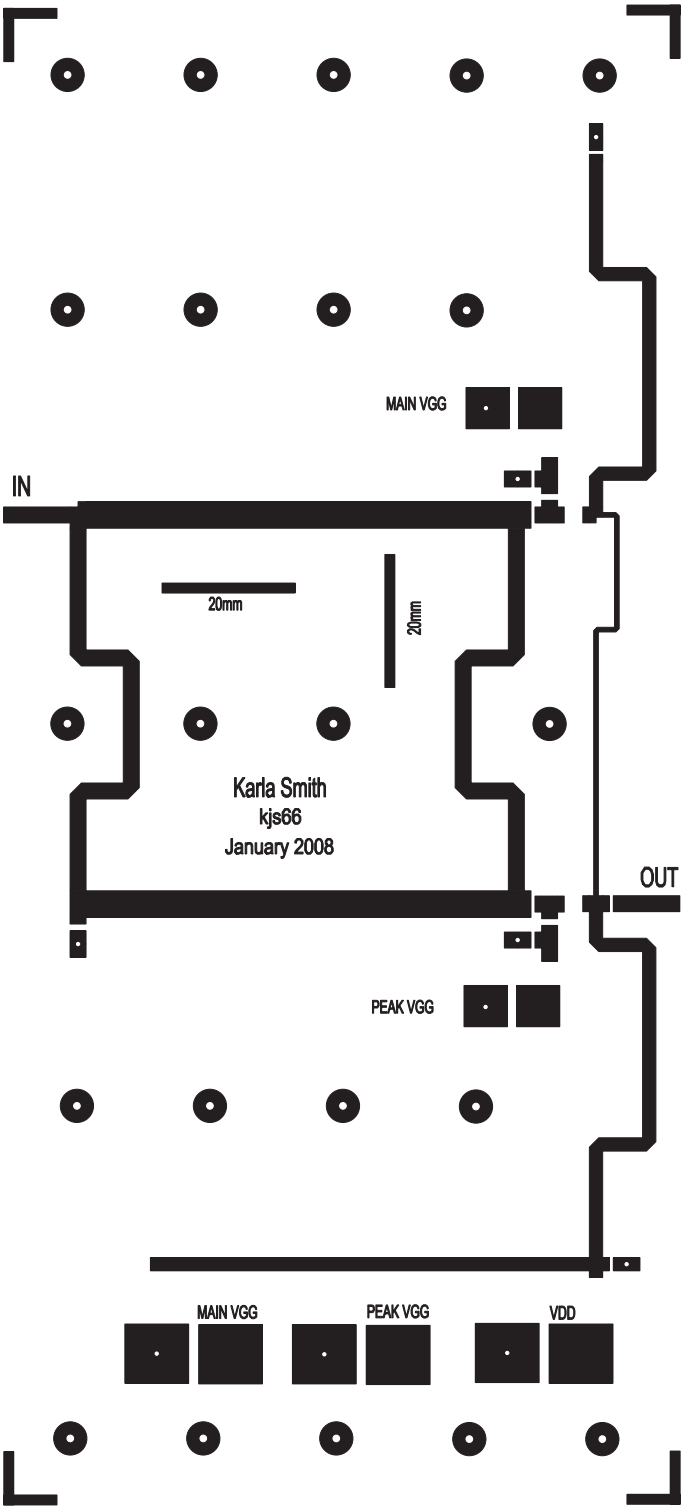


Figure D.2: Layout for the prototype circuit used in the bias control research

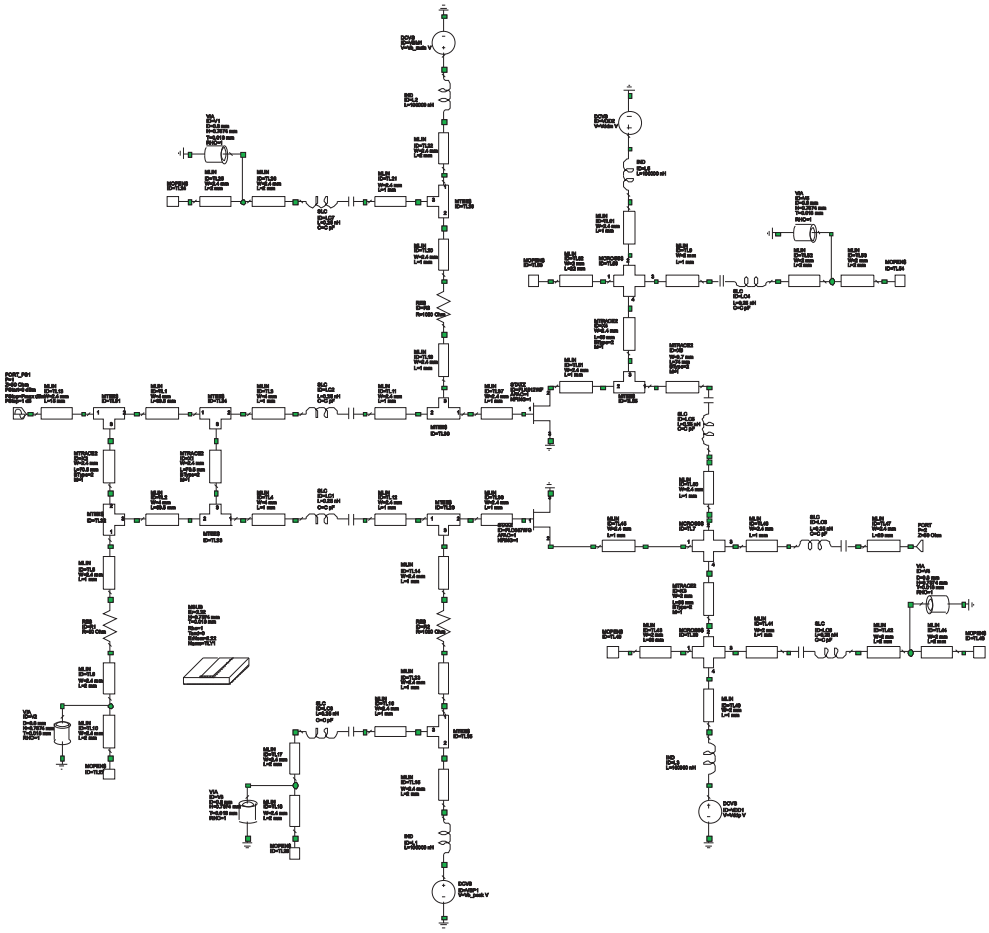


Figure D.3: Circuit diagram for the prototype used in the harmonic load modulation

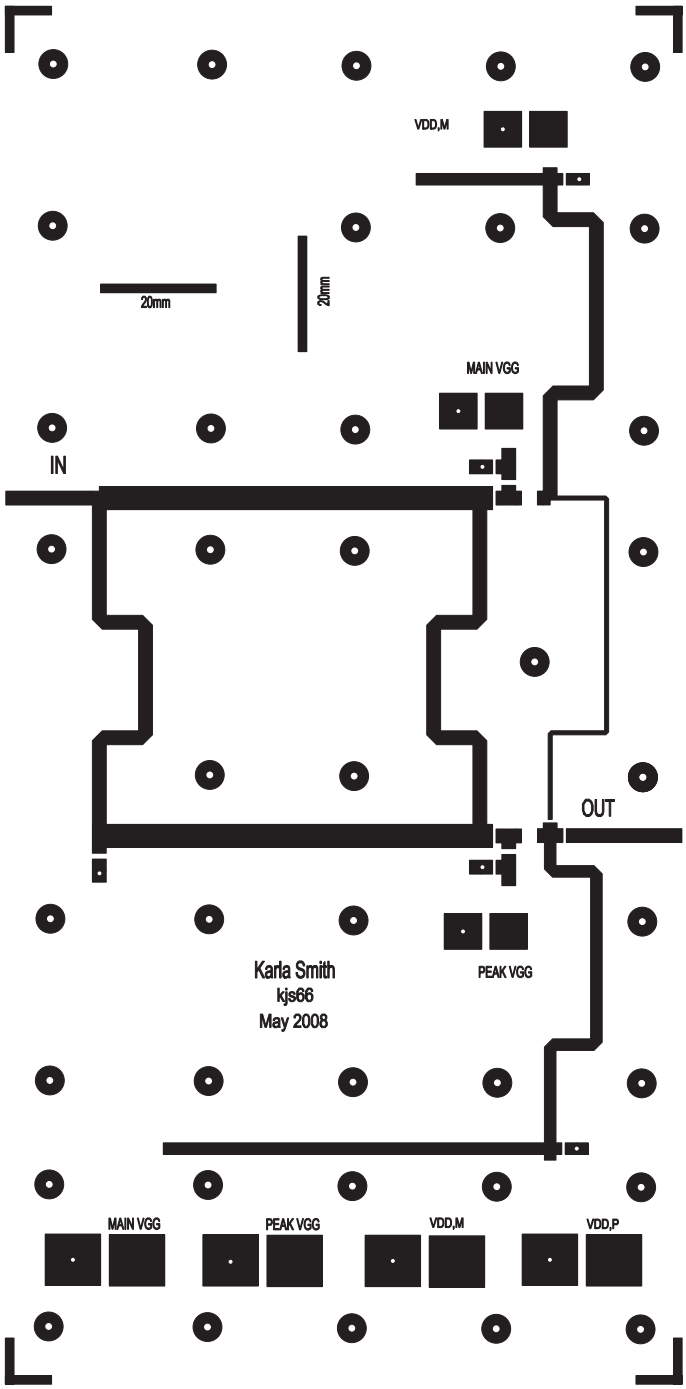
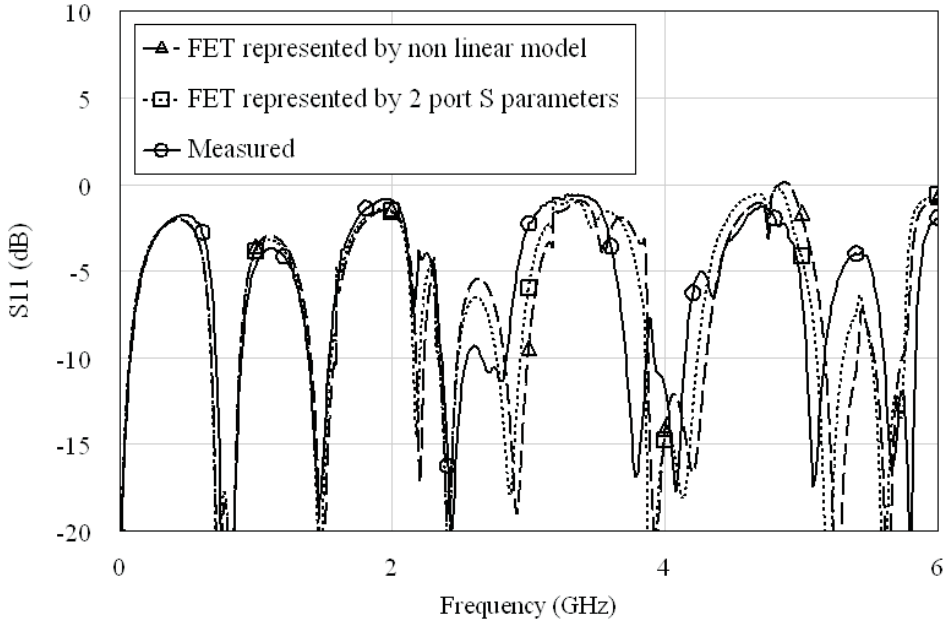


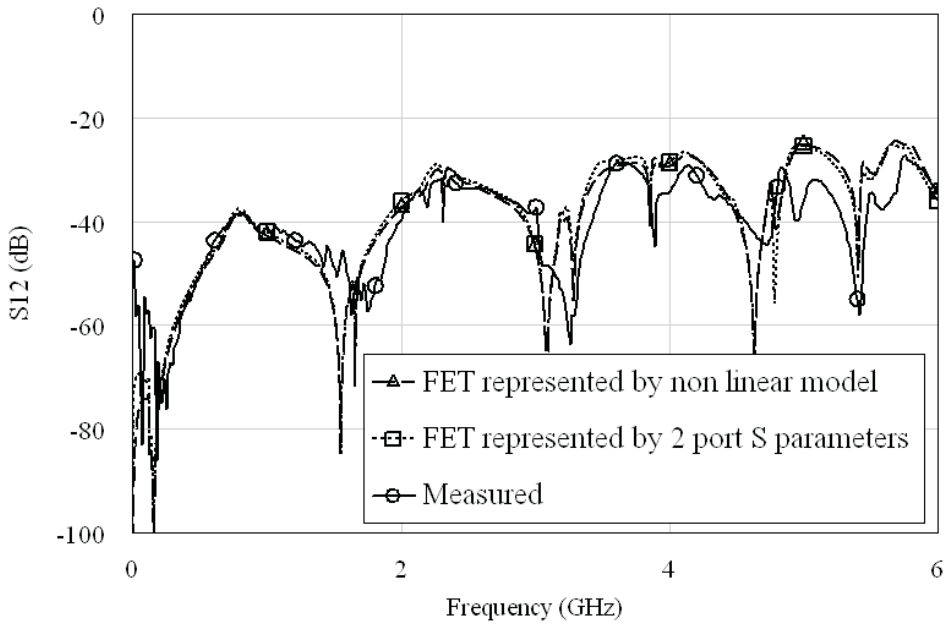
Figure D.4: Layout for the prototype circuit used in the harmonic load modulation

Appendix E

S-PARAMETERS OF PROTOTYPE DOHERTY AMPLIFIERS

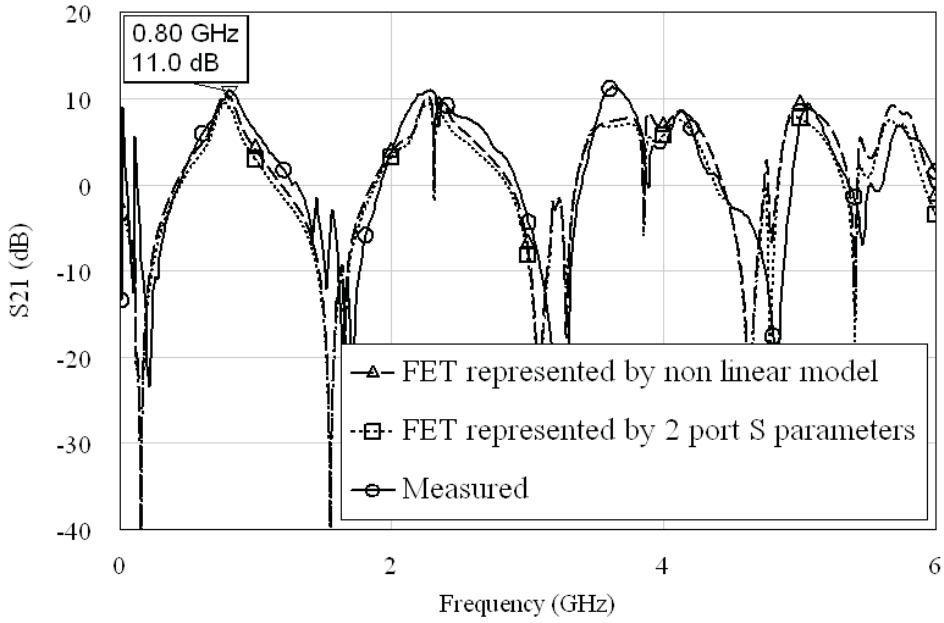


(a) S_{11} of the prototype bias controlled amplifier

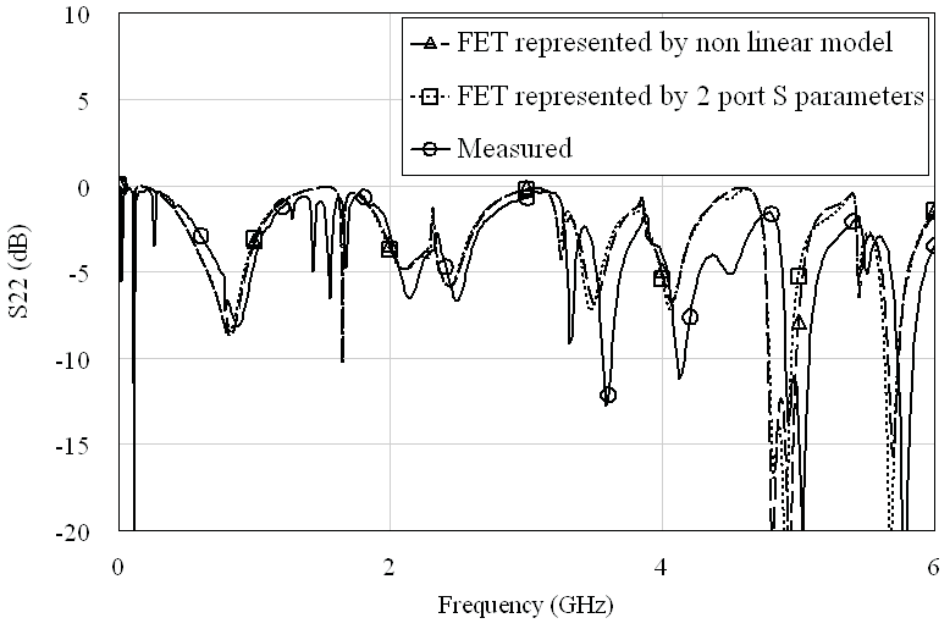


(b) S_{12} of the prototype bias controlled amplifier

Figure E.1: S-parameters of the prototype bias controlled amplifier

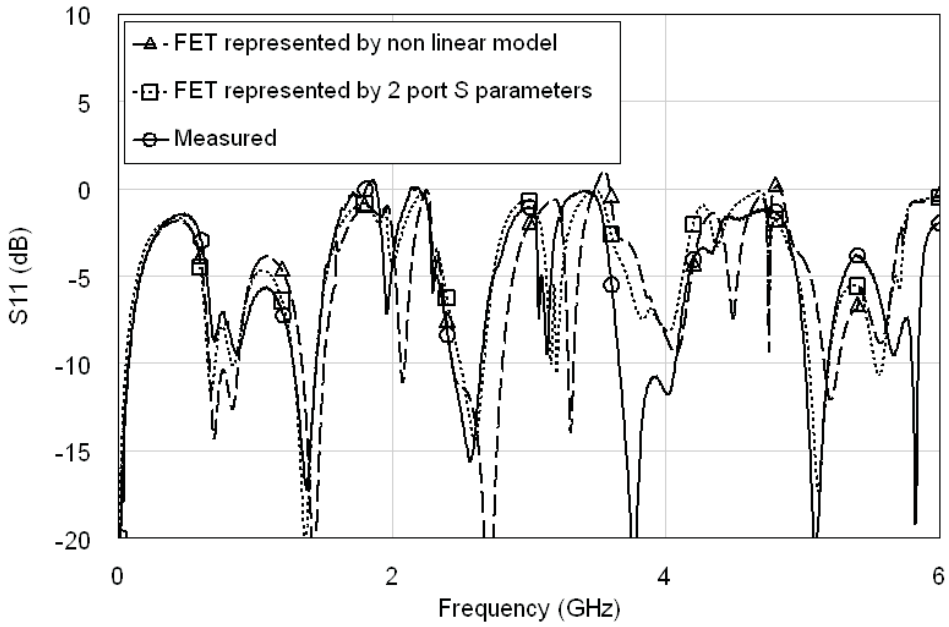


(c) S_{21} of the prototype bias controlled amplifier

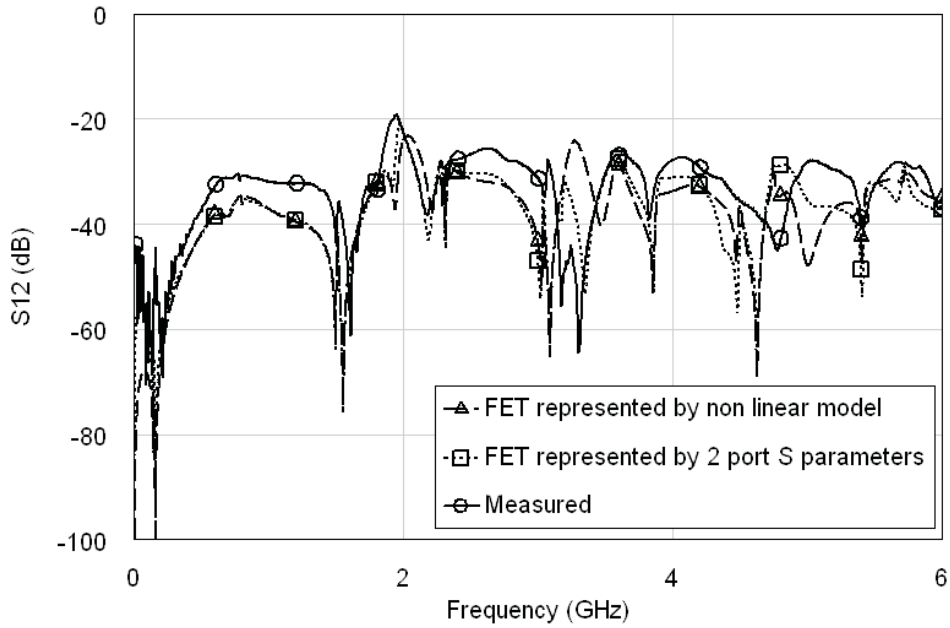


(d) S_{22} of the prototype bias controlled amplifier

Figure E.1: S-parameters of the prototype bias controlled amplifier

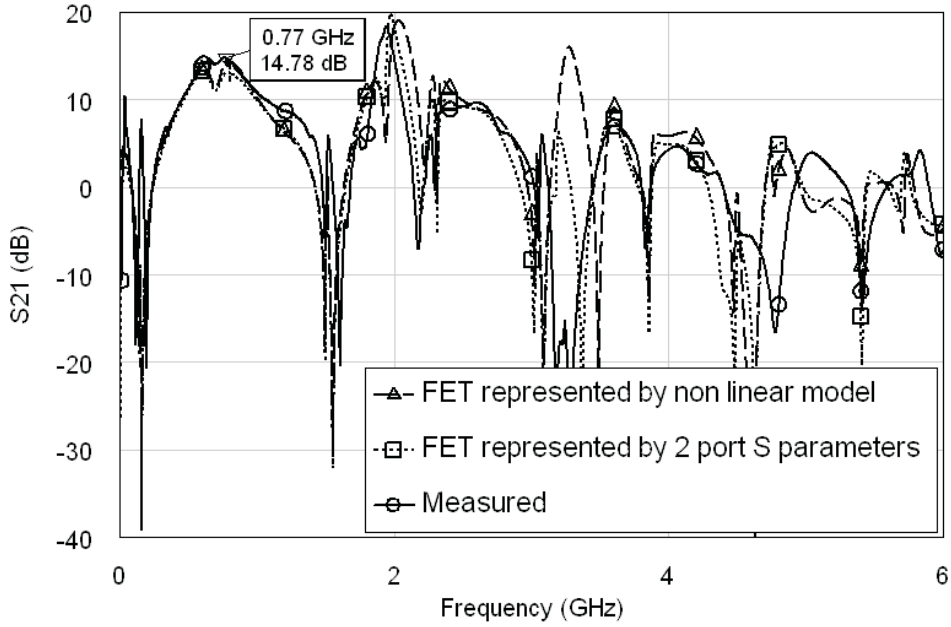


(a) S_{11} of the prototype harmonic load modulated amplifier

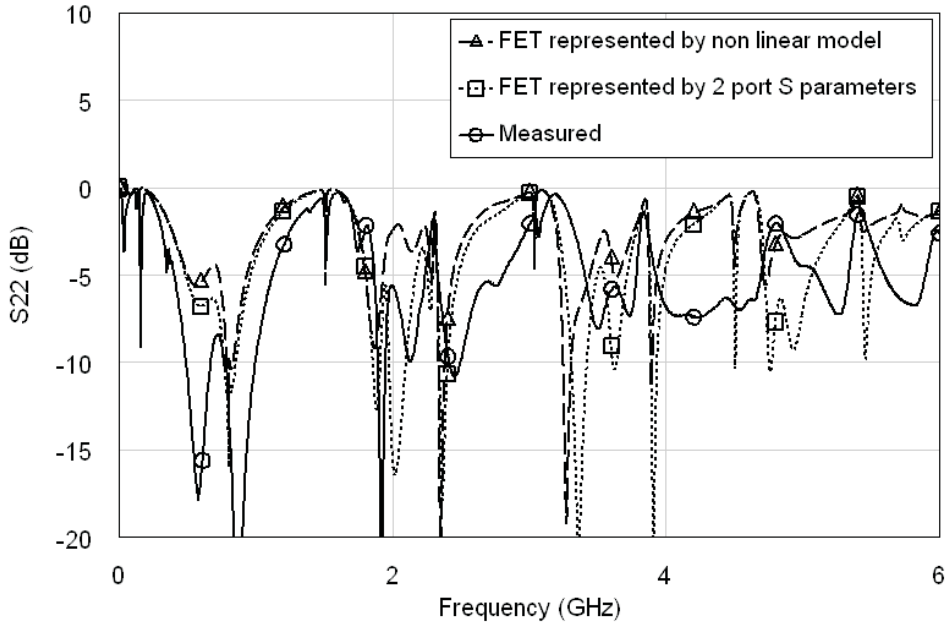


(b) S_{12} of the prototype harmonic load modulated amplifier

Figure E.2: S-parameters of the prototype harmonic load modulated amplifier



(c) S_{21} of the prototype harmonic load modulated amplifier



(d) S_{22} of the prototype harmonic load modulated amplifier

Figure E.2: S-parameters of the prototype harmonic load modulated amplifier

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