Adaptive digital polynomial predistortion linearisation for RF power amplifiers

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ABSTRACT

Development of linear modulation schemes has opened the way for spectrally efficient, high speed digital communication systems for voice and data applications. A trend has been to develop ultra wide and wide bandwidth modulation formats, which has meant feedback linearisation schemes (both analogue and digital) are no longer effective. This has in turn led to a number of approaches that involve predistorting the signal prior to amplification, with a characteristic that is the inverse to that of the power amplifier (PA). This thesis presents a polynomial based predistortion for linearisation of an RF PA. The predistortion characteristic is adaptive, using the LMS algorithm to minimise the mean squared error between output of the PA, and a scaled version of the baseband signal. This system can reduce third-order intermodulation by 40 dB when running in real time.

GLOSSARY

A

ACP (Adjacent ahannel power) Power level in the adjacent channel in dB.

ACPR (Adjacent channel power ratio) The ratio of power levels between a channel and its adjacent channel in dB.

ADC (Analogue to digital converter) Converts an analogue voltage level into a digital signal.

C

CORDIC (Co-ordinate rotation digital computer) Iterative hardware algorithm used to compute trigonometric functions.

D

DAC (Digital to analogue converter) Converts a digital sample into an analogue voltage level.

DSP (Digital signal processor) A micro-computer designed for digital signal processing applications.

F

FPGA (Field programmable gate array) Reconfigurable hardware device.

G

GUI (Graphical user interface) An graphical way to interact with the hardware.

I

IIR (Infinite impulse response) A filter which has an impulse response that is infinitely long.

IMD Intermodulation distortion.

J

JTAG (Joint test action group) General purpose programming and debug standard interface.

L

LAB (Logic array block) Stratix architectural block containing LEs RAM and DSP blocks.

LDMOS Lateral double diffuse metal oxide semiconductor.

LE (Logic element) Lookup table for implementing logic functionality in an FPGA.

LMS Least means squared adaption algorithm.

LO Local oscillator.

LUT (Look up table) Table mapping input value(s) to output value(s).

M

MLP (Multi-layer perceptron) Multi-layer architecture of a nueral net.

MMIC Monolithic microwave integrated circuit.

MSE Mean squared error.

MSPS Mega samples per second.

N

NN Neural net.

O

OFDM Orthogonal frequency division modulation.

P

PA (Power amplifier) Amplifies a modulated RF signal.

PLL (Phase-locked loop) Generates a clk signal that is phase locked to a reference signal.

Python An object oriented programming language.

R

RF Radio frequency.

RLS Recursive least squares.

RS232 (Recommended standard 232) Serial communications standard.

S

SFDR (Spurious free dynamic range) Level of spurious emisions produced by a device.

U

UART Universal asyncronous teceiver/transmitter.

V

VHDL (VHSIC hardware description language) A hardware description language often used in the programming of FPGA devices.

VHSIC (Very high speed integrated circuits) Program initiated by the US armed forces that led to development and advance of the CMOS semiconductor industry.

VSA (Vector signal analyser) Apparatus used to measure the spectrum of the output signals.

Chapter 1

INTRODUCTION

Typical modern radio applications use digital hardware and digital signal processing techniques at baseband in conjunction with analogue circuitry at radio frequency (RF) as shown in Figure 1.1, with the trend pushing the digital to analogue interface closer to the antenna. As more demands are placed on frequency spectrum, there is a need for increasing the spectral efficiency of radio systems. Distortion of the RF signal by the power amplifier (PA) is often the largest contributor to spectral inefficiency through the increase in out-of-band signal power. The non-linear transfer function of power amplifiers used in radio applications has been understood for some time, along with the distortion caused to the RF signal as it is amplified. The linearisation of the PA can be achieved using various methods in both the analogue and digital domains. Recently, predistortion linearisation systems have been developed that operate on the baseband signal. Many of these systems make use of an adaptive algorithm but few systems have been implemented.

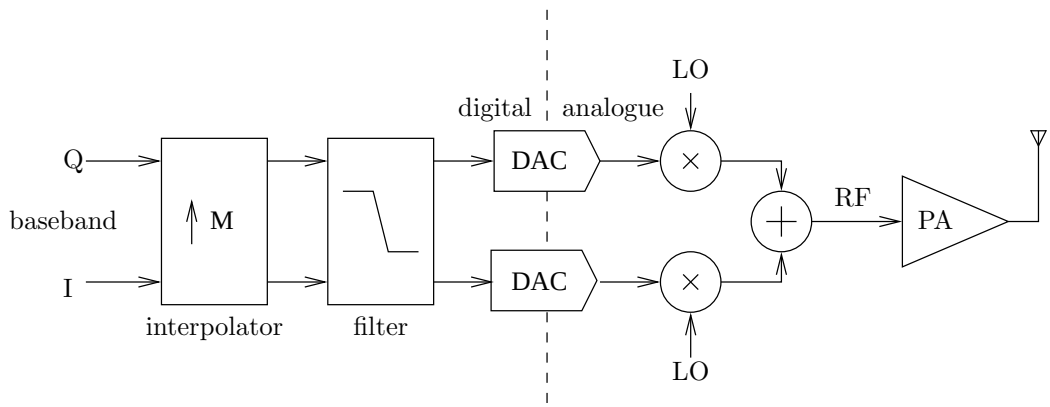

Figure 1.1: Radio architecture.

1.1 RESEARCH OBJECTIVES

The aim of this research is to design and implement a predistortion linearisation system that operates in real time. The implemented predistortion system is to be independent of RF frequency, modulation format and PA transfer characteristic so must adapt its transfer characteristic in real time. The design will be based on topologies and algorithms that have been previously designed and presented in the public domain.

1.2 THESIS OUTLINE

The principals of non-linearity are presented in Chapter 2, along with a brief overview of different methods of PA linearisation – feedback, feed-forward and predistortion. A literature review of predistortion linearisation, beginning with early analogue solutions is provided in Chapter 3. The proposed predistortion and adaption methods are used to design the high level architecture of the implementation. The modelling of the PA and design of the predistortion lineariser is discussed in Chapter 4. Simulation verification of this system is presented in Chapter 5. This provides a verification of the baseband power series predistorter topology working with an LMS adaption algorithm to minimise the error on the RF signal. The system implementation on a FPGA is discussed in Chapter 6. The implementation of the predistorter and adaption algorithm is discussed, along with methods of control and data acquisition. System verification and results are discussed in Chapter 7. The implemented predistortion lineariser runs in real time on a hardware development platform.

1.3 CONTRIBUTION

The design and simulated performance of the adaptive polynomial predistortion linearisation system has been presented at the Electronics New Zealand Conference 2006 [1].

Chapter 2

POWER AMPLIFIER NON-LINEARITIES

This chapter provides a background to power amplifier (PA) non-linearities and how these manifest themselves in a communications system. The traditional feedback and feed-forward linearisation methods will be briefly discussed.

2.1 NON-LINEARITY

In order to discuss the properties and analysis of non-linear devices, non-linearity must first be defined. To simplify discussion in this chapter, the definition of a circuit is extended to include single elements. A linear circuit has a response that follows the principle of superposition. Specifically, a linear combination of responses is also a response. If a linear circuit described by

$$y = f(x) \tag{2.1}$$

is excited individually with x_1 and x_2 it has responses,

$$y_1 = f(x_1) \tag{2.2}$$

$$y_2 = f(x_2). \tag{2.3}$$

The response of the circuit when excited with a complex excitation can be found by,

$$f(k \cdot x_1) = k \cdot y_1 \tag{2.4}$$

$$f(x_1 + x_2) = y_1 + y_2 \tag{2.5}$$

$$f(A \cdot x_1 + B \cdot x_2) = A \cdot y_1 + B \cdot y_2. \tag{2.6}$$

where A, B and k are constants. This principle can be extended to cover as many excitations as is desired.

All circuits exhibit some non-linear behaviour although adequate analysis can often be performed under the assumption the circuit response is linear and using linear analysis techniques. Linear analysis techniques can be used when the excitation of the circuit is sufficiently small for that circuit to have a linear response. A circuit can be classified as strongly non-linear, weakly non-linear, or quasi-linear, although these categories are not formally defined. It is generally accepted that a weakly non-linear circuit can be accurately modelled using power series analysis [2] which is described in Section 2.1.2.

2.1.1 Non-linear effects

The most significant effects of non-linear circuits are observed as 'frequency generation' where frequency components not in the input are present on the output. These phenomena are given a range of names but are often manifestations of the same non-linear effects [2].

The following sections will examine non-linear effects common in communication systems, in reference to Figure 2.1. Effects that limit system performance such as harmonic distortion, intermodulation distortion and amplitude to phase conversion will be focused on. Consider the non-linear circuit in Figure 2.1 in which the source impedance is zero. The response of this circuit can be found easily from a Taylor series expansion,

$$v_{\text{out}} = f_{\text{nl}}(v_{\text{in}}) = a_1 v_{\text{in}} + a_2 v_{\text{in}}^2 + a_3 v_{\text{in}}^3 \tag{2.7}$$

where a_1, a_2 and a_3 are real constants.

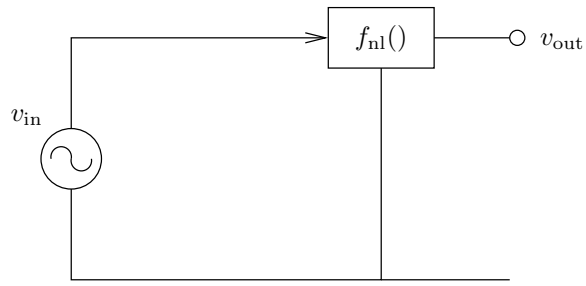

Figure 2.1: Non-linear circuit element with voltage source excitation.

Harmonic generation is one of the most common and obvious effects of a non-linear circuit. The harmonic frequency components of an input frequency are any integer multiples of the input frequency. Harmonic generation causes very few problems with small bandwidth receivers, but in the case of transmitters may cause frequency components that interfere with other systems. Consider a system described as,

$$v_{\mathrm{out}} = a_1 v_{\mathrm{in}}(t) + a_2 v_{\mathrm{in}}(t)^2 + a_3 v_{\mathrm{in}}(t)^3 + a_4 v_{\mathrm{in}}(t)^4 + \cdots + a_{\mathrm{n}} v_{\mathrm{in}}(t)^{\mathrm{n}}, \tag{2.8}$$

where a_{n} are real coefficients. To simplify the analysis all coefficients of order greater than three are set equal to zero to truncate the series,

$$v_{\mathrm{out}} = a_1 v_{\mathrm{in}}(t) + a_2 v_{\mathrm{in}}(t)^2 + a_3 v_{\mathrm{in}}(t)^3, \tag{2.9}$$

although the derivation can be shown for any number of coefficients. To investigate the effects of harmonic distortion, consider a single tone excitation,

$$v_{\mathrm{in}} = A \cdot \cos(\omega t). \tag{2.10}$$

By substituting Equation 2.10 into Equation 2.9 an expression for v_{out} in terms of the three components of a series expansion can be found,

$$
\begin{aligned}
v_{\text{out}} &= a_1 A\cos(\omega t) + a_2(A\cos(\omega t))^2 + a_3(A\cos(\omega t))^3 \\
&= \frac{a_2}{2} + \\
&\quad [a_1 + \frac{3}{4}a_3A^2]A \cdot \cos(\omega t) + \\
&\quad \frac{1}{2}a_2A^2\cos(2\omega t) + \\
&\quad \frac{1}{4}a_3A^3\cos(3\omega t).
\end{aligned} \tag{2.11}
$$

The response consists of a DC term and frequencies that are multiples of the input frequency. As is evident in Figure 2.2, the unwanted frequency components introduced by harmonic distortion can easily be removed by filters, as they are widely spaced.

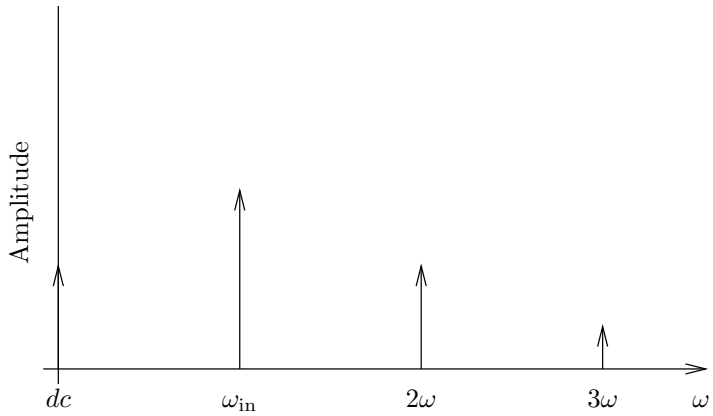

Figure 2.2: Harmonic distortion spectrum.

Intermodulation is observed as frequency components that are a linear combination of two or more of the excitation frequencies. Intermodulation components can pose serious problems when generated in either an amplifier or receiver as they can interfere with or be mistaken for the desired signal [2]. Consider again the circuit in Figure 2.1, but with a two-tone excitation,

$$v_{\text{in}} = V_1\cos(\omega_1 t) + V_2\cos(\omega_2 t). \tag{2.12}$$

By substituting Equation 2.12 into Equation 2.7 the three response terms can be evaluated.

$$
\begin{aligned}
v_{\mathrm{a}_1}(t) &= a_1 v_{\mathrm{in}}(t) \\
&= a_1 V_1 \cos(\omega_1 t) + a_1 V_2 \cos(\omega_2 t)
\end{aligned} \tag{2.13}
$$

$$
\begin{aligned}
v_{\mathrm{a}_2}(t) &= a_2 v_{\mathrm{in}}(t)^2 \\
&= \frac{1}{2} a_2 \Big\{ V_1^2 + V_2^2 + V_1^2 \cos(2\omega_1 t) + V_2^2 \cos(2\omega_2 t) \\
&\quad + 2V_1 V_2 [\cos((\omega_1 + \omega_2)t) + \cos((\omega_1 - \omega_2)t)] \Big\}
\end{aligned} \tag{2.14}
$$

$$
\begin{aligned}
v_{\mathrm{a}_3}(t) &= a_3 v_{\mathrm{in}}(t)^3 \\
&= \frac{1}{2} a_3 \Big\{ V_1^3 \cos(3\omega_1 t) + V_2^3 \cos(3\omega_2 t) \\
&\quad + 3V_1^2 V_2 \Big[\cos((2\omega_1 + \omega_2)t) + \cos((2\omega_1 - \omega_2)t) \Big] \\
&\quad + 3V_1 V_2^2 \Big[\cos((2\omega_2 + \omega_1)t) + \cos((2\omega_2 - \omega_1)t) \Big] \\
&\quad + 3(V_1^3 + 2V_1 V_2^2) \cos(\omega_1 t) + 3(V_2^3 + 2V_1 V_2^2) \cos(\omega_2 t) \Big\}.
\end{aligned} \tag{2.15}
$$

Collecting the terms gives the total response,

$$
\begin{aligned}
v_{\text{out}} &= v_{\text{a1}} + v_{\text{a2}} + v_{\text{a3}} \\
&= \frac{1}{2}a_2(V_1^2 + V_2^2) + \\
&\quad (a_1V_1 + \frac{3}{2}a_3(V_1^3 + 2V_1V_2^2))\cos(\omega_1 t) + \\
&\quad (a_1V_2 + \frac{3}{2}a_3(V_2^3 + 2V_2V_1^2))\cos(\omega_2 t) + \\
&\quad a_2V_1V_2\cos((\omega_1 - \omega_2)t) + \\
&\quad a_2V_1V_2\cos((\omega_1 + \omega_2)t) + \\
&\quad \frac{1}{2}a_2V_1^2\cos(2\omega_1 t) + \\
&\quad \frac{1}{2}a_2V_2^2\cos(2\omega_2 t) + \\
&\quad \frac{1}{2}a_3V_1^3\cos(3\omega_1 t) + \\
&\quad \frac{1}{2}a_3V_2^3\cos(3\omega_2 t) + \\
&\quad \frac{3}{2}a_3V_1^2V_2\cos((2\omega_1 - \omega_2)t) + \\
&\quad \frac{3}{2}a_3V_1^2V_2\cos((2\omega_1 + \omega_2)t) + \\
&\quad \frac{3}{2}a_3V_1V_2^2\cos((2\omega_2 - \omega_1)t) + \\
&\quad \frac{3}{2}a_3V_1V_2^2\cos((2\omega_2 + \omega_1)t). \qquad (2.16)
\end{aligned}
$$

This power series can be evaluated to any degree of accuracy, although the analysis quickly becomes mathematically tedious. Note also that all the generated frequencies are a linear combination of the excitation frequencies, so the response frequencies from a two-tone excitation will follow,

$$\omega_{\text{m,n}} = M\omega_1 \pm N\omega_2 \qquad (2.17)$$

where M and N are real integers [2]. For $\omega_{\text{m,n}}$ to be distinct, ω_1 and ω_2 must be non-commensurate (the ratio of mixing frequencies is not a rational number). As can be seen in Figure 2.3, the intermodulation distortion (IMD) products are close to the fundamental. To remove these by filtering would require an unrealisably high

order filter to get a transition between the passband and stopband to filter out the intermodulation products and let the fundamental frequencies pass. Hence other methods of removing these distortion components must be investigated.

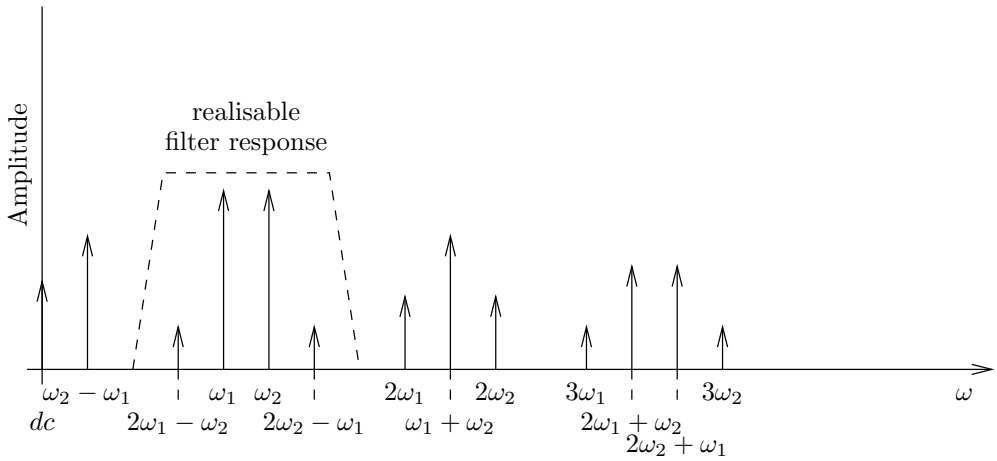

Figure 2.3: Third-order IMD products with bandpass filter response.

If an amplifier is driven by a large and a small signal, the large signal can drive the amplifier into saturation. If the amplifier is driven into saturation, the gain for the small excitation signal is also decreased. This phenomena is called desensitisation. Saturation occurs when the coefficient of the cubic term is negative (the term does not increase as the excitation increases).

Amplitude to phase distortion is a change in the amplitude of an excitation signal causing a phase change on the output. This can cause large problems in a system where the phase is important [2], such as modern modulation schemes where both amplitude and phase carry information such as quadrature amplitude modulation (QAM) [3][4].

2.1.2 Analysis

The process of analysing non-linear circuits is complicated by the differing degrees of non-linearity, as different analysis techniques are more accurate for different degrees of non-linearity. Power series analysis will be the focus of this section as it is accurate for weakly driven, weakly non-linear circuits.

Low frequency analysis of non-linear circuits can be performed using time-domain analysis. Basic circuit theory can be used to derive time-domain differential equations that describe a non-linear circuit which can be solved numerically. This method has the following characteristics:

- Time-domain analysis can be used for lumped or distributed models.
- Frequency domain properties such as impedances are not catered for.
- It is difficult to analyse non-commensurate excitations.

Consider a weakly non-linear circuit with multiple non-commensurate small-signal excitations. The non-linearities present typically have a negligible effect on the linear response of the circuit. Thus we can model a non-linear system as shown in Figure 2.4.

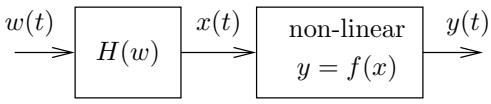

Figure 2.4: Non-linear system model.

The transfer function $H(w)$ is linear, whereas $f(x)$ is non-linear and has the form of a power series,

$$y(t) = f(x(t)) = \sum_{\mathrm{n}=1}^{\mathrm{N}} a_{\mathrm{n}} x^{\mathrm{n}}. \tag{2.18}$$

For practicality, the series must be restricted; values of N = 3 – 5 give results accurate enough as the third and fifth order terms are the primary interference components in a power amplifier. In order to apply power series analysis techniques, $w(t)$ and $x(t)$ must be small-signal current or voltage, with $f(x)$ being single valued and weakly non-linear.

For example Figure 2.5 shows a simplified FET equivalent circuit model, with an input linear transfer function $H(\omega)$, where $V(\omega)$ and $V_{\mathrm{s}}(\omega)$ are the frequency domain equivalents of $v(t)$ and $v_{\mathrm{s}}(t)$.

$$H(\omega) = \frac{V(\omega)}{V_{\mathrm{s}}(\omega)} = \frac{1}{(R_{\mathrm{s}} + R_{\mathrm{i}})C_{\mathrm{i}} j\omega - L_{\mathrm{s}} C_{\mathrm{i}} \omega^2 + 1} \tag{2.19}$$

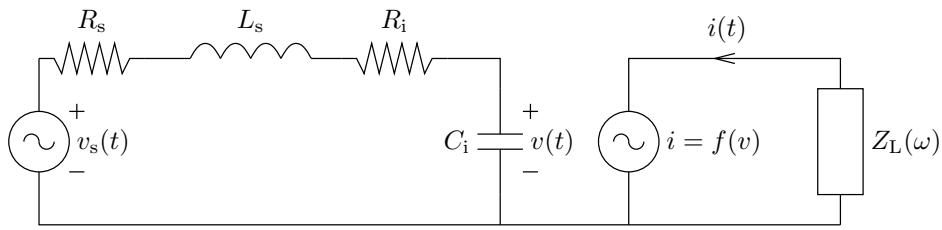

Figure 2.5: Simplified model of a FET, with linear and non-linear stages.

The only non-linearity in the circuit is the transfer function $i = f(v)$ between gate voltage $v(t)$ and drain current $i(t)$, which can be found by power series expansion of the large-signal drain current,

$$\begin{aligned} f(v) &= F(V_{g,0} + v) - F(V_{g,0}) \\ &= \left.\frac{dF(V)}{dV}\right|_{V=V_{g,0}} v + \frac{1}{2}\left.\frac{d^2 f(V)}{dV^2}\right|_{V=V_{g,0}} v^2 \\ &\quad + \frac{1}{6}\left.\frac{d^3 F(V)}{dV^3}\right|_{V=V_{g,0}} v^3 + \cdots \end{aligned} \tag{2.20}$$

where $V_{g,0}$ is the DC bias voltage across the capacitor.

Frequency domain analysis provides the frequency information desired. Frequency domain analysis is also better suited to multiple non-commensurate excitations as is common. Excitations are typically of the form,

$$\begin{aligned} v_s(t) &= \frac{1}{2}\sum_{q=1}^{Q}\left[V_{s,q}^{*}\exp(j\omega_q t) + V_{s,q}\exp(j\omega_q t)\right] \\ &= \frac{1}{2}\sum_{\substack{q=-Q,\\ q\neq 0}}^{Q} V_{s,q}\exp(j\omega_q t), \end{aligned} \tag{2.21}$$

where $\omega_{-q} = -\omega, V_{s,-q} = V_{s,q}^{*}$ and $H(\omega_{-q}) = H^{*}(\omega_q)$. This assumes no DC component which is normal for microwave excitations. Nonlinearities can produce DC components, however, this is rarely the case with small-signal driven weakly non-linear circuits [2] which are of importance here. Given the excitation of Equation 2.21, the response of the linear section of Figure 2.5 can be expressed,

$$v(t) = \frac{1}{2}\sum_{\mathrm{q}=-\mathrm{Q}}^{\mathrm{Q}} V_{\mathrm{s,q}} H(\omega_{\mathrm{q}}) \exp(j\omega_{\mathrm{q}} t) \tag{2.22}$$

By substituting Equation 2.22 into Equation 2.18 and solving for $a_{\mathrm{n}} v^{\mathrm{n}}(t)$ the entire response $i(t)$ can be found,

$$i(t) = \sum_{\mathrm{n}=1}^{\mathrm{N}} a_{\mathrm{n}} v^{\mathrm{n}}(t). \tag{2.23}$$

where

$$\begin{aligned} a_{\mathrm{n}} v^{\mathrm{n}}(t) &= a_{\mathrm{n}} \left[\frac{1}{2} \sum_{\mathrm{q}=-\mathrm{Q}}^{\mathrm{Q}} V_{\mathrm{s,q}} H(\omega_{\mathrm{q}} t) \right]^{\mathrm{n}} \\ &= \frac{a_{\mathrm{n}}}{2^{\mathrm{n}}} \sum_{\mathrm{q1}=-\mathrm{Q}}^{\mathrm{Q}} \sum_{\mathrm{q2}=-\mathrm{Q}}^{\mathrm{Q}} \cdots \sum_{\mathrm{qn}=-\mathrm{Q}}^{\mathrm{Q}} \\ &\quad V_{\mathrm{s,q1}} V_{\mathrm{s,q2}} \cdots V_{\mathrm{s,qn}} H(\omega_{\mathrm{q1}}) H(\omega_{\mathrm{q2}}) \cdots H(\omega_{\mathrm{qn}}) \\ &\quad \exp[j(\omega_{\mathrm{q1}} + \omega_{\mathrm{q2}} + \cdots \omega_{\mathrm{qn}})t] \end{aligned} \tag{2.24}$$

It is evident that a large number of new frequencies are generated by the non-linearities, with n^{th} degree terms and Q excitation frequencies. The total response of the system is the sum of all possible linear combinations of Q excitation frequencies. Some of the lower order intermodulation terms are shown in Figure 2.6.

An nth order mixing frequency is one that arises from the sum of n excitation frequencies. The situation of most concern during system design is a two-tone excitation (Q = 2) and N $\leq$ 3 [2]. It is impossible to determine the order of a mixing product from its frequency, as the particular frequency may be obtained from many mixing frequencies as shown in Equation 2.25

$$\begin{aligned} 2\omega_1 - \omega_2 &= \omega_1 + \omega_1 + \omega_2 (3^{\mathrm{rd}}) \\ &= \omega_1 + \omega_1 + \omega_1 - \omega_1 + \omega_2 (5^{\mathrm{th}}). \end{aligned} \tag{2.25}$$

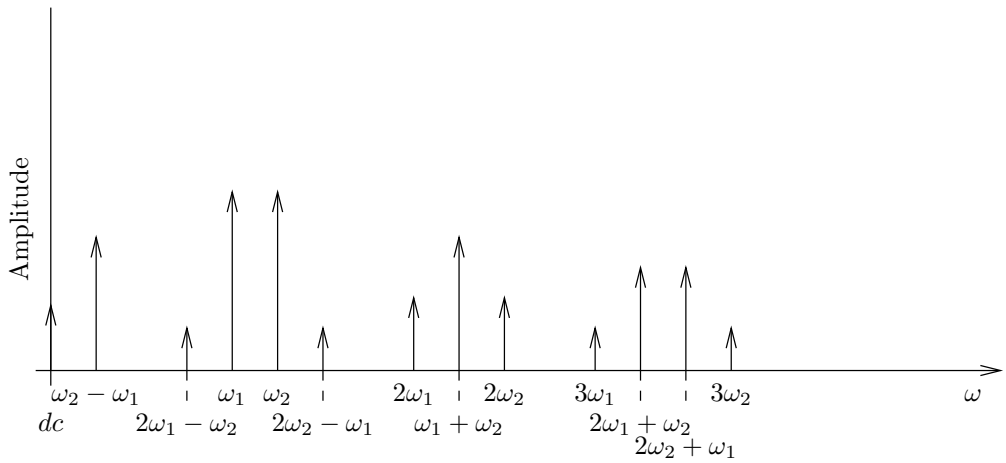

Figure 2.6: Frequency spectrum of the lower intermodulation frequencies produced by exciting a non-linear circuit with a two-tone signal.

To demonstrate power series analysis, consider a two-tone excitation. The second order component of the response $i_2(t)$ can be found,

$$\begin{aligned} i_2(t) &= a_2 v^2(t) \\ &= \frac{a_2}{4} \sum_{\mathrm{q1}=-2}^{2} \sum_{\mathrm{q2}=-1}^{2} V_{\mathrm{s,q1}} V_{\mathrm{s,q2}} H(\omega_{\mathrm{q1}}) H(\omega_{\mathrm{q2}}) \cdot \exp[j(\omega_{\mathrm{q1}} + \omega_{\mathrm{q2}})t]. \end{aligned} \tag{2.26}$$

These terms include harmonics of the input frequencies, repeated terms and DC terms as well as intermodulation terms. All the terms appear in complex conjugate pairs and can therefore be expressed as shown for $\omega_1 - \omega_2$,

$$\begin{aligned} i_2'(t) &= a_2 v^2(t)\Big|_{\omega_1 - \omega_2} \\ &= a_2 |V_{\mathrm{s},1} V_{\mathrm{s},2} H(\omega_1) H(\omega_2)| \cos[(\omega_1 - \omega_2)t]. \end{aligned} \tag{2.27}$$

Similarly, the third degree term $i_3(t)$ can be found,

$$\begin{aligned} i_3(t) &= a_3 v^3(t) \\ &= \frac{a_3}{8} \sum_{\mathrm{q1}=-2}^{2} \sum_{\mathrm{q2}=-2}^{2} \sum_{\mathrm{q3}=-2}^{2} V_{\mathrm{s,q1}} V_{\mathrm{s,q2}} V_{\mathrm{s,q3}} H(\omega_{\mathrm{q1}}) H(\omega_{\mathrm{q2}}) H(\omega_{\mathrm{q3}}) \\ &\quad \cdot \exp[j(\omega_{\mathrm{q1}} + \omega_{\mathrm{q2}} \omega_{\mathrm{q3}})t] \end{aligned} \tag{2.28}$$

This summation has $(2Q)^{\mathrm{n}} = 4^3 = 64$ terms, although as in the case of $i_2(t)$ these do not all represent different mixing frequencies. Each of these mixing frequencies can also be expressed in a cosine form as shown for $2\omega_2 - \omega_1$:

$$\begin{aligned} i_3'(t) &= a_3 v^3(t) \Big|_{2\omega_2 - \omega_1} \\ &= \frac{3a_3}{4} \Big| V_{\mathrm{s},1} V_{\mathrm{s},2}^2 H(\omega_1) H^2(\omega_2) \Big| \cos[(\omega_2 - \omega_1)t] \end{aligned} \tag{2.29}$$

Volterra series is similar to power series analysis, but also caters for analysis of phase distortion.

2.2 LINEARISATION

Frequency governing bodies stipulate the power levels that can be transmitted into the unlicensed spectrum. With non-linear effects as previously discussed causing spectral emissions at frequencies that are not present on the input, this poses a problem for radio communication devices. As in Figure 2.6, the two main areas of spectral emissions are at the harmonics of the input frequencies and at the intermodulation frequencies. Filtering can be used to reduce the harmonic emissions to acceptable levels, but are not plausible to remove the intermodulation emissions. A number of methods to reduce these emissions by way of linearising the PA are used for this purpose, such as feedback or feed-forward linearisation, which are discussed in detail in the following sections. The main restriction imposed by feed-forward linearisation for communications systems is the power efficiency. Power amplifiers can be linearised somewhat by

operating in the linear region, however, to increase the power efficiency they are often driven nearer the saturation region. Predistortion linearisation is discussed further in the following chapter.

2.2.1 Feedback

As the name suggests, feedback linearisation is achieved by feeding the output signal back into the input. This can be implemented in a range of ways, the most basic idea of which is shown in Figure 2.7. More complex variations of feedback linearisation use the feedback signal in different ways, such as in IF and baseband feedback linearisation schemes as discussed in this section.

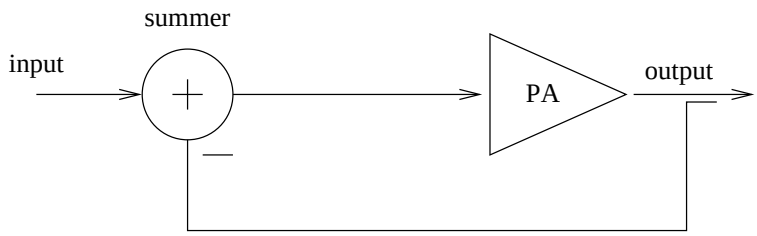

Figure 2.7: Basic diagram of feedback linearisation.

Feedback linearisation schemes correct for non-linearities over a narrow bandwidth because a bandpass filter is used to limit the bandwidth of the loop to maintain loop stability [3]. For stable loop operation the gain of the loop must be less than one at any point of operation where the phase margin is exceeded, which is controlled by the bandpass filter [3]. As any delay causes a phase shift, the total delay in the loop must also be small enough to ensure against instability due to phase margin violation. Over time, different methods of feedback linearisation have been developed to simplify implementation and increase performance. The basic distinction between implementations is the stage filtering and summing takes place (RF, IF or baseband).

The most simple feedback linearisation scheme when inspected as a full system is shown in Figure 2.8. Difficulties arise, however, as filters and amplifiers are more difficult to design at higher RF frequencies [3]. The filters used in RF feedback linearisation are typically cavity resonators, which only operate at a fixed frequency and are difficult to tune [5]. Maintaining stability is crucial in a feedback linearisation

system, regardless of whether it is implemented at RF, IF or baseband. The stability of the system is affected by the loop delay and the open loop gain. Feedback linearisation is like all feedback systems in that instability results from violating the gain or phase margins. As the overall gain margin must be preserved, a feedback linearisation system uses a bandpass filter to allow high gain over the bandwidth which requires linearisation and low gain for the remainder of the bandwidth of the system. This means that there is a trade off between bandwidth and gain to maintain the overall open loop gain margin.

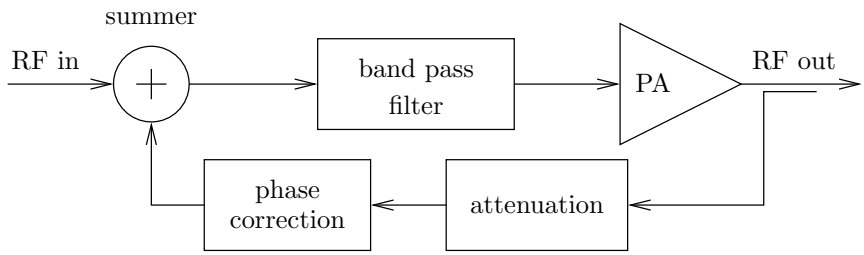

Figure 2.8: Feedback linearisation at RF.

The primary motivation to implement feedback linearisation at an intermediate frequency is to simplify the filter design [3]. Figure 2.9 shows an IF feedback circuit diagram. Note that the circuit is more complicated than the RF circuit in Figure 2.8 requiring mixers, additional filters and amplifiers. The phase shift no longer needs to be implemented in the feedback path, as a phase shift of the last mixer has the same effect.

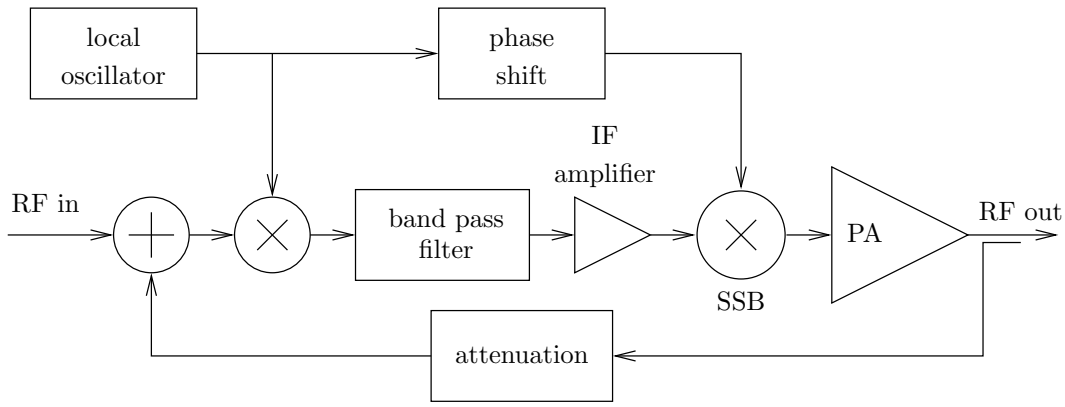

Figure 2.9: IF feedback linearisation circuit.

A typical loop filter includes two poles and a zero, as this offers better perfor-

mance than single resonator cavities [3]. The up-converter must be a single side-band mixer, as the unwanted side-band causes distortion through the power amplifier [3]. Additional filtering of the output of the power amplifier is also required to reduce the effects of the LO and unwanted side-band [3].

Baseband feedback seeks to simplify the filtering requirements even further than IF feedback by fully demodulating the signal and implementing the feedback summer and filters at baseband. The main form of baseband feedback linearisation is Cartesian loop feedback, as shown in Figure 2.10, and has been evaluated for both narrow bandwidth systems (10 k symbols/s) and wide bandwidth systems (500 k symbols/s) [6] as discussed later in this section.

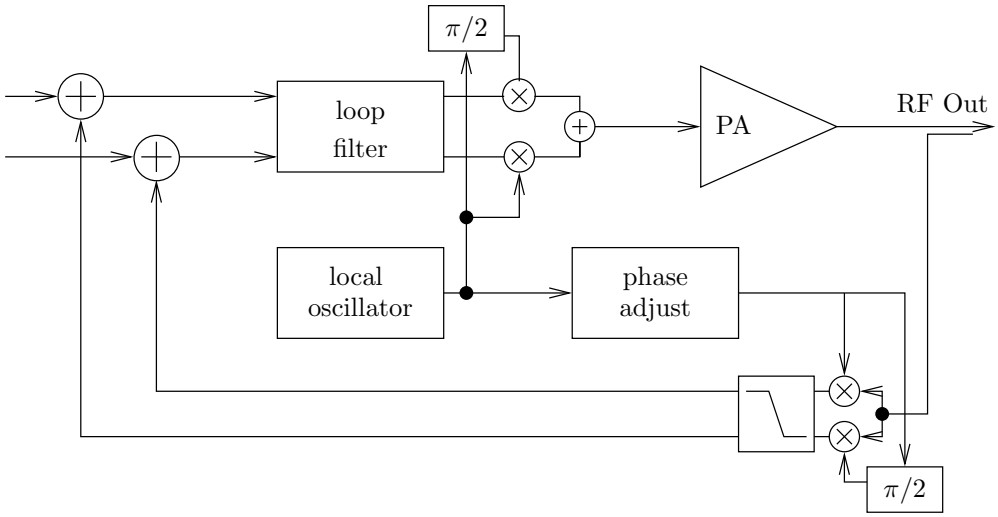

Figure 2.10: Cartesian feedback linearisation circuit.

Feedback systems were originally designed with the feedback summing and filtering all done in analogue at RF, IF or baseband. As the development of digital signal processor (DSP) devices, analogue to digital converters and digital to analogue converters progresses, there is also a progression to digitally implement as much of the loop as possible. In the case of Cartesian feedback loops this removes the need for quadrature modulators and demodulators, as these can be implemented digitally and mixed up to RF from an digitally generated IF [7].

Feedback linearisation can offer up to 35 dB correction, with a 60% power efficiency in its most complex baseband configurations such as Cartesian loop [8]. This

however can only be applied to a narrow bandwidth system (less then 1 MHz linearised bandwidth). Correction in the order of 35 dB can only be expected from the complicated baseband correction schemes, with IF systems providing around 30 dB correction and RF feedback providing as little as 10 dB IMD correction [8].

2.2.2 Feed-forward

Much of the effect of non-linearities in a power amplifier are observed as third order intermodulation on the output. Feed-forward linearisation seeks to cancel the intermodulation distortion by creating a distortion signal with an auxiliary amplifier, to cancel the distortion produced in the power amplifier. Figure 2.11 shows a block diagram of a feed-forward linearisation system. Note that the forward loop has two parts. The input signal is split into two paths, one through the main PA and the other through a delay element with a delay equal to the delay through the PA. The signal at the output of the main PA has both the amplified signal and distortion components. The signal component is cancelled by the delayed version of the input at coupler C_3 leaving only the distortion components. These components are amplified through the auxiliary amplifier and used to cancel the distortion components of the output of the main PA at coupler C_4.

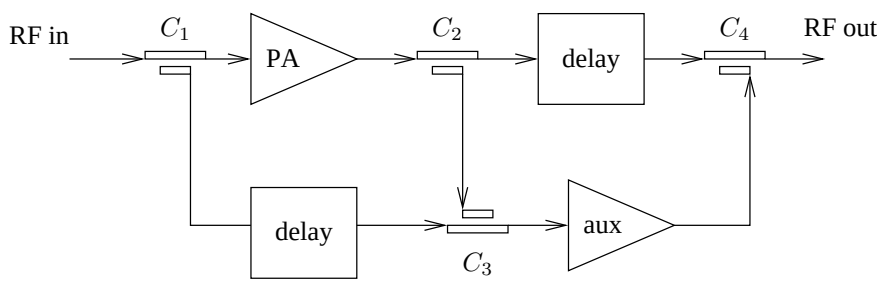

Figure 2.11: Basic feed-forward linearisation system.

As discussed in Section 2.2.1, feedback linearisation is only stable over narrow bandwidths which limits its use in high bandwidth applications. Feedfoward linearisation, however, is unconditionally stable [9] leading to high bandwidth correction capabilities. Successful linearisation through the removal of distortion components can only be achieved through precise signal cancellation over the frequency band of

the system. To achieve a 30dB cancellation, the amplitudes must be matched within 0.22dB and the phases must be matched to within 1.2^{o} [8].

Feed-forward linearisation requires two amplifiers, lowering the power efficiency. The most important design consideration for feed-forward linearisation systems is the two delay components. For optimal linearisation, these delays must be exactly the same as the delay through the amplifiers to ensure the distortion component cancels the signal at the correct point in time. The couplers are also an important design consideration. Couplers are used to both sample and sum signals throughout feed-forward linearisation. As couplers are typically constructed using $\frac{1}{4}$ wavelength strip-line, they must be designed for the frequency band in use.

Design of the auxiliary amplifier is also an important consideration. The gain of this amplifier is substantially lower than the power amplifier, but care must be taken that the signal does not further distorted through this amplifier. As the delay elements are critical to the performance of feed-forward linearisation systems, they have been the focus of much research. Performance can be improved by replacing the typical linear delay elements with phase distorting elements that match the phase distortion characteristics of the amplifiers. This approach increases both the bandwidth of the system and correction levels [10].

Distortion correction of around 25 dB – 30 dB can typically be achieved in manufactured equipment, with the limiting factor nearly always being the bandwidth over which a given accuracy can be achieved [8].

The outputs from the main amplifier and error amplifiers are typically combined using couplers that maximise power transfer from the main amplifier. A 10 dB coupling ratio is often used, so 90% of the power from the main amplifier reaches the load. However this means that only 10% of the power from the auxiliary amplifier reaches the load, so 10 times the distortion in the main amplifier must be produced. As a result, the auxiliary amplifier can consume a significant amount of power. Additional to this, it may be necessary to operate both amplifiers well into back-off to improve linearity. These affects may reduce the overall efficiency of a feed-forward transmitter

to 10% - 15% [8].

2.3 PREDISTORTION

This section provides a brief explanation of predistortion linearisation, which is further discussed in the following chapter. Predistortion linearisation in its simplest form involves distorting the signal prior to amplification in the inverse manner to which the power amplifier will distort the signal [8]. The output v_{pa} of the power amplifier will be a non-linear function of its input v_{in}. Consider the predistortion lineariser with an excitation signal in Figure 2.12. The output of the power amplifier will be a non-linear function of the input,

$$v_{\mathrm{pa}} = f_{\mathrm{nl}}(v_{\mathrm{pd}}). \tag{2.30}$$

Conversely, if the input signal is distorted with a non-linear function prior to amplification, then the output is a non-linear function of that distorted signal,

$$v_{\mathrm{pd}} = g_{\mathrm{nl}}(v_{\mathrm{in}}), \tag{2.31}$$

where v_{pd} is a non-linear function of the predistorter input v_{in}. The predistorter is designed such that

$$\begin{aligned} v_{\mathrm{pa}} = \quad & f_{\mathrm{nl}}[g_{\mathrm{nl}}(v_{\mathrm{in}})] \\ & f_{\mathrm{nl}}[g_{\mathrm{nl}}(v_{\mathrm{in}})] \quad = k \cdot v_{\mathrm{in}}, \end{aligned} \tag{2.32}$$

where k is a constant.

As discussed in Chapter 2, the AM-AM distortion and AM-PM are significant in typical PAs. The AM-AM characteristic is determined by the saturation level of the amplifier. As the input power level is increased, the power gain of the PA decreases.

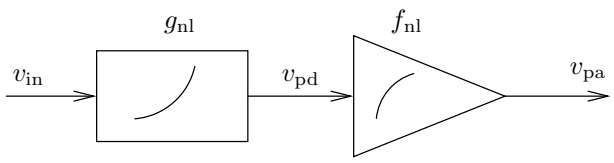

Figure 2.12: Predistortion linearisation in its simplest form.

The AM-PM characteristic is caused by a changing phase shift of a signal through the amplifier, which is also a function of the input power level. Memory effects can also cause distortion. Predistortion linearisation has the potential for excellent wideband performance [11] and can be implemented a number of different ways, using either analogue or digital circuitry and at both RF, IF and baseband [8].

Early predistortion linearisation techniques were based around an analogue distortion or signal injection. Methods of injecting third-order and fifth order intermodulation products with a single distortion element were found to be less effective than individual generation. This performance gain, however, comes at the cost of a more complex system [12]. A higher level of linearisation is possible using digital systems to control either analogue or digitally generated IM products. Further performance improvements are realised when predistortion is applied to the complex baseband signal, with the PA output attenuated and demodulated to use in adapting the predistorter's transfer characteristic. As is the case with previously discussed linearisation methods, the more complicated schemes provide superior correction, with adaptive digital predistortion out-performing analogue implementations.

Predistortion linearisation at RF or IF, as shown in Figure 2.13 is the most simplistic configuration, with a non-linear element placed before the amplifier. A system of this configuration is limited to analogue implementation, as digital signal processing can not be performed fast enough to manipulate an RF signal.

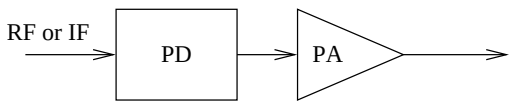

Figure 2.13: Predistortion linearisation at IF and RF.

Most of the design considerations associated with predistortion linearisation relate

to the complexity of the system and the level of correction required. A small level of correction can easily be obtained by use of analogue distortion at RF, whereas more correction can be realised with a complex adaptive algorithm at baseband using a full demodulation of the PA output signal for adaption. Predistortion is explored in detail in Chapter 3.

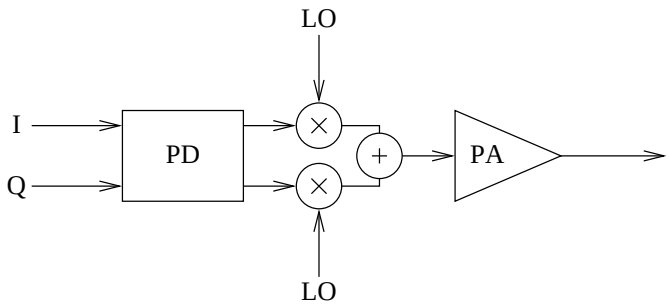

Figure 2.14: Predistortion linearisation at baseband.

Chapter 3

PREDISTORTION LINEARISATION

In this chapter the theory of predistortion linearisation is presented along with the technology progression from earlier analogue implementations through to digital baseband systems. As discussed in Chapter 2, the traditional approaches to linearisation have disadvantages of low bandwidth (feedback) or low power efficiency (feed-forward), both of which are undesirable for modern communication systems. Predistortion linearisation provides a higher bandwidth, higher power efficiency linearisation option.

3.1 ANALOGUE

Analogue predistortion is typically performed at radio frequency (RF). As with feed-forward predistortion, the bandwidth of the system is limited by the consistency of gain and phase of an analogue predistorter over the operational bandwidth. Additional limitations are from memory effects in the power amplifier (PA). Analogue predistortion linearisation demonstrates the potential of this technology but quickly becomes a complex system. Independent non-linear analogue elements can be used to provide a number of fixed predistortion characteristics that are difficult to adjust. Each of the independent predistortion characteristics must then be combined to form the complete predistortion characteristic. This means each analogue RF predistorter must be designed for a specific PA and its operating conditions. As in the case of feed-forward linearisation, performance is often limited by the gain and phase flatness of the predistorter itself. Unlike feed-forward linearisation, however, the predistortion

linearisation architecture does not inherently require a second amplifier and thus is able to provide higher power efficiency.

Different methods of predistortion all generate intermodulation products from the input signal and then combine this distorted signal with the input to produce the predistorted input to the PA. As with feed-forward linearisation, matching the phase of the two signal paths increases the system complexity. To overcome this, a branch FET can be used to directly distort the input signal of the PA, providing third-order linearisation [13]. This method of predistortion as shown in Figure 3.1 does not require phase matching circuitry. A two-tone test with tone separation of 4 MHz at 902 MHz shows an reduction in third-order intermodulation products by 13 dB. This predistortion could be implemented in a monolithic microwave integrated circuit (MMIC).

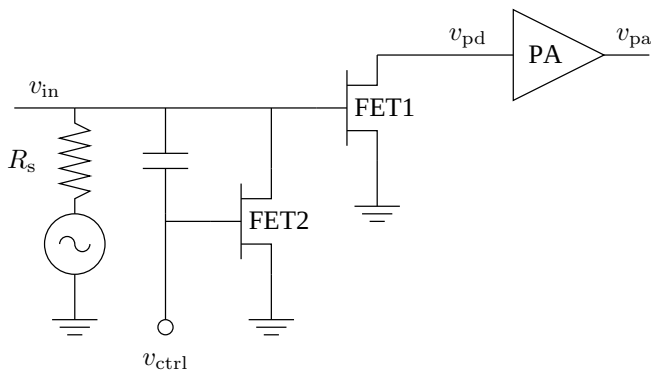

Figure 3.1: Branch FET predistortion linearisation.

An analogue third-order signal injection predistorter for use in CDMA systems [11] is shown in Figure 3.2. The fixed third-order product is generated by a cubic non-linearity and combined into the main RF path, delayed to match the phase of the two parallel paths. In a two-tone test an 18 dB reduction in the third-order intermodulation is achieved, however, the performance is limited by the unwanted additional higher order intermodulation products produced by the predistorter. Fifth order intermodulation products are 4 dB higher than the third-order so the total intermodulation improvement is 14 dB. This architecture allows for bandwidths of up to 60 MHz, with an RF carrier range from 100 MHz to 1 GHz.

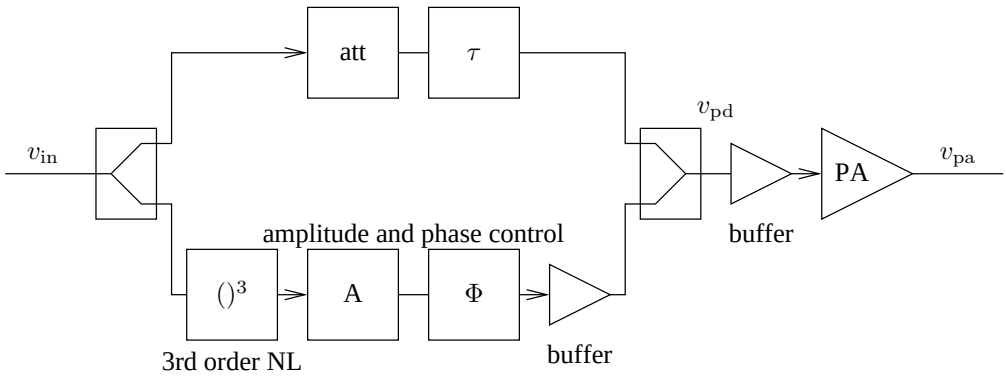

Figure 3.2: Third-order signal injection predistortion.

A more complex intermodulation generation system shown in Figure 3.3 as proposed in [12] demonstrates an increase in linearisation performance. The system uses independent amplifiers to produce third and fifth order distortion products which are phase adjusted and combined with the fundamental. The PA used is a two stage lateral double diffuse metal oxide semiconductor (LDMOS) class AB amplifier with a 450 W peak power output. The third and fifth order intermodulation phases vary relative to each other over the input power range, so independent phase control of the third and fifth order linearisation products is required. The complexity of the two stage amplifier also makes it difficult to match the non-linear characteristics of the predistorter and the PA because they differ both in size and the number of stages. Experimental results with a 10 MHz spacing two-tone signal at 2.385 GHz reduces the intermodulation products by 30-35 dB. When used in combination with a CDMA signal with 8.192 MHz bandwidth, the adjacent channel power (ACP) is reduced by 9 dB [12].

An alternative to using error generation amplifiers is to generate the intermodulation products by generating even order terms and using these even order terms to generate odd order terms. The system shown in Figure 3.4 uses I/Q balanced modulators and double balanced ring diode mixers as intermodulation generators [14]. The low frequency second order intermodulation component $(\omega_2 - \omega_1)$ is generated with a non-linear power amplifier, with the fourth order intermodulation $(2\omega_2 - 2\omega_1)$ being generated with an analogue multiplier. The third and fifth order intermod-

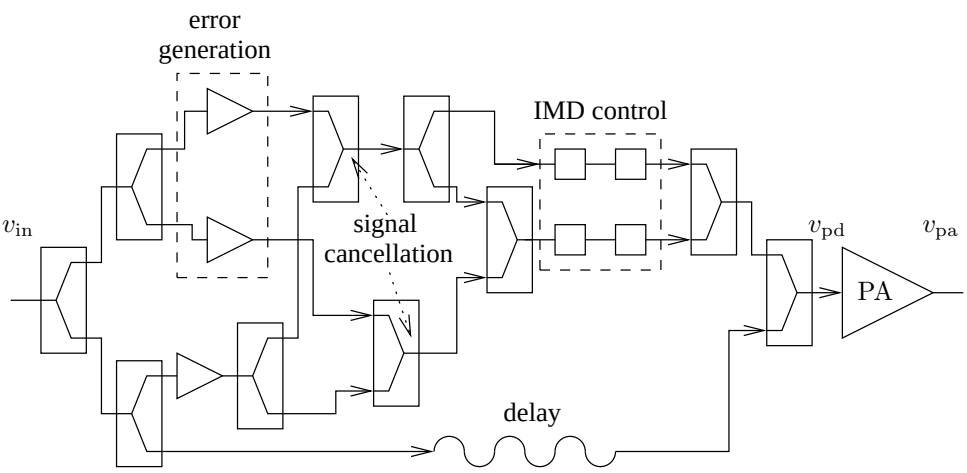

Figure 3.3: Third and fifth order predistortion using error amplifiers.

ulation components are generated and phase adjusted, before being combined with the RF signal. As with error amplifiers, the intermodulation product amplitude and phase can both be independently controlled. Experimental results using an MHL21336 35 dBm PA from Motorola, with a 1 MHz spacing two-tone test at 2.150 GHz shows a 23 dB reduction in third-order intermodulation and 10 dB reduction in fifth order intermodulation [14].

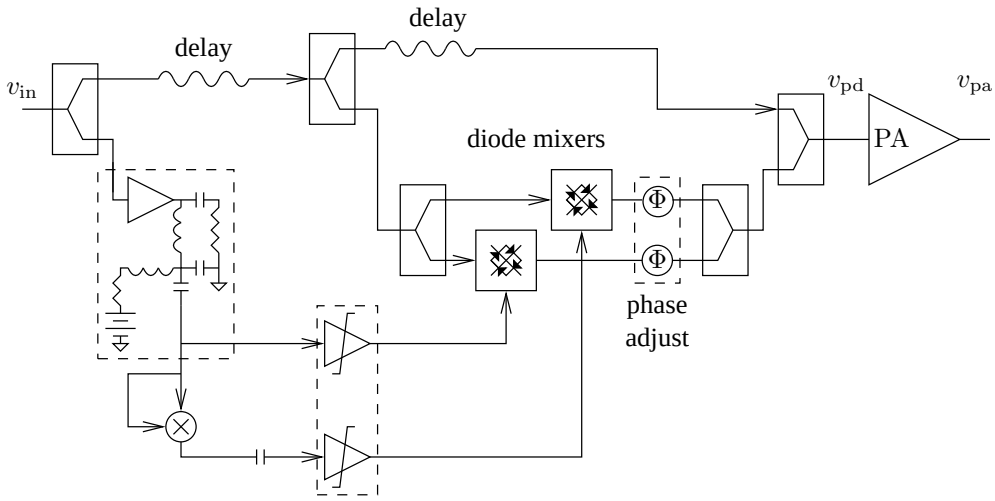

Figure 3.4: Third and fifth order predistortion using even order terms.

3.2 ANALOGUE PREDISTORTION WITH DIGITAL CONTROL

To provide more correction to third and higher order intermodulation products, digital methods of predistortion have been investigated. Initial digital predistortion algorithms used look up tables (LUTs) to map an input signal to a predistorter output signal [15][16]. As with all predistortion linearisation systems, the predistorter output drives the input of the PA. With digital predistortion came adaptive capability, which allows the predistortion characteristic to be adjusted to improve the intermodulation reductions. Adaptive predistortion also means that a general predistortion system can be used with different amplifiers and configurations, which exhibit different distortion characteristics.

As identified in the previous section, there is a need to control the generation of different intermodulation products for predistortion linearisation independently, as they are independent functions of the input signal. It is also known that not only do different PAs have different transfer functions but that the transfer function of an amplifier will vary over its range of operating frequencies and environmental conditions. An extension to fixed analogue predistortion is to provide a method by which the predistortion transfer function can adapt in real time to linearise an amplifier operating under different and changing conditions causing the PA's transfer characteristic to vary. This section will investigate the addition of digital adaption algorithms to analogue predistorters.

The general architecture of a digitally adapted analogue predistorter is shown in Figure 3.5. The predistortion is performed at RF, with detectors to provide information for a digital adaption algorithm. This sort of architecture means that the system must be designed around the characteristics of the modulated RF signal. Typically the adaption is calculated from the envelope of the input signal and the amplified predistorted signal envelope, as these signals are at low enough frequencies to perform operations on digitally.

The wide range of digital predistorters available vary in both intermodulation reduction performance, convergence rate and system bandwidth.

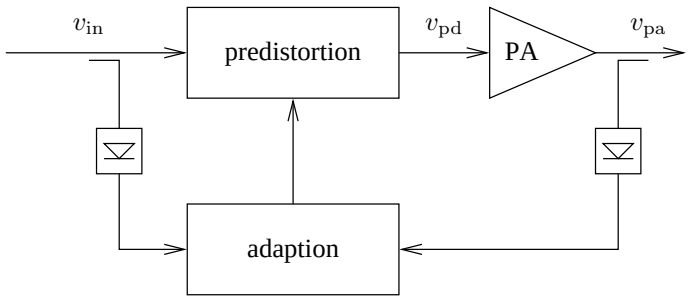

Figure 3.5: Adaptive predistortion calculated from the envelope and applied at RF.

A predistorter which is integrated onto an monolithic microwave integrated circuit (MMIC) that also contains a PA is shown in Figure 3.6 [15]. The input to the module is filtered and then passes through a phase shifter and a variable gain block. A dual gate FET is used for the gain controlling block with the gain easily being controlled by varying the voltage on its second gate. This causes a phase shift on the output of the gain controlling block which must also be corrected by the phase shifter. The phase and gain of the predistorter are controlled with analogue control signals derived from lookup tables (LUTs) addressed by the input envelope level. The contents of the two lookup tables are updated by an algorithm that compares the input envelope with the PA's output envelope. This module has been designed for CDMA handset terminals and therefore has a bandwidth of 1.2288 MHz and a centre frequency of 906 MHz. Two-tone tests demonstrate a reduction in the third-order intermodulation products of 20 dB when tested with an N-CDMA signal, adjacent channel power (ACP) is reduced by 7 dB [15].

Increasing the characteristic information available to a digital/RF predistorter as presented in [16] further increases the linearisation capabilities. In the system shown in Figure 3.7, the lookup table is able to better reproduce the predistortion characteristic as it is a two dimension lookup table, with non-uniform input quantisation. This is known as mapping predistortion, as the lookup table maps the input envelope to I and Q correction vectors. The input RF signal envelope is detected and used to find I and Q vectors which are multiplied onto the RF input to the PA. As the I and Q are predistorted with independent lookup tables, the input to the PA and its distorted output are demodulated to complex baseband and used in the adaption

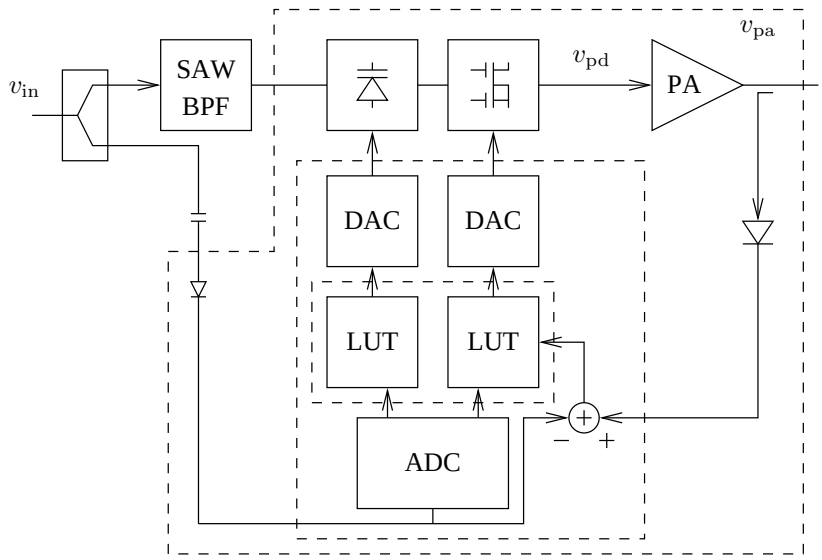

Figure 3.6: RF predistortion PA system.

algorithm to adjust the lookup table contents. The lookup table predistortion is implemented in an FPGA with adaption performed by a DSP. This method again requires precise phase matching of the RF signal and the output from the lookup table. A two-tone test with tone separation of 1 MHz at 1960 MHz demonstrates a reduction of the third-order intermodulation by 20 dB. With a CDMA IS95 input signal, third-order intermodulation is reduced by 15 dB. When compared with complex gain predistortion, the two-tone performance is similar, however, the adjacent channel power of a CDMA signal is reduced a further 8 dB by the more complex mapping predistorter [16].

When predistortion is applied at RF, the predistortion system must be designed specifically for the bandwidth and frequency of the modulated RF signal. In order to design a predistortion system that operates independent of the RF signal characteristics, the predistortion must be applied at baseband. As baseband processing is typically done digitally in modern communications systems, there is a trend towards digital implementation of baseband predistortion as discussed in Section 3.3. The linearisation shown in Figure 3.8 demonstrated a digitally adapted analogue predistorter operating at baseband [17]. The complex baseband I and Q signals are predistorted through a power series with third and fifth order coefficients,

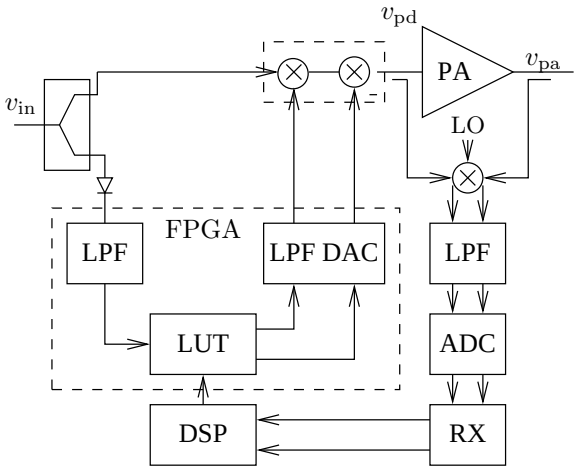

Figure 3.7: Mapping predistorter architecture.

$$v_{\mathrm{I,pd}} = v^1_{\mathrm{I,in}} + C_{\mathrm{I},3} v^3_{\mathrm{I,in}} + C_{\mathrm{I},5} v^5_{\mathrm{Q,in}} \tag{3.1}$$

$$v_{\mathrm{Q,pd}} = v^1_{\mathrm{Q,in}} + C_{\mathrm{Q},3} v^3_{\mathrm{Q,in}} + C_{\mathrm{Q},5} v^5_{\mathrm{Q,in}} \tag{3.2}$$

The coefficients are calculated using the Hooke and Jeeve algorithm which uses the side-band power as the minimisation criterion. This system reduces third-order intermodulation by 20 dB with a 2 MHz tone separation at 35 MHz [17].

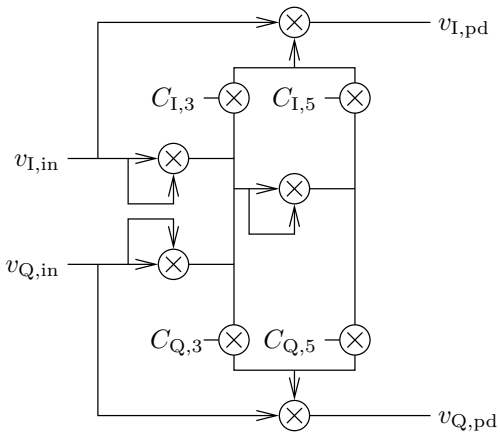

Figure 3.8: Analogue baseband predistortion.

3.3 DIGITAL BASEBAND PREDISTORTION

This section outlines the basics of complex baseband manipulation before discussing predistortion linearisation methods that operate on the baseband signal.

A typical digital radio system has the architecture shown in Figure 3.9. A digital bit stream is modulated onto a complex baseband signal with in-phase (I) and quadrature (Q) components. For any given modulation format a binary word of length N bits is mapped onto a symbol on the complex plane, such that each binary word has a unique symbol. The complex baseband is then up-sampled and filtered to limit the bandwidth of the signal before being modulated onto an RF carrier. Each symbol of the complex baseband corresponds to an amplitude and phase of the RF signal as

$$RF = Q \cdot \cos(\omega_c t) + I \cdot \sin(\omega_c t) \tag{3.3}$$

As this process of quadrature modulation can be reversed to recover the I and Q, it follows that predistortion of the complex baseband signal can linearise the non-linear transfer characteristic of the PA operating at RF.

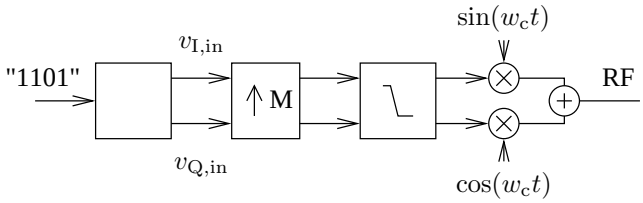

Figure 3.9: Digital radio baseband architecture.

The process of digital baseband predistortion can be divided into two main categories:

- LUT-based
- Model based

Lookup table based methods use a lookup table to find a distorted output based on the input values. Adjusting the contents of the lookup table is done to adapt the

predistortion characteristic. Model based predistorters calculate a pre-distorted output from a mathematical model of the predistortion transfer characteristic. Adjusting the model parameters adapts the transfer characteristic of the predistortion to minimise an error criterion. In the following section lookup table based predistortion is discussed, followed by discussion of model-based predistortion.

3.3.1 Baseband lookup table predistortion

This section will look at examples of lookup table predistorters which can be divided into two categories:

- Complex gain predistortion
- Mapping predistortion

As its name suggests, a mapping predistorter maps a pure input signal to a distorted output signal. A complex gain predistorter, however, uses a function of the input signal (often the input power) to index the output distorted signal level.

The pioneering research into digital baseband predistortion employs a mapping LUT architecture [18] shown in Figure 3.10. The complex baseband signal v_{in} is used to index a two dimensional lookup table. The output of the lookup table is added to v_{in} to find the predistorted complex baseband signal v_{pd}. This is converted to analogue, quadrature modulated and up-converted to RF before being amplified. The output of the PA is down-converted and demodulated to recover the complex baseband which in turn is used to adapt the contents of the lookup table. This architecture is capable of reducing the out-of-band power of a QPSK channel to -60 dBc – a 30 dB reduction to the third-order intermodulation. The time this predistorter takes to converge to a steady state is slow – around 5-10 seconds, due to the large memory contents to be updated.

A constant-gain predistorter [19] is shown in Figure 3.11. The instantaneous power of the complex baseband signal is calculated and used as an input to a single dimension LUT. The output of this LUT is multiplied by the input v_{in} to calculate v_{pd},

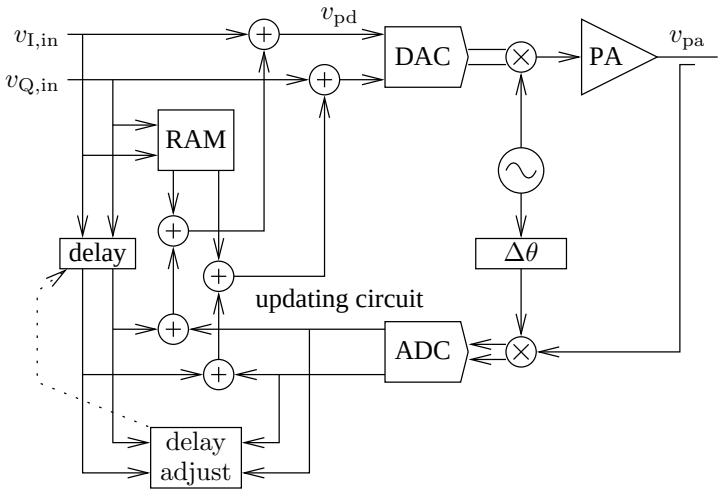

Figure 3.10: Mapping predistorter.

the predistorted complex baseband signal. In an implementation of a complex gain predistorter, v_{pd} would be converted to analogue complex baseband and modulated onto an RF carrier. In simulation results this system is capable of reducing up to 15th order intermodulation products. The third-order intermodulation of this system is reduced by 55 dB to -75 dBc, however, the seventh order intermodulation raises the out-of-band power to -65 dBc. When simulating the linearisation of a 16 QAM channel, the third-order intermodulation is reduced to -60 dBc from -32 dBc. This predistorter linearises up to 95% of a PA's saturated power output level. Convergence to a steady state takes 4 ms, a significant reduction from 5-10 seconds for a mapping predistorter.

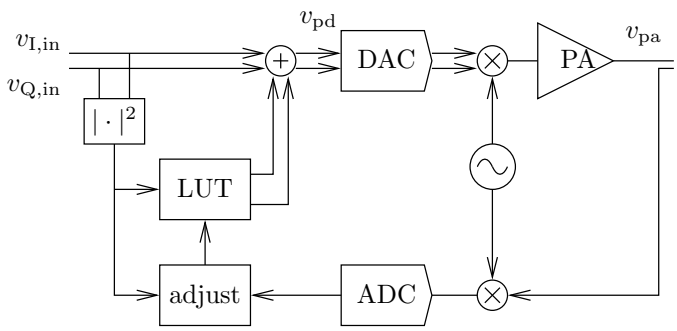

Figure 3.11: Constant gain predistorter.

Further developments into the area of LUT-based baseband predistortion have been in the refinement of the way the LUT is stored and adapted. One such method as shown in Figure 3.12 uses cubic spline interpolation to populate a complex gain predistorter LUT [20]. The instantaneous power of the complex baseband is calculated and used as an input to an LUT, the output of which is added to the complex baseband I and Q samples. The LUT table contents is updated by an AM-AM and AM-PM estimator which compares the pre-distorted complex baseband with the demodulated output of the PA. This estimator calculates r, r' and θ' values using cubic spline interpolation,

$$r = \sqrt{v_{\mathrm{I,in}}^2 + v_{\mathrm{Q,in}}^2} \tag{3.4}$$

$$r' = \sqrt{v_{\mathrm{Q}'}^2 + v_{\mathrm{Q}'}^2} \tag{3.5}$$

$$\theta' = \tan^{-1}(\frac{v_{\mathrm{Q}'}}{v_{\mathrm{i}'}}), \tag{3.6}$$

where for an input to the LUT m, the updated values of the amplitude characteristic m' and phase characteristic ϕ' are calculated. Thus the predistorted signal is the sum of the LUT output and the complex baseband signal,

$$v_{\mathrm{I,pd}} = v_{\mathrm{I,in}} + r' \cdot \cos\theta' \tag{3.7}$$

$$v_{\mathrm{Q,pd}} = v_{\mathrm{Q,in}} + r' \cdot \sin\theta'. \tag{3.8}$$

This system performance is analysed using simulation of a class AB PA characteristic with both two-tone and DQPSK input signals. With a two-tone at 22.25 kHz, third-order and fifth order intermodulation are reduced to -80.3 dBc and -81.2 dBc respectively from -29.6 dBc and -38.1 dB respectively. With a 40 kHz DQPSK channel third and fifth order emissions are both reduced by 40 dB to -80 dBc.

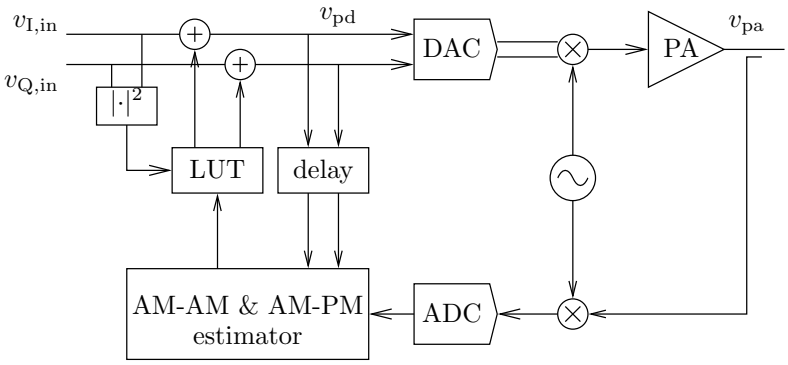

Figure 3.12: Cubic spline predistortion architecture.

3.3.2 Baseband model predistortion

Further improvement in the correction capability of predistortion systems are provided by using a mathematical model of the predistortion function. These systems use a predistorter that can calculate the required predistortion characteristic from a small number of model parameters. The model parameters can be adapted more quickly than the contents of an LUT, but more computation is required to apply the predistortion. Due to limitations of micro-processor based DSPs, this type of predistortion can only be implemented at baseband, or a low intermediate frequency. Much of the research into this area has been on one of two main thrusts:

- Increasing predistorter performance with more accurate and complex models
- Refining the process used to adapt model parameters to reduce convergence times

The expected results from this research have been extensively simulated, however, many of the approaches have not been implemented in real-time operational systems.

The predistortion system shown in Figure 3.13 applies a predistortion characteristic to the complex baseband signal in polar co-ordinate format [21]. As described in Chapter 2 the distortion characteristics of a typical PA have independent AM-AM and AM-PM functions. This makes application of a predistortion straightforward, as shown in Figure 3.13. The AM-AM and AM-PM predistortion functions are modelled independantly by finite order polynomials of ρ^2 the input power,

$$|v_{\mathrm{pd}}| = v_{\mathrm{in}} \cdot \sum_{\mathrm{i}=0}^{\mathrm{N}} \alpha_{\mathrm{i}} \rho^{2\mathrm{i}}, \tag{3.9}$$

$$\angle v_{\mathrm{pd}} = v_{\mathrm{in}} \cdot \sum_{\mathrm{i}=0}^{\mathrm{M}} \beta_{\mathrm{i}} \rho^{2\mathrm{i}}. \tag{3.10}$$

In this case, i is chosen as 2. Input complex baseband signal instantaneous power ρ_{x}^2 is calculated and used as an input to the independent amplitude and phase polynomials. The output from the amplitude and phase polynomials are multiplied with the complex baseband signals after being converted back into rectangular co-ordinates to realise the predistorted complex baseband signal. The coefficients of the polynomials are updated by minimizing the following cost function,

$$C_2 = \sum_{\mathrm{i}=1}^{\mathrm{N}} w(\rho^2)[A(\rho^2) - A_{\mathrm{N}}(\rho^2)]^2. \tag{3.11}$$

where A is the AM-AM transfer function. With a 256 QAM signal, this method reports a further 5.2 dB decrease in out-of-band power compared with a popular third-order predistorter with transfer function,

$$v_{\mathrm{pd}} = f(a_{\mathrm{t}} + b^{\mathrm{t}} \rho^2) \tag{3.12}$$

when compared with a popular fifth order predistorter with transfer function, an additional 2 dB reduction of out-of-band power is obtained,

$$v_{\mathrm{pd}} = f(a_{\mathrm{t}} + b^{\mathrm{t}} \rho^2 + c^{\mathrm{t}} \rho^4). \tag{3.13}$$

An alternative to using independent polynomials for AM-AM and AM-PM predistortion is to have a polynomial predistorter with complex coefficients [22]. As is shown in Figure 3.14, the complex baseband signal is distorted through a polynomial predistorter before being converted into analogue signals, modulated and then amplified. A small amount of the PA output is coupled and demodulated, before being

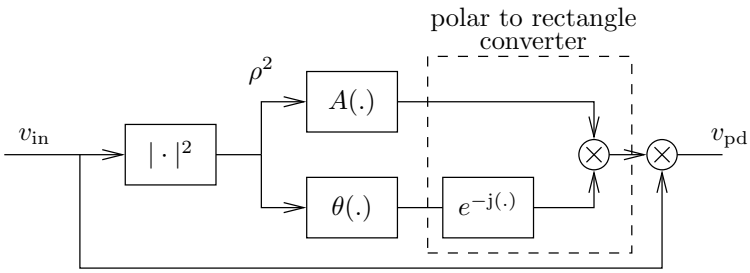

Figure 3.13: Polar polynomial predistorter architecture.

sampled into a digital complex baseband. The LMS algorithm is used to adapt the coefficients of the predistorter by minimising the error between the complex baseband signal and the complex feedback from the PA output as

$$f(n) = f(n-1) - \mu \cdot \bigtriangledown J(n), \tag{3.14}$$

where $f(n)$ is the vector of the polynomial coefficients and $\bigtriangledown J(n)$ is the gradient of the error $v_{\text{in}} - v_{\text{pa}}$.

Simulations [22] of this predistortion system use a 9th order polynomial model of the transfer characteristic of a class AB MOSFET amplifier and a third-order predistorter 3.14. When a QPSK modulation format is used, with a bandwidth of 0.5 F_{s}, the channel power is reduced by 4 dB and third-order intermodulation is reduced by 20 dB. The reduction in the output power of the PA also reduces the fifth, seventh and ninth intermodulation products by 8 dB. With an orthogonal frequency division modulation (OFDM) format, the channel power is reduced by 5 dB and third-order intermodulation is reduced by 25 dB, with fifth, seventh and ninth intermodulation products all being reduced by 15 dB due to the lower power output of the PA.

Figure 3.15 shows a model based predistortion lineariser using independent AM-AM and AM-PM polynomials with odd order coefficients only [23]. The predistorted signal is a function of the amplitude of the complex baseband signal $r(t)$,

$$v_{\text{pd}}(t) = F(r(t))e^{\text{j}(\theta(\text{t})+\Psi(\text{r}_{\text{in}}(\text{t})))}, \tag{3.15}$$

where $F(r(t))$ and $\Psi(r(t))$ are the AM-AM and AM-PM predistorter functions.

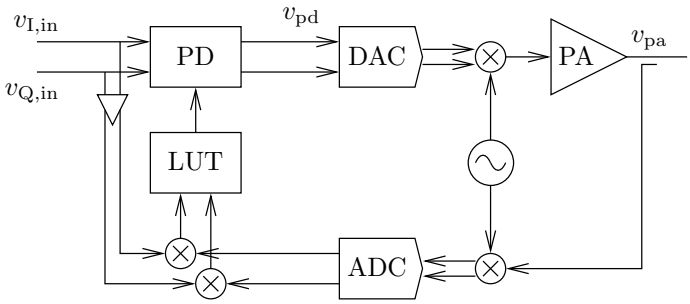

Figure 3.14: Power series predistorter architecture.

The amplitude of the input complex envelope is calculated and used as an input to the two predistortion functions. The AM-AM distortion is applied by multiplying the calculated distortion with the complex baseband. AM-PM distortion is applied using a LUT to get values of cos and sin for a rotation matrix. The transfer functions of the two predistortion functions are adapted by minimising the mean squared error criteria,

$$J_{\mathrm{AM-AM}} = E((\alpha r - G(V^{\mathrm{T}} R_{\mathrm{f}}))^2) \tag{3.16}$$

$$J_{\mathrm{AM-PM}} = E((\Phi(V_{\mathrm{opt}}^{\mathrm{T}} R_{\mathrm{f}}) + P^{\mathrm{T}} R_{\mathrm{phi}})^2). \tag{3.17}$$

With coefficients being updated using,

$$V_{\mathrm{k+1}} = V_{\mathrm{k}} + \mu_{\mathrm{v}} \Gamma_{\mathrm{f}} R_{\mathrm{f,k}} \alpha - G(V_{\mathrm{k}}|^{\mathrm{T}} R_{\mathrm{f,k}}) \tag{3.18}$$

$$P_{\mathrm{k+1}} = P_{\mathrm{k}} - \mu_{\phi}(\Phi(V_{\mathrm{k}}^{\mathrm{T}} R_{\mathrm{f,k}}) + P_{\mathrm{k}}^{\mathrm{T}} R_{\phi,\mathrm{k}}) \Gamma_{\mathrm{phi}} R_{\mathrm{phi,k}}, \tag{3.19}$$

where α is the desired linear gain, $\Gamma_{\mathrm{x}} = \sqrt{E(R_{\mathrm{x,k}} R_{\mathrm{x,k}}^{\mathrm{T}})}$ and both μ_{v} and μ_{ϕ} are step sizes.

In simulated two-tone tests with a tone separation of $0.15F_{\mathrm{s}}$ the intermodulation is lowered to -60 dBc compared with -40 dBc intermodulation with no predistortion and 10 dB back-off. With a 16 QAM channel simulation, intermodulation is improved

by 30 dB.

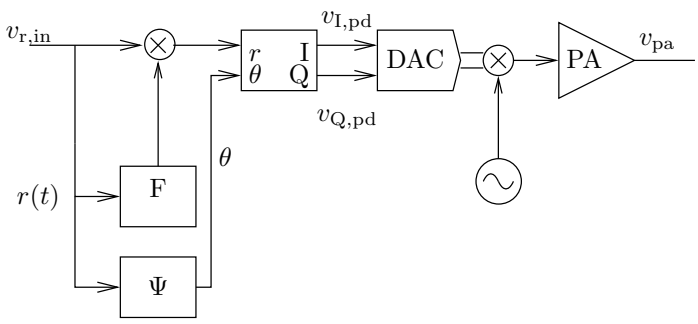

Figure 3.15: Odd order polynomial predistortion architecture.

Minimisation of the distortion caused by PA memory effects can be achieved with a Volterra series predistorter. This transfer characteristic allows correction of AM-AM, AM-PM and memory effect distortion [24]. As shown in Figure 3.16, the complex baseband signal is predistorted with an adaptive Volterra filter. The adaption is applied using a direct inversion, where the output of the PA is iteratively adapted to find the predistortion coefficients which are copied to the predistorter model. The Volterra filter coefficient vector has third-order terms, with a delay line of 2 samples to allow for cancellation of the distortion caused by memory effects within the PA. The predistorter model coefficients are updated using,

$$C_{\mathrm{t=n}} = C_{\mathrm{t=n-1}} + G \cdot v_{\mathrm{e,t=n-1}}, \tag{3.20}$$

where G is the gain V-vector and the error v_{e} is the difference between the desired signal v_{d} and the volterra filter output,

$$v_{\mathrm{e}} = v_{\mathrm{d}} - C^{\mathrm{T}} V_{\mathrm{in}} \tag{3.21}$$

where V_{in} is the input vector to the volterra filter coefficients C with the form

$$C_{\mathrm{k}} = \sum_{\mathrm{m=1}}^{\mathrm{M}} \sum_{\mathrm{k=1}}^{\mathrm{K}} C_{\mathrm{k,m}} v_{\mathrm{in,t=n-k}}^{\mathrm{m}}. \tag{3.22}$$

This predistorter was simulated with:

1. 25 kHz spaced two-tone signal, reducing third-order intermodulation by 15 dB

2. IS95 CDMA, reducing third-order intermodulation by 10 dB

3. WCDMA signals, reducing third-order intermodulation by 9 dB

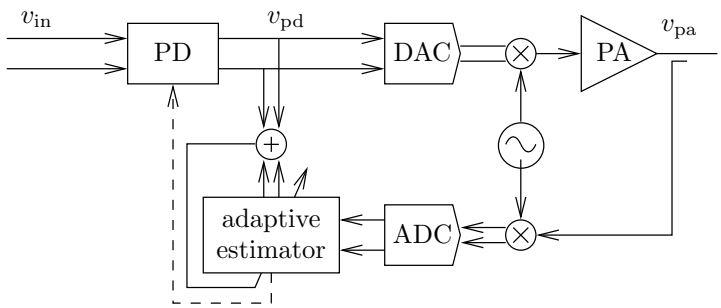

Figure 3.16: Volterra predistorter architecture.

In order to decrease convergence times, different algorithms can be employed to adapt the parameters of a model based predistorter. One such method is to use the Recursive Least Squares (RLS) algorithm [25]. The RLS algorithm has high computation requirements, which are decreased by breaking the predistortion polynomials into two sub functions which are computed in parallel, as shown in Figure 3.17. This system also uses a direct inversion method where the output from the PA is distorted by two sub functions, the output of which are combined into v_{PAd} the distorted output of the PA. The difference between v_{PAd} and the predistorted baseband signal v_{d} is used to adapt one sub function at a time. Use of the RLS algorithm in this way has a lower mean squared error (MSE) (1.5 x 10^{-1}), when compared with the use of a single function for each of the phase and amplitude predistortion characteristics (2 x 10^{-2}). This method of adaption and predistortion capability is verified in simulations [26] with a 16 QAM baseband signal. With a power back off of less than 7 dB, the proposed sub function predistorter provides 4 dB reduction in PA degradation.

Another method for providing adaptive non-linear systems is to use multi-layer perception (MLP) neural nets (NN) as a predistorter [27]. As shown in Figure 3.18, the predistorter is based on a three level single input double output multi-layer perception. The complex baseband v_{in} in polar format is split into R and θ components.

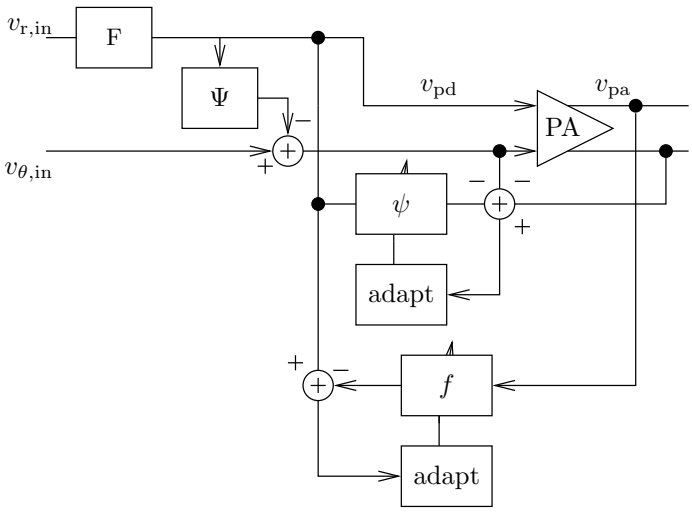

Figure 3.17: RLS predistorter architecture.

The multilayer perception input is v_{in} which calculates the r_{pd} and ϕ_{pd} components of v_{pd}. A back propagation algorithm is used to adapt the multilayer perception transfer function. Simulation results [28] with a 400 kHz DQPSK signal along with implementation results demonstrate the capabilities of this predistortion architecture. In simulation, the third-order intermodulation products are reduced by 20 dB. An implementation on a TMS320C6711 DSP achieved a reduction of third-order intermodulation of 25 dB.

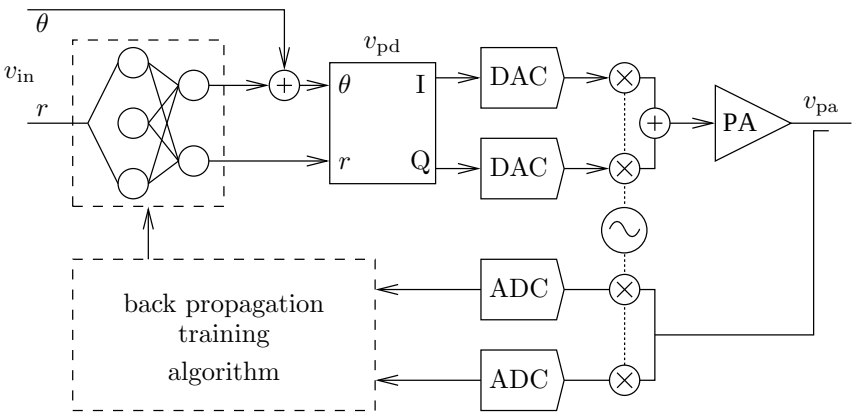

Figure 3.18: Multi-layer perception predistorter architecture.

As summarised in Table 3.1, the progression of technology from analogue predistortion at RF to digital predistortion at baseband increases the level of intermodulation correction of predistortion linearisation. This gain comes from increased com-

plexity, either in analogue or digital domains. The best linearisation performance is provided by digital adaptive model based predistorters. The system design presented in Chapter 4 will draw on some of the predistortion systems reviewed here, with a view to implementing an adaptive predistortion linearisation system that operates in real time.

Predistortion technology						
Architecture	PA	RF	2 tone BW	2 tone ACP reduction (dB) level(dBc)	channel	channel ACP reduction (dB) level(dBc)
			Analogue			
Branch FET [13]		902 MHz	4 MHz	13 dB		
Third-order [11]			60 MHz	14 dB		
Error amplifer [12]	LDMOS	2.385 GHz	10 MHz	30 dB	8.192 MHz	9 dB
Ring diode mixer [14]	MHL21336	2.150 GHz	1 MHz	23 dB		
			Hybrid			
MMIC [15]		906 MHz	1.2288 MHz	20 dB	1.2288	7 dB
RF vector multiplier [16]		1960 MHz	1 MHz	20 dB	IS95 CDMA	15 dB
Baseband multiplier [17]		35 MHz	2 MHz	20 dB		
			Digital LUT			
Mapping [18]	(simulation)			30 dB		-60 dBc
Complex gain [19]	(simulation)			35 dB		28 dB
Cubic spline [20]	(simulation)			50.6 dB	4 kHz DQPSK	40 dB
			Digital model			
Polar model [21]	(simulation)					
Power series [22]	(simulation)				0.5 Fs QPSK	20 dB
				0.5 Fs OFDM	25 dB	
Odd order [23]	(simulation)		0.15 Fs	20	16 QAM	30 dB
Volterra Series [24]	(simulation)		25 kHz	15 dB	IS95CDMA	10 dB
				WCDMA	9 dB	
RLS adaption [25],[26]	(simulation)				16 QAM	4 dB
Neural Net [27]	(simulation)				400 kHz DQPSK	20 dB
Neural Net [28]	(implementation)				400 kHz DQPSK	25 dB

Table 3.1: Summary of predistorter performance and capabilities.

Chapter 4

PA MODELLING AND DESIGN

This chapter covers the measurement and modelling of the non-linear transfer characteristic of a typical PA, along with the design of an adaptive polynomial predistortion lineariser. As shown in Chapter 3, simulations of model based predistortion linearisation of PAs show promise, but implementations have not been presented. The two main aspects of a predistortion linearisation system are the inverse model of the PA and the method for adapting the transfer characteristic of this model.

4.1 AMPLIFIER MODELLING

Many papers that present linearisation schemes base their research on the two parameter model proposed by Saleh [29] – that the amplitude and phase distortion caused by a PA can be modelled as independent functions of the modulated envelope r_{in}:

$$A(r_{\text{in}}) = \frac{\alpha_{\text{A}} \cdot r_{\text{in}}}{1 + \beta_{\text{A}} \cdot r_{\text{in}}^2} \tag{4.1}$$

$$\Phi(r_{\text{in}}) = \frac{\alpha_{\Phi} \cdot r_{\text{in}}^2}{1 + \beta_{\Phi} \cdot r_{\text{in}}^2} \tag{4.2}$$

As this is a common model used in the design, simulation and evaluation of linearisation methods, this model will also be used to evaluate the performance of the proposed predistortion linearisation method alongside the polynomial based models that have been extracted from the ZFL-2000[1].

[1] www.minicircuits.com

For the purposes of this research, a ZFL-2000 amplifier available from Minicircuits was chosen. As with most PAs the ZFL-2000 amplifier has a transfer function which distorts the amplitude and phase of a signal. This transfer characteristic was measured by performing a power sweep with a HP8753D network analyser as depicted in Figure 4.1. The HP8753D was configured to perform a power sweep at 130 MHz, with the input power level varied between -15 dBm and 5 dBm at intervals of 0.10 dBm.

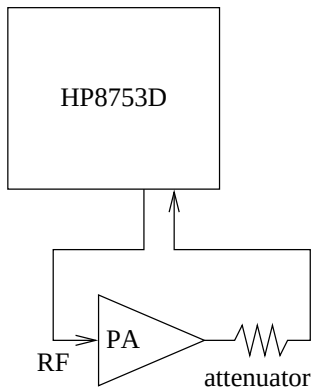

Figure 4.1: Setup used for measuring the amplitude and phase response of the ZFL-2000 amplifier.

The output amplitude and phase data was recorded and used to extract polynomial PA models for simulation purposes. The measured amplitude and phase transfer characteristics of the ZFL-2000 amplifier are shown in Figure 4.2 and are typical of many PAs. The AM-AM distortion is evident as a compression curve, with a 1dB compression point at 0 dBm input power [30] which was verified by measurement. The AM-PM distortion on the output is reasonably low, with a variation of only 1°. Both the amplitude and phase responses of the amplitude are a non-linear function of the input power level.

The transfer characteristics of the ZFL-2000 amplifier were converted into several polynomial models using a least squares polynomial fitting method. Initially both a fifth and seventh order model were investigated, however, as the order of the model is increased, the numerical error in the coefficients causes large error in the intermodulation level outputs. This happens regardless of how well the polynomial appears to model the measured AM-AM and AM-PM distortion characteristic of the PA. The coefficients for the two models are given in Table 4.1. For a microwave PA, the DC

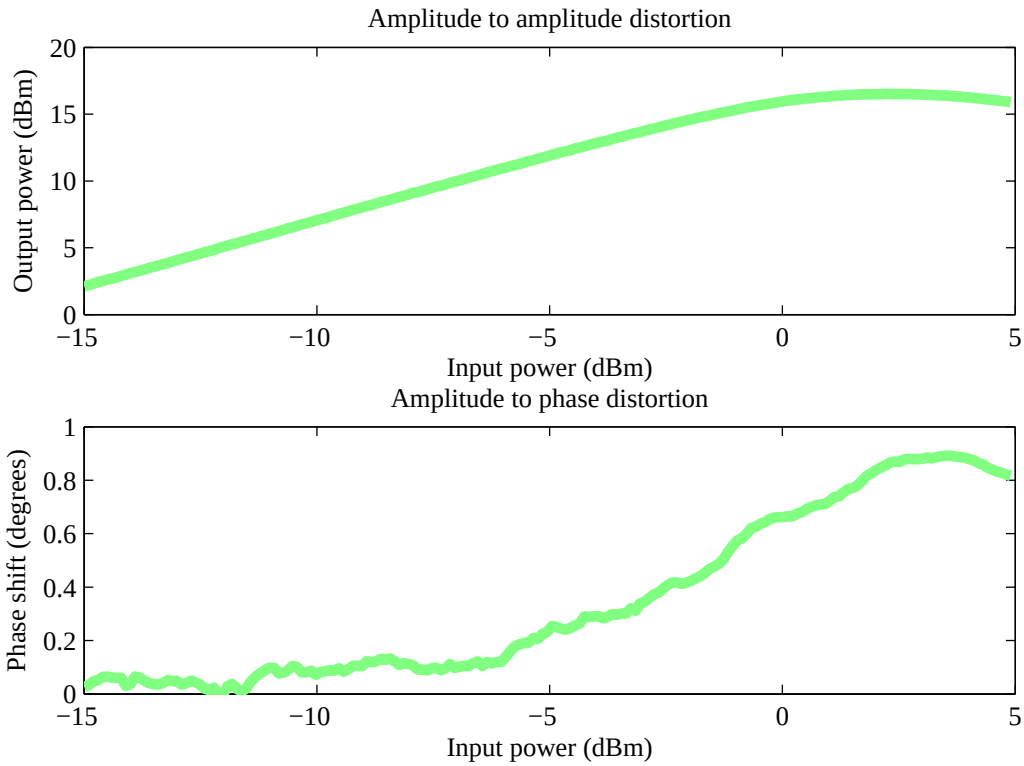

Figure 4.2: Transfer characteristics of the ZFL-2000 amplifier used in the implementation of digital adaptive predistortion linearisation.

coefficient a_0 will ideally be 0, however, this is not the case for the model derived from the measured ZFL-2000 characteristic. In predistortion simulation presented in Chapter 5 a_0 has been set to zero. The transfer characteristic of the Saleh model configured to model the ZFL-2000 is also shown in Figure 4.3 alongside the fifth order polynomial model characteristics and the measured transfer characteristic. The polynomial model appears to model the ZFL-2000 more accurately then the Saleh model. The Saleh model is a function of modulated envelope level,

$$A(r_{\text{in}}) = \frac{8 \cdot r_{\text{in}}}{1 + 0.45 \cdot r_{\text{in}}^2} \tag{4.3}$$

$$\Phi(r_{\text{in}}) = \frac{\pi/3 \cdot r_{\text{in}}^2}{1 + 0.7 \cdot r_{\text{in}}^2}. \tag{4.4}$$

To evaluate the accuracy of the models that will be used with the proposed linearisation scheme a two-tone test of the polynomial models was compared with a

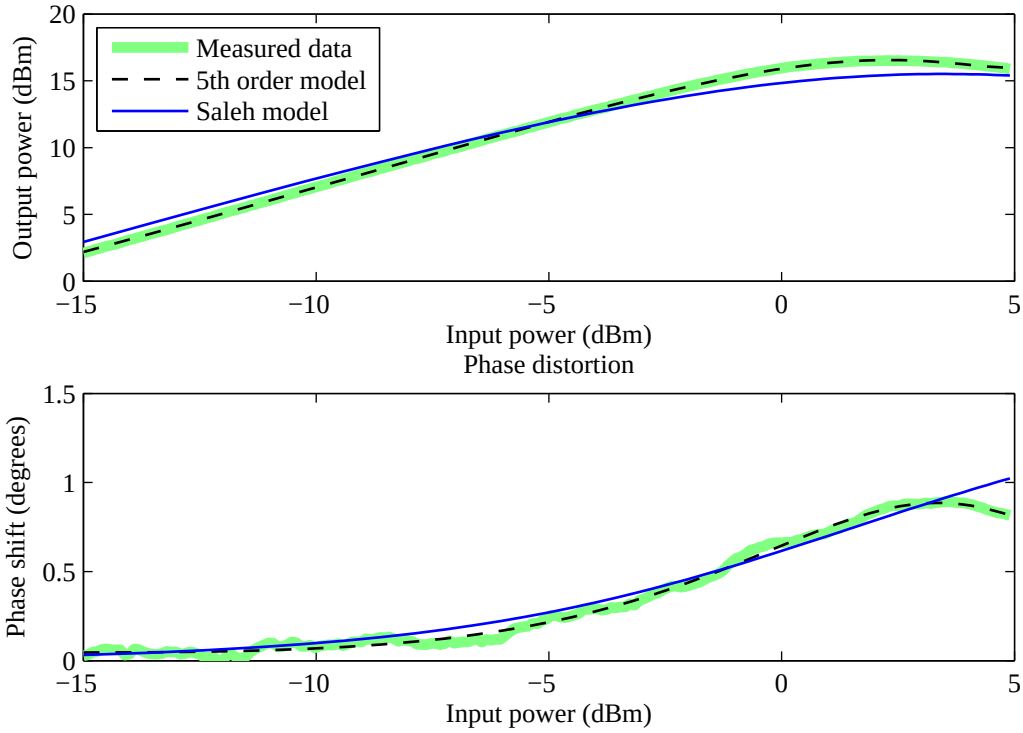

Figure 4.3: Comparison of amplifier model transfer characteristics.

two-tone test of the ZFL-2000. The tests were carried out at 130 MHz with a tone separation of 150 kHz. 150 kHz is the bandwidth of wider bandwidth modulation formats (such as TIA 902.CBAB), and is outside the bandwidth feedback linearisation can typically operate over. The combined input power level of the two-tones was varied between -16 dBm and 0 dBm as the models and PA were designed for this input power range. The simulated 5th order and measured PA output with input levels of -16 dBm and 0 dBm are shown in Figures 4.4 and 4.5 respectively. Note that the fifth order model matches the third and fifth order intermodulation products accurately, but fails to match the seventh and higher order intermodulation products. This is part of the limitations of using a fifth order model, however, raising the order of the model quickly leads to inaccurate modelling of all the intermodulation products due to the increased error from quantisation effects and model inacuracy. For this reason a fifth order polynomial PA model is proposed. From Figures 4.4 and 4.5 it is evident that these models do model the two-tone performance of the ZFL-2000. Tables 4.2 and 4.3 show the intermodulation levels.

PA model coefficients				
$y = \Sigma a_{\mathrm{n}} x^{\mathrm{n}}$				
Coefficient	Fifth		Seventh	
	AM-AM	AM-PM	AM-AM	AM-PM
a_0	0.1142	0.4732	-0.0209	0.4673
a_1	6.3785	-0.0060	7.1178	0.0626
a_2	1.0653	0.0123	2.4647	-0.2856
a_3	1.2735	0.0229	-13.8306	0.6638
a_4	-3.9114	-0.0256	30.3502	-0.7757
a_5	1.3169	0.0063	-33.1413	0.4915
a_6			16.2321	-0.1627
a_7			-2.9158	0.0221

Table 4.1: Power series model coefficients fitted to the measured ZFL-2000 transfer characteristic using least squares curve fitting.

PA model evaluation		
IMD	Measured	Simulated
3	-71.3 dBc	-70.3 dBc
5	N/A	-116.7 dBc

Table 4.2: IMD levels -16 dBm input power level. Note the third and fifth IMD products are below the noise floor of the measuring equipment.

PA model evaluation		
IMD	Measured	Simulated
3	-17.0 dBc	-16.8 dBc
5	-39.1 dBc	-36.7 dBc

Table 4.3: IMD levels relative to fundamentals, with 0 dBm input power level.

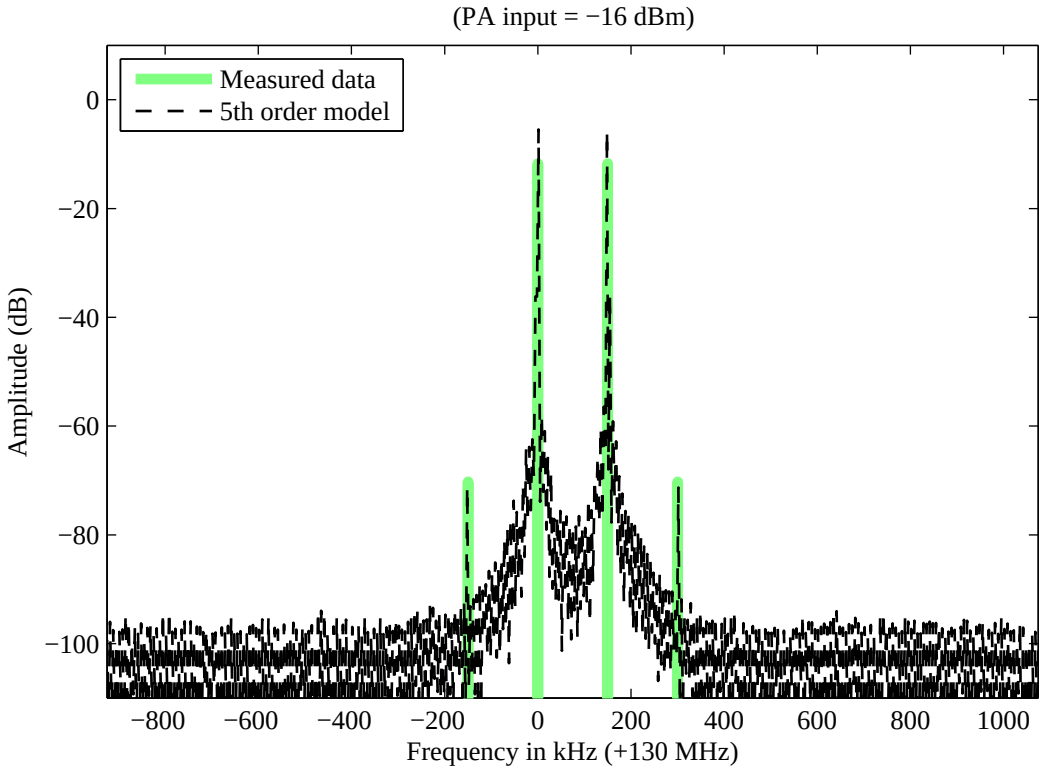

Figure 4.4: Two-tone test: -16 dBm input level.

To further confirm the performance of the models, the level of the 3rd and 5th order intermodulation products, the measured intermodulation levels, along with the simulated intermodulation levels are displayed in Figure 4.6. The deviation of the fifth order intermodulation at the lower power levels is not due to model inaccuracy, but is caused by the noise floor of the equipment used to measure the output of the ZFL-2000 amplifier.

4.2 SYSTEM DESIGN

The main requirement of the predistortion linearisation system is to have a system that can be implemented in real time. This approach places restrictions on the complexity of both the adaption algorithm and the predistorter model complexity. The predistortion linearisation system was designed around a main requirement of implementation in real time. Current FPGA technology provides a high level of parallel processing capability. As presented in Chapter 3 power series models are have been

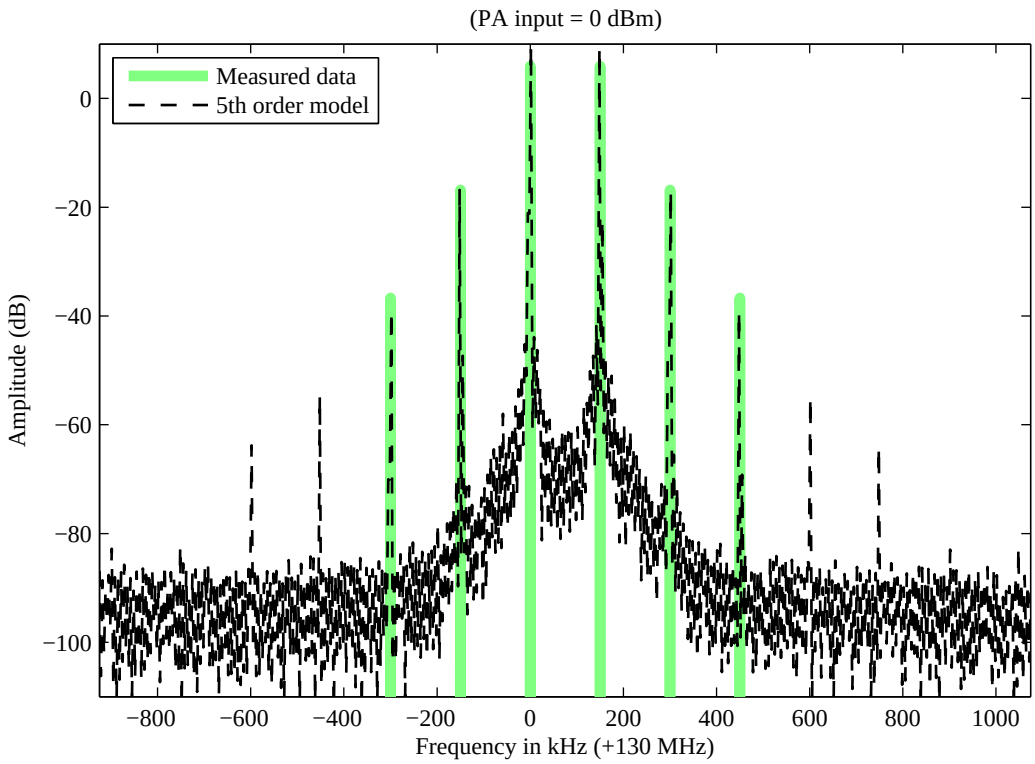

Figure 4.5: Two-tone test: 0 dBm input level.

used in simulations to demonstrate their usefulness in providing AM-AM and AM-PM predistortion linearisation. The design of the predistortion linearisation draws largely from the architectures proposed in [21] and [22] and is shown in Figure 4.7. The complex baseband signal is predistorted by a power series giving independent control of the AM-AM and AM-PM transfer characteristic. This predistorted signal is modulated onto an RF carrier and amplified by a PA. The output of the PA is coupled and used to adapt the predistorter power series coefficients using the LMS algorithm.

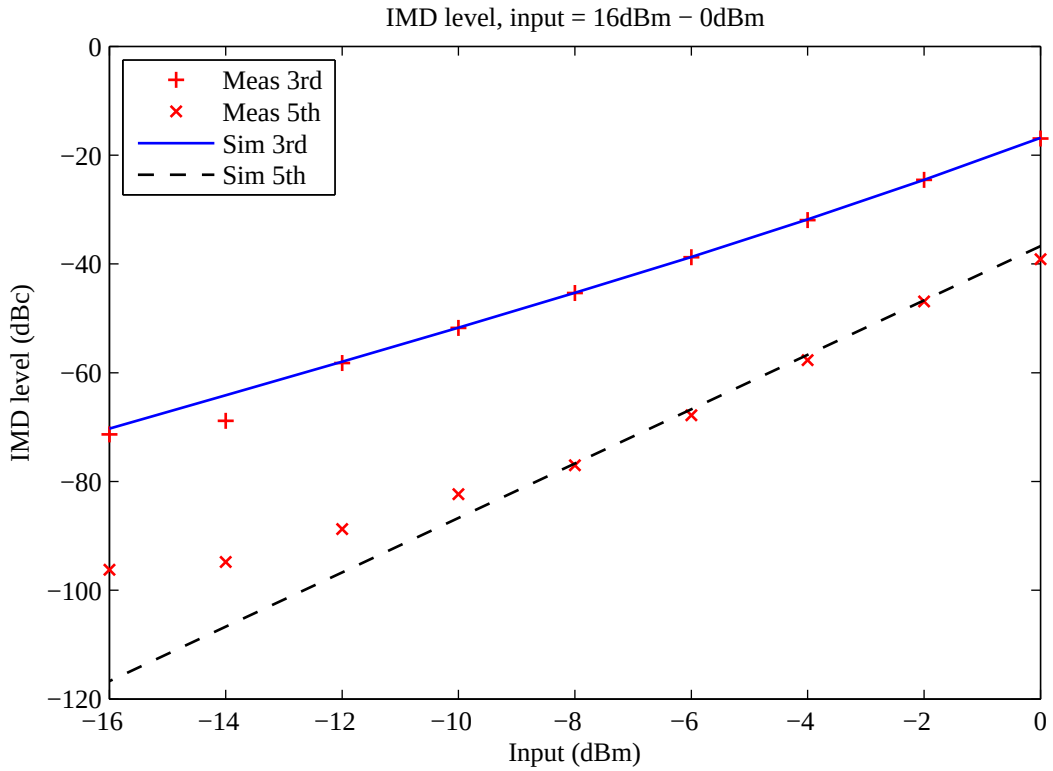

Figure 4.6: Comparison of simulated and measured IMD levels.

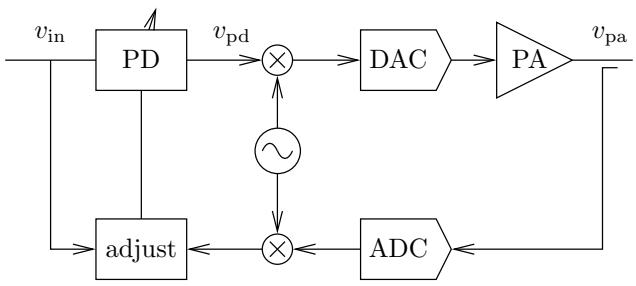

Figure 4.7: High level predistortion.

Chapter 5

SIMULATION VERIFICATION OF DESIGNED PREDISTORTER

This chapter presents the simulation of the predistortion lineariser designed in Chapter 4. Firstly the adaption algorithm is verified by converging to a forward model of the PA transfer function. A power series model-based predistorter is then used to linearise the model PA transfer characteristic discussed in Chapter 4.

As discussed in Chapter 2, the function of a predisortion lineariser is to distort a baseband signal in such a way that the output of the PA is a linear function of the PA input. In order to provide a predistortion linearisation scheme that is independant of the amplifier and modulation scheme, the system must have provision to adapt itself to different component non-linearities and also adaptively track effects introduced by changes in these components over time. As discussed in Chapter 4, the proposed solution is to use a power series to distort the baseband signal, with the coefficients of this power series being updated in real time. The polynomial that corrects for the distortion introduced by the PA can be realised using a standard inverse architecture as shown in Figure 5.1 or a direct inverse architecture. In the standard architecture, the adjustment of the predistorter is calculated from the undistorted input signal and the output from the PA to minimise the error between these two signals.

A direct inverse architecture as shown in Figure 5.2. In this architecture, the output of the PA is sampled and distorted through an inverse model to minimise the error between the input to the PA and the output of the inverse model. The coefficients of the inverse model are then copied to the predistorter. This architecture is often used in inverse control problems to keep the error used to adjust the inverse

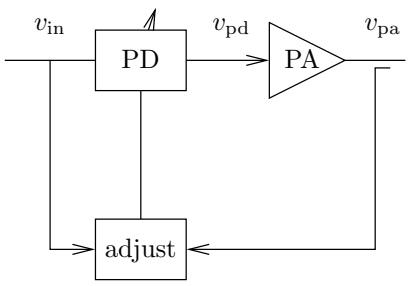

Figure 5.1: Standard inverse predistortion architecture.

model in the inverse domain, which can increase stability. Simulations indicate that there is no difference between the performance of these architectures with the ZFL-2000 PA model. An adaptive algorithm can be used to find the predistortion power series required to correct the distortion added by the PA. The LMS algorithm is well known as being one of the least complex adaptive algorithms to implement and is also one of the more stable algorithms. There is, however, a slower convergence rate, but this is not a concern with the predistortion linearisation problem, as the transfer function of the PA will change slowly. As shown in Appendix A the coefficients of an adaptive FIR filter at time $k+1$ are calculated from

$$W_{\mathrm{k+1}} = W_{\mathrm{k}} + 2\mu e_{\mathrm{k}} X_{\mathrm{k}}. \tag{5.1}$$

This principle is extended to adapt the N power series coefficients $c_{\mathrm{t=k,n}}$

$$c_{\mathrm{t=k+1,n}} = c_{\mathrm{t=k,n}} + 2\mu e_{\mathrm{k}} v^{\mathrm{n}}_{\mathrm{in,t=k}}. \tag{5.2}$$

Where $c_{\mathrm{t=k,n}}$ is the nth of N coefficients at time k.

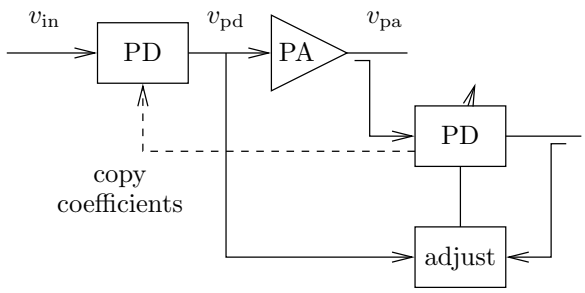

Figure 5.2: Direct predistortion architecture.

5.1 SIMULATION SIMPLIFICATIONS

The predistortion linearisation is to be applied to a digital baseband signal, as shown in Figure 5.3. The baseband signal is distorted before being modulated onto a carrier digital-to-analogue converted and amplified by a PA. The output of the PA is coupled before being demodulated and analogue to digitally converted to be used for adaption purposes. As the modulation process is reversible the system can be simplified to model the modulation after the PA and use a baseband model of the PA. The analogue-to-digital conversion and digital-to-analogue conversion can be modelled by quantisation of the signal, so the simulation system can be simplified as shown in Figure 5.4. The following simulations all use this system.

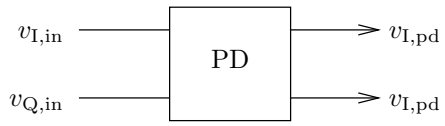

Figure 5.3: Predistortion system architecture.

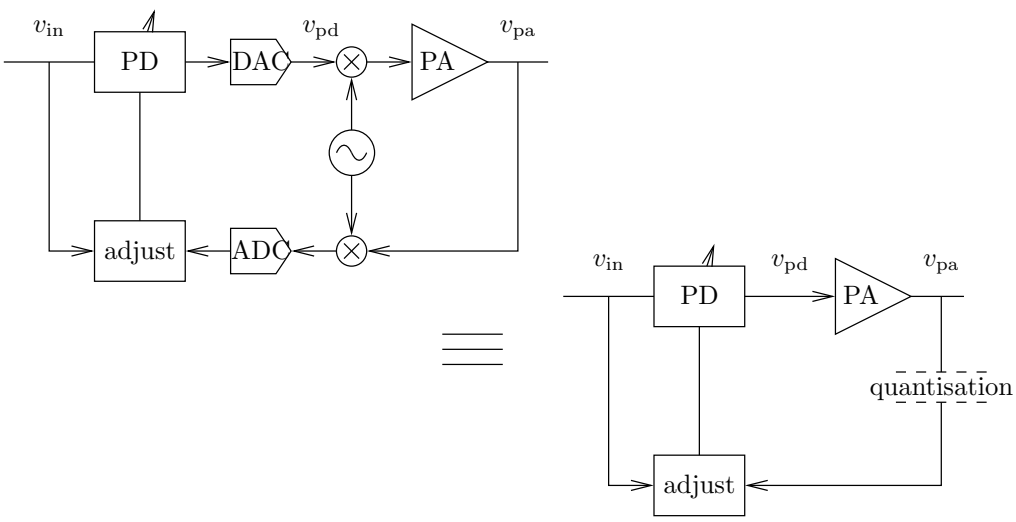

Figure 5.4: Simplified simulation system.

5.2 FORWARD CONVERGENCE VERIFICATION

To verify the operation of the LMS algorithm to adapt the coefficients of a power series, the configuration shown in Figure 5.5 was tested in Matlab. The two-tone

input signal, v_{in} has a tone separation of 150 kHz. This signal is distorted by a power series PA model, the output of which v_{pa} is used as the desired signal v_{d} to adapt the LMS model coefficients. The LMS adaption algorithm updates the coefficients of the LMS model to minimise the difference between v_{lms} and v_{pa}. The PA is modelled using a fifth order power series, extracted from the measured characteristics of the ZFL-2000. The aim of this exercise was to test the convergence of the algorithm to a forward model (same transfer characteristic) of the ZFL-2000 AM-AM characteristic, as the coefficients of this power series are known.

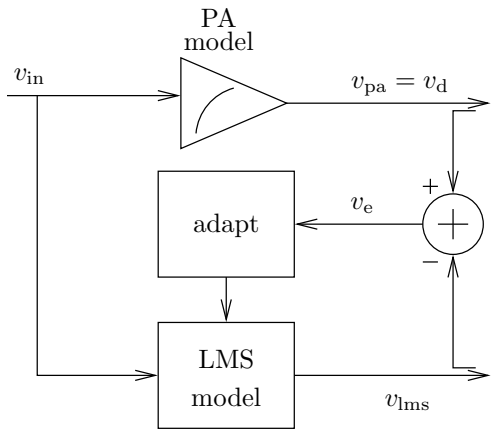

Figure 5.5: LMS adaptive power series configuration used to test convergence on a forward model of the amplifier.

Figure 5.6 shows the initial convergence of the coefficients along with values after steady state has been reached. The initial state of all coefficients being set to zero means the system has a large error as the LMS algorithm starts. As the error is large, the system quickly approaches the ideal value but as error decreases, the convergence rate also slows down. Although this gives the LMS adaption a long convergence time, the steady state error is small. When the adaptive predistortion linearisation coefficients have converged, the change over time will be slow, thus the LMS algorithm is ideal for this type of problem.

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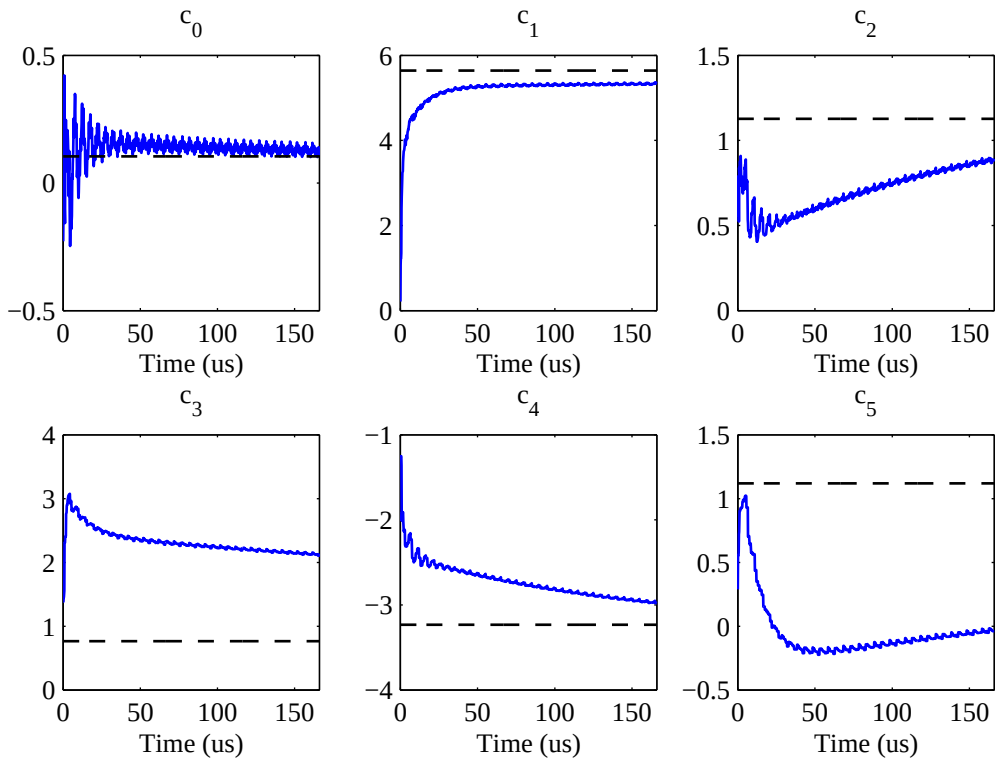

Figure 5.6: Convergence to the forward PA model coefficients from initialised values.

5.2.1 Inverse predistortion

As the LMS adaptive algorithm has been demonstrated in adapting a power series to minimise an error function, the predistortion linearisation system depicted in Figure 5.7 is simulated. The input signal v_{in} is predistorted with an amplitude expansion to correct for the compression characteristic of the PA. The baseband signal is also multiplied by a linear gain equal to the required total system gain to form a desired signal v_{d}. The output from the predistorter v_{pd} is distorted with the transfer characteristic of the PA by a power series v_{pa}. The error signal is calculated from v_{d} and v_{pa} and used to adapt the coefficients of the predistorter as detailed in Appendix A. The desired v_{d} signal into the system is a linear gain of the input and the PA v_{pa} output is fed back into the algorithm for error calculations. The only knowledge of the PA transfer characteristic the system has is the distorted version of the input that is fed back and used for error calculation and adaption of the coefficients. In this initial investigation of adaptive predistortion linearisation, the amplitude distortion

characteristic is linearised without phase distortion.

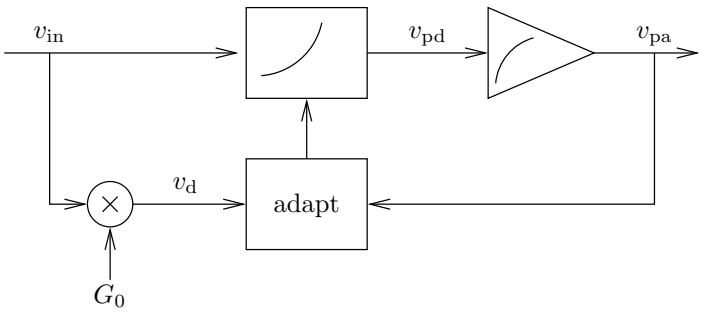

Figure 5.7: LMS Adaptive predistortion system diagram.

Figure 5.8 shows the convergence of the predistortion model coefficients. Note that the coefficients of the inverse of the PA transfer characteristic converge at a similar rate to the forward model coefficients. This is because the value of μ is not optimised for either case. Stability also becomes more of a problem with the inverse model and therefore the value of μ must also be smaller.

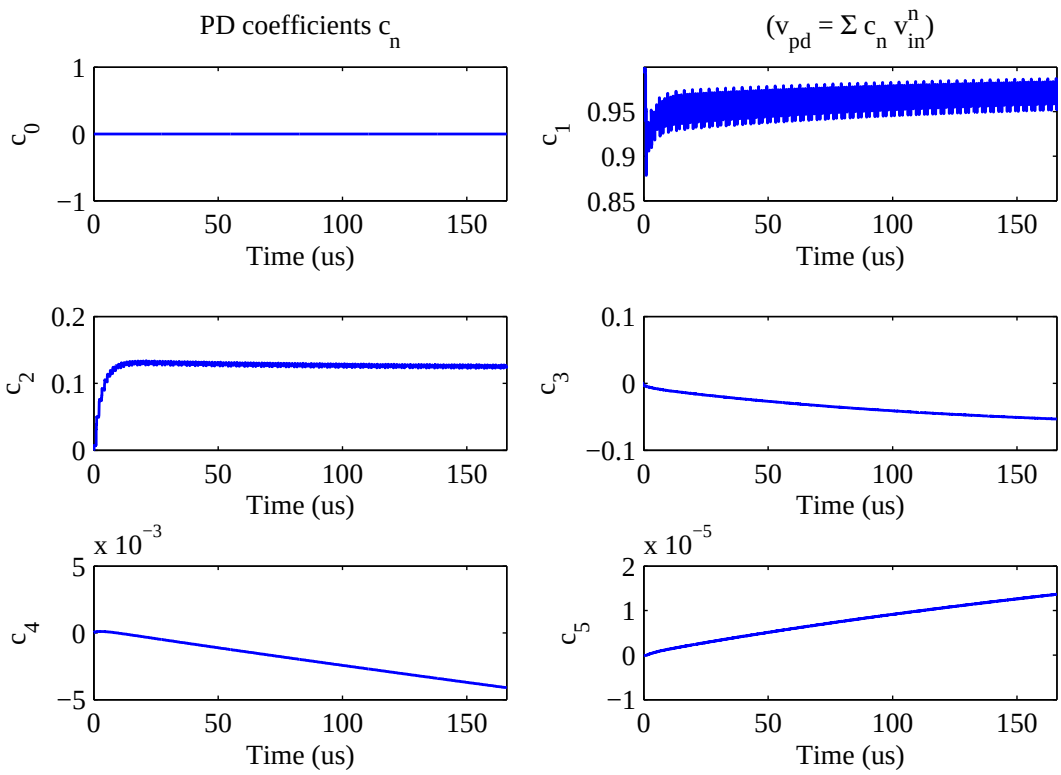

Figure 5.8: Convergence of the coefficients of an amplitude correcting adaptive predistortion linearisation system.

The transfer functions of both the amplifier and the predistorter are shown in Figure 5.9. The predistorter has a gain of approximately one, with an expansion characteristic. There is a limit to the range that can be linearised, since if the predistorter attempts to linearise too far into the compression region, an increase in the input power level will result in a decrease in output power. This will cause the predistorter to further increase the input power to correct for the lower peak output power, which leads to a further distorted PA output. Both the corrected and uncorrected spectrums are shown in Figure 5.10. It is evident from this that adaptive predistortion linearisation can significantly reduce intermodulation from caused by the PA's AM-AM characteristic. Additional frequency components in the corrected spectrum is caused by jitter on the predistorter coefficients, as steady state has not been reached in Figure 5.10.

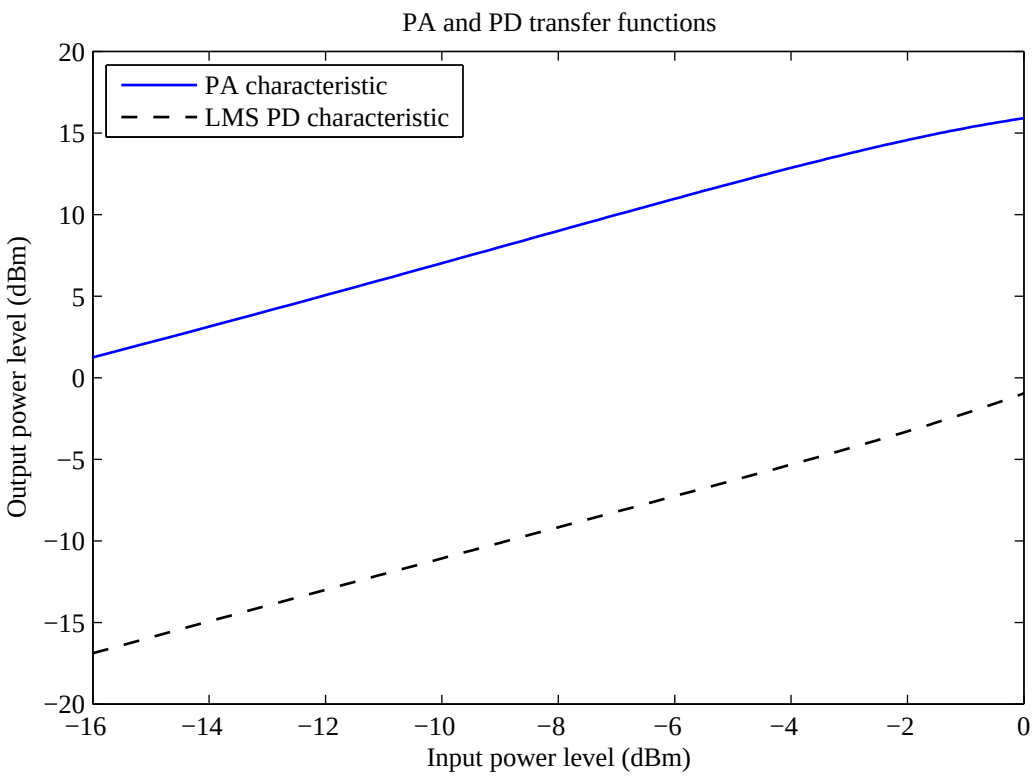

Figure 5.9: PA and predistortion linearisation transfer functions.

The above examples of adaptive predistortion concern only the amplitude distortion as this is easier to observe. However as is shown in Section 4.1, the PA transfer

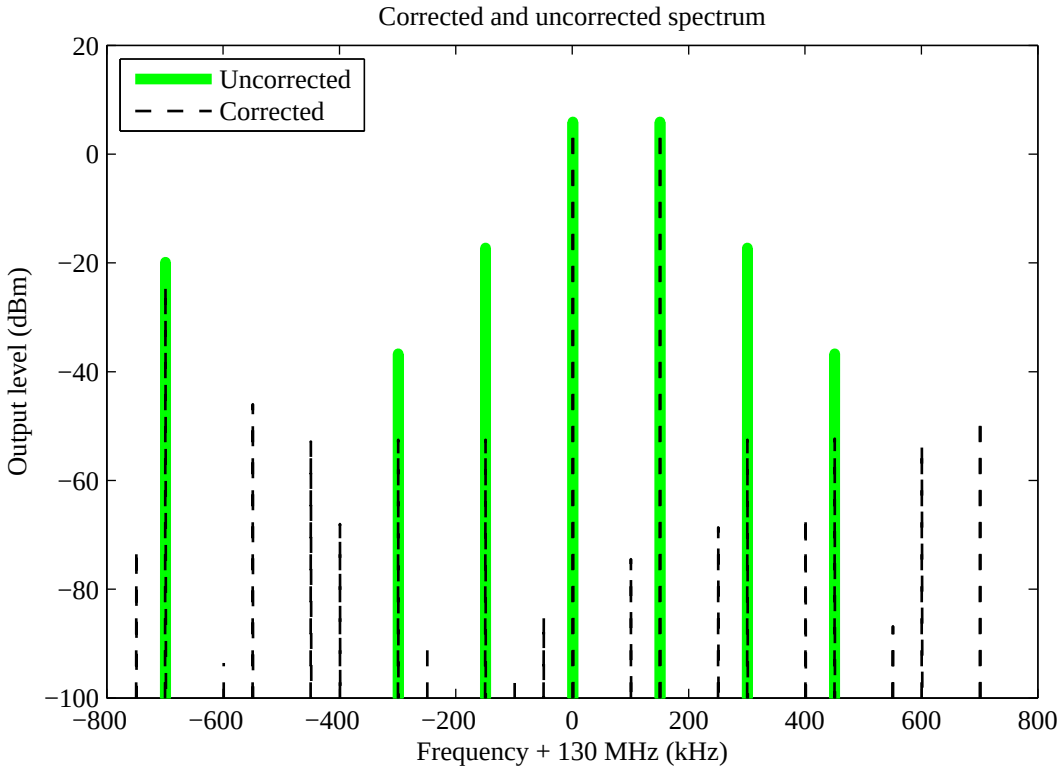

Figure 5.10: AM-AM predistortion linearisation spectrum, with correction enabled and disabled.

characteristics will introduce both amplitude to amplitude (AM-AM) distortion and amplitude to phase (AM-PM) distortion to the input signal. Thus the predistorter must apply both an amplitude and phase predistortion to the input signal. The system has been designed around a polar representation of the baseband signal and PA, allowing independent AM-AM and AM-PM predistortion power series models. These could be converted into Cartesian representation for implementation with complex baseband I and Q. Figure 5.11 shows how the amplitude and phase predistortion is applied to the signal. This system is similar to the previous amplitude only system. The baseband signal is reduced to its magnitude and phase components, to allow for the amplitude and phase predistortion to be applied independently. The transfer functions after the system has had time to converge are shown in Figure 5.12. The reduction in the intermodulation products by the converged predistortion system is shown in Figure 5.13.

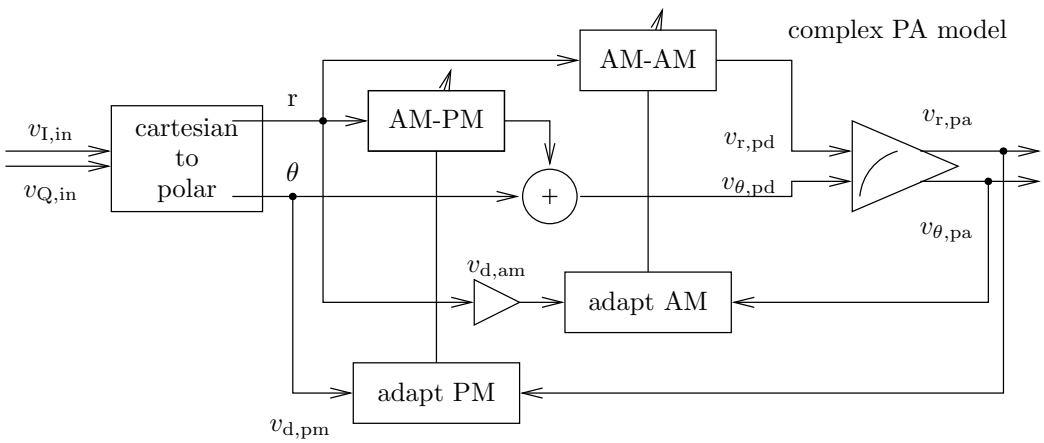

Figure 5.11: System diagram of an adaptive predistortion linearisation system to correct for both amplitude and phase distortion.

5.2.2 Tracking

The main advantages of an adaptive predistortion linearisation system are twofold:

1. The system is not designed around a particular amplifier transfer characteristic and can therefore be used to linearise PAs in many different configurations.

2. As the transfer characteristic of the amplifier changes due to component ageing, temperature fluctuations and its' environment, the predistorter will track the changes automatically maintaining an optimal level of linearisation.

To test the performance of this aspect of the predistortion linearisation scheme, the adaptive system was brought to a point of convergence and then the PA model parameters were changed and the system monitored. Figure 5.14 shows the transfer function before and after the PA model coefficients were changed and the transfer function of the predisorter. Only the first, third and fifth order coefficients were changed, as the even order coefficients do not effect the intermodulation levels.

To illustrate the convergence of predistortion coefficients after the PA transfer characteristic is changed, Figure 5.15 shows the predistorter coefficients as it adapts from a converged state. As is shown in Figure 5.15 the odd order coefficients which perform the intermodulation correction are close to converged within approximately 10000 samples, which corresponds to 166 us with a clock rate of 60 MSPS.

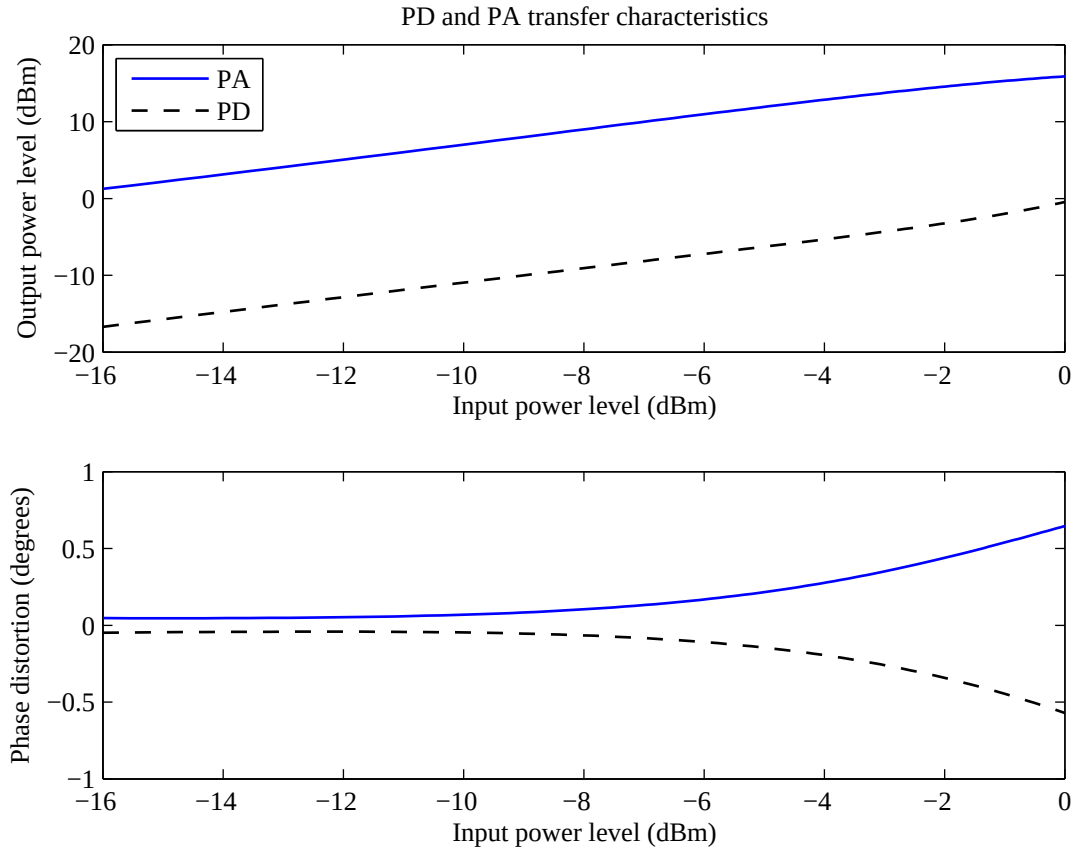

Figure 5.12: Amplitude and phase transfer functions of PA and predistortion lineariser.

Although the system will take time to converge fully, the reduction of the third and fifth order intermodulation products to below the seventh order intermodulation product as shown in Figure 5.16 is reached within 1000 samples (16 us). This is a slightly different situation to the properties a PA would exhibit due to temperature changes, as this is an instantaneous transfer function change. Due to the nature of the LMS algorithm continually adapting the coefficients to minimise the error, tracking PA changes is handled well by the predistortion linearisation system.

5.2.3 Quantisation

Implementation of the adaptive predistortion is performed using fixed point arithmetic, which will suffer from quantisation effects. Within the FPGA there are enough programmable logic resources to allow for data paths as wide as is required to repre-

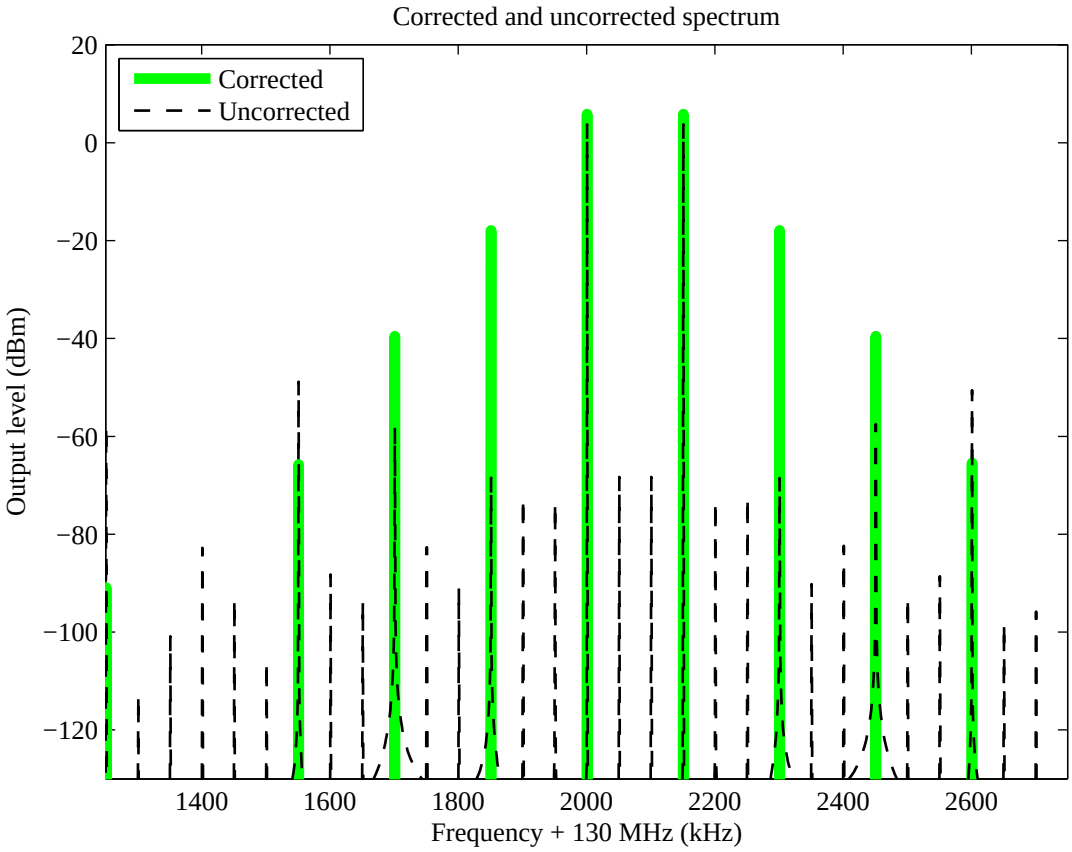

Figure 5.13: Uncorrected and corrected spectrums with amplitude and phase predistortion.

sent the signals. The main restriction of the system is at the DAC and ADC interfaces. These data widths are restricted to 14 and 10 bits respectively. In order to simulate the effect the quantisation will have on the system, quantisation to 10 bits was done as shown in Figure 5.17. Figure 5.18 shows the spectrums of a predistortion system modelling the quantisation effects of the DAC and ADC interfaces. It is obvious, yet important to note that the system still converges with quantisation noise.

5.3 PERFORMANCE

The performance of the system as a whole can only be formally evaluated after the implementation has been completed, however, simulation does give an indication of the performance. Figure 5.13 shows how well the system can reduce the third and fifth order intermodulation products with a seventh order predistorter. Table 5.1 shows the

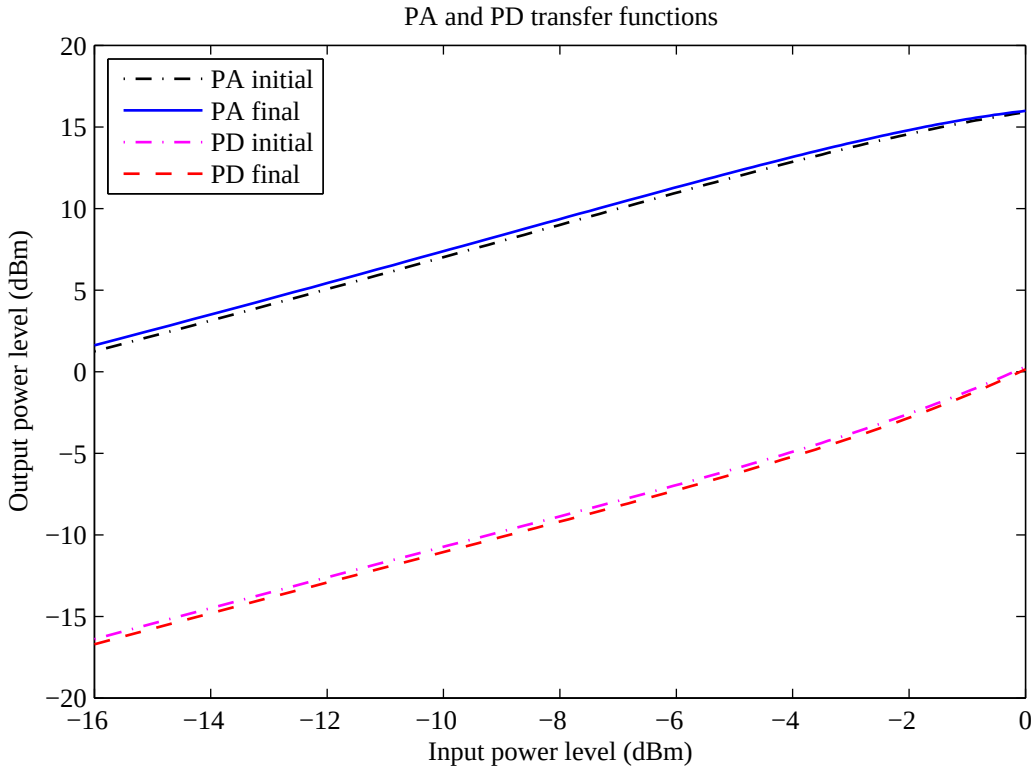

Figure 5.14: Transfer functions of PA and predistorter, as the PA model characteristic changes.

level of the third fifth and seventh order intermodulation products with and without predistortion linearisation. From these simulation it is clear that amplitude and phase predistortion linearisation can provide substantial increase in adjacent channel power ratio (ACPR) – in the order of -64 dBc. Changes in the overall design of the system may provide better correction, however, these will be further discussed in Chapter 7.

IMD Levels		
	Uncorrected	Corrected
Fundamental	6 dBm	4 dBm
3rd order IMD	-18 dBm	-85 dbm
5th order IMD	-39 dbm	-76 dBm
7th order IMD	N/A	-60 dBm

Table 5.1: IMD levels with AM-AM and AM-PM predistortion correction.

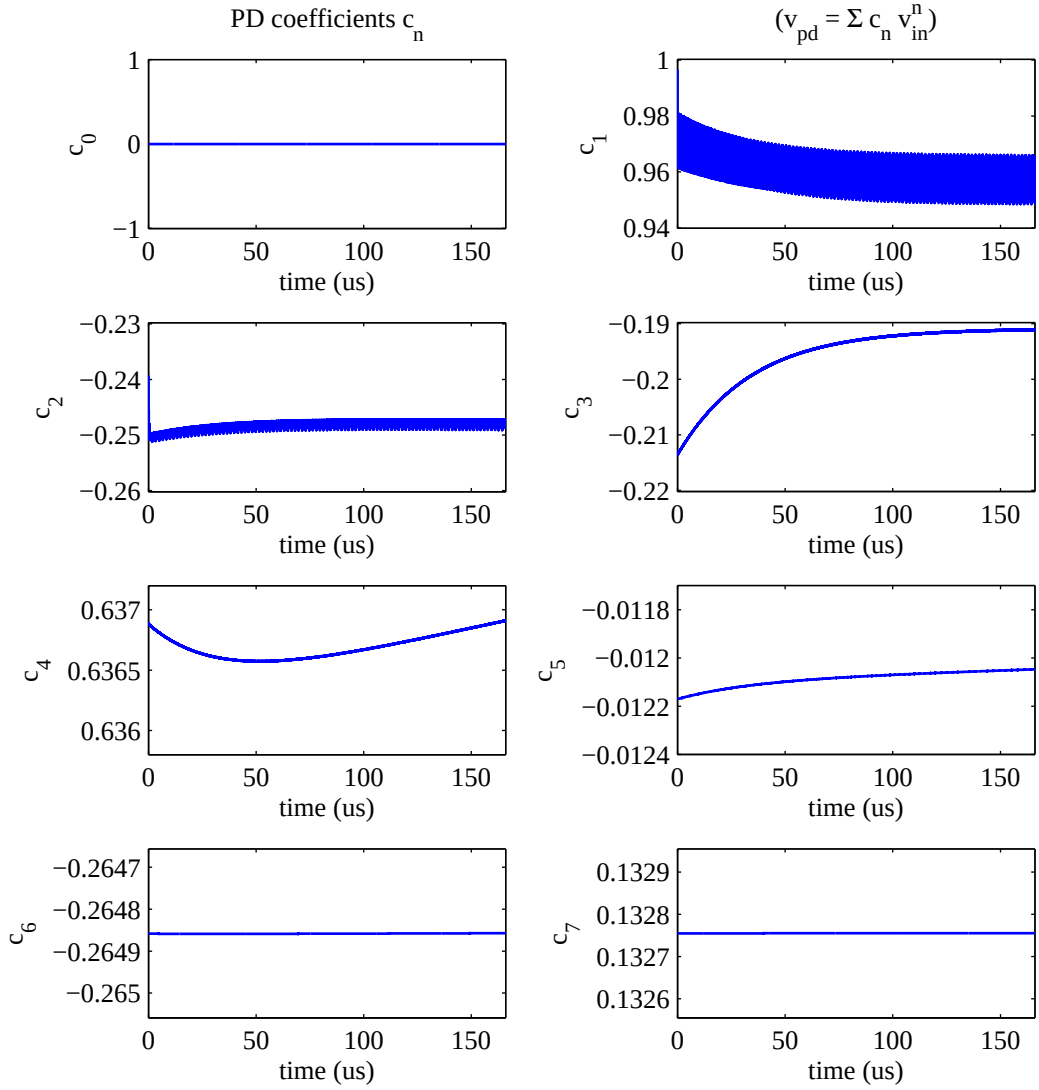

Figure 5.15: Predistorter coefficients changing to track a change in PA transfer characteristic.

IMD Levels		
	Uncorrected	Corrected
Fundamental	6 dBm	4 dBm
3rd order IMD	-18 dBm	-85 dbm
5th order IMD	-39 dbm	-76 dBm
7th order IMD	N/A	-60 dBm

Table 5.2: IMD levels with AM-AM and AM-PM predistortion correction.

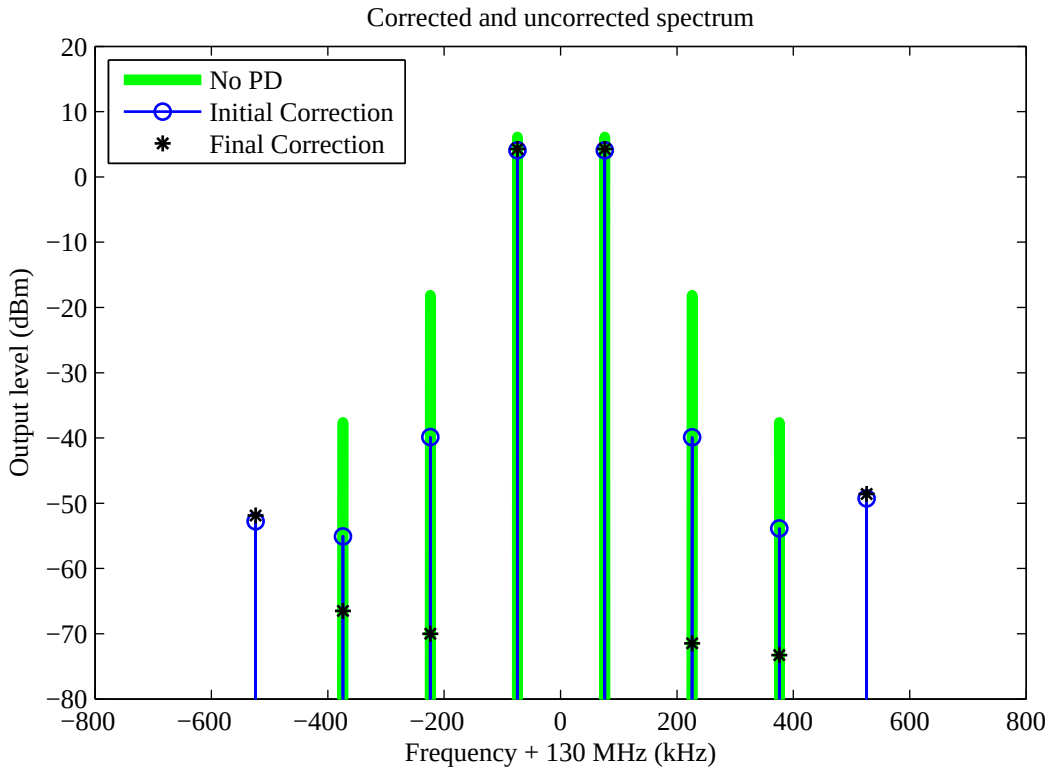

Figure 5.16: Linearisation of a changing PA transfer characteristic.

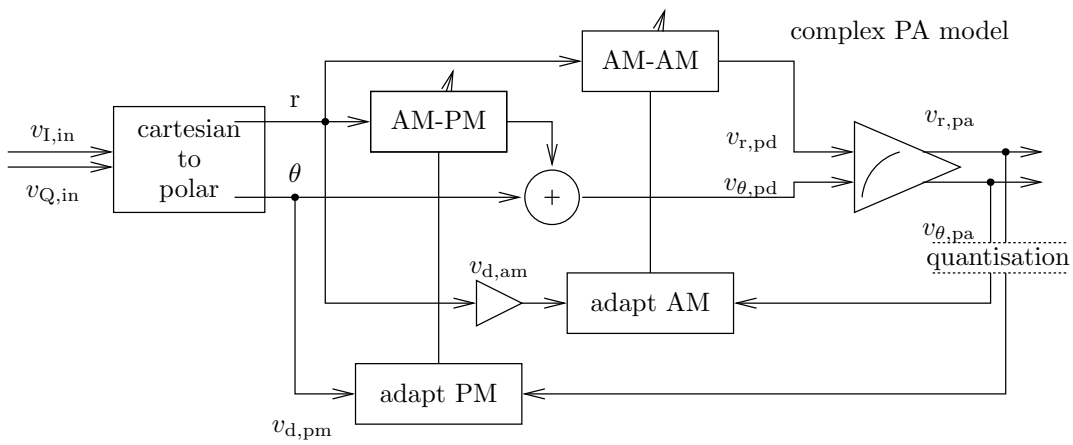

Figure 5.17: Predistortion linearisation with quantisation effects.

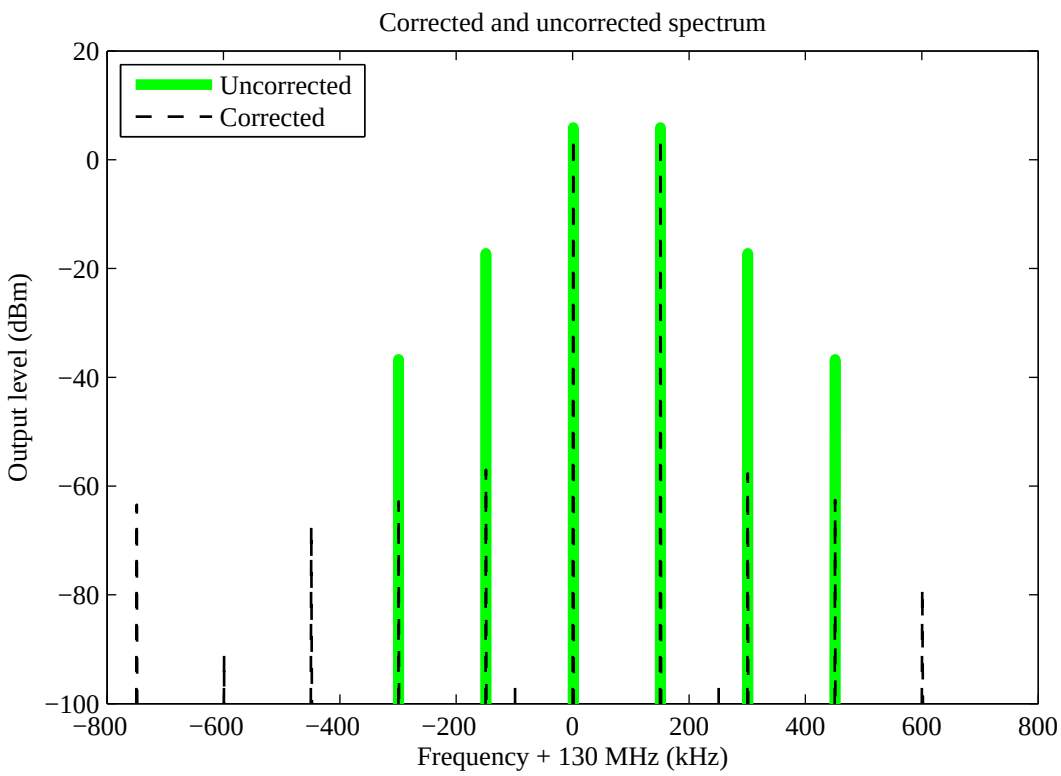

Figure 5.18: Spectrum of correction with quantisation.

Chapter 6

IMPLEMENTATION

This chapter discusses the implementation and verification of the predistortion linearisation scheme as proposed and simulated in the previous chapter. The VHDL simulation method is also discussed. Before discussing the details of each functional block of the predistortion linearisation system, the system in its entirety is introduced. The system can be broken into two main sections:

1. The digital part of the system, which is essentially inside a field programmable gate array (FPGA)

2. The analogue section which includes the power amplifier (PA) being linearised.

Furthermore, the digital section is divided into two clock domains with baseband DSP at a 60 MSPS and the RF functions performed at a 120 MSPS.

The signal flow of the system is as follows: The baseband signal is generated using co-ordinate rotation digital computers (CORDIC) to produce a single tone, with a sample rate of 60 MSPS. This baseband signal is predistorted using a polynomial which has adjustable coefficients. The predistorter has an ideal transfer function which is the inverse of the non-linear transfer function of the PA. The adaption block employs a least means squared (LMS) algorithm to minimise the error between the actual output of the PA and a scaled version of the input to the predistorter (PD) by iteratively adjusting the coefficients of the predistorter power series.

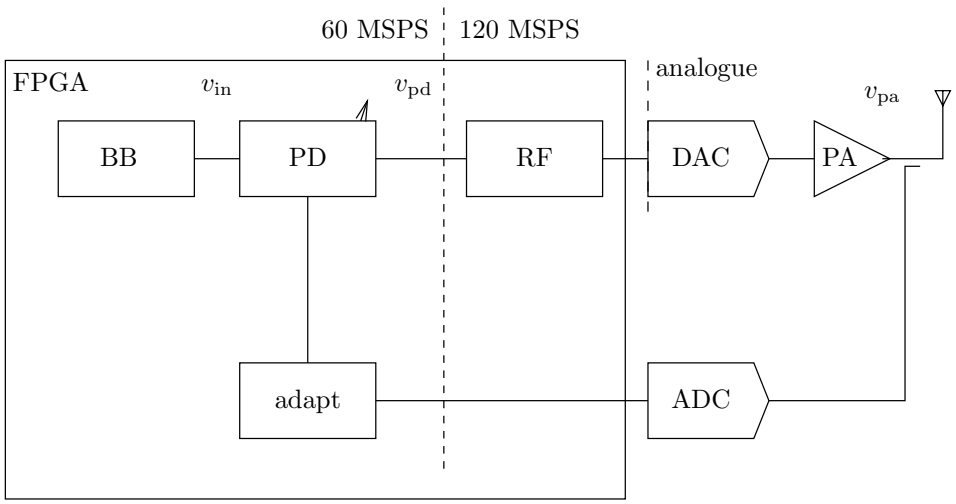

Figure 6.1: High-level predistortion linearisation system diagram.

6.1 SYSTEM HARDWARE

As mentioned in Chapter 4 the predistortion linearisation method has been designed to take advantage of the parallel processing capabilities of FPGA-based technology. The development platform in Figure 6.2, consisting of a digital board and an analogue interface board, was chosen to implement the linearisation scheme. The DSP functionality was written in VHDL and synthesised for the FPGA. Unlike conventional digital signal processors (DSPs), which perform operations sequentially, FPGAs can be programmed to perform many different operations in parallel and at different clock frequencies. The combination of this parallel processing and pipelined architecture provides a throughput higher than what would be available using a DSP or similar device. The theory behind the architectural advantages of an FPGA is discussed further in Section 6.2.

The digital board provides an EP1S25 Stratix I FPGA from Altera[1], along with digital output lines, LED outputs, an RS232 interface to control the design and a joint test action group JTAG interface for programming and extracting signals from the FPGA. The FPGA device has 25,000 logic elements, 10 DSP blocks and 80 dedicated multipliers. Dedicated multipliers and DSP blocks aid in high-speed multiplies and multiply accumulates which are required in the implementation of the power series

[1] www.altera.com

and filtering at high sample rates.

The analogue interface board provides the conversion required to take the digitally processed baseband signal in and out of the analogue domain. The digital to analogue converter (DAC) is a DAC5672 [31] from Texas Instruments[2] which has a maximum clock frequency of 200 MSPS and a data width of 14 bits. The analogue to digital converter (ADC) used in the feedback path is performed by an LTC2232 [32] from Linear Technologies[3], which has a maximum clock frequency of 105 MSPS and a data width of 10 bits. As all the predistortion is applied at baseband using DSP techniques, the interface between the analogue and digital domains is a crucial part of the system. In the forward path the DAC limits the output performance of the system with its spurious performance and noise floor. A clock frequency of 120 MSPS was chosen for the DAC, as it far exceeds the required clock frequencies for the RF carrier of 6 MHz being produced. With a 120 MSPS, 6 MHz output, the DAC has a noise floor of -85 dB and an spurious free dynamic range (SFDR) of 87 dBc [31]. In the feedback path the LTC2232 with a noise floor of -85 dB [32] limits the performance of the feedback path. The ZFL2000 PA, as characterised in Chapter 4 is used to provide a comparison between the simulations and real time implementation results

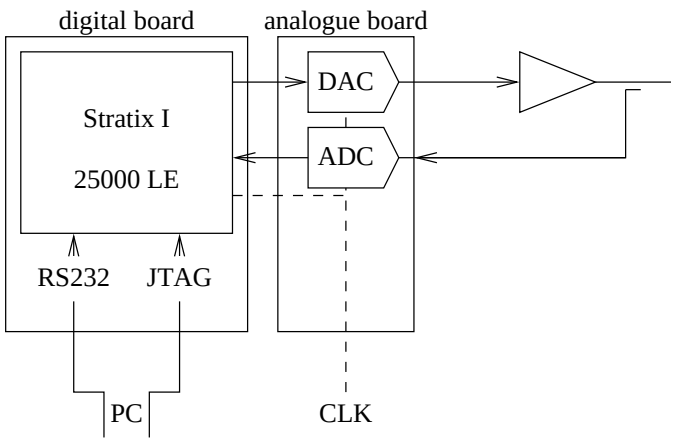

Figure 6.2: Hardware platform diagram.

[2]www.ti.com
[3]www.linear.com

6.2 COMPONENT VERIFICATION

Following is a discussion of the development and functionality of each major component developed for the implementation. Each hardware block was developed independently, with functionality being simulated in ModelSim v6.1c[4], with the verified components being used on the FPGA. The interaction of these components is discussed below, followed by a more detailed explanation of the functionality of each block. Each component was designed to maximise data throughput with pipeline stages and high levels of parallel processing.

The transition from a simulated system to real-time implementation brings about two significant changes to the way math functions are performed. Firstly the simulations were performed using 32 bit floating point arithmetic, whereas the implementation makes use of fixed point arithmetic. In the course of simulation, the feedback signal was restricted to 10 bits to briefly investigate the effects of quantisation at the most restrictive point in the system. This, however, does not take into consideration the quantisation and truncation effects at other points in the system.

In order to design a wide bandwidth predistortion lineariser, a high sample rate baseband is needed. Like all synchronous systems, FPGA-based design is basically made up of combinational logic blocks separated by registers as shown in Figure 6.3. Data takes time to propagate from the input of combinational logic to become valid outputs (propagation delay). Registers require the data to be valid for a setup time before an active clock edge and remain valid for a hold time after the active clock edge. The data throughput of the system is set by the clock rate of the registers of the system. The maximum system clock frequency is therefore determined by the longest propagation delay as well as the timing requirements of the registers:

$$T_{\text{min}} = T_{\text{comb}} + T_{\text{setup}} \tag{6.1}$$

[4]www.model.com

where:

$$f_{\max} = \frac{1}{T_{\min}} \tag{6.2}$$

This requires $T_{\text{hold}} < T_{\text{comb}}$ so that data is constant at the input of the register for the T_{hold} duration required after the clock edge.

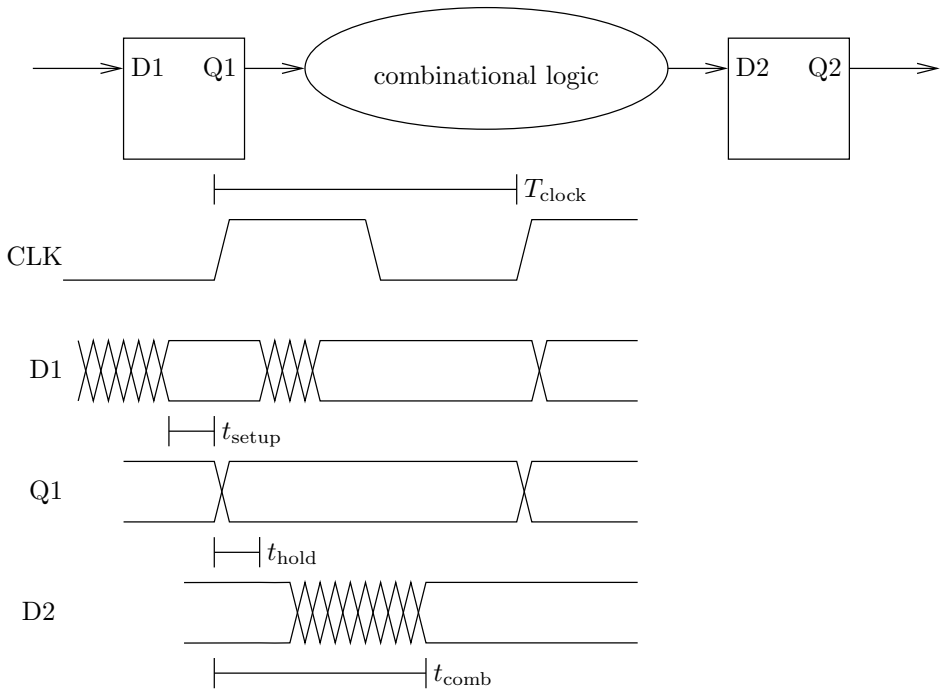

Figure 6.3: Timing diagram showing setup and hold requirements of a typical synchronous section.

As the maximum clock frequency is limited by the length of time taken for a signal to pass through the combinational logic, there are two ways to increase the clock speed.

- Increase the speed of the combinational logic using different manufacturing processes
- Split the combinational logic in half, separating each half by another D flip flop (pipeline).

The former of these is set by the manufacturing of the Stratix device used in this research, leaving only the latter option. This is is known as a pipelined architecture, with each section of combinational logic between two flipflops called a pipeline stage.

Pipelining as shown in Figure 6.4 is used in the implementation of the predistortion linearisation system.

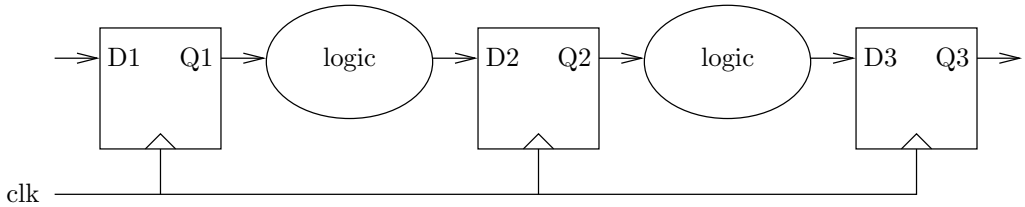

Figure 6.4: Pipelining of combinational logic to increase clock frequency.

The implementation of the predistortion linearisation system as shown in Figure 6.1 is discussed in the following sections. Each of the main components are built out of a hierarchy of smaller, simpler design blocks. Some of these smaller design blocks are interfaces into hardware logic functionality provided by the Stratix family of FPGA devices such as arithmetic, memory and clock functions.

6.2.1 Manufacturer provided logic functionality

Altera[5] [33] provides basic hardware functional blocks (megafunctions) which were used in the implementation of the design. Phase-locked loops (PLLs) were used to condition the input clock signals, while multiplication, addition, subtraction and RAM blocks were used in a number of system blocks.

The Stratix I FPGA [33] has six PLL's which were configured using PLL megafunctions provided by Altera. A PLL megafunction was configured to take a 120 MHz input clock signal and produce 60 MHz and 120 MHz clock signals for use within the FPGA.

Addition, subtraction and multiplication functions were used as building blocks for the main system components of the predistorter. Different configurations were used to create DSP-specific multipliers for the high-speed signal path, as well as allowing a number of different data widths at different points of the system. As the Stratix I has 9 bit DSP blocks, most of the data path used 18 bit wide multipliers and additions. In the case of the power series, the 36 bit output was truncated after multiplication.

[5] www.altera.com

RAM blocks were used in the implementation of circular buffers to synchronise the signals for the adaption process. Table 6.1 summarises the use of megafunctions within the system.

Use of megafunctions	
PLL	
PLL0	60 MHz and 120 MHz system clock derivation
Multiplication	
18 bit DSP	Modulation Demodulation Power Series Adaption Filters
18 bit non-DSP	Constant gain blocks
Addition	
18 bit	Adaption Power series Filters
Subtraction	
18 bit	Error calculation in adaption
RAM	
18 bit	Circular buffers for delay lines Indirectly for SignalTap acquisitions

Table 6.1: Megafunctions used in the predistortion system.

6.2.2 Sinusoid generation

The implementation requires a number of sinusoidal waves with different frequencies. To produce these signals and allow flexibility of amplitude and frequency, CORDICs [34] were used. A CORDIC is an iterative algorithm that can be configured to produce trigonometric, logarithmic and exponential functions in hardware. Sinusoidal signals could also have been generated using a ROM in the FPGA programmed with a sinusoid. The advantage of using a CORDIC is that the output amplitude and frequency can be adjusted dynamically, whereas a ROM would require reprogramming for each different frequency. A CORDIC can be configured in either a rotation mode, or a vectoring mode. In rotation mode, the CORDIC equations are,

$$
\begin{aligned}
x_{\mathrm{n}} &= A_{\mathrm{n}} x_0 \cdot (z_0) - y_0 \cdot \sin(z_0) \\
y_{\mathrm{n}} &= A_{\mathrm{n}} y_0 \cdot \sin(z_0) - x_0 \cdot \cos(z_0)
\end{aligned}
\tag{6.3}
$$

where x and y are input vector amplitudes and n is the iteration number which sets the resolution in bits. So if y_0 is set to zero, the x_{n} and y_{n} outputs are $A_{\mathrm{n}} \cdot \cos(z_0)$ and $A_{\mathrm{n}} \cdot \sin(z_0)$ respectively. To increase throughput in the implementation, an unrolled pipelined version of the CORDIC was chosen. Unrolling the CORDIC architecture uses multiple copies of the logic used for each iteration in parallel, thus increasing the throughput. Pipelined CORDICs were used in rotation mode in the implementation of the predistorter to generate baseband test tones and the RF carrier. A diagram of the unrolled pipelined CORDIC is shown in Figure 6.5.

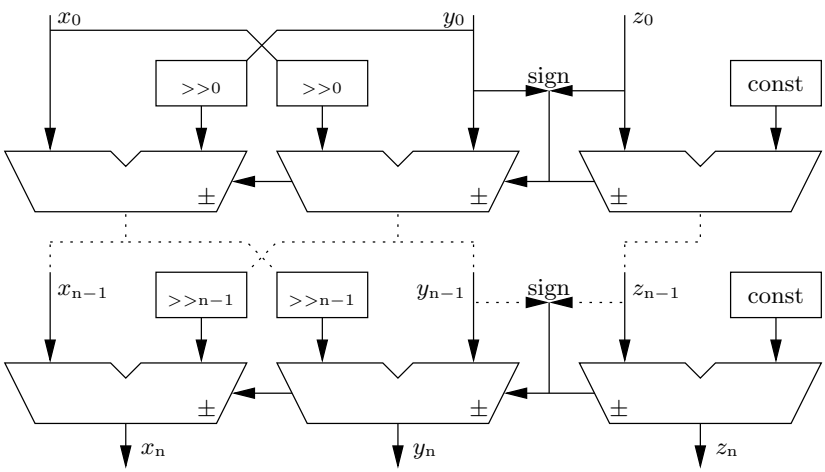

Figure 6.5: Unrolled, pipelined CORDIC.

The diagram in Figure 6.6 shows the block diagram of a CORDIC and a phase accumulator. The phase accumulator produces a rotating phase vector z_0 which sets the frequency of the output sinusoids. Input x_0 sets the amplitude of the output and y_0 is fixed at 0. The frequency word input to the phase accumulator is the value the phase is increased by each clock cycle. Thus the frequency of the output is set,

$$f_{\text{CORDIC}} = \frac{f_{\text{clk}}}{\max(\text{word}_f)} \cdot \text{word}_f \tag{6.4}$$

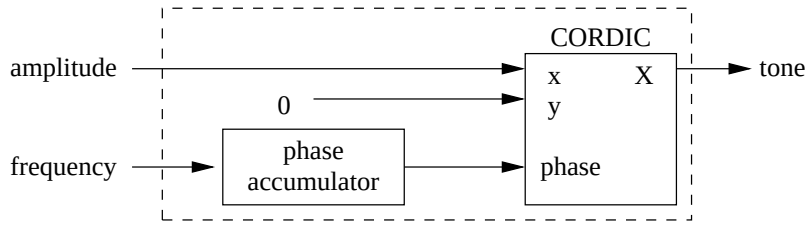

Figure 6.6: CORDIC and phase accumulator.

These CORDIC and phase accumulators are used to produce BB and RF tones for the design.

6.2.3 Modulation and demodulation

For the predistortion system, modulation onto a carrier signal is required in the forward path and demodulation to baseband in the reverse path. These functions are typically implemented in the analogue domain, but can also be performed digitally as in this research. The mixing process is essentially a multiplication of the baseband signal with RF carrier frequency,

$$\begin{aligned} \cos(\omega_{\text{BB}}) \cdot \cos(\omega_{\text{Carrier}}) &= \frac{1}{2}\cos(\omega t_{\text{Carrier}} \pm \omega t_{\text{BB}} t) \\ &= \cos(\omega t_{\text{RF}} t), \end{aligned} \tag{6.5}$$

or in the process of demodulation down to baseband from RF,

$$\begin{aligned} \cos(\omega_{\text{RF}} t) \cdot \cos(\omega_{\text{Carrier}} t) &= \frac{1}{2} \cdot \cos(\omega_{\text{Carrier}} t \pm \omega_{\text{BB}} t) \\ &= \frac{1}{4} \cdot \cos(\omega_{\text{BB}} t \pm \omega_{\text{Carrier}} t \pm \omega_{\text{Carrier}} t) \\ &= \frac{1}{4} \cdot \cos(\omega_{\text{BB}} t \pm 2 \cdot \omega_{\text{Carrier}} t). \end{aligned} \tag{6.6}$$

This said, the modulation and demodulation processes are identical comprising a multiplier as shown in Figure 6.7. The multiplier is configured to be synthesised into DSP blocks to maximise the clock frequency. The local oscilator (LO) is implemented using a CORDIC.

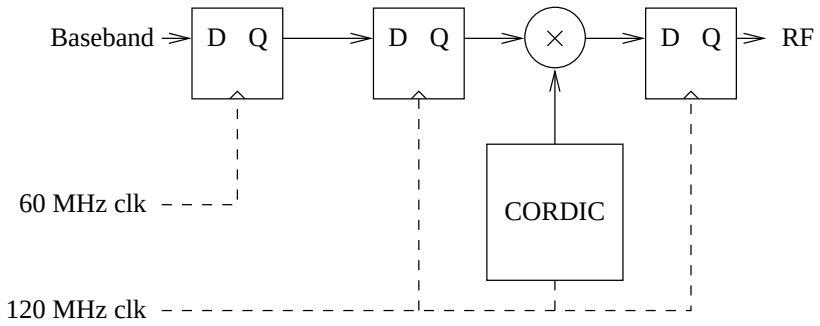

Figure 6.7: Modulator/demodulator architecture.

6.2.4 Baseband recovery

To provide information for the adaption algorithm to operate with, the baseband must be fully recovered from the RF PA output. Following the demodulation process, the baseband signal is contaminated with additional frequency components and also has a phase change caused by delays in both the digital processing and analogue components in the feedback loop. In order to recover all the information for the adaption algorithm, the forward and reverse baseband signals need to be synchronised in the time domain and frequency components that are added by the modulator, demodulator and sampling rate changes need to be removed.

Following demodulation, there are a number of frequency components on the baseband signal. The main unwanted frequency component on the demodulated signal derived above is the 12 MHz component introduced by the process of demodulation as described by Equation 6.6. There are also frequency components at the harmonics of the carrier, produced by the even order terms of the PA non-linearity. These unwanted components are removed by three stages of IIR filters. A notch filter at 12 MHz removes the 12 MHz component, while three second order low pass filters remove the harmonic frequencies. The basic architecture of the filters is shown in Figure 6.8.

Transfer functions for the filters are shown in Figure 6.9.

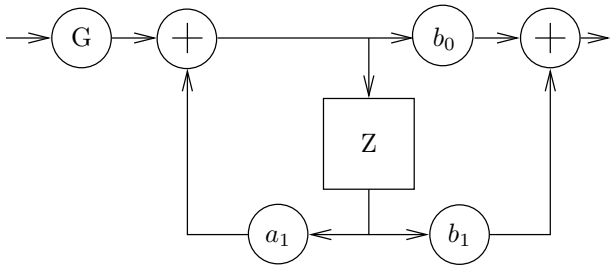

Figure 6.8: Filter architecture.

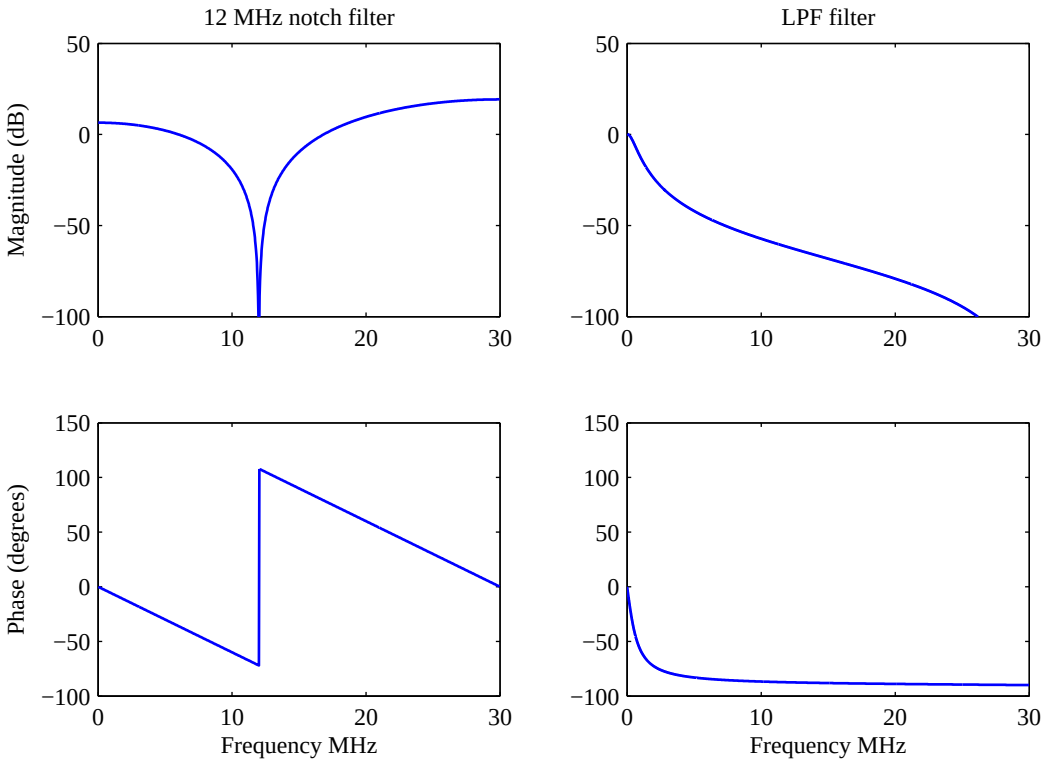

Figure 6.9: Filter transfer functions.

The phase of each of the signals is aligned using three different delay lines to match the total loop delay causing the phase change. Firstly, a delay line in the RF path to the demodulator is used to match the phase of the RF carrier and the RF demodulation. The frequency of the RF signal and the sample rate determine the delay line requirements in order to match the phase of the baseband signals. The RF signal has a frequency of 6 MHz and the system clock frequency of the RF section is 120 MSPS which means the signal is oversampled 20 times. A one clock cycle delay

caused by a register therefore causes a $360/20 = 18^{o}$ degree phase lag with respect to the 6 MHz carrier. This means the phase of the feedback signal and the demodulator RF can be synchronised to within 18 degrees, so the baseband delay line must provide phase adjustment of ±18 degrees at baseband. The three delay lines are all based on a RAM block circular buffer that has a variable delay which is set as the predistortion system runs. Figure 6.10 shows how the filters and delay lines are used to recover the baseband for predistortion adjustment.

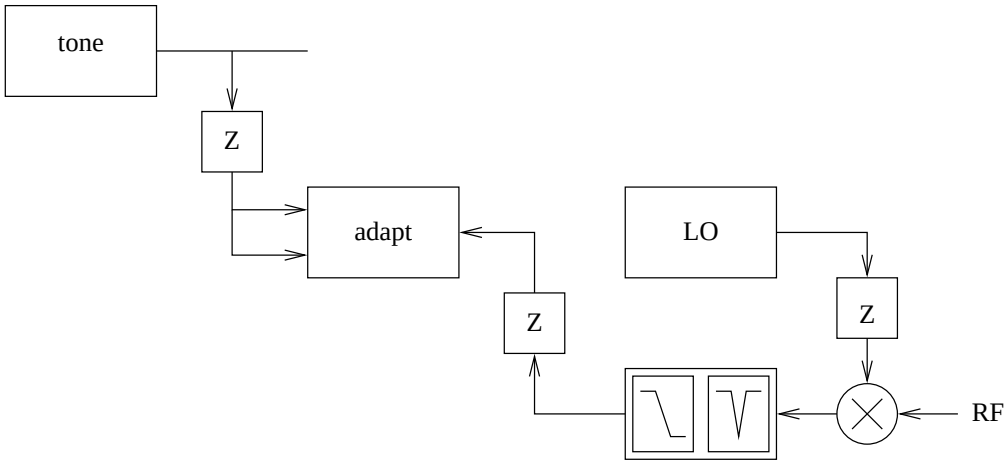

Figure 6.10: Filters and delays used to recover the baseband signal.

6.2.5 Control

In order to control the hardware platform, the graphical user interface (GUI) shown in Figure 6.11 was written using the Python language was used to send control words from a PC via RS232. A universal asynchronous receiver/transmitter (UART) was developed to receive these control words and decode the instructions into a register space used to control the operation of many of the system components. Table 6.2 summarises the control available via RS232. General functionality of the system is controlled with the enabling and resetting of the predistorter, enabling of the modulator and demodulator and the system reset. The baseband frequency is adjustable, as is the amplitude. The amplitude is used to ensure that the predistorter power series multipliers do not overflow. The RF frequency is also adjustable, along with

the amplitude which adjusts the output level to the DAC. The synchronisation of the input, desired and actual signals is controlled by the delay and gain controls.

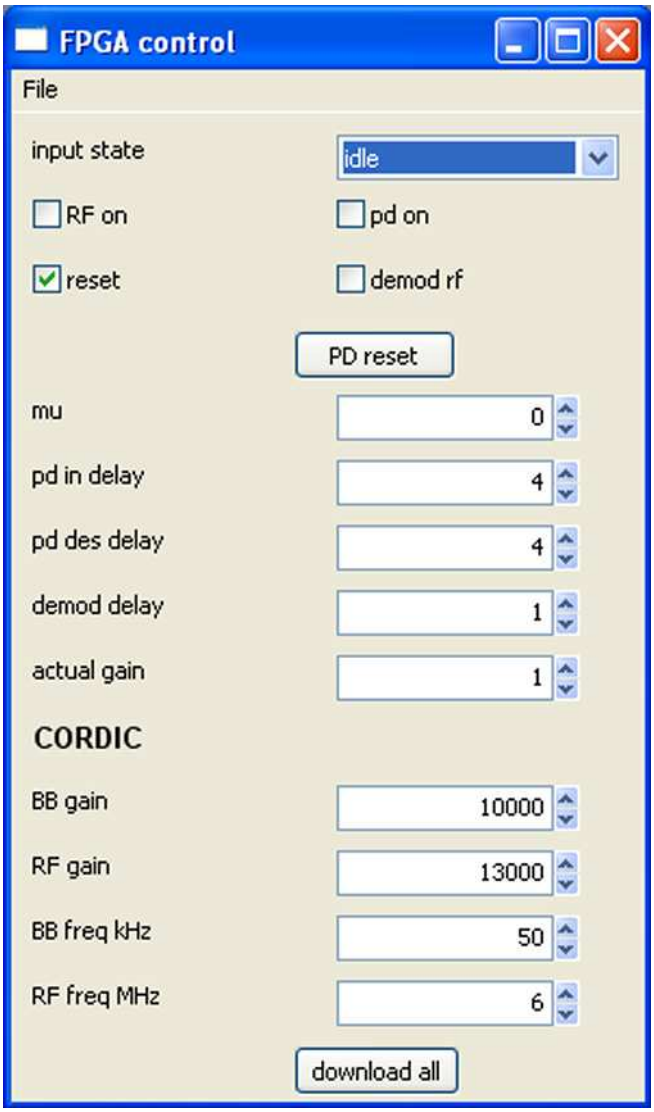

Figure 6.11: GUI used to control the implemented predistorter.

6.2.6 Predistortion

As in the simulations presented in Chapter 5, the predistortion is applied to the baseband signal with a fifth order power series, which is pipelined to increase the maximum clock frequency. The pipeline stages are shown in Figure 6.12. The structure is such that the latency from only one multiply incurred between each register in the pipeline. It is important to ensure the parallel data paths all have the same delay, caused by

RS232 control system	
General	
DAC MUX OUT	Switch the MUX output between the PD output, and the tone output
PD on	Enable the predistorter
RF on	Enable the modulator LO
Demod RF	Enable the demodulator LO
Sinusoidal aspects	
BB freq	Baseband tone frequency
BB gain	Baseband amplitude
RF freq	LO frequency for modulation and demodulation
RF gain	LO amplitude for modulation and demodulation
Adaption parameters	
PD in	Adjusts the delay of the input signal to the adaption block
PD des	Adjusts the delay of the desired signal to the adaption block
Demod delay	Adjusts the phase between the modulator and demodulator
Actual gain	Gain of the predistorter

Table 6.2: Functions of the system controlled via RS232.

the pipeline stages. In the first stage v_{in}^2 is calculated, with v_{in}^3 and v_{in}^4 in the second pipeline stage and v_{in}^5, v_{in}^6 and v_{in}^7 in the third stage. Each power of v_{in} is then multiplied by the coefficients and the outputs are all added together. As there is no DC component to the PD transfer function, the zeroth order term is fixed at zero and therefore not calculated.

In order to verify the functionality of the VHDL power series, its output is compared with the output of the Matlab power series used in the simulation of the predistorter. The same input signal is distorted by a VHDL and a Matlab forward model of the ZFL-2000 PA. Figure 6.13 shows how the power series implementation matches the operation of the Matlab simulation. The timing difference between the simulated predistorter and the VHDL predistorter is caused by the pipelined architecture of the VHDL implementation.

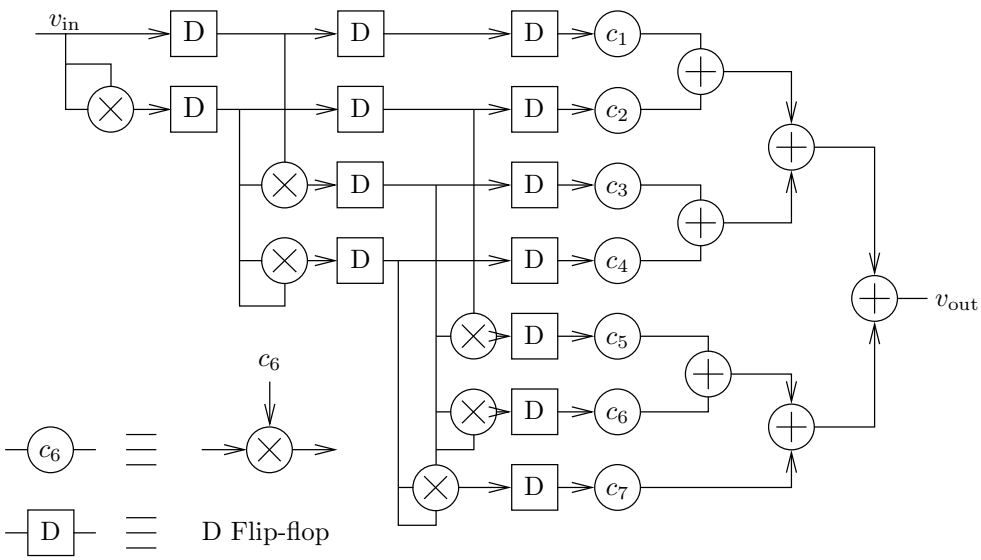

Figure 6.12: Pipelined structure of the power series.

6.2.7 Adaption

The adaption of the predistorter coefficients was achieved using the same LMS algorithm as in the simulation and design of the system. Recall from Chapter 5 the coefficients at time $k+1$ are calculated from

$$C_{\mathrm{k+1}} = C_{\mathrm{k}} + 2\mu e_{\mathrm{k}} v_{\mathrm{in,k}}^{\mathrm{n}}. \tag{6.7}$$

Like the power series the implementation is pipelined to increase the maximum clock rate. During each clock cycle only one of the coefficients is updated, so it takes seven clock cycles to update all seven coefficients. As is evident in Figure 6.14, the LMS adaption block has two paths. One path raises the input to powers of 1 through to 7 whilst the other shifts by a scale factor Δ, where $\mu = \frac{1}{2}^{\Delta}$. Multiplexers are used to select the input raised to the power of the coefficient that is currently being updated, which is multiplied by the scaled error and demultiplexed onto the updated coefficient.

Figure 6.15 shows the implemented LMS algorithm compared with the Matlab simulated design from Chapter 5. The difference between the simulated adaption of the predistorter coefficients and the VHDL implementation is caused by the VHDL

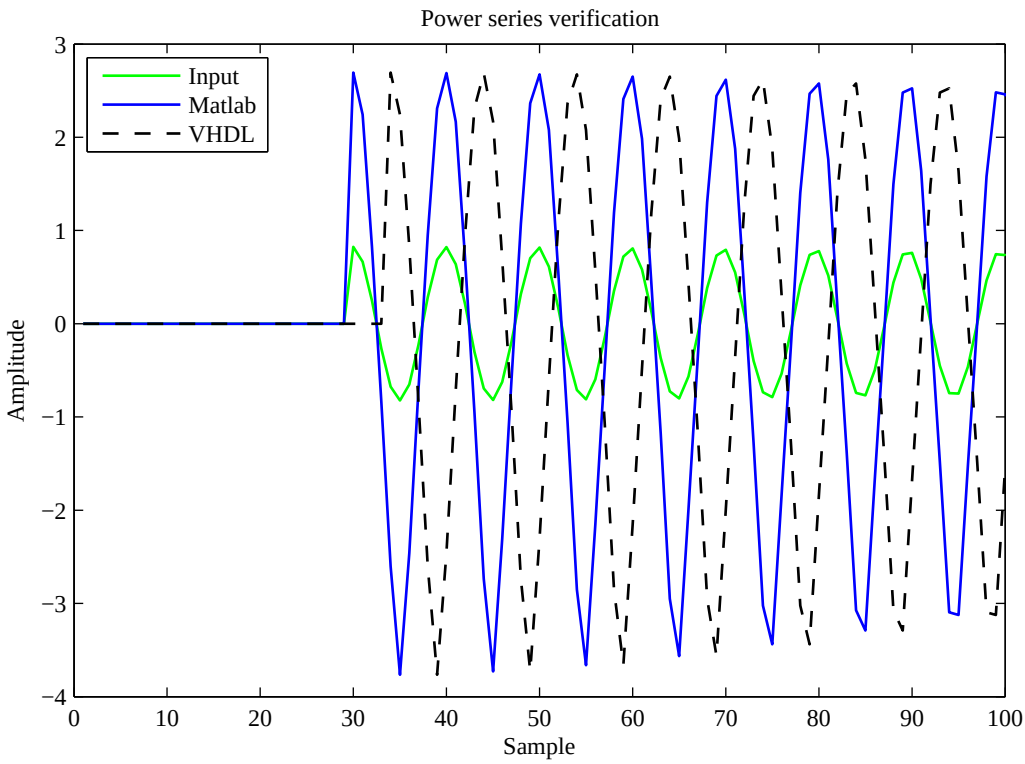

Figure 6.13: Verification of the power series functionality with Matlab simulation data.

pipelined architecture.

The operation of this system is described in detail in Chapter 7. Each of the system components have been verified against the simulations performed using Matlab, as detailed in Chapter 5 and perform adequately.

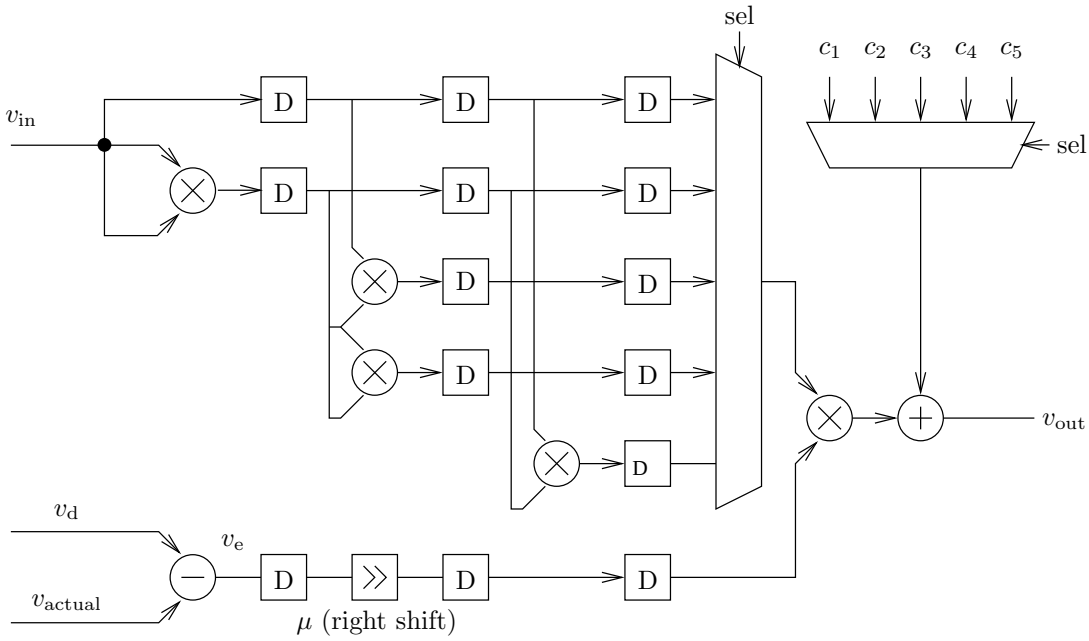

Figure 6.14: Structure of the LMS adaption algorithm.

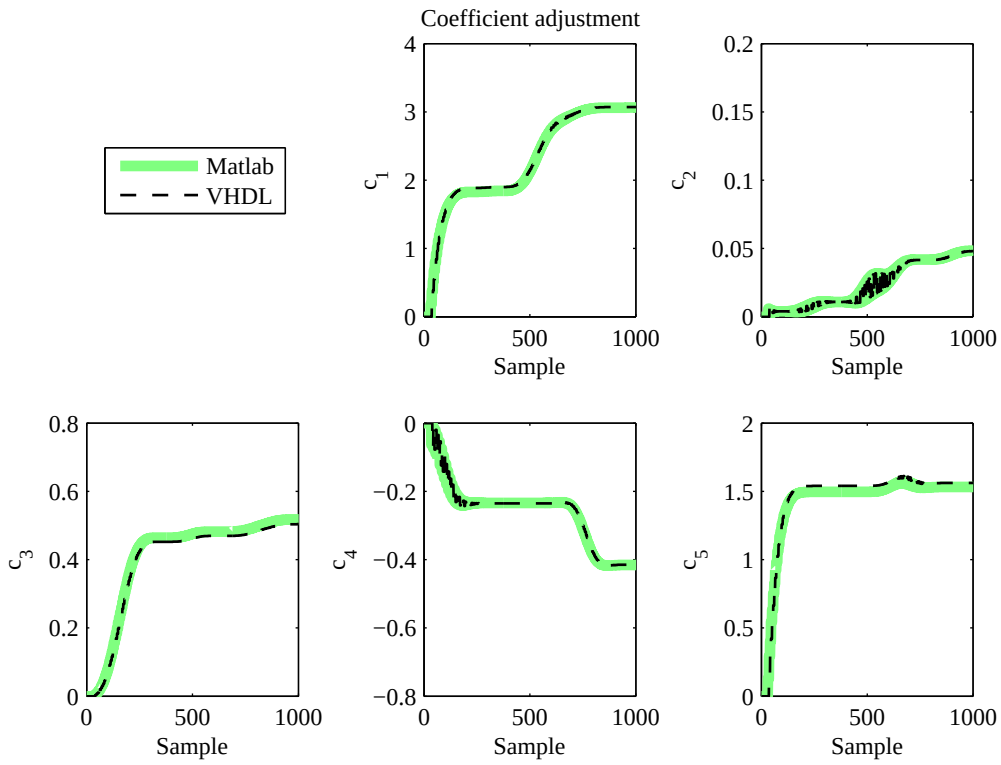

Figure 6.15: Verification of the LMS adaption algorithm compared with Matlab simulation data.

Chapter 7

SYSTEM VERIFICATION AND RESULTS

This chapter discusses the verification and results of a real time predistortion lineariser, as presented over the previous two chapters. Where possible, the performance is be compared with the simulation results. Before discussing the predistortion lineariser, an integration of all system components used in a forward PA modelling exercise is presented, along with linearisation of the PA model. Following this linearisation of a ZFL2000 PA is presented at three different input power levels, using three different configurations of the predistortion lineariser. The system verification is performed with an AM-AM characteristic power series and ignores the AM-PM characteristic of the PA because:

- The AM-PM transfer characteristic of the ZFL-2000 is small (only 1 degree variation of phase over the input power range) so the effects of AM-PM are small.
- Because of the parallel nature of the FPGA architecture, the computational requirements imposed on an FPGA do not increase by adding a second predistortion power series, only the number of logic resources required increases.

7.1 INTERNAL PA MODELLING

Simulations in Chapter 5 make use of a ZFL-2000 transfer characteristic modelled at baseband, under the assumption that the modulation and demodulation processes result in complete baseband recovery. The first verification stage, therefore, is to verify the interaction of all the system components by testing convergence to a forward model

of the PA on the FPGA as shown in Figure 7.1. For the FPGA implementation, the same PA model coefficients used in Chapter 5 are used in a VHDL baseband PA model. A digital feedback path is used in the adaption process to verify the system operation without the added complications of modulation, demodulation and the analogue domain.

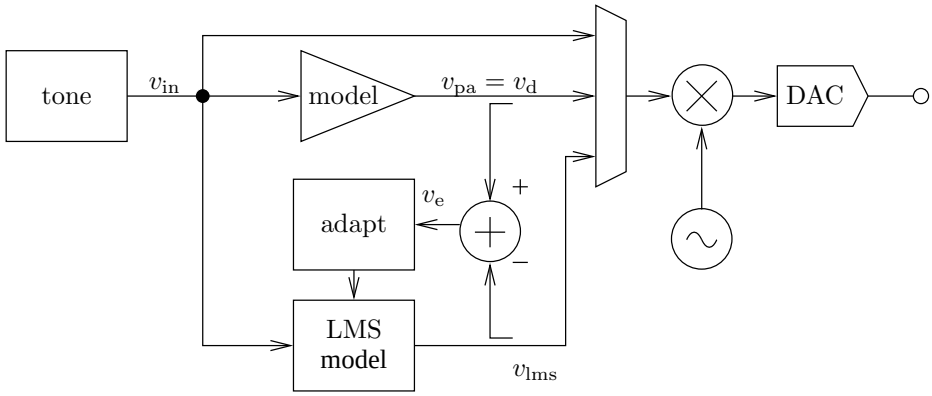

Figure 7.1: System diagram of forward model LMS verification.

As shown in Figure 7.1 a VHDL model of the PA is used to distort the baseband signal v_{in}. This distorted PA model output signal is used at the desired signal v_{d} for the LMS adaption of a fifth order power series which is adapted to have the same transfer characteristic as the PA model. The input v_{in} to the LMS model is the same baseband signal as the PA model. A multiplexer is used to select between the PA model v_{pa} and the LMS model output v_{lms}, which is modulated onto a 6 MHz carrier and digital-to-analogue converted.

The spectrums of the input signal v_{in}, the PA model output v_{pa} and converged LMS model output v_{lms} are shown in Figure 7.2. The input to both the PA model and the LMS model is a single tone of 50 kHz and an amplitude of one sixteenth full scale. When this baseband tone is modulated onto a 6 MHz carrier and converted to an analogue signal, it has the spectrum shown in Figure 7.2(a). When the input signal v_{in} is distorted with the same baseband PA model used in Chapter 5 and modulated onto a 6 MHz carrier, the output signal is distorted as shown in Figure 7.2(b). The fifth order PA model produces third and fifth order intermodulation products, while the even order terms produce carrier leakage which further intermodulates with existing

frequency components.

The spectrum shown in Figure 7.2(c) shows the output of the converged LMS model also modulated onto a 6 MHz carrier.

Table 7.1 shows the intermodulation levels of the PA model and the converged LMS model. Both the third-order and fifth order intermodulation products of the PA model are well modelled by the LMS model. The distortion produced by the LMS model causes the same frequency terms caused by the PA model, which verifies the forward converging LMS system is operating correctly.

	IMD levels	
	VHDL-PA model	LMS fwd
IMD3	-22.3 dBc	-22.3 dBc
IMD5	-50.0 dBc	-52.1 dBc

Table 7.1: IMD levels of an forward LMS model of a PA model.

The LMS algorithm adapts the coefficients of the forward LMS model to minimise the error between the output of the PA model and the output of the LMS model. Figure 7.3 shows the adaption of the coefficients from an initial linear transfer function

$$v_{\text{lms}} = 0 \cdot v_{\text{in}}^0 + 1 \cdot v_{\text{in}}^1 + 0 \cdot v_{\text{in}}^2 + 0 \cdot v_{\text{in}}^3 + 0 \cdot v_{\text{in}}^4 + 0 \cdot v_{\text{in}}^5 \tag{7.1}$$

$$= v_{\text{in}} \tag{7.2}$$

over a 2.7 ms time period.

The LMS algorithm is weighted to prioritise the adaption of the lower order coefficients. This means that the first order coefficient converges at a higher rate then the other coefficients. The nature of the LMS algorithm means that the initial convergence is fast, but the convergence rate declines as the error is reduced. Though the coefficients have not fully converged after this time, it is clear the error function is being minimised. The value of μ, the adaption scaling coefficient, for this system is 0.5 which results in high steady state error. The steady state error can be reduced by

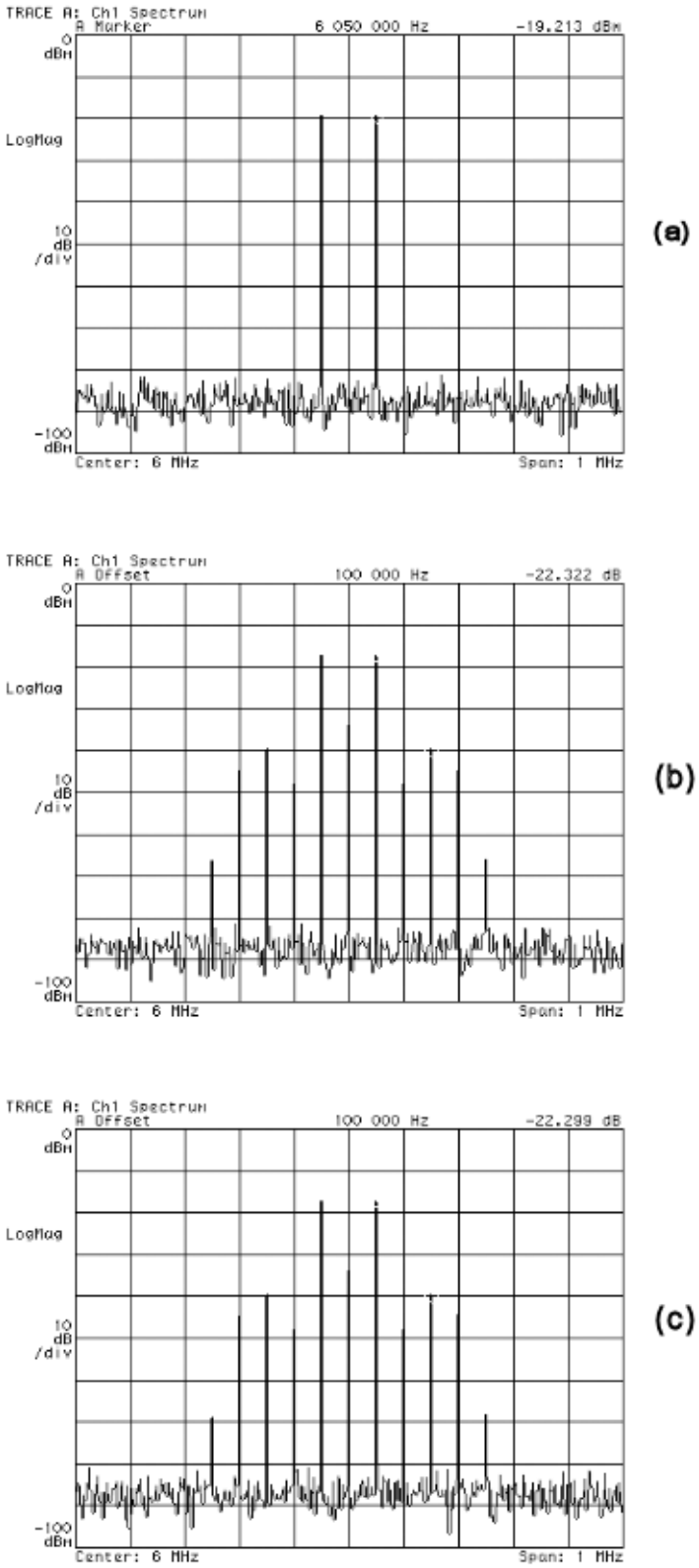

Figure 7.2: Spectrum's of showing adaption to a forward model of the PA model on the FPGA: (a) input (b) PA output (c) LMS model output.

reducing the value of μ, however, this increases the time the model takes to converge to steady state.

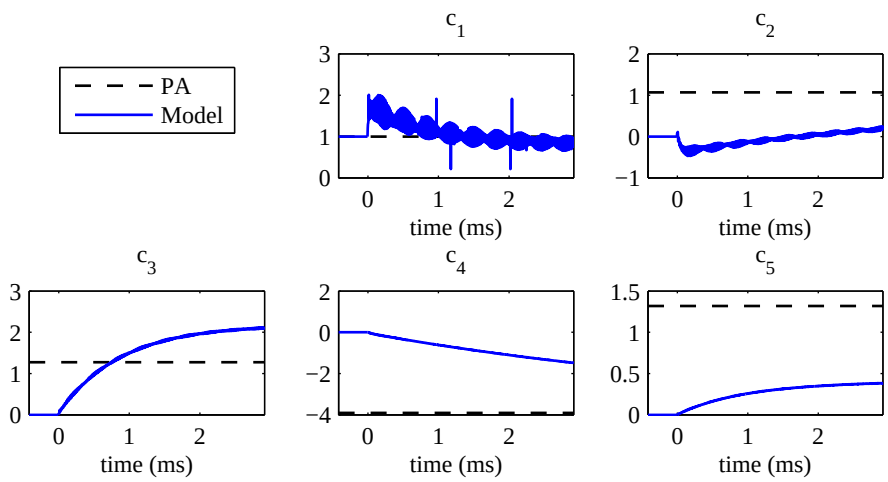

Figure 7.3: Convergence of the LMS coefficients on the FPGA over 2.7 ms.

The error between the output of the PA model and the LMS adapted power series model is shown in Figure 7.4. At the time the LMS algorithm is enabled (t = 0 ms) the error signal is highest. As the LMS algorithm adapts to minimise this error signal, the error decays exponentially.

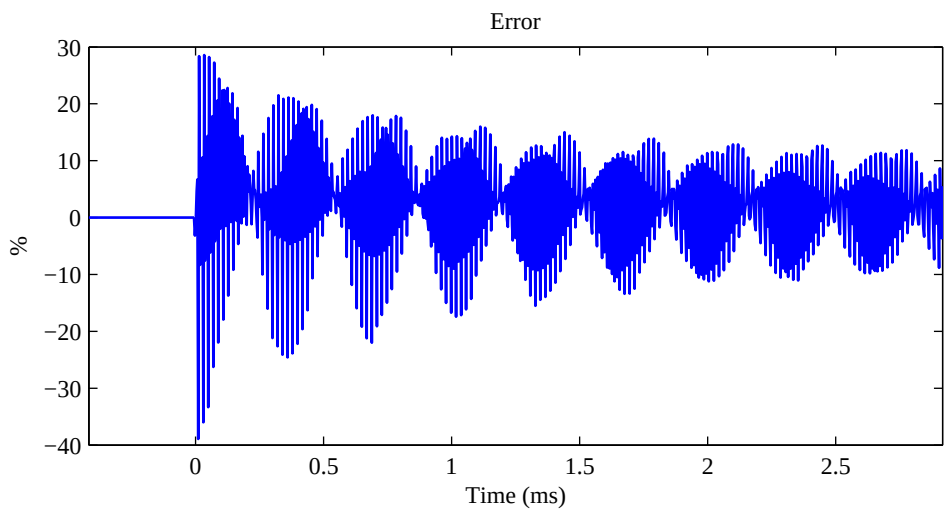

Figure 7.4: Error as the coefficients converge to a forward model of the PA on the FPGA over 2.7 ms.

The LMS algorithm can successfully adapt the coefficients of a power series to a forward model of an unknown PA model in real time. The third-order intermodulation

product levels produced by the LMS adapted PA model are within 0.1 dB of those produced by the PA model being adapted towards. The following sections detail the operation of LMS adapted predistortion.

7.2 LINEARISATION OF INTERNAL PA MODEL

Further verification of the predistortion linearisation system comes through repeating the linearisation of a baseband PA model simulated in Chapter 5. The linearisation of a PA model inside the FPGA is depicted in Figure 7.5. The baseband signal v_{in} is predistorted through a seventh order power series before being distorted with the PA model of the ZFL-2000. The predistorter can be enabled and reset via the RS232 interface to allow a comparison between the linearised and uncorrected PA model output. When the predistorter is disabled, the first order coefficient is set to one and all other coefficients are set to zero to provide an undistorted transfer function of

$$v_{\text{pd}} = v_{\text{in}}. \tag{7.3}$$

As with the forward LMS system, the output of the PA model is modulated onto a 6 MHz RF carrier and digital-to-analogue converted to be measured.

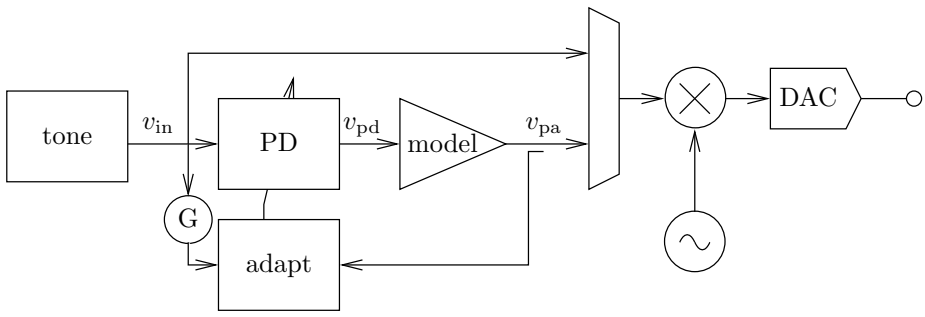

Figure 7.5: System diagram of PD model with internal feedback LMS verification.

Figure 7.6(a) shows the PA input spectrum with the uncorrected PA model output spectrum shown in Figure 7.6(b). The PA model output spectrum with predistortion linearisation is shown in Figure 7.6(c). The predistorter is configured such that the fundamental output level of the PA is within 1 dB of the uncorrected output level.

The input to the PA is a single tone with a frequency of 50 kHz and an amplitude of $\frac{1}{16}$ full scale. The spectrum of the input tone modulated onto a 6 MHz carrier is shown in Figure 7.6(a). With no predistortion linearisation, the output of the PA model is distorted, producing third and fifth order intermodulation products on the modulated output, as shown in Figure 7.6(b).

With the predistortion enabled, the intermodulation products are reduced, as shown in Figure 7.6(c). This real time implementation reduces the third-order intermodulation is by 47 dB and the fifth order by 31 dB, however, these figures are restricted by the noise floor of the measurement equipment. With a fixed point implementation running in real time as shown in Figure 7.6(c) both the third and fifth order intermodulation products are reduced to the noise floor of -85 dBm. Third and fifth order intermodulation levels are shown in Tables 7.2 and 7.3. In simulations the third-order intermodulation was reduced by 67 dB and the fifth order intermodulation was reduced by 37 dB.

	IMD levels (dBc)	
	PD disabled	PD enabled
IMD3	-22.4	-69.4
IMD5	-48.9	-79.1

Table 7.2: IMD levels of an internal LMS PD.

	IMD level reduction (dB)	
	Simulation	Real time
IMD3	67	47
IMD5	37	31

Table 7.3: IMD levels of an internal LMS PD compared with simulation.

While the forward LMS adaption process took 2.5 ms to converge, the predistortion linearisation is quicker taking only 0.1 ms. This is differs from the convergence time in simulations because a more ideal value for μ is used in real time verification. Figure 7.7 shows the converging values of the predistorter coefficients over the first 0.1 ms after being enabled. The steady state values are also shown in the same axis. The error between the PA model v_{pa} output and the linear gain of the input v_{in} is

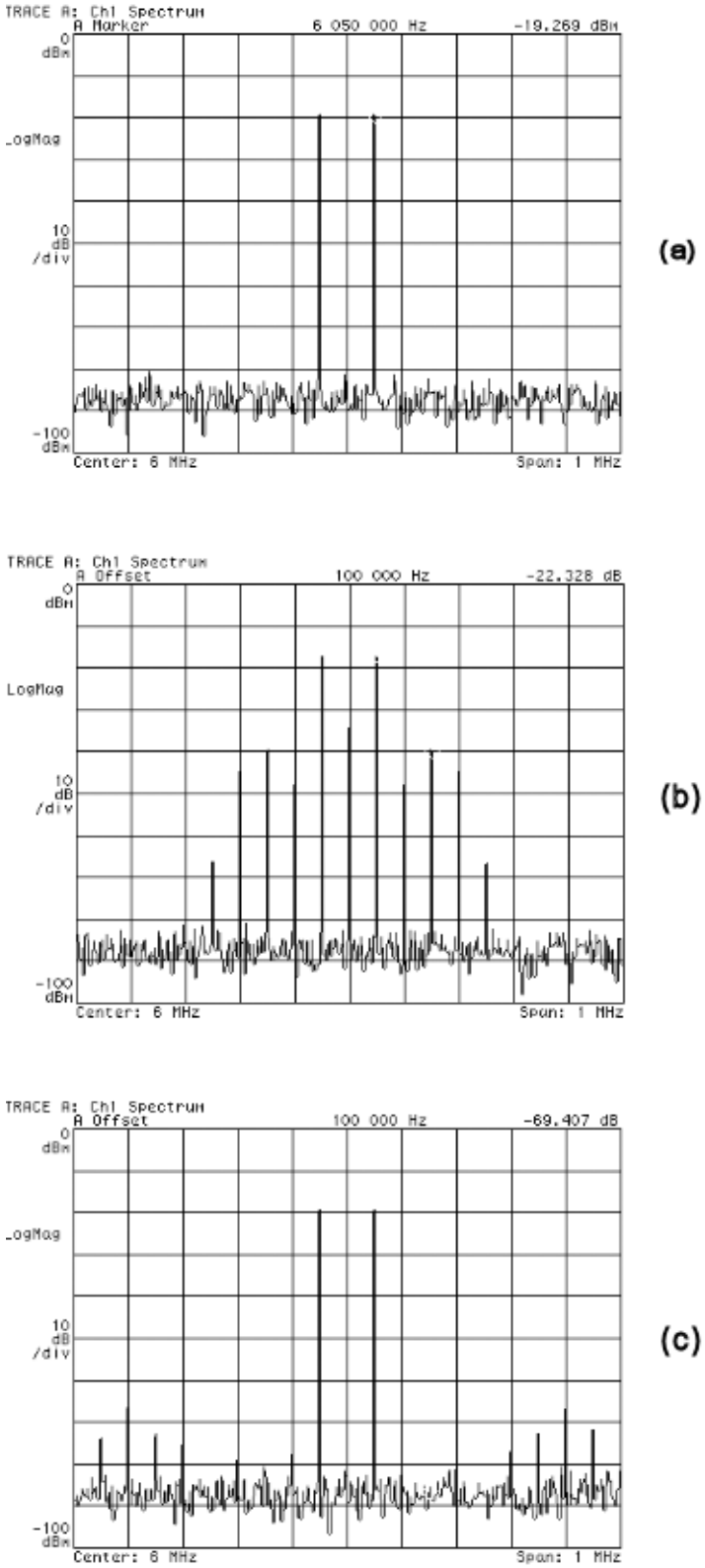

Figure 7.6: Spectrums of the PD linearistion of a PA model: (a) input (b)PA output, no linearisation (c) linearised PA output.

shown in Figure 7.8. At t = 0, the error is at a maximum as the predistorter has an initial linear pass through transfer function. The error reduces to 15% over 0.1 ms as the coefficients approach steady state.

This verifies the operation of the predistortion linearisation system with an internal PA model. The performance of the predistortion linearisation system with a ZFL-2000 PA from Mini-Circuits is presented in the following section.

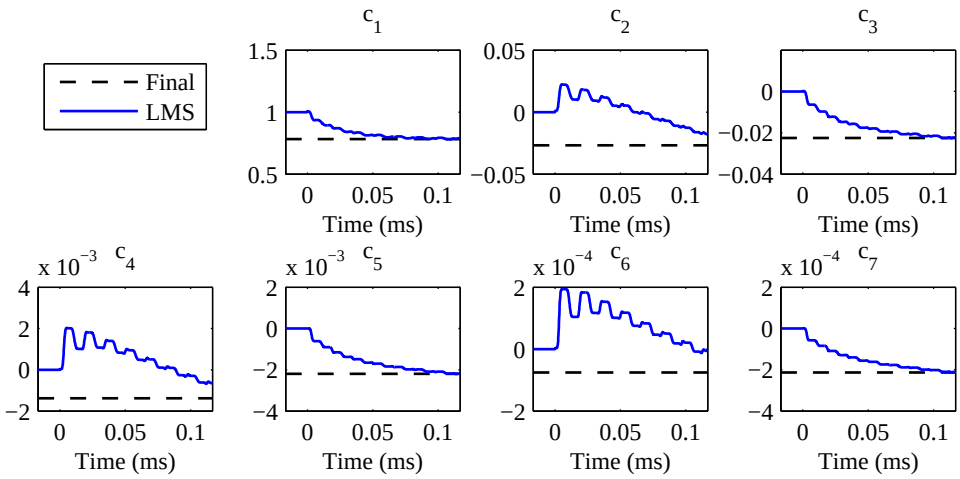

Figure 7.7: Predistortion lineariser coefficients converging over 0.1 ms, with an internal PA model.

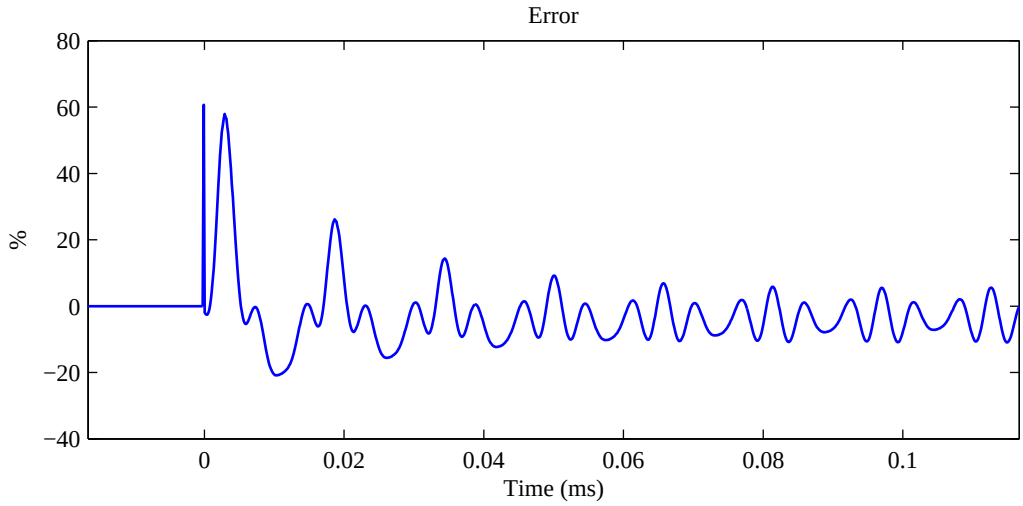

Figure 7.8: Error over 0.1 ms as coefficients of a predistortion lineariser converge, with an internal PA model.

7.3 EXTERNAL PA LINEARISATION

The hardware platform discussed in Section 6.1 and the test instruments are shown in Figure 7.9. Attenuators are used to set drive levels to various parts of the system and a ZXE60-6013E buffer amplifier[1] [35] is used to drive the ZFL2000 into compression to produce third and fifth order intermodulation products. A resistive splitter is used to split the PA output into the feedback path and a measurement path. All of the spectrum measurements are obtained using a HP89441A Vector Signal Analyser (VSA). The HP8647A Signal generator generates a 240 MHz clock for the development platform. This clock is divided by two on the mixed signal interface board to clock the DAC at 120 MSPS and divided by four to clock the ADC at 60 MSPS. The 60 MHz clock also drives the FPGA. The predistortion linearisation system implemented on the FPGA is applied at baseband and modulated onto a 6 MHz carrier. The output from the FPGA is a predistorted digital RF signal to the DAC at 120 MSPS. This RF signal is converted to an analogue signal and drives a ZX60-6013E [35] buffer amplifier, which in turn drives a ZFL-2000 PA. The output of the PA is attenuated by 10 dB and split using a resistive splitter, resulting in an additional 6 dB loss. The feedback path is attenuated by a further 6 dB before being analogue to digitally converted. The digital feedback RF signal at 60 MSPS is used by the predistortion linearisation system to adapt its transfer characteristic. The RF spectrum is measured using an HP89411A vector signal analyser.

Figure 7.10 shows the topology of the predistortion system used to linearise a PA. The 50 kHz baseband signal v_{in} is generated at 60 MSPS and passes through a predistorter to produce v_{pd}. The predistorter can be disabled to allow undistorted transfer of the input signal. The output of the predistorter is modulated onto a 6 MHz RF signal at 120 MSPS before being converted to the analogue domain and amplified by a buffer amplifier and a PA. The output of the PA is sampled at 60 MSPS and converted to a digital signal by the ADC. This digital signal is demodulated and filtered to recover the baseband signal v_{actual} and used with the desired signal $v_{\text{d}} = v_{\text{in}}$

[1] www.minicircuits.com

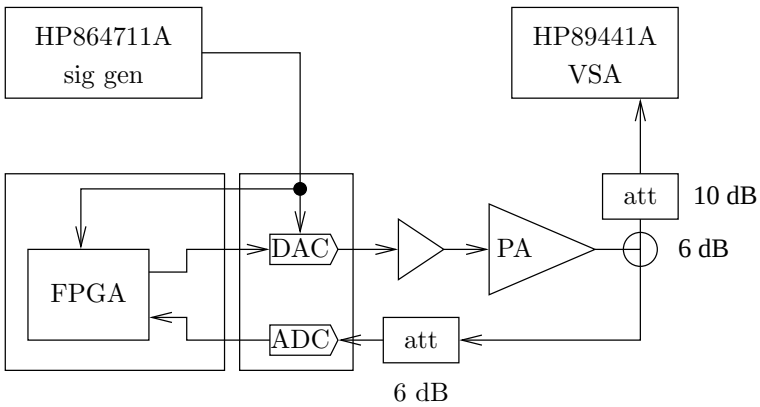

Figure 7.9: Hardware configuration and test instruments used to collect the results in this chapter.

to adapt the predistortion transfer characteristic.

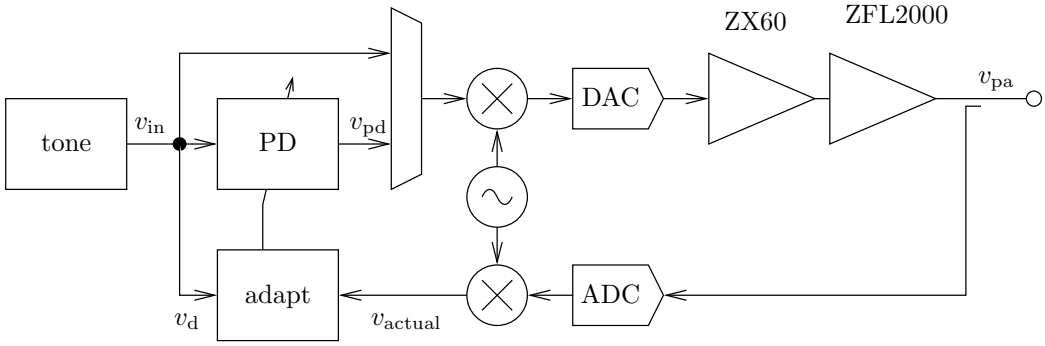

Figure 7.10: Predistortion system configuration with external PA.

The predistortion linearisation system is configured to operate in three different modes. The power series used to generate the predistortion can be a fifth order, seventh order, or odd-only seventh order. All three configurations are realised using the same seventh order power series predistorter and zeroing unwanted coefficients. The zeroeth order coefficient is always fixed at zero, as there should not be a DC component on the baseband signal. For a fifth order predistorter, the sixth and seventh order coefficients are fixed at zero, as are the even order coefficients for the odd-only seventh order predistorter. Each of these configurations is evaluated at three different input power levels. All spectrums in this chapter are reduced by a 6 dB loss through the splitter and 10 dB attenuation in the forward path as depicted in Figure 7.9, so are measured 16 dB smaller then at the outout of the ZFL-2000. The

PA input power level used are -13 dBm, a mid range input power level of -7 dBm and higher input power level of -3.4 dBm.

The low power PA input spectrum and the corresponding output spectrum are shown in Figure 7.11. Figure 7.11(a) shows the input spectrum is free of intermodulation products and carrier leakage, with a noise floor of approximately -90 dBm. Each tone has a input level of -13 dBm and are separated by 100 kHz. Figure 7.11(b) shows the PA output with third and fifth order intermodulation products. The output level of each tone is 5 dBm, with the third-order intermodulation products at -48 dBc.

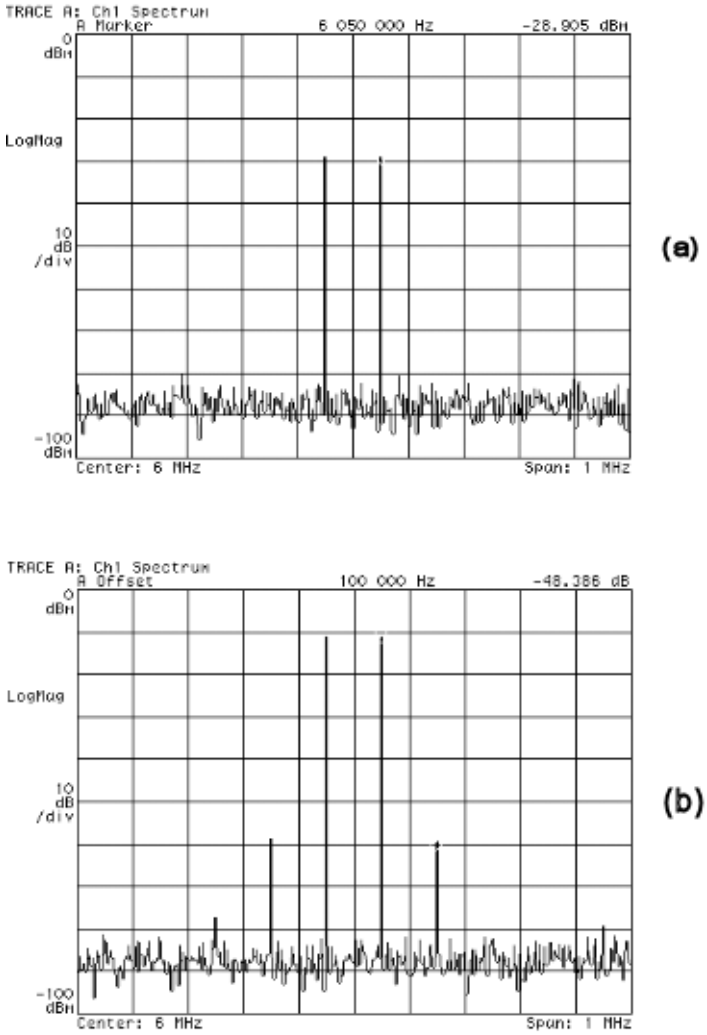

Figure 7.11: Spectrums with -13 dBm (low power) input: (a) PA input (b) PA output.

Figure 7.12 shows linearised PA output with all three configurations of predistor-

tion linearisation. Figure 7.12(a) shows the performance of the fifth order predistortion linearisation system. Both the third and the fifth order intermodulation products are reduced to the noise floor, however, carrier leakage and carrier intermodulation is evident. Increasing the predistorter order to seven does not provide a measurable increase in performance, as shown in Figure 7.12(b). The third-order intermodulation products remain at -72 dBc while the fifth order intermodulation increases by 12 dB. The carrier leakage also increases, as do the fifth order intermodulation products. Removing the even order terms of the predistorter reduces the carrier leakage terms, as shown in Figure 7.12(c), however, the fifth order intermodulation product is 10 dB larger than with no predistortion linearisation. Table 7.4 summarises the intermodulation levels for all three predistortion configurations.

IMD levels with low input power level (-13 dBm)		
	PD enabled	PD Disabled
	5th order PD	
IMD3	-72.0 dBc	-48.4 dBc
IMD5	-76.4 dBc	-66.6 dBc
IMD7	N/A	N/A
	7th order PD	
IMD3	-72.8 dBc	-48.4 dBc
IMD5	-64.3 dBc	-66.6 dBc
IMD7	N/A	N/A
	Odd only 7th order PD	
IMD3	-70.9 dBc	-48.4 dBc
IMD5	-61.8 dBc	-66.6 dBc
IMD7	N/A	N/A

Table 7.4: intermodulation levels, low power input.

Input and PA output spectra with a PA input power level of -7 dBm is shown in Figure 7.13. Figure 7.13(a) show the input spectrum is free of intermodulation products and carrier leakage, with a noise floor of approximately -90 dB. Each of the two input tones has an input power level of -7 dBm and are separated by 100 kHz. Figure 7.13(b) shows the PA output with third and fifth order intermodulation products. The output level of each tone is -7 dBm, with the third-order intermodulation products at -31.0 dBc.

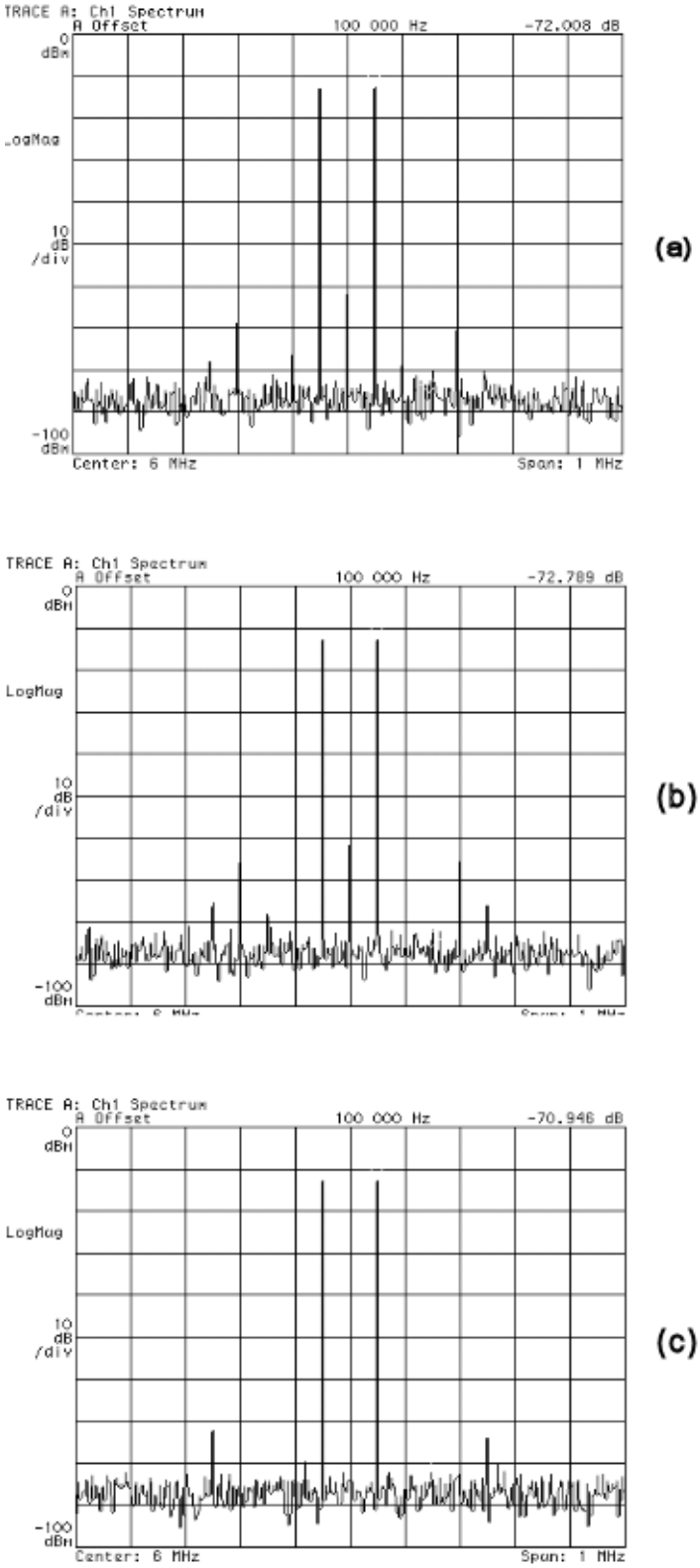

Figure 7.12: Spectrum of the linearised PA output, low power input: (a) 5th order PD (b) 7th order PD (c) Odd-only 7th order PD.

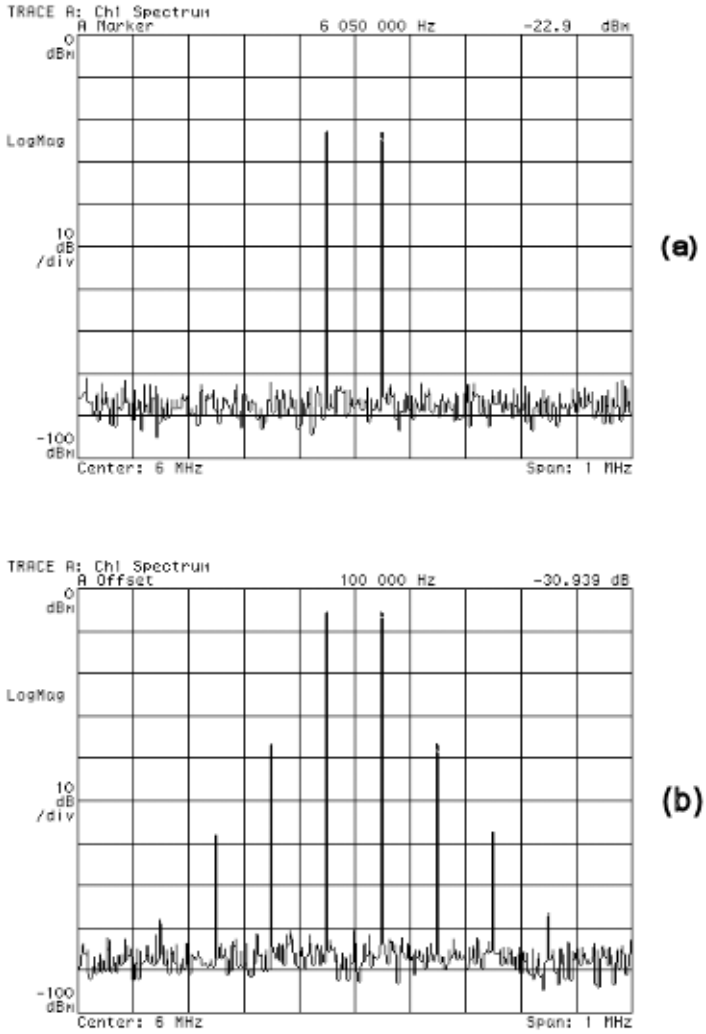

Figure 7.13: Spectrum with -7 dB (mid power)input: (a) PA input (b) PA output.

Figure 7.14 shows linearised PA output with all three configurations of predistortion linearisation. Figure 7.14(a) shows the performance of the fifth order predistortion linearisation system. The third-order intermodulation products are reduced to -60.4 dBc, while the fifth is reduced to the noise floor. Increasing the predistorter order to seven does not provide a measurable increase in performance, as shown in Figure 7.14(b). The carrier leakage is increased, as are the fifth and seventh order intermodulation products.

Removing the even order terms of the predistorter reduces the carrier leakage terms, as shown in Figure 7.14(c). Fifth and seventh order intermodulation products

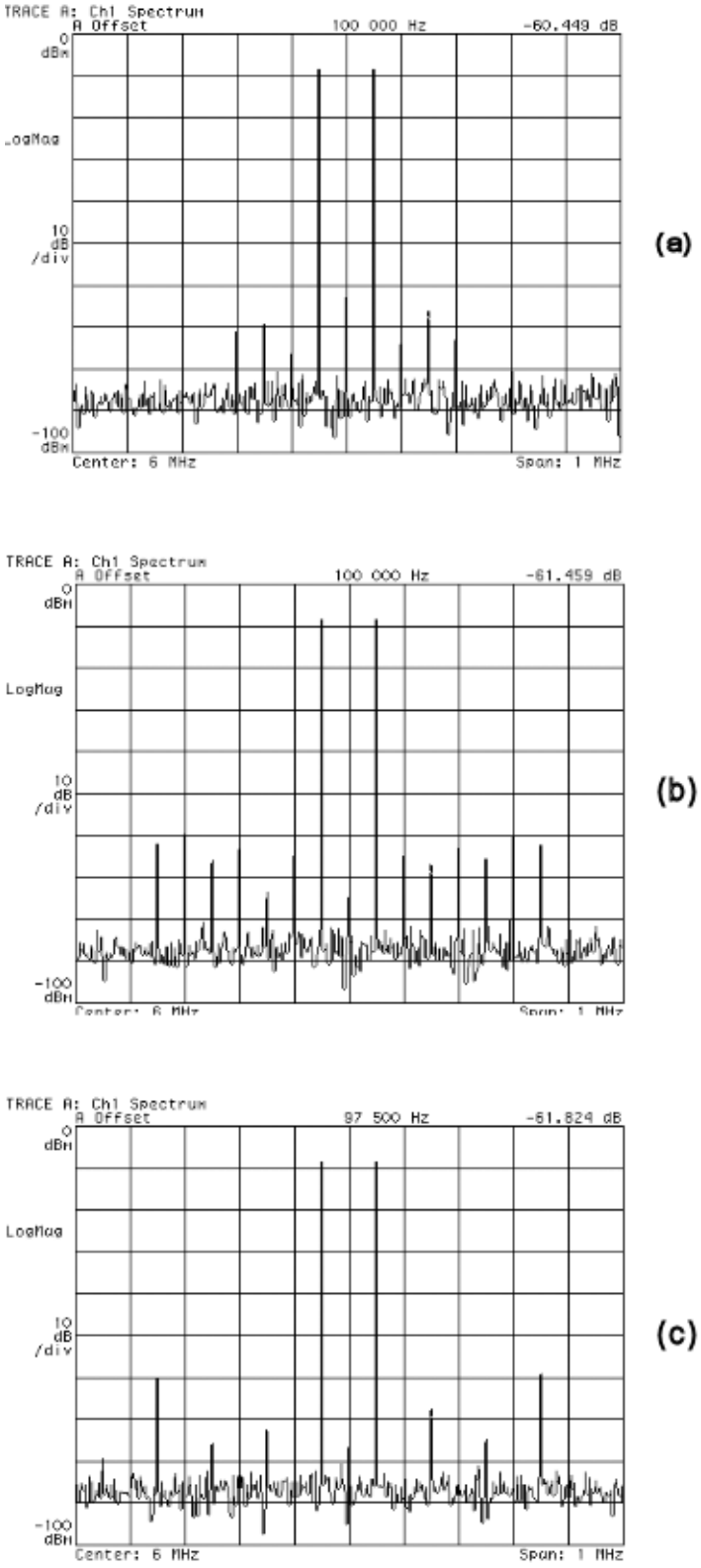

Figure 7.14: Spectrum of the linearised PA output, mid power input: (a) 5th order PD (b) 7th order PD (c) Odd-only 7th order PD.

are larger. The seventh order intermodulation product is 21 dB larger then with a fifth order predistortion linearisation. Table 7.5 summarises the intermodulation levels for all three predistortion configurations.

IMD levels with mid input power level (-7 dBm)		
	PD enabled	PD Disabled
5th order PD		
IMD3	-60.4 dBc	-30.9 dBc
IMD5	-77.3 dBc	-51.7 dBc
IMD7	-75.2 dBc	-70.4 dBc
7th order PD		
IMD3	-61.5 dBc	-30.9 dBc
IMD5	-61.2 dBc	-51.7 dBc
IMD7	-62.0 dBc	-70.4 dBc
Odd only 7th order PD		
IMD3	-61.3 dBc	-30.9 dBc
IMD5	-70.0 dBc	-51.7 dBc
IMD7	-62.1 dBc	-70.4 dBc

Table 7.5: Intermodulation levels, mid power input level.

PA input and output spectra with a PA input power level of -3.4 dBm are shown in Figure 7.15. Figure 7.15(a) shows the input spectrum is free of intermodulation products and carrier leakage, with a noise floor of approximately -90 dBm. Each of the two tones has an input power level of -3.4 dB and the two are separated by 100 kHz. Figure 7.15(b) shows the PA output with third and fifth order intermodulation products. The output level of each tone is 13 dBm, with the third-order intermodulation products at -20 dBc.

Figure 7.16 shows linearised PA output with all three configurations of predistortion linearisation. Figure 7.16(a) shows the performance of the fifth order predistortion linearisation system. The third-order intermodulation products are reduced to -43 dBc from -19 dBc. Fifth order intermodulation is reduced to -56dBc from -36 dBc and seventh order intermodulation increases by 4 dB. Carrier leakage and intermodulation is also evident but to a lesser extent compared with the two lower power input levels. Increasing the predistorter order to seven does not provide a measurable increase in performance to third and fifth order intermodulation, as shown in

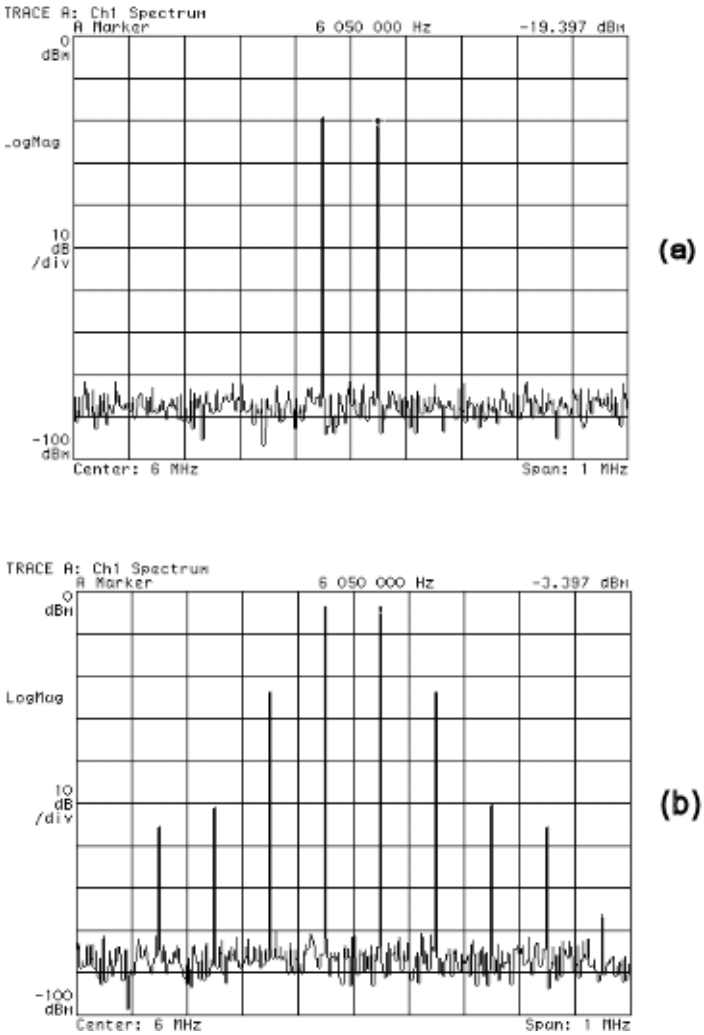

Figure 7.15: Spectrums with -3.4 dB dB (high power) input: (a) PA input (b) PA output.

Figure 7.16(b), but seventh order intermodulation is reduced by 17 dB. The carrier leakage is also reduced. Removing the even order terms of the predistorter removes the carrier leakage terms, as shown in Figure 7.16(c). Third-order intermodulation products are reduced a further 17 dB from the seventh order predistorter and fifth order is reduced 13 dB, while the 7th order increases 10 dB. Table 7.6 shows the intermodulation levels for all three predistortion configurations.

As discussed in Chapter 5, the adaption algorithm minimises the error signal (difference between the baseband signal and the demodulated output of the PA) by

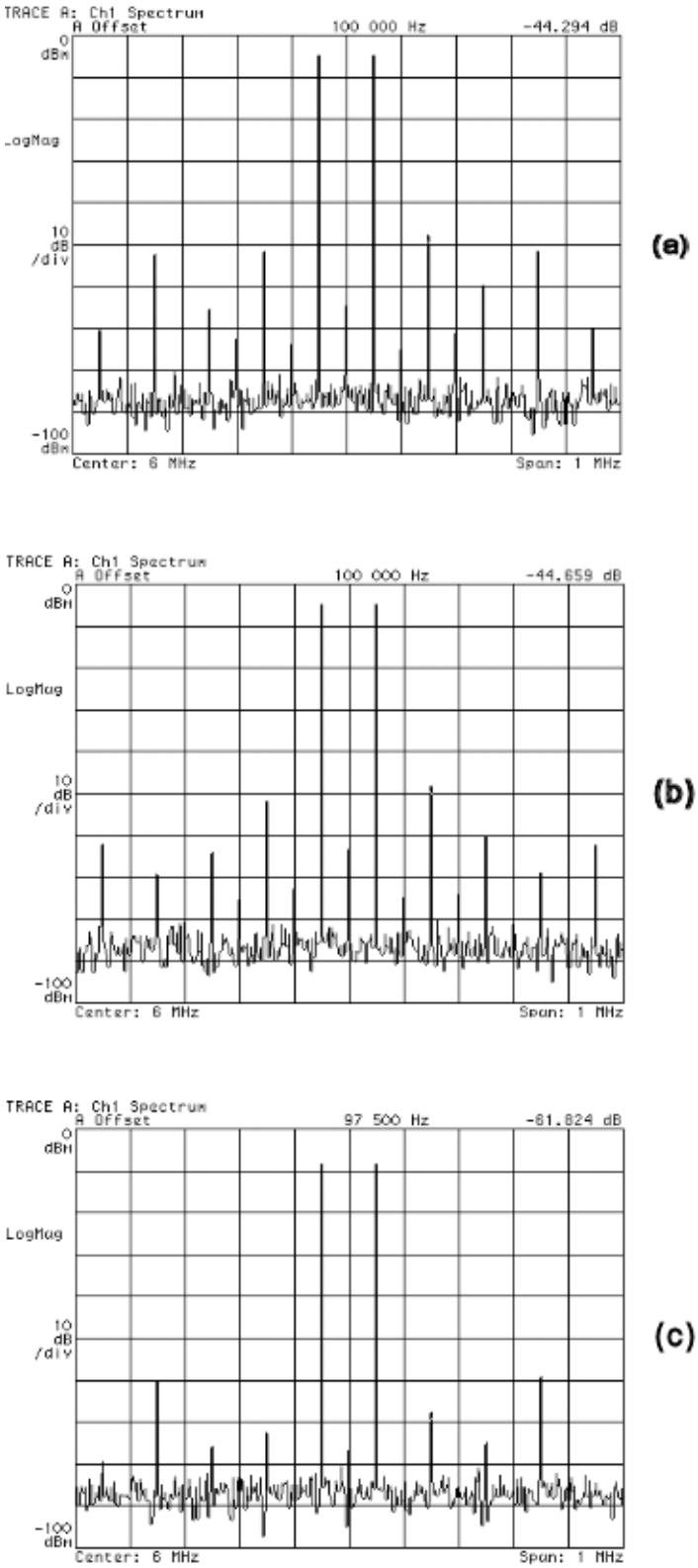

Figure 7.16: Spectrums of the linearised PA output, with a high power input: (a) 5th order PD (b) 7th order PD (c) Odd-only 7th order PD.

IMD with high input power level (-3.4dBm)		
	PD enabled	PD Disabled
5th order PD		
IMD3	-43.0 dBc	-19.1 dBc
IMD5	-54.0 dBc	-46.8 dBc
IMD7	-48.0 dBc	-52.3 dBc
7th order PD		
IMD3	-44.8 dBc	-19.1 dBc
IMD5	-56.0 dBc	-46.8 dBc
IMD7	-65.0 dBc	-52.3 dBc
Odd only 7th order PD		
IMD3	-61.3 dBc	-19.1 dBc
IMD5	-69.1 dBc	-46.8 dBc
IMD7	-50.2 dBc	-52.3 dBc

Table 7.6: Intermodulation levels, high power input level.

adjusting the predistorter coefficients. As the error signal is reduced, the rate at which the predistorter coefficients are adapted also reduces. The adaption of the fifth order, seventh order and odd-only seventh order configurations of predistorter is presented in Figures 7.17, 7.18 and 7.19 respectively. The error signals for these predistorters as they adapt from an initial transfer function of

$$v_{\text{pd}} = 0 \cdot v_{\text{in}}^0 + 1 \cdot v_{\text{in}}^1 + 0 \cdot v_{\text{in}}^2 + 0 \cdot v_{\text{in}}^3 + ... \tag{7.4}$$

$$= v_{\text{in}} \tag{7.5}$$

is shown in Figures 7.17, 7.18 and 7.19 respectively. The input power to the PA is -3.4 dB (highest PA input power level used) for the evaluation of all three predistorter configurations.

Figure 7.17 shows the fifth order predistorter coefficients as they are adapted to minimise the error.

The sixth and seventh order coefficients are held at zero to produce a fifth order predistorter. Within 0.1 ms the coefficients are seen to be approaching the steady state values which provide the results shown in Figure 7.16.

The LMS algorithm employed to adapt the predistorter adapts one coefficient each clock cycle. Although the sixth and seventh order coefficients are fixed at zero, the adaption block still takes seven clock cycles to update all five coefficients, effectively throwing away the updated coefficient value for the sixth and seventh coefficients. If the adaption block only calculated five updated coefficient values, it would follow that the time to converge would decrease to $\frac{5}{7} \cdot 0.1$ ms.

Figure 7.18 shows the seventh order predistorter coefficients as they are adapted to minimise the error . All seven coefficients are adapted to minimise the error signal, so the adaption algorithm must update one coefficient each clock cycle.

Figure 7.19 shows the seventh order predistorter coefficients as they are adapted to minimise the error. The first, third and fifth order coefficients are adapted to minimise the error signal and all even order coefficient updates are discarded. Thus the adaption algorithm convergence time would decrease to $\frac{4}{7} \cdot 0.1$ ms if the algorithm calculated updated values for the odd coefficients only.

7.4 CONCLUSION

The predistortion linearisation system presented in this thesis was designed to operate in real time. The predistortion is applied to the baseband signal before being modulated onto an RF carrier. The transfer function of the predistorter is adapted in real time to minimise the error between the demodulated output of the PA and the undistorted baseband signal. The predistorter can provide up to 25 dB reduction in third-order intermodulation distortion. The LMS based adaption algorithm reduces the error signal to $\pm 10\%$ within 0.1 ms from initial coefficients providing a linear transfer characteristic,

$$v_{\mathrm{pd}} = v_{\mathrm{in}}. \tag{7.6}$$

The research accomplishes its objective of designing and implementing a digital adaptive predistortion linearisation system that operates in real time. The operating predistortion lineariser is shown in Figure 7.20.

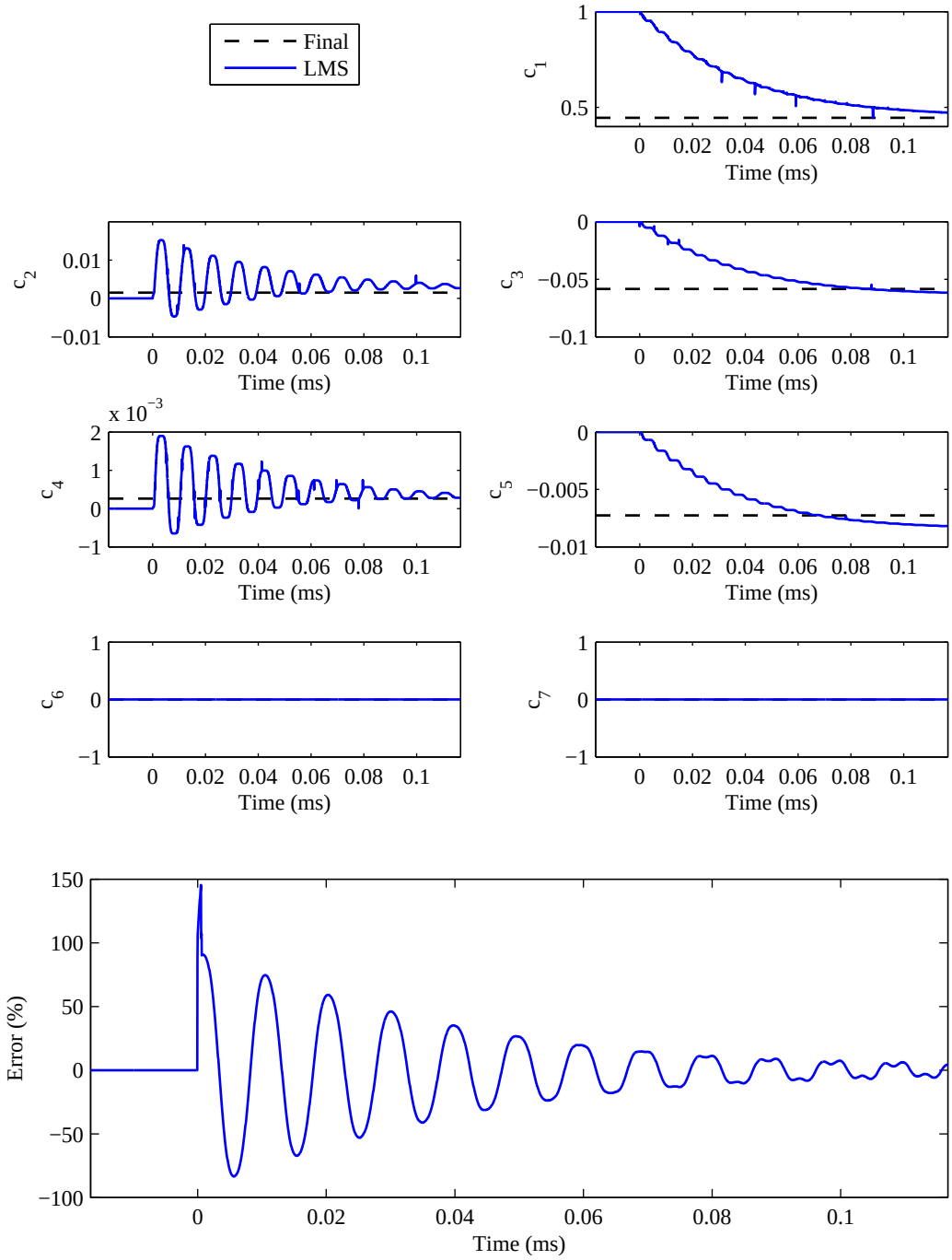

Figure 7.17: Fifth order coefficients and error over 0.1 ms.

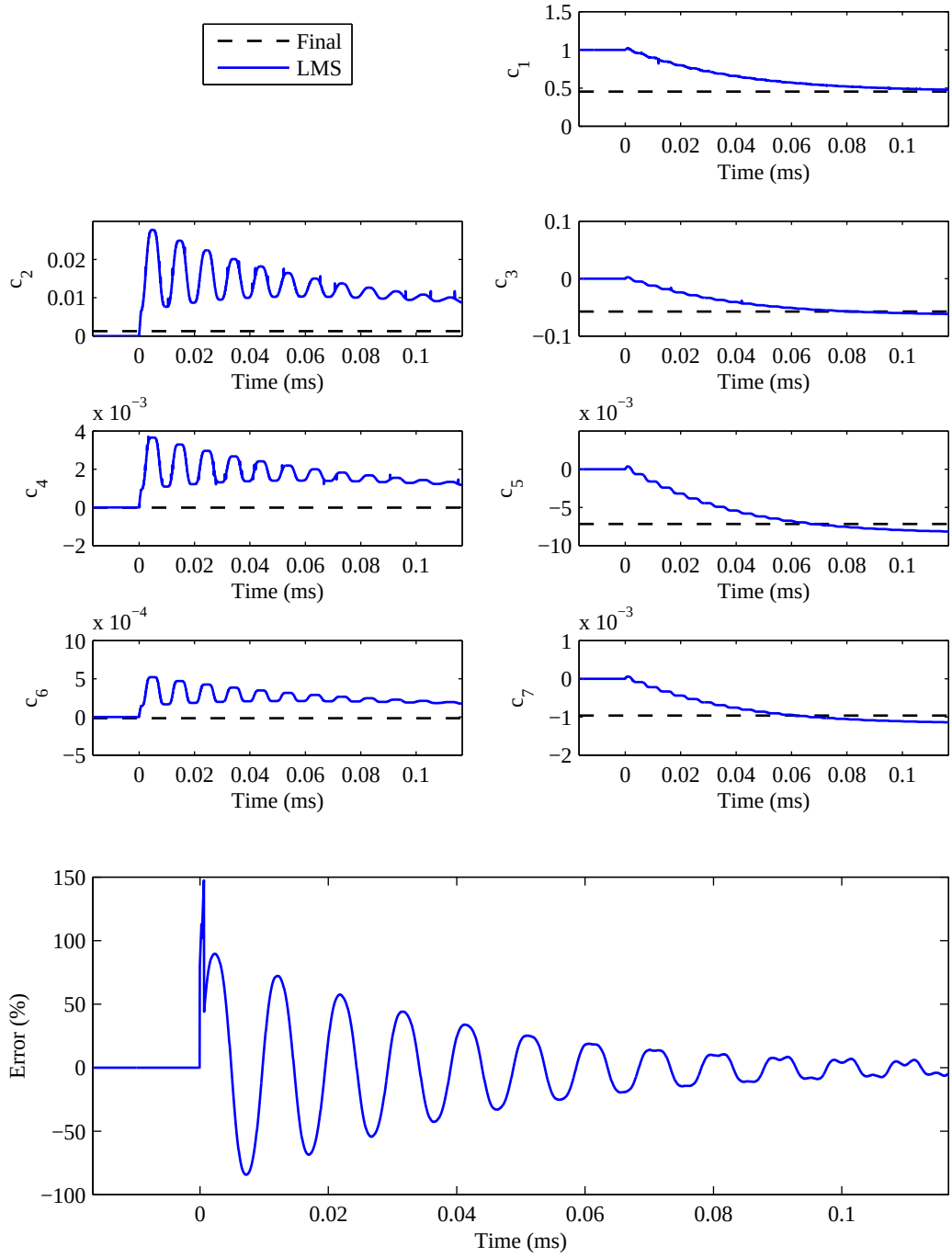

Figure 7.18: Seventh order coefficients convergence and error over 0.1 ms.

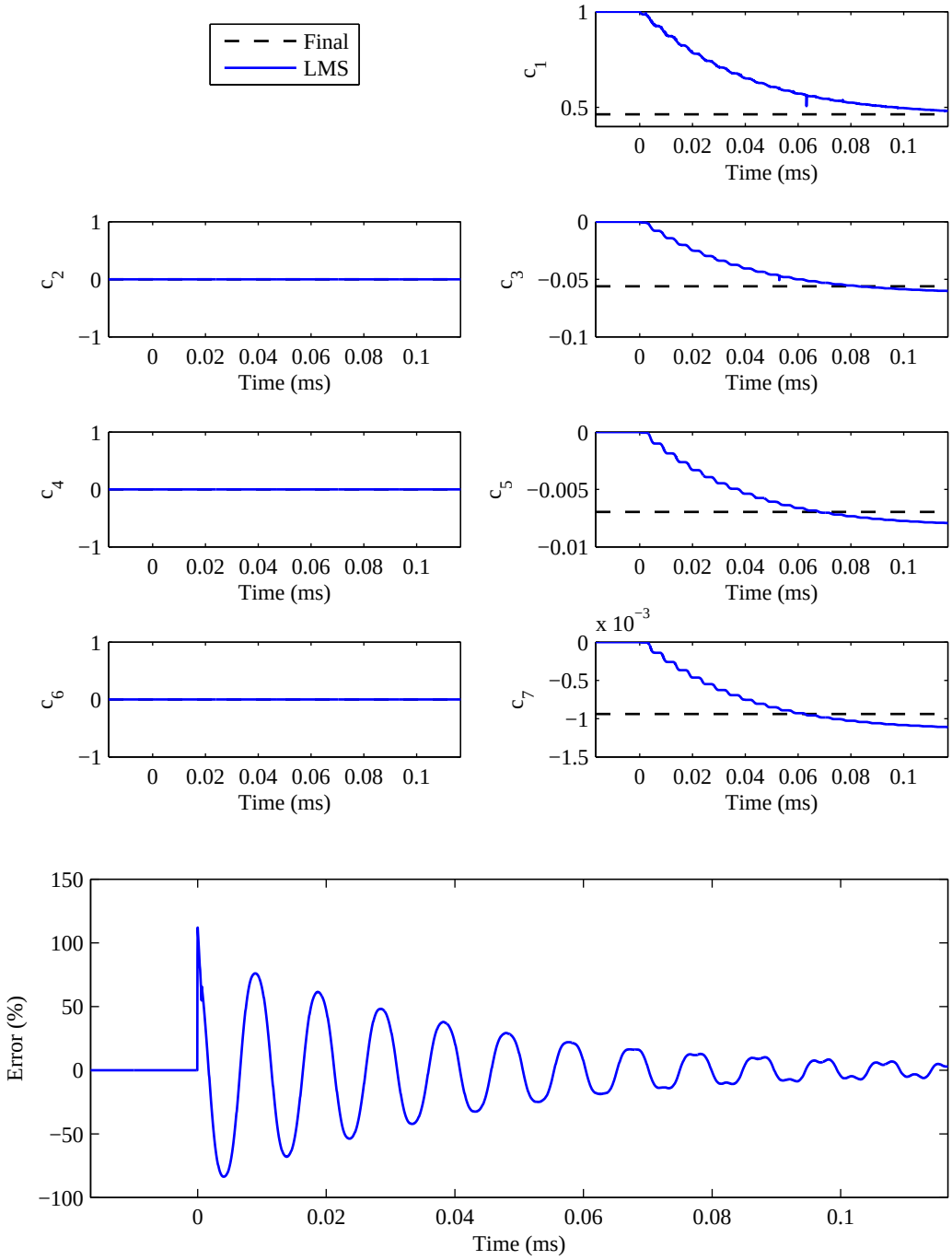

Figure 7.19: Odd-only seventh order coefficient convergence and error over 0.1 ms.

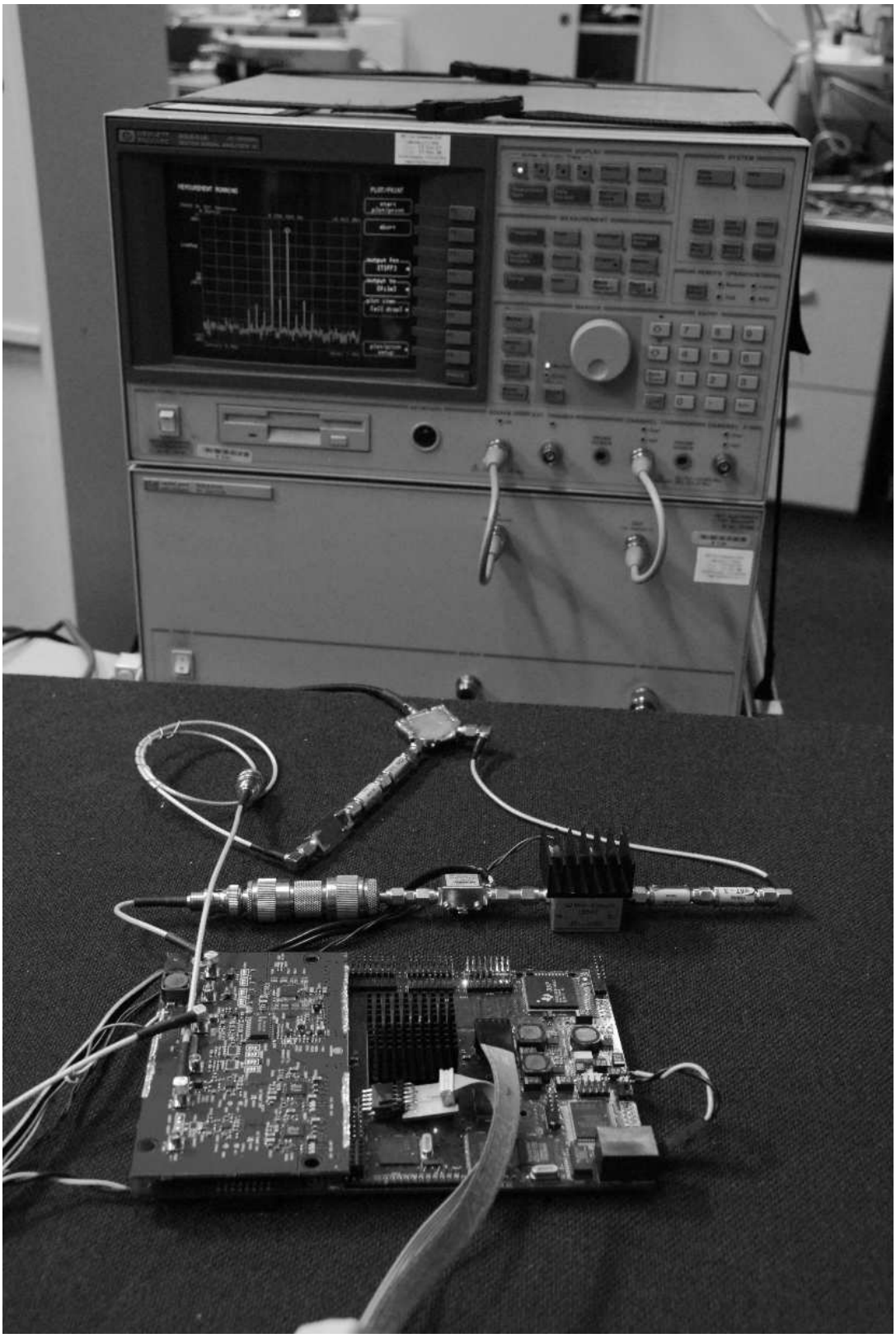

Figure 7.20: Photo of the operating predistortion lineariser.

Chapter 8

CONCLUSIONS

The objective of this research was to design a predistorter based on previous research, and implement it in real time. The presented predistorter has the following attributes:

- Model based predistortion architecture
- Applies predistortion transfer function to complex baseband signal
- Adapts its transfer function in real time to minimise the distortion on the output of the PA
- Implemented on FPGA development platform
- Up to ≈40 dB reduction in third-order intermodulation distortion.

Each of these aspects of the predistorter are briefly discussed in this chapter, along with some suggestions of further work that would add to this research.

8.1 PREDISTORTION IMPLEMENTATION

The predistorter employs a power series architecture to apply the predistortion characteristic to the complex baseband representation of the signal. Three different power series models were evaluated,

- Fifth order
- Seventh order
- Seventh order, with odd orders only (first, third, fifth and seventh).

All three of these predistortion models were able to substantially reduce the intermodulation products on the PA output. As the intermodulation distortion is caused by the coefficients of odd order, using a seventh order predistortion model with odd coefficients only has several advantages:

- The even order terms in the predistorter generate harmonic frequency terms, including DC which are can easily be removed with filters. Therefore, the even order coefficients of a predistorter increase the number of multipliers required to implement the power series model, yet do no increase the performance of the predistorter.
- Adapting the even order coefficients as well as the odd order coefficients means that the predistorter takes longer to adapt to minimise the error on the PA output.

All three predistorter models provide similar levels of reduction to third and fifth order intermodulation, at the two lower input power levels. With an input power level of -13 dBm, third-order intermodulation was reduced by around 20 dB, and fifth order by around 9 dB. At this power level, the predistorters which modelled even order terms performed 2-3 dB better then the seventh order predistorter with odd order terms only. With an input power level of -7 dBm both the seventh order predistorters create additional seventh order intermodulation. As the PA is driven further into compression with an input power level of -3.4 dBm, the seventh order model with only odd coefficients provides greater reduction of both third and fifth order intermodulation products.

All three predistortion architectures make use of the same LMS adaption algorithm. An error signal is derived from the difference between the input to the predistorter, and a demodulated sample of the output of the PA. This error signal is minimised in real time by adjusting the coefficients of the predistortion power series.

The predistorter was implemented on an FPGA development platform, using a Stratix I FPGA. The architecture of FPGA technology leads itself to parallel signal processing, which was utilised in the power series implementation. The FPGA

was used to generate the baseband tone, apply the predistortion characteristic and modulate the predistorted baseband onto an RF carrier.

This research achieved its objective of implementing an adaptive model based predistorter that is applied to a baseband signal. This system, running in real time with no prior knowledge of the PA transfer function can provide up to 30 dB reduction in third-order intermodulation distortion, and can track changes in PA transfer characteristic caused by temperature, signal statistics and ageing. There are several avenues for further research to build on these findings, as discussed in the following section.

8.2 FURTHER WORK

As discussed in Chapter 3, much of the research into model based predistortion has been towards a reduction in the time taken to converge to a minimised error, or the accuracy of the predistortion model. As the transfer characteristic of a PA is slow changing, and well able to be tracked by the LMS algorithm, the latter of these approaches is of a higher importance. The model used in this research was a simple power series to represent the AM-AM transfer characteristic. In simulations another power series to represent the AM-PM predistortion characteristic. Though they were applied to a polar representation of the complex baseband signal in simulations, they can also be applied to the in-phase (I) and quadrature (Q) baseband signals. An extension to the implementation to correct for both AM-AM and AM-PM distortion in the amplifier would be valuable further work.

As the bandwidth of a RF communications signals increase, the memory effects of a PA's transfer characteristic can inhibit the performance of a system. Adding the facility to correct for a PA's memory effects in the predistorter requires the predistorter model and transfer characteristic to exhibit memory effects. This can be done a number of ways, including use of a Volterra filter structure, as presented in [24], or by using a number of power series models, the input of which is a delay line. This structure is shown in Figure 8.1.

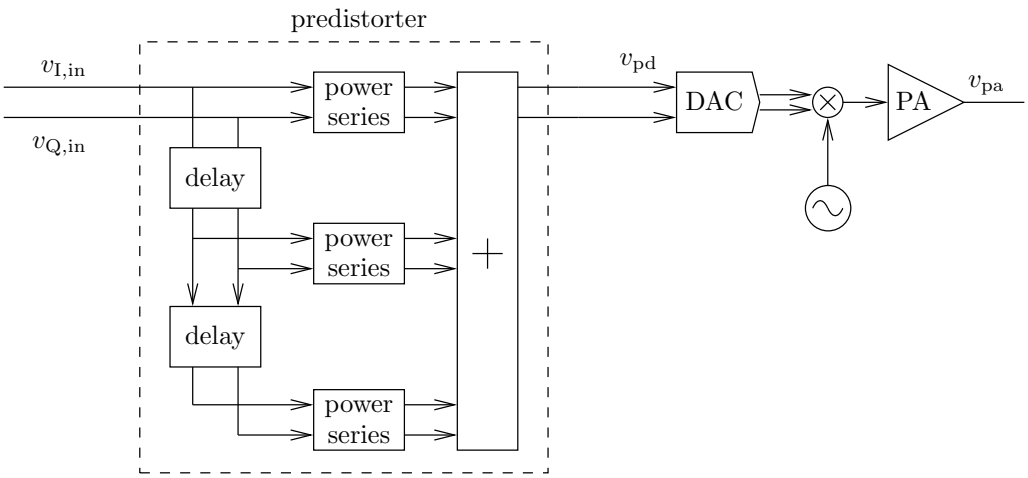

Figure 8.1: Model based predistorter architecture to correct for memory effects.

Appendix A

LMS ALGORITHM

The least mean squares (LMS) algorithm is a widely used algorithm for adapting linear systems, such as FIR filters. The algorithm tracks a multi-dimensional error function to its minimum, and is a descendant of the steepest descent algorithm. The steepest descent algorithm updates weight vectors as follows:

$$W_{\mathrm{k}+1} = W_{\mathrm{k}} - \mu \bigtriangledown_{\mathrm{k}} \tag{A.1}$$

Where k is the iteration number, W_{k} is the current filter coefficient vector, $\bigtriangledown_{\mathrm{k}}$ is the current gradient vector of the error function, and μ is used to control the convergence of the algorithm. As is evident from Equation A.1, the steepest descent algorithm requires knowledge of the gradient of the error function. Calculation of the error function is a computationally expensive operation [36], so the LMS is used as a practical method to recursively reduce the error by modifying the coefficients as follows:

1. Calculate the error
2. Adjust the coefficients using,

$$W_{\mathrm{k}+1} = W_{\mathrm{k}} + 2\mu e_{\mathrm{k}} X_{\mathrm{k}}. \tag{A.2}$$

where W is the coefficient vector, X is the input vector to the adaptive filter, and the error e is calculated from

$$e_{\mathrm{k}} = d_{\mathrm{k}} - y_{\mathrm{k}}, \tag{A.3}$$

where d_{k} is the desired output from the system, and y_{k} is the current output of the system.

In the case of a FIR filter, all of the filter taps can be updated at the same time, as the input value to each tap is different, due to the delay line nature of the structure. However, with a power series structure, the input to each coefficient is not through a delay line structure, so the coefficients need to be updated independently. This is done by modifying a single coefficient for each input sample, and using the input raised to the power of the coefficient being adapted

$$c_{\mathrm{t=k+1,n}} = c_{\mathrm{t=k,n}} + 2\mu e_{\mathrm{k}} v^{\mathrm{n}}_{\mathrm{in,t=k}}. \tag{A.4}$$

Where $c_{\mathrm{t=k,n}}$ is the nth of N coefficients at time k.

Appendix B

FPGA ARCHITECTURE

This appendix provides a brief overview of Field Programmable Gate Array (FPGA) technology and architecture. There are subtle differences between different manufacturers FPGAs, however the architectures are very similar. FPGAs are a reprogrammable hardware device that are rich in IO pins. The research was implemented on an Stratix I device from Altera. The top level architecture of a Stratix device is shown in Figure B.1. Stratix devices contain two dimensional lookup tables to implement custom logic functions in a logic array block (LAB). These LABs are interconnected to memory blocks and DSP blocks within the device. Different types of memory are provided, including:

- M512 512 bit simple dual port RAM
- M4K 4K bit true dual port RAM
- M-RAM 512 bit dual port RAM.

The DSP blocks provide high speed 9, 18 or 36 bit multipliers with add or subtract features and 18 bit shift registers. The IO pins are driven by input output elements which provide data transfer speeds up to 840 Mbps using LVDS, LVPECL, PCML or HyperTransport technology IO standards.

The logic array blocks are used to interconnect most of the blocks of functionality within the FPGA, and consists of 10 Logic Elements (LE), LE carry chains, control signals, local interconnects, LUT chain and register chain connection lines. Local interconnects are used to transfer data between LEs in the same logic array block,

whereas LUT chain connects transfer data to LUTs in adjacent LEs for fast sequential LUT connections. Register chain connections transfer data from the output of one LE to the input of an adjacent LE.

Each LE contains a four input LUT which can implement any logic function of four variables, a programmable register and a carry chain. Each LE supports dynamic single bit addition or subtraction which is selected by an LAB-wide control signal. The output of an LE can drive any type of interconnect or chain of an LAB.

Logic functionality is provided by the LE, as shown in Figure B.2. The programmable register can be configured to operate as a D, T, JK or SR, and has data, asynchronous data, lock, clock enable, clear and asynchronous load and preset inputs. The clock and clear control signals can be driven by global signals, IO pin signals or internal logic signals. The register can be bypassed for combinatorial functions, or used for synchronous functions. The output of the LUT can be driven independently to the output of the register, so the LUT and the register can be used for unrelated logic functionality.

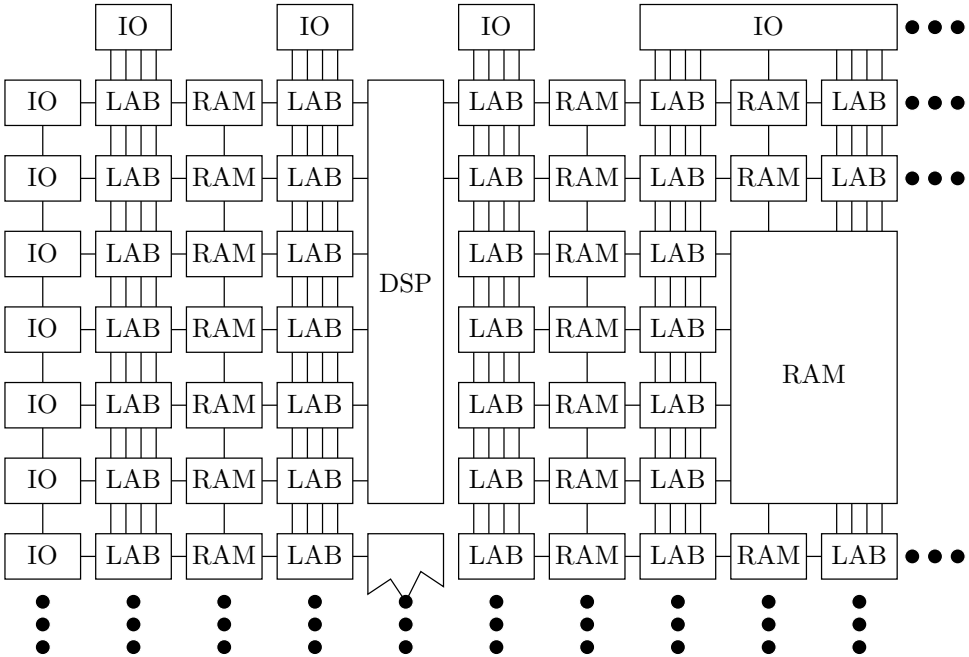

Figure B.1: Architecture of a Stratix I device.

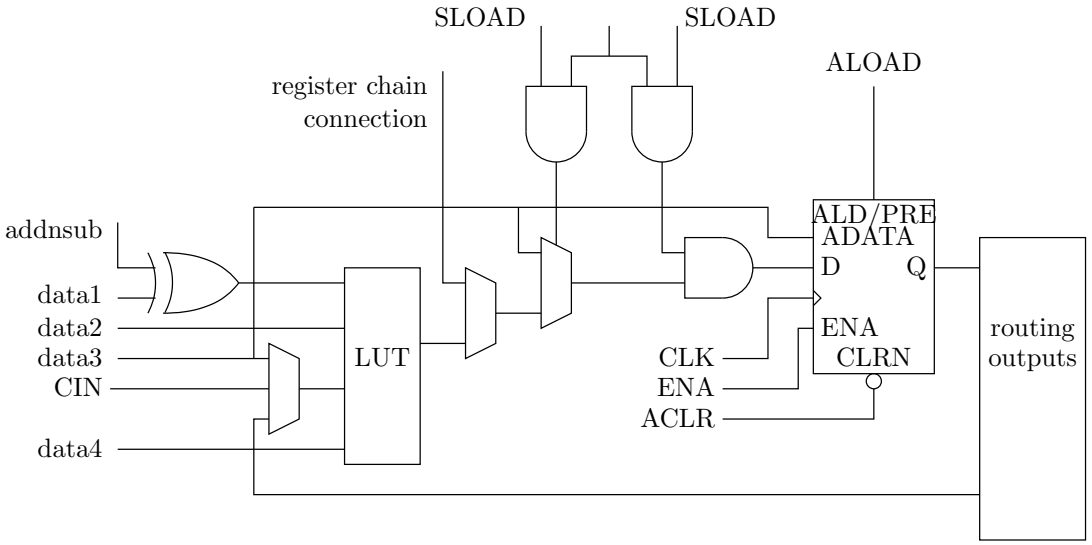

Figure B.2: LE architecture.

REFERENCES

[1] D. Giesbers, S. Mann, and K. Eccleston, "Adaptive digital predistortion linearisation for RF power amplifiers," *Proceedings of the 13th ENZCon*, pp. 244 – 248, November 2006.

[2] S. A. Maas, *Nonlinear Microwave Circuits.* Artech House, 1988.

[3] K. G. Voyce and J. H. McCandless, "Power amplifier linearization using IF feedback," *1989 IEEE MTT-S Digest*, vol. 3, pp. 863–866, June 1989.

[4] E. Bertan and J. Berenguer, "Analogue adaptive feedback lineariser," *33rd European Microwave Conference*, 2003.

[5] M. Faulkner, D.Contos, and M. Johansson, "Linearisation of power amplifiers using RF feedback," *Electronics Letters*, vol. 31, pp. 2023–2024, November 1995.

[6] M. Johansson and T. Mattsson, "Transmitter linearization using cartiesian feedback for linear TDMA modulation," *IEEE*, pp. 439–444, 1991.

[7] S. I. Mann, M. A. Beach, and K. A. Morris, "Digital baseband cartesian loop transmitter," *Electronics Letters*, vol. 37, pp. 1360–1361, October 2001.

[8] F. H. Raab, P. Asbeck, S. Cripps, P. B. Kennington, Z. B. Pabovic, N. Pothecary, J. F. Servic, and N. O. Sokal, "Power amplifiers and transmitters for RF and microwave," *IEEE Transactions on Microwave Theory and Techniques*, vol. 50, pp. 814–826, March 2002.

[9] R. D. Stewart and F. F. Tusubira, "Feedforward linearisation of 950 mhz amplifiers," *Microwave, Antennas and Propogation IEE proceedings*, vol. 135, pp. 347–350, October 1988.

[10] Y. K. G. Hau, V. Postoyalko, and J. Richardson, "A microwave feedforward amplifier with improved phase compensation and wideband distortion cancellation," *IEEE Symposium on Technologies for Wireless Applications*, pp. 75 –78, February 1997.

[11] K. Morris and P. Kenington, "Power amplifier linearisation using predistortion techiniques," *IEE Colloquim on Components for Communication Systems*, pp. 6/1–6/6, April 1997.

[12] J. Yi, Y. Yang, M. Park, W. Kang, and B. Kim, "Analog predistortion linearizer for high-power RF amplifiers," *IEEE Transactions of Microwave Theory and Techniques*, vol. 48, pp. 2709–2713, December 2000.

[13] M. Kim, C. Kim, H. Yu, and J. Lee, "An FET-level linearization method using a predistortion branch FET," *IEEE Microwave and Guided Wave Letters*, vol. 9, pp. 233–235, June 1999.

[14] Y. Yang, Y. Y. Woo, and B. Kim, "New predistortion linearizer using low-frequency even order intermodulation components," *IEEE transaction on microwave theory and technique*, vol. 50, pp. 446–452, February 2002.

[15] S. Kusunoki, K. Yamamoto, T. Hatsugai, H. Nagaoka, K. Tagami, N. Tominaga, K. Osawa, K. Tanabe, S. Sakurai, and T. Iida, "Power amplifier module with digital adaptive predistortion for cellular phones," *IEEE Transactions on Microwave Theory and Techniques*, vol. 50, pp. 1979–2986, December 2002.

[16] S. Boumaiza, J. Li, M. Jaidane-Saidane, and F. M. Ghannouchi, "Adaptive digital/RF predistortion using a nonuniform LUT indexing function with built-in dependence on the amplifier nonlinearity," *IEEE Transactions on Microwave Theory and Techniques*, vol. 52, pp. 2670–2677, December 2004.

[17] T. Rahkonen and T. Kankaala, "An analogue predistortion integrated circuit for linearizing power amplifiers," *Midwest Symposium on Circuits and Systems, Proceedings.*, pp. 480–483, August 1998.

[18] Y. Nagata, "Linear amplification technique for digital mobile communications," *1989 IEEE Vehicular Technology Conference (VTC 1989)*, pp. 159–164, May 1989.

[19] J. K. Cavers, "Amplifier linearization using a digital predistorter with fast adaption and low memory requirements," *1990 IEEE Transactions on Vehicular Technology*, vol. 39, pp. 374–382, November 1990.

[20] A. Lohtia, P. A. Goud, and C. G. Engfield, "Power amplifier linearization using cubic spline interpolation," *1993 IEEE Vehicular Technology Conference (VTC 1993)*, pp. 676–679, May 1993.

[21] A. N. D'Andrea, V. Lottici, and R. Regiannini, "RF power amplifier linearization through amplitude and phase predistortion," *IEEE Transactions on Communications*, vol. 44, pp. 1477–1484, November 1996.

[22] G. Baudoin and P. Jardin, "Adaptive polynomial pre-distortion for linearization of power amplifiers in wireless communcations and WLAN," *International conference on trends in communications*, vol. 1, pp. 157–160, July 2001.

[23] H. Besbes, T. le Ngoc, and H. Lin, "A fast adaptive polynomial predistorter for power amplifiers," *Global Telecommunications Conference, 2001. IEEE*, vol. 1, pp. 659–663, November 2001.

[24] A. Zhu and T. J. Brazil, "An adaptive volterra predistorter for the linearization of RF high power amplifiers," *IEEE MTT-S Digest*, pp. 461–464, 2002.

[25] M. Jin, S. K. Shin, D. Oh, and J. Kim, "Reduced order RLS polynomial predistortion," *Proceedings of the International Symposium on Circuits and Systems ISCAS*, vol. 4, pp. 333 – 336, May 2003.

[26] M. Jin, S. Kim, and D. Oh, "A novel predistorter for power amplifier," *3rd International conference on Microwave and Millimeter Wave Technology Proceedings*, pp. 1129–1133, 2002.

[27] N. Naskas and Y. Papananos, "Adaptive baseband predistorter for radio frequency power amplifiers based on a multilayer perception," *IEEE*, 2002.

[28] N. Naskas and Y. Papanonos, "Neural-network-based adaptive baseband predistortion method for RF power amplifiers," *IEEE Transactions on Circuits and Systems*, vol. 51, pp. 619–623, November 2004.

[29] A. A. M. Saleh, "Frequency independant and frequency dependant nonlinear models of TWT amplifiers," *IEEE Transactions on Communications*, vol. COM-29, pp. 1715 – 1720, November 1981.

[30] Minicircuits, "ZFL2000 datasheet,"

[31] T. Instruments, "Dac5672 dual 14-bit 200 MSPS digital -to-analog converter," *Data Sheet*, pp. 1–22, September 2004.

[32] L. T. Corporation, "LTC2232/LTC2233 10-Bit, 105 Msps/80Msps ADCs," *Data Sheet*, pp. 1–24, 2004.

[33] Altera Corporation, "Stratix device handbook," *Data Sheet*, pp. 1–1 to 1–24, 2002-2007.

[34] R. Andraka, "A survey of CORDIC algorithms for FPGA based computers," *Proceedings of the 1998 ACM/SIGDA Sixth International Symposium on Field Programmable Gate Arrays*, pp. 191–200, March 1998.

[35] Mini-Circuits, "Connectorized amplifier," pp. 1 – 2.

[36] S. Haykin, *Adaptive Filter Theory.* Prentice Hall, 4 ed., 1996.